1997

DATA ACQUISITION PRODUCTS

HARRIS

DB
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A/D and D/A Converters, Switches, Muxes, Interface,
Display Drivers, Counters, Timebase Generators

DATA ACQUISITION PRODUCTS 1997

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1. Do you have access to CD-ROM capabilities?
   ❑ At Work ❑ At Home ❑ No
2. Do you have access to the Internet?
   ❑ At Work ❑ At Home ❑ No
3. What is your preferred source of product data sheets? Select one:
   ❑ Data Books ❑ CD-ROM ❑ Internet
   ❑ Stand-Alone Data Sheets
4. Would you prefer to have a CD-ROM Data Book, a printed Data Book, or both?
   ❑ CD-ROM Book ❑ Printed Book ❑ Both
5. Which best describes your current design stage? Select one:____
   A. Information Collection D. Initial Production
   B. Prototyping E. Breadboarding
   C. Design Concept F. Full Production
6. When will your design be finalized?
   Month _____ Year _____
7. Expected Annual Volume at full production. Select one:____
   A. 1 to 999 C. 5K to 100K
   B. 1K to 4999 D. > 100K
8. This location has as its primary function: Select one:____
   A. Manufacturing B. Design C. Both

Which category best describes your primary end market? Select One:_____

1100 Video/Imaging
1101 - Desktop Multimedia
1102 - Prof/Broadcast Video
1103 - Medical Imaging
1104 - Cable TV
1105 - Video Conferencing
1199 - Other Video/Imaging

1200 Wireless Communication
1201 - Base Stations
1202 - Wireless LAN/PCS/PB
1203 - Handset/Terminals
1204 - Satellite Communication
1205 - Wireless Local Loop
1299 - Other Wireless Comm.

1300 Government/Military
1301 - Space
1302 - Guidance/Control
1303 - Radar
1304 - Communications
1305 - Avionics
1399 - General Gov't/Military

1400 Telecom
1401 - PBX or CO Line Cards
1402 - Fiber-in-the-Loop
1403 - Wireless Local Loop
1404 - Fiber Optics
1405 - ADSL/HDSL
1406 - Other High Speed Datacomm
1499 - Other Telecom

1500 Computers/Peripherals
1501 - Laptops/Palmtops
1502 - Desktop PCs
1503 - Workstation/File Server
1504 - Disk/Tape Drives
1505 - Printers/Plotter/Scanner
1506 - Datacomm
1599 - General Computer/EDP

1600 Transportation/Consumer
1601 - Power Train
1602 - Vehicle Control
1603 - Safety & Convenience
1604 - Driver Information
1605 - Entertainment
1606 - Electric Vehicles
1607 - Consumer
1699 - Other Transportation

1700 Power Supply/Power Mgmt
1701 - UPS (Uninterruptible Power Supplies)
1702 - AC-DC Power Supplies
1703 - DC-DC Power Supplies
1704 - Transmission Lines
1705 - Utility Substations
1706 - Panel Boxes
1707 - General Protection
1799 - Other Power Supplies/Mgmt

1800 Motor Control
1801 - AC Motors
1802 - 3 Phase Motors
1803 - Brushless
1804 - DC Motors
1805 - Stepper Motors
1899 - Other Motor Control

1900 Industrial Controls & Instrumentation
1901 - Manufacturing System
1902 - High Speed Instrumentation
1903 - Handheld Instruments
1904 - Medical Electronics
1905 - HVAC
1906 - Automatic Test Equipment (ATE)
1999 - General Industrial & Instrumentation

2000 Other Electronics, Not Listed Above

Which best describes your job function? Select one:____
A. Consultant
B. Corporate/Operating Management
C. Documentation
D. Education
E. Engineering
F. Manufacturing
G. Marketing
H. Purchasing
I. Quality Assurance
J. Sales
K. Systems

What is your primary product interest? Select one:____
A. Analog
B. Protection Devices
C. Power Control
D. Converter
E. Digital
F. DSP
G. Telecom
H. Rad Hard
I. Power Discrete
J. Multimedia
K. Wireless

Which best describes your job responsibility Select one:____
A. President/Owner
B. Vice-President/Director
C. Manager/Section Head
D. Engineer
E. Assistant
F. Independent Contractor

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Harris Semiconductor is a pioneer in developing and producing advanced products for the most demanding Commercial, Industrial and Military applications worldwide. Harris offers an extensive line of components including: A/D Converters, D/A Converters, Switches, Multiplexers, Serial Interfaces, and Counters with Display Drivers and Timebase Generators.

This data book fully describes Harris Semiconductor's Data Acquisition ICs. It includes a complete set of data sheets for product specifications, application note abstracts, and a description of the Harris Quality and Reliability program. Section 17, Harris' On-Line Services, describes how our customers have access to the most recent technical updates.

It is our intention to provide you with the most up-to-date information on Data Acquisition Products. For complete, current and detailed technical specifications on any Harris devices, please contact the nearest Harris sales, representative or distributor office, listed in Section 18; or direct literature requests to:

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For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (PSG201; ordering information above).

See Section 17 for Harris' On-Line Services

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HARRIS SEMICONDUCTOR

DATA ACQUISITION PRODUCTS

FOR COMMERCIAL, INDUSTRIAL, AND MILITARY APPLICATIONS

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HI1177	8-Bit, 40 MSPS, YC 2-Channel D/A Converter	4114
HI1178	8-Bit, 40 MSPS, RGB 3-Channel D/A Converter	4115
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HI1826	6-Bit, 140 MSPS, Flash A/D Converter	4107
HI1866	6-Bit, 140 MSPS, Flash A/D Converter	4108
HI20203	8-Bit, 160 MSPS, Ultra High-Speed D/A Converters	4096
HI20206	8-Bit, 35 MSPS, RGB 3-Channel D/A Converter (TTL Input)	4111
HI2300	8-Bit, 18 MSPS, Video A/D Converter with 3.3V Power Supply Operation Function	4103
HI2301	8-Bit, 30 MSPS, Video A/D Converter with Built-In Amplifier/Clamp	4104
HI2302	8-Bit, 50 MSPS, Video A/D Converter with Clamp Function	4105
HI2303	8-Bit, 3-Channel, 50 MSPS, Video A/D Converter With Clamp Function	4106
HI2304	8-Bit, 20 MSPS, RGB 3-Channel D/A Converter	4116
HI2307	10-Bit, 50 MSPS, RGB 3-Channel D/A Converter	4117
HI2309	10-Bit, 50 MSPS, 3-Channel D/A Converter	4118
HI2315	10-Bit, 80 MSPS, 1-Channel D/A Converter (Ultra-Low Glitch Version)	4119
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HI3050	10-Bit, 50MHz, High Speed 3-Channel D/A Converter	3936
HI3086	6-Bit, 140 MSPS, Flash A/D Converter	4110
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HI5728	10-Bit, 125 MSPS, Dual High Speed D/A Converter	4321
HI5731	12-Bit, High Speed D/A Converter	4070
HI5735	12-Bit, High Speed Video D/A Converter	4133
HI5741	14-Bit, High Speed D/A Converter	4071
HI5746	10-Bit, 40 MSPS A/D Converter	4129
HI5760	10-Bit, 125 MSPS, High Speed D/A Converter	4320
HI5762	Dual 10-Bit, 40/60 MSPS A/D Converter with Internal Voltage Reference	4318

New Products from Harris Semiconductor

PART NUMBER	DESCRIPTION	DOCUMENT NUMBER
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HI5767	10-Bit, 20/40/60 MSPS A/D Converter with Internal Voltage Reference	4319
HI5804	12-Bit, 5 MSPS A/D Converter	4026
HI5805	12-Bit, 5 MSPS A/D Converter	3984
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HIN230 thru HIN241	+5V Powered RS-232 Transmitters/Receivers	3138
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HGTD3N60C3, HGTD3N60C3S	6A, 600V, UFS Series N-Channel IGBT	4139
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HGTP3N60B3D, HGT1S3N60B3D, HGT1S3N60B3DS	7A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode	TBD
HGTP12N60C3R, HGT1S12N60C3R, HGT1S12N60C3RS	24A, 600V, Rugged UFS Series N-Channel IGBT	TBD
HGTP12N60C3DR, HGT1S12N60C3DR, HGT1S12N60CRDRS, HGTG12N60C3DR	24A, 600V, Rugged UFS Series N-Channel IGBT with Anti-Parallel Ultrafast Diode	TBD

New Products from Harris Semiconductor

PART NUMBER	DESCRIPTION	DOCUMENT NUMBER
HGTD7N60C3, HGTD7N60C3S, HGTP7N60C3	14A, 600V, UFS Series N-Channel IGBT	4141
HGTG12N60C3D	24A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode	4043
HGTG15N120C3D	35A, 1200V, UFS Series N-Channel IGBT	4267
HGTG20N60C3DR	40A, 600V, Rugged, UFS Series N-Channel IGBT with Anti-Parallel Ultrafast Diode	4234
HGTG27N60C3DR	54A, 600V, Rugged UFS Series N-Channel IGBT with Anti-Parallel Ultrafast Diode	4262
HGTG27N60C3R	54A, 600V, Rugged UFS Series N-Channel IGBT	4245
HGTG30N60C3	63A, 600V, UFS Series N-Channel IGBT	4042
HGTG30N60C3D	63A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode	4041
HGTG40N60C3R	75A, 600V, Rugged, UFS Series N-Channel IGBT	4312
HGTP12N60C3, HGT1S12N60C3, HGT1S12N60C3S	24A, 600V, UFS Series N-Channel IGBT	4040
HGTP3N60C3D, HGT1S3N60C3D, HGT1S3N60C3DS	6A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode	4140
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HGTP12N60C3D, HGT1S12N60C3D, HGT1S12N60C3DS	24A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode	4261
HGTP15N120C3	35A, 1200V, UFS Series N-Channel IGBT	4244
RF1K49211	12V, 7A, 0.020 Ohm, Single N-Channel, Logic Level	4303
RF1K49221	60V, 2.5A, 0.130 Ohm Dual N-Channel	4314
RF1K49223	30V, 2.5A, 0.150 Ohm, Dual P-Channel	4322
RF1K49224	30V, 2.5A, 0.150 Ohm, P-Channel, 30V, 3.5A, 0.060 Ohm, N-Channel, Complementary N/P Channel	4330
RF1S4N100, RF1S4N100SM	1000V, 4A, 3.5 Ohm, N-Channel	TBD
RF1S15N06, RF1S15N06SM	60V, 15A, 0.140 Ohm, N-Channel, Logic Level	TBD
RF1S15N08L, RF1S15N08LSM	80V, 15A, 0.140 Ohm, N-Channell, Logic Level	TBD
RF1S17N06L, RF1S17N06LSM	60V, 17A, 0.100 Ohm, N-Channel, Logic Level	TBD
RF1S22N10, RF1S22N10SM	100V, 22A, 0.080 Ohm, N-Channel	TBD
RFD8P06LE, RFD8P06LESM	60V, 8A, 0.300 Ohm, P-Channel, Logic Level	4273
RFD16N02L, RFD16N02LSM	16A, 20V, 0.022 Ohm , N-Channel Logic Level Power MOSFET	4341
RFD16N03L, RFD16N03LSM	16A, 30V, 0.025 Ohm, Avalanche Rated N-Channel Logic Level, Enhancement-Mode Power MOSFETs	4013
RFG45N06LE, RFP45N06LE, RF1S45N06LE, RF1S45N06LESM	45A, 60V, 0.028 Ohm, ESD Rated, Avalanche Rated, Logic Level N-Channel, Enhancement-Mode Power MOSFETs	4076
RFG50N06LE, RFP50N06LE, RF1S50N06LE, RF1S50N06LESM	60V, 50A, 0.022 Ohm, N-Channel, Logic Level	4072
RFP8P06LE	60V, 8A, 0.300 Ohm, P-Channel, Logic Level	4273
RFP42N03L, RF1S42N03L, RF1S42N03LSM	42A, 30V, 0.025 Ohm, N-Channel Logic Level Power MOSFETs	4302

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RFP45N02L, RF1S45N02L, RF1S45N02LSM	45A, 20V, 0.022 Ohm, N-Channel Logic Level Power MOSFETs	4342
HUF75307P3, HUF75307D3, HUF75307D3S	13A, 55V, 0.090 Ohm, N-Channel UltraFET(TM) Power MOSFET	4353
HUF75309P3, HUF75309D3, HUF75309D3S	17A, 55V, 0.070 Ohm, N-Channel UltraFET(TM) Power MOSFET	4358
HUF75321D3, HUF75321D3S	20A, 55V, 0.032 Ohm, N-Channel UltraFET(TM) Power MOSFET	4351
HUF75321P3, HUF75321S3, HUF75321S3S	31A, 55V, 0.032Ohm, N-Channel UltraFET(TM) Power MOSFET	4360
HUF75329G3, HUF75329P3, HUF75329S3, HUF75329S3S	42A, 55V, 0.025 Ohm, N-Channel UltraFET(TM) Power MOSFET	4361
HUF75329D3, HUF75329D3S	20A, 55V, 0.025 Ohm N-Channel UltraFET(TM) Power MOSFET	TBD
HUF75333G3, HUF75333P3, HUF75333S3, HUF75333S3S	56A, 55V, 0.016 Ohm, N-Channel UltraFET(TM) Power MOSFET	4362
HUF75339G3, HUF75339P3, HUF75339S3, HUF75339S3S	70A, 55V, 0.012 Ohm, N-Channel UltraFET(TM) Power MOSFET	4363
HUF75343G3, HUF75343P3, HUF75343S3, HUF75343S3S	75A, 55V, 0.009 Ohm, N-Channel UltraFET(TM) Power MOSFET	4352
HUF75345G3, HUF75345P3, HUF75345S3, HUF75345S3S	75A, 55V, 0.007 Ohm, N-Channel UltraFET(TM) Power MOSFET	4365
HUF75337G3, HUF75337P3, HUF75337S3, HUF75337S3S	58A, 55V, 0.015 Ohm, N-Channel UltraFET(TM) Power MOSFET	4369
	LINEAR AND TELECOMMUNICATIONS	
HA456	150MHz, Low Power, 8 x 8 Video Crosspoint Switch	4153
HA4244	480MHz, 1 x 1 Video Crosspoint Switch with Synchronous Enable	4078
HC-5502B1	SLIC Subscriber Line Interface Circuit	4127
HC5503	Subscriber Line Interface Circuit	4344
HC-5504B1	SLIC Subscriber Line Interface Circuit	4125
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HC5519	SLIC Subscriber Line Interface Circuit	4232
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HC5523	Subscriber Line Interface Circuit	4144
HC5526	Subscriber Line Interface Circuit	4151
HC55171	5 REN Ringing SLIC Subscriber Line Interface Circuit	4323
HC6094	ADSL Analog Front End Chip	4260
HFA1412	Quad, 350MHz, Low Power, Programmable Gain Buffer Amplifier	4152

New Products from Harris Semiconductor

PART NUMBER	DESCRIPTION	DOCUMENT NUMBER
MULTILAYER TRANSIENT VOLTAGE SURGE SUPPRESSORS		
UltraMOV Series - V07E130, V10E130, V14E130, V20E130, V07E140, V10E140, V14E140, V20E140, V07E150, V10E150, V14E150, V20E150, V07E175, V10E175, V14E175, V20E175, V07E230, V10E230, V14E230, V20E230, V07E250, V10E250, V14E250, V20E250, V07E275, V10E275, V14E275, V20E275, V07E300, V10E300, V14E300, V20E300, V07E320, V10E320, V14E320, V20E320	Metal Oxide Varistors	4366
HAC Series - HAC120, HAC120L, HAC240, HAC240L	Two Electrode AC Line Protectors	4332
HG3 Series - HG3-1.0, HG3-1.0L, HG3-1.5, HG3-1.5L, HG3-2.0, HG3-2.0L, HG3-2.5, HG3-2.5L, HG3-3.0, HG3-3.0L, HG3-4.0, HG3-4.0L, HG3-5.0, HG3-5.0L, HG3-7.5, HG3-7.5L, HG3-8.5, HG3-8.5L	Two Electrode High Voltage Surge Arresters	4336
HG Series, HG2 Series	Two Electrode Surge Arrestors	4333
HPMT3 Series - HPMT3-150, HPMT3-150L, HPMT3-230, HPMT3-230L, HPMT3-250, HPMT3-250L, HPMT3-350, HPMT3-350L, HPMT3-400, HPMT3-400L, HPMT3-500, HPMT3-500L	Three Electrode Surge Arresters	4337
ML Series - V3.5MLA0603, V5.5MLA0603, V9MLA0603, V14MLA0603, V18MLA0603	Multilayer Surface Mount Transient Voltage Surge Suppressor	2461
MLE Series - V18MLE0603, V18MLE0805, V18MLE1206	Multilayer Surface Mount ESD Suppressor/Filter	4263
MULTIMEDIA		
HMP8112	NTSC/PAL Video Decoder	4221
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New Products from Harris Semiconductor

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HIP0051	0.25A/50V Octal Low Side Power Driverwith Serial Bus Control	4155
HIP0063	Hex Low Side MOSFET Driver with Serial or Parallel Interface and Diagnostic Fault Control	4009
HIP1011	Power Distribution Controller	4311
HIP2060	60V, 10A Half Bridge Power MOSFET Array	3983
HIP2100	100V/2A Peak, Low Cost, High Frequency Half Bridge Driver	4022
HIP4020	Half Amp Full Bridge Power Driver for Small 3V, 5V and 12V DC Motors	3976
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NOTE: Bold type designates a new product from Harris.

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Linear Product Offerings

COMPARATORS

CA139, CA139A, CA239, CA239A, CA339, CA339A, LM339, LM339A, LM2901, LM3302	Quad Voltage Comparators for Industrial, Commercial and Military Applications
CA3290	BiMOS Dual Voltage Comparator with MOSFET Input, Bipolar Output
HA-4900, HA-4902, HA-4905	Precision Quad Comparators

OPERATIONAL AMPLIFIERS

CA124, CA224, CA324, LM324, LM2902	Quad, 1MHz, Operational Amplifiers for Commercial, Industrial, and Military Applications
CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358, LM2904	Dual, 1MHz, Operational Amplifiers for Commercial, Industrial, and Military Applications
CA741, CA741C, CA1458, CA1558, LM741, LM741C, LM1458	Single and Dual, High Gain Operational Amplifiers for Military, Industrial and Commercial Applications
CA3078, CA3078A	2kHz, Micropower Operational Amplifier
CA3080, CA3080A	2MHz, Operational Transconductance Amplifier (OTA)
CA3100	38MHz Operational Amplifier
CA3130, CA3130A	15MHz BiMOS Operational Amplifier with MOSFET Input/CMOS Output
CA3140, CA3140A	4.5MHz BiMOS Operational Amplifier with MOSFET Input/Bipolar Output
CA3160, CA3160A	4MHz BiMOS Operational Amplifiers with MOSFET Input/CMOS Output
CA3240, CA3240A	Dual, 4.5MHz, BiMOS Operational Amplifier with MOSFET Input/Bipolar Output
CA3260, CA3260A	4MHz, BiMOS Operational Amplifier with MOSFET Input/CMOS Output
CA3280, CA3280A	Dual, 9MHz, Operational Transconductance Amplifier (OTA)
CA5260, CA5260A	3MHz, BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output
CA5420, CA5420A	0.5MHz, Low Supply Voltage, Low Input Current BiMOS Operational Amplifiers
CA5470	Quad, 14MHz, Microprocessor BiMOS-E Operational Amplifier with MOSFET Input/Bipolar Output
HA-2400, HA-2404, HA-2405	40MHz, PRAM Four Channel Programmable Amplifiers
HA-2406	30MHz, Digitally Selectable Four Channel Operational Amplifier
HA-2444	50MHz, Selectable, Four Channel Video Operational Amplifier
HA-2500, HA-2502, HA-2505	12MHz, High Input Impedance, Operational Amplifiers
HA-2510, HA-2512, HA-2515	12MHz, High Input Impedance, Operational Amplifiers
HA-2520, HA-2522, HA-2525	20MHz, High Slew Rate, Uncompensated, High Input Impedance, Operational Amplifiers
HA-2539	600MHz, Very High Slew Rate Operational Amplifier
HA-2540	400MHz, Fast Settling Operational Amplifier

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Linear Product Offerings (Continued)

HA-2541	40MHz, Fast Settling, Unity Gain Stable, Operational Amplifier
HA-2542	70MHz, High Slew Rate, High Output Current Operational Amplifier
HA-2544	50MHz, Video Operational Amplifier
HA-2600, HA-2602, HA-2605	12MHz, High Input Impedance Operational Amplifiers
HA-2620, HA-2622, HA-2625	100MHz, High Input Impedance, Very Wideband, Uncompensated Operational Amplifiers
HA-2640, HA-2645	4MHz, High Supply Voltage Operational Amplifiers
HA-2839	600MHz, Very High Slew Rate Operational Amplifier
HA-2840	600MHz, Very High Slew Rate Operational Amplifier
HA-2841	50MHz, Fast Settling, Unity Gain Stable, Video Operational Amplifier
HA-2842	80MHz, High Slew Rate, High Output Current, Video Operational Amplifier
HA-2850	470MHz, Low Power, High Slew Rate Operational Amplifier
HA-4741	Quad, 3.5MHz, Operational Amplifier
HA-5002	110MHz, High Slew Rate, High Output Current Buffer
HA5013	**Triple, 125MHz Video Amplifier**
HA-5020	**100MHz Current Feedback Video Amplifier With Disable**
HA5022	**Dual, 125MHz, Video Current Feedback Amplifier with Disable**
HA5023	**Dual 125MHz Video Current Feedback Amplifier**
HA5024	**Quad 125MHz Video Current Feedback Amplifier with Disable**
HA5025	Quad, 125MHz Video Current Feedback Amplifier
HA-5033	250MHz Video Buffer
HA-5101, HA-5111	10MHz and 100MHz, Low Noise, Operational Amplifiers
HA-5102, HA-5104, HA-5112, HA-5114	Dual and Quad, 8MHz and 60MHz, Low Noise Operational Amplifiers
HA-5127, HA-5127A	8.5MHz, Ultra-Low Noise Precision Operational Amplifier
HA-5130, HA-5135	2.5MHz, Precision Operational Amplifiers
HA-5134	4MHz, Precision, Quad Operational Amplifier
HA-5137, HA-5137A	63MHz, Ultra-Low Noise Precision Operational Amplifier
HA-5142, HA-5144	Dual/Quad, 400kHz, Ultra-Low Power Operational Amplifiers
HA-5147, HA-5147A	120MHz, Ultra-Low Noise Precision Operational Amplifiers
HA-5160, HA-5162	100MHz, JFET Input, High Slew Rate, Uncompensated, Operational Amplifiers
HA-5170	8MHz, Precision, JFET Input Operational Amplifier
HA-5190, HA-5195	150MHz, Fast Settling Operational Amplifiers
HA-5221, HA-5222	100MHz, Single and Dual Low Noise, Precision Operational Amplifiers
HFA1100, HFA1120	850MHz, Low Distortion Current Feedback Operational Amplifiers
HFA1102	600MHz Current Feedback Amplifier with Compensation Pin
HFA1103	200MHz, Video Op Amp with High Speed Sync Stripper
HFA1105	330MHz, Low Power, Current Feedback Video Operational Amplifier
HFA1106	315MHz, Low Power, Video Operational Amplifier with Compensation Pin
HFA1109, HFA1149	550MHz, Low Power, Current Feedback Operational Amplifiers
HFA1110	750MHz, Low Distortion Unity Gain, Closed Loop Buffer
HFA1112	850MHz, Low Distortion Programmable Gain Buffer Amplifier

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Linear Product Offerings (Continued)

HFA1113	850MHz, Low Distortion, Output Limiting, Programmable Gain, Buffer Amplifier
HFA1114	850MHz Video Cable Driving Buffer
HFA1115	**225MHz, Low Power, Output Limiting, Closed Loop Buffer Amplifier**
HFA1118, HFA1119	500MHz Programmable Gain Video Buffers with Output Limiting and Output Disable
HFA1130	850MHz, Output Limiting, Low Distortion Current Feedback Operational Amplifie
HFA1135	**360MHz, Low Power, Video Operational Amplifier with Output Limiting**
HFA1145	**330MHz, Low Power, Current Feedback Video Operational Amplifier with Output Disable**
HFA1205	**Dual, 400MHz, Low Power, Video Operational Amplifie**
HFA1212	Dual 350MHz, Low Power Closed Loop Buffer Amplifier
HFA1245	Dual, 530MHz, Low Power, Video Operational Amplifier with Disable
HFA1405	Quad, 560MHz, Low Power, Video Operational Amplifier
HFA1412	Quad, 350MHz, Low Power, Programmable Gain Buffer Amplifie
ICL7611, ICL7612	1.4MHz, Low Power CMOS Operational Amplifiers
ICL7621, ICL7641, ICL7642	Dual/Quad, Low Power CMOS Operational Amplifiers
ICL7650S	2MHz, Super Chopper-Stabilized Operational Amplifier

SAMPLE AND HOLD AMPLIFIERS

HA-2420, HA-2425	**3.2μs Sample and Hold Amplifiers**
HA-5320	1μs Precision Sample and Hold Amplifier
HA-5330	650ns Precision Sample and Hold Amplifier
HA-5340	700ns, Low Distortion, Precision Sample and Hold Amplifier
HA5351	64ns Sample and Hold Amplifier

SPECIAL ANALOG CIRCUITS

CA555, CA555C, LM555, LM555C	Timers for Timing Delays and Oscillator Application in Commercial, Industrial and Military Equipment
CA3256	25MHz, BiMOS Analog Video Switch and Amplifier
HA-2546	30MHz, Voltage Output, Two Quadrant Analog Multiplier
HA-2556	57MHz, Wideband, Four Quadrant, Voltage Output Analog Multiplier
HA-2557	130MHz, Four Quadrant, Current Output Analog Multiplier
HA7210, HA7211	10kHz to 10MHz, Low Power Crystal Oscillator
HFA5251	**800MHz Monolithic Pin Driver**
HFA5253	**800MHz, Ultra High-Speed Monolithic Pin Driver**
ICL8013	**1MHz, Four Quadrant Analog Multiplier**
ICL8038	**Precision Waveform Generator/Voltage Controlled Oscillator**
ICM7242	Long Range Fixed Timer
ICM7555, ICM7556	General Purpose Timers

TRANSISTOR AND DIODE ARRAY, AND DIFFERENTIAL AMPLIFIER DATA SHEETS

CA3028A, CA3028B, CA3053	Differential/Cascode Amplifiers for Commercial and Industrial Equipment from DC to 120MHz

NOTE: Bold type designates a new product from Harris.

Linear Product Offerings (Continued)

CA3039	Diode Array
CA3045, CA3046	General Purpose NPN Transistor Arrays
CA3049, CA3102	Dual High Frequency Differential Amplifiers For Low Power Applications Up to 500MHz
CA3054	Dual Independent Differential Amp for Low Power Applications from DC to 120MHz
CA3081, CA3082	General Purpose High Current NPN Transistor Arrays
CA3083	General Purpose High Current NPN Transistor Array
CA3086	General Purpose NPN Transistor Array
CA3096, CA3096A, CA3096C	NPN/PNP Transistor Arrays
CA3127	**High Frequency NPN Transistor Array**
CA3146, CA3146A, CA3183, CA3183A	**High-Voltage Transistor Arrays**
CA3227, CA3246	High-Frequency NPN Transistor Arrays For Low-Power Applications at Frequencies Up to 1.5GHz
HFA3046, HFA3096, HFA3127, HFA3128	Ultra High Frequency Transistor Arrays
HFA3101	**Gilbert Cell UHF Transistor Array**
HFA3102	**Dual Long-Tailed Pair Transistor Array**

VIDEO CROSSPOINT SWITCHES

HA4201	**480MHz, 1 x 1 Video Crosspoint Switch with Tally Output**
HA4244	**480MHz, 1 x 1 Video Crosspoint Switch with Synchronous Enable**
HA4314B	400MHz, 4 x 1 Video Crosspoint Switch
HA4344B	350MHz, 4 x 1 Video Crosspoint Switch with Synchronous Controls
HA4404B	330MHz, 4 x 1 Video Crosspoint Switch with Tally Outputs
HA455	130MHz, 8 x 8 Video Crosspoint Switch
HA456	80MHz, Low Power, 8 x 8 Video Crosspoint Switch
HA457	170MHz, AV = +2, 8 x 8 Video Crosspoint Switch
HA4600	480MHz, Video Buffer with Output Disable

Telecom Product Offerings

TELECOMMUNICATIONS

CD22100	CMOS 4 x 4 Crosspoint Switch with Control Memory High-Voltage Type (20V Rating)
CD22101, CD22102	CMOS 4 x 4 x 2 Crosspoint Switch with Control Memory
CD22103A	CMOS HDB3 (High Density Bipolar 3) Transcoder for 2.048/8.448Mb/s Transmission Applications
HC-5560	PCM Transcoder AMI, HDB3, B6ZS, B8ZS
CD22202, CD22203	5V Low Power DTMF Receiver
CD22204	5V Low Power Subscriber DTMF Receiver
CD22301	Monolithic PCM Repeater
CD22354A, CD22357A	CMOS Single-Chip, Full-Feature PCM CODEC
CD22M3493	12 x 8 x 1 BiMOS-E Crosspoint Switch
CD22M3494	16 x 8 x 1 BiMOS-E Crosspoint Switch

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Telecom Product Offerings (Continued)

CD22859	Monolithic Silicon COS/MOS Dual-Tone Multifrequency Tone Generator
CD74HC22106, CD74HCT22106	QMOS 8 x 8 x 1 Crosspoint Switch with Memory Control
HC-5502B	EIA/ITU PABX SLIC with 30mA Loop Feed
HC5503	**Low Cost 24 Volt SLIC for PABX/Key Systems**
HC-5504B	EIA/ITU PABX SLIC with 40mA Loop Feed
HC-5504B1	ITU Low Cost, PABX SLIC with 40mA Loop Feed
HC5509A1R3060	ITU CO/Loop Carrier SLIC
HC-5509B	ITU CO/Loop Carrier SLIC
HC5513	TR909 DLC/FLC SLIC with Low Power Standby
HC5515	ITU CO/PABX SLIC with Low Power Standby
HC5517	**3 REN Ringing SLIC for ISDN Modem/TA and WLL**
HC5517B	**Low Cost 3 REN Ringing SLIC for ISDN Modem/TA and WLL**
HC55171	**5 REN Ringing SLIC for ISDN Modem/TA and WLL**
HC55171B	**Low Cost 5 REN Ringing SLIC for ISDN Modem/TA and WLL**
HC5519	ITU CO SLIC with Polarity Reversal and Integrated Combo
HC5520	ITU CO SLIC with Polarity Reversal
HC5523	LSSGR/TR57 CO/Loop Carrier SLIC with Low Power Standby
HC5526	ITU CO/PABX SLIC with Low Power Standby
HC-5524	EIA/ITU 24 Volt PABX SLIC with 25mA Loop Feed
HC-55536, HC-55564	Continuously Variable Slope Delta-Demodulator (CVSD)

Digital Signal Processing Product Offerings

DEVELOPMENT TOOLS

DECI • MATE	Harris HSP43220 Decimating Digital Filter Development Software
HSP-EVAL	DSP Evaluation Platform
HSP45116-DB	HSP46116 Daughter Board
HSP50016-EV	DDC Evaluation Platform
HSP50110/210EVAL	DSP Demodulator Evaluation Board
Serinade	Development Software for HSP43124 Serial I/O Filter

DOWN CONVERSION AND DEMODULATION

HSP50016	Digital Down Converter
HSP50110	Digital Quadrature Tuner
HSP50210	Digital Costas Loop
HSP50214	Programmable Downconverter
ST-114	ST-114 Harris HSP50214 Downconverter Evaluation Board (Sigtek 410-290-3918)
HSP50306	Digital QPSK Demodulator

UP CONVERSION AND MODULATION

HSP50215	Digital Upconverter
HSP50307	Burst QPSK Modulator
HSP50307EVAL1	Burst QPSK Modulator Evaluation Board

NOTE: Bold type designates a new product from Harris.

Digital Signal Processing Product Offerings (Continued)

MULTIPLIERS

HMA510	16 x 16-Bit CMOS Parallel Multiplier Accumulator
HMA510/883	16 x 16-Bit CMOS Parallel Multiplier Accumulator
HMU16/HMU17	16 x 16-Bit CMOS Parallel Multipliers
HMU16/883	16 x 16-Bit CMOS Parallel Multiplier
HMU17/883	16 x 16-Bit CMOS Parallel Multiplier

ONE DIMENSIONAL FILTERS

HSP43124	Serial I/O Filter
HSP43168	Dual FIR Filter
HSP43168/883	Dual FIR Filter
HSP43216	Halfband Filter
HSP43220	Decimating Digital Filter
HSP43220/883	Decimating Digital Filter
HSP43881	Digital Filter
HSP43881/883	Digital Filter
HSP43891	Digital Filter
HSP43891/883	Digital Filter

SIGNAL SYNTHESIZERS

HSP45102	12-Bit Numerically Controlled Oscillator
HSP45106	16-Bit Numerically Controled Oscillator
HSP45106/883	16-Bit Numerically Controlled Oscillator
HSP45116	Numerically Controlled Oscillator/Modulator
HSP45116/883	Numerically Controlled Oscillator/Modulator
HSP45116A	Numerically Controlled Oscillator/Modulator

SPECIAL FUNCTION

HSP45240	Address Sequencer
HSP45240/883	Address Sequencer
HSP45256	Binary Correlator
HSP45256/833	Binary Correlator
HSP9520, HSP9521	Multilevel Pipeline Registers

VIDEO PROCESSING

HSP48212	Digital Video Mixer
HSP48410	Histogrammer/Accumulating Buffer
HSP48410/883	Histogrammer/Accumulating Buffer
HSP48901	3 x 3 Image Filter
HSP48908	Two Dimensional Convolver
HSP48908/883	Two Dimensional Convolver
HSP9501	Programmable Data Buffer

BLOCK DIAGRAM FOLDOUTS

FO-006	A Digital Programmable Downconverter for AMPS, North Americal TDMA, GSM and CDMA Signal Applications
FO-007	Offering Advanced DSP Parts for Today's Communication SOlutions (Block Diagram for HSP50110, HSP50210, HSP50110/210EVAL)

NOTE: Bold type designates a new product from Harris.

DATA ACQUISITION 3

A/D CONVERTERS - DISPLAY

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A/D Converters - Display Data Sheets		
CA3162, CA3162A	A/D Converters for 3-Digit Display	3-5
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ICL7116, ICL7117	$3^1/_2$ Digit, LCD/LED Display, A/D Converter with Display Hold	3-29
ICL7126	$3^1/_2$ Digit, Low Power, Single-Chip A/D Converter	3-30
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ANALOG TO DIGITAL CONVERTERS - DISPLAY

(NOTES 2, 3) DEVICE	SUFFIX CODES	DISPLAY TYPE	DISPLAY DRIVE	CONVERSION TYPE	CONVERSION TIME (ms)	TECHNOLOGY	RANGE MIN	LINEARITY COUNTS	FEATURES
3 DIGIT WITH LED DRIVERS									
CA3162A	E	BCD	Common Anode (CA3161)	Integrating	10, 250	Bipolar-JI	+999mV to -99mV	±1	BCD to 7 Segment Converter, 2 Chip Set Makes a Complete DPM. Analog to Digital Converter, 3 Digit Output, "EEE": Positive Over-Range Indication, "-": Negative Over-Range Display.
CA3162	E	BCD	Common Anode (CA3161)	Integrating	10, 250	Bipolar-JI	+999mV to -99mV	±1	
$3^1/_2$ DIGIT WITH LED/LCD DRIVERS									
HI7131	CM44, CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	High Common Mode Front End No Over-Range Hangover
HI7133	CM44, CPL	LED	Common Anode	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	High Common Mode Front End No Over-Range Hangover
ICL7106	CM44, CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	
ICL7106R	CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	Reversed Leads
ICL7107	CM44, CPL	LED	Common Anode	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	
ICL7107R	CPL	LED	Common Anode	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	Reversed Leads
ICL7116	CM44, CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	ICL7106 with Display Hold Function
ICL7117	CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	ICL7107 with Display Hold Function
ICL7126	CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	Low Power Version of ICL7106
ICL7126R	CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	Low Power Version of ICL7106 Reversed Leads
ICL7136	CM44, CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	Low Power Version of ICL7106
ICL7136R	CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	Low Power Version of ICL7106 Reversed Leads

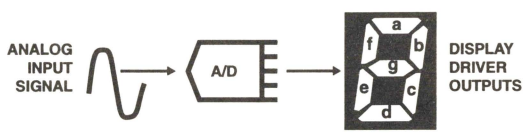
ANALOG TO DIGITAL CONVERTERS - DISPLAY (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	DISPLAY TYPE	DISPLAY DRIVE	CONVERSION TYPE	CONVERSION TIME (ms)	TECHNOLOGY	RANGE MIN	LINEARITY COUNTS	FEATURES
ICL7137	CPL	LED	Common Anode	Auto-Zero	333 Typ	CMOS-JI	±0.2V	±1	Low Power Version of ICL7107
$3^3/_4$ DIGIT WITH LCD DRIVERS									
ICL7139	CPL	LCD	Duplex	Auto Zero	400	CMOS-JI	±0.4V	±1	13 Ranges, Autoranging Multimeter, AC Internal
ICL7149	CM44, CPL	LCD	Duplex	Auto-Zero Integrating	400	CMOS-JI	±0.4V	±1	18 Ranges, Autoranging Multimeter, AC External
$4^1/_2$ DIGIT WITH LCD DRIVERS									
ICL7129	CM44, CPL	LCD	Triplexed	Auto-Zero Integrating	500	CMOS-JI	±0.2V	±1 Typ	10μV Resolution. 1X, 10X Range Selection
ICL7129R	CPL	LCD	Triplexed	Auto-Zero Integrating	500	CMOS-JI	±0.2V	±1 Typ	10μV Resolution. 1X, 10X Range Selection, PDIP Reversed Leads

ANALOG TO DIGITAL CONVERTERS WITH DISPLAY OUTPUTS (2 Chip Sets)

PART NUMBER	OUTPUT TYPE	RESOLUTION	CONVERSION TIME (SAMPLE RATE)	PACKAGE TYPES	FEATURES
CA3162	LED, CA, BCD	3 Digits	10ms/250ms (96SPS/4SPS)	16 Lead Plastic DIP	2 Chip Set Makes a Complete DPM A/D Converter, 3 Digit Output, "EEE": Positive Over-Range Indication, "-": Negative Over-Range Display
CA3161					

NOTE: Sorted by ascending resolution (Digits) and conversion time.



CA3162, CA3162A

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

A/D Converters for 3-Digit Display

Features

- Dual Slope A/D Conversion
- Multiplexed BCD Display
- Ultra Stable Internal Band Gap Voltage Reference
- Capable of Reading 99mV Below Ground with Single Supply
- Differential Input
- Internal Timing - No External Clock Required
- Choice of Low Speed (4Hz) or High Speed (96Hz) Conversion Rate
- "Hold" Inhibits Conversion but Maintains Delay
- Overrange Indication
  - "EEE" for Reading Greater than +999mV, "-" for Reading More Negative than -99mV When Used With CA3161E
- Extended Temperature Range Version Available

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3162E	0 to 70	16 Ld PDIP	E16.3
CA3162AE	-40 to 85	16 Ld PDIP	E16.3

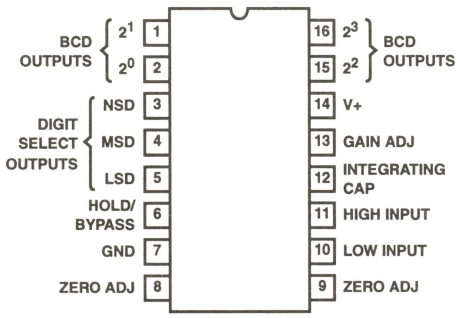
Description

The CA3162E and CA3162AE are I^2L monolithic A/D converters that provide a 3 digit multiplexed BCD output. They are used with the CA3161E BCD-to-Seven-Segment Decoder/Driver and a minimum of external parts to implement a complete 3-digit display. The CA3162AE is identical to the CA3162E except for an extended operating temperature range.

The CA3161E is described in the Display Drivers section of this data book.

Pinout

CA3162
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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HARRIS SEMICONDUCTOR

HI7131, HI7133

$3^1/_2$ Digit, Low Power, High CMRR, LCD/LED Display-Type A/D Converters

August 1997

Features

- 120dB CMRR Equal to ±0.01 Count/V of Common Mode Voltage Error
- Fast Recovery from Input Overrange Results "Correct First-Reading" After Overload
- Guaranteed 0000 Reading for 0V Input
- True Polarity at Zero for Precise Null Detection
- 1pA Input Current (Typ)
- True Differential Input and Reference
- Single or Dual Supply Operation Capability
- Direct LCD Display Drive - HI7131
- Direct LED Display Drive - HI7133
- Low Noise, 15μV_{P-P} Without Hysteresis or Overrange Hangover
- Low Power Dissipation, Guaranteed Less Than 1mW, Results 8000 Hours (Typ) 9V Battery Life
- No Additional Active Components Required

Applications

- Handheld Instruments
- Basic Measurements: Voltage, Current, Resistance Pressure, Temperature, Fluid Flow and Level, pH, Weight, Light Intensity
- DMMs and DPMs

Description

The Harris HI7131 and HI7133 are $3^1/_2$ digit, A/D converters that have been optimized for superior DC Common Mode Rejection (CMRR) when used with a split ±5V supply or a single 9V battery. The HI7131 contains all the necessary active components on a single IC to directly interface an LCD (Liquid Crystal Display). The supply current is under 100µA and is ideally suited for battery operation. The HI7133 contains all the necessary active components on a single IC to directly interface an LED (Light Emitting Diode).

The HI7131 and HI7133 feature high accuracy performance like, 120dB of CMRR, auto-zero to less than 10µV of offset, fast recovery from over load, zero drift of less than 1µV/°C, input bias current of 10pA maximum, and rollover error of less than one count. A true differential signal and reference inputs are useful features in all systems, but gives the designer an advantage when measuring load cells, strain gauges and other bridge-type transducers.

The HI7131 and HI7133 are supplied in a 40 lead plastic DIP and a 44 lead metric plastic quad flatpack package.

Ordering Information

PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI7131CPL	0 to 70	40 Ld PDIP	E40.6
HI7131CM44	0 to 70	44 Ld MQFP	Q44.10x10
HI7133CPL	0 to 70	40 Ld PDIP	E40.6
HI7133CM44	0 to 70	44 Ld MQFP	Q44.10x10

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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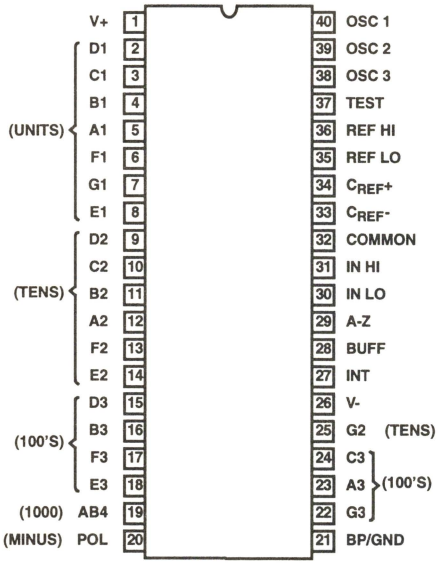
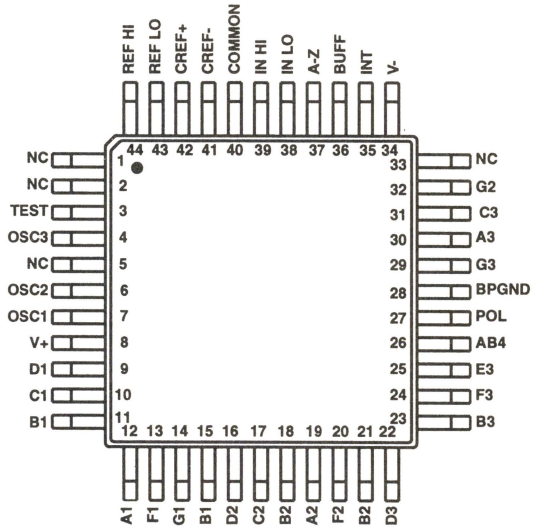
File Number **3373.2**

Pinouts

HI7131CPL, HI7133CPL
(PDIP)
TOP VIEW



HI7131CM44, HI7133CM44
(MQFP)
TOP VIEW



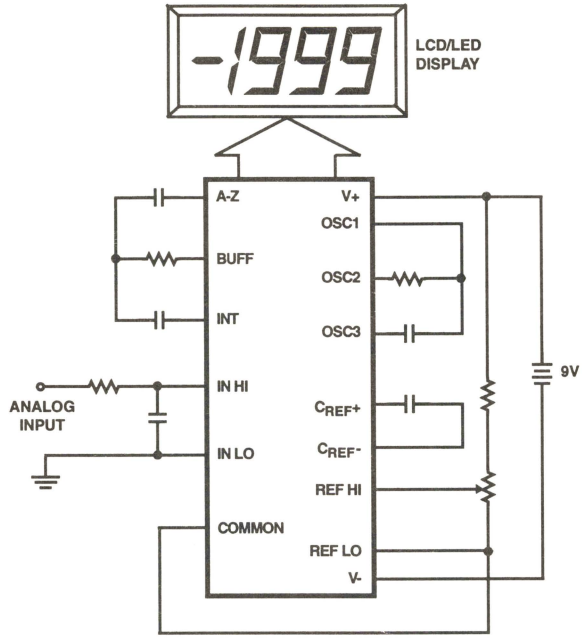
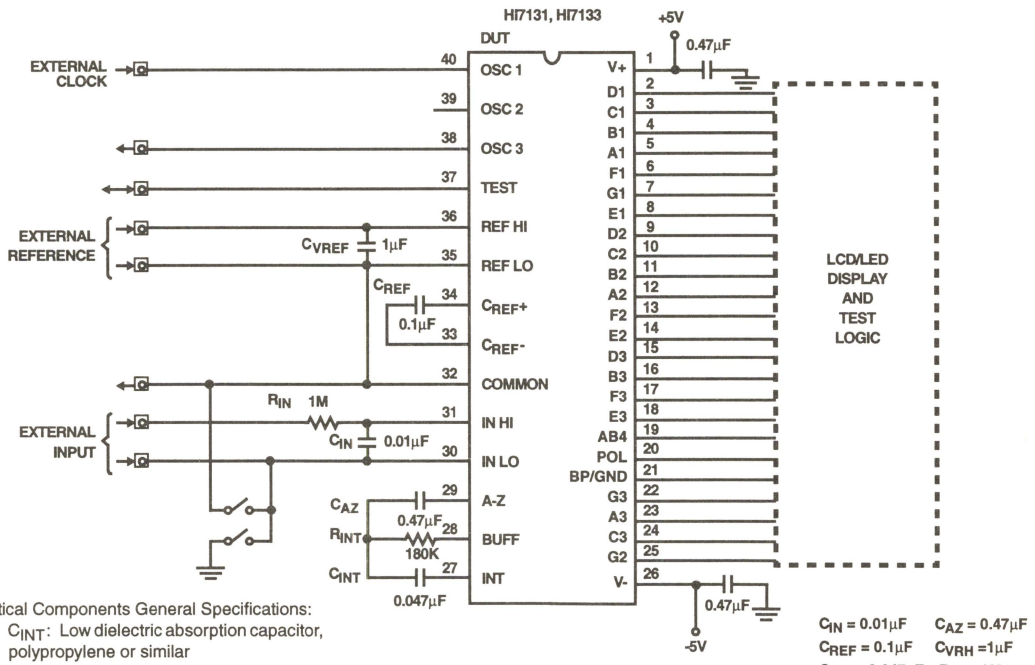


FIGURE 1. TYPICAL APPLICATION CIRCUIT



Critical Components General Specifications:

1. C_{INT}: Low dielectric absorption capacitor, polypropylene or similar
2. C_{AZ}, C_{REF}, C_{IN}: Low leakage capacitors

FIGURE 2. TEST CIRCUIT

Absolute Maximum Ratings

Supply Voltage, V+ to V- . . . . . +15V
Signal Inputs, Pin# 30, 31 (Note 1) . . . . . V+ to V-
Reference Inputs, Pin# 35, 36 . . . . . V+ to V-
Clock Input, OSC1, Pin# 40 (Note 2) . . . . . TEST pin to V+
All Other Analog Leads, Pin# 27-29, 32-34 . . . . . V+ to V-
All Other Digital Leads,
Pin# 2-25, 38, 39 (Note 2) . . . . . TEST Pin to V^+

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^oC/W$)
PDIP Package	50
MQFP Package	80

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature, PDIP Package (Soldering 10s) 300^oC
(MQFP - Lead Tips Only)

Operating Conditions

Operating Temperature, T_A . . . . . 0^oC to 70^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.
2. TEST pin is connected to internally generated digital ground through a 500Ω resistor (see text for TEST pin description).
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

(Notes 5, 6, 7) $T_A = 25^oC$. Device is Tested in the Circuit Shown in Figure 2. Full Scale Range (FSR) = 200.0mV, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Zero Input Reading	V_{IN} = 0V	-000	±000	+000	Reading
Ratiometric Reading	$V_{IN\ HI} = V_{REF\ HI}$, $V_{IN\ LO} = V_{REF\ LO} = V_{COMMON}$ $V_{REF\ HI} - V_{REF\ LO}$ = 100mV	999	999/ 1000	1001	Reading
Rollover Error	V_{IN} = ±199mV	-	±0.2	±1	Count
Linearity Error	FSR = 200mV or 2V (Notes 5, 8)	-	±0.2	±1	Count
Zero Input Reading Drift	V_{IN} = 0V Over Full Temperature Range (Notes 5, 8)	-	±0.2	±1 ±0.01	µV/^oC Count/^oC
Scale Factor Temperature Coefficient	V_{IN} = 199mV, Over Full Temperature Range, Reference Drift Not Included (Notes 5, 8)	-	±1	±5 ±0.01	ppm/^oC Count/^oC
Equivalent Input Noise (Peak-To-Peak Value Not Exceeded 95% of the Time)	V_{IN} = 0V (Notes 5, 8)	-	15 0.15	-	µV Count
INPUT					
Common Mode Voltage Sensitivity	V_{CM} = ±1V, V_{IN} = 0V (Notes 5, 6, 8, 9)	-	-	1 0.01	µV/V Count/V
Input Leakage Current	V_{IN} = 0V (Notes 5, 8)	-	1	10	pA
Overload Recovery Period	V_{IN} Changing from ±10V to 0V (Notes 5, 8)	-	-	1	Conversion Cycle
COMMON PIN					
COMMON Pin Voltage (With Respect to V+, i.e., V+ - V_{COMMON})	V+ to V- = 10V	2.4	2.8	3.2	V
COMMON Pin Voltage Temperature Coefficient	V+ to V- = 10V (Notes 5, 8)	-	150	-	ppm/^oC
COMMON Pin Sink Current	+0.1V Change on V_{COMMON} (Note 5)	-	3	-	mA
COMMON Pin Source Current	-0.1V Change on V_{COMMON} (Note 5)	-	1	-	µA

Electrical Specifications (Notes 5, 6, 7) $T_A = 25^oC$. Device is Tested in the Circuit Shown in Figure 2. Full Scale Range (FSR) = 200.0mV, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DISPLAY DRIVER (HI7131)					
Peak-To-Peak Segment Drive Voltage	V+ to V- = 10V	4	5	6	V
Peak-To-Peak Backplane Drive Voltage		4	5	6	V
POWER SUPPLY (Nominal Supply Voltage; V+ to V- = 10V)					
Supply Current (Does Not Include COMMON Pin Current)	V_{IN} = 0V (Note 10) Oscillator Frequency = 16kHz	-	70	100	µA
Power Dissipation Capacitance	VS Clock Frequency (Notes 5, 8)	-	40	-	pF
DISPLAY DRIVER (HI7133)					
Segment Sink Current (Except Pins 19 and 20)	V+ = +5.0V Driver Pin Voltage = 3.0V	5	8.5	-	mA
Pin 19 Sink Current		10	16	-	mA
Pin 20 Sink Current		4	7	-	mA
POWER SUPPLY Nominal Supply Voltage; V+ = +5V, V- = -5V, Both Respect to GND Pin					
V+ Supply Current (Note 10)	V_{IN} = 0V Oscillator Frequency = 16kHz Does Not Include COMMON Pin and Display Current	-	70	100	µA
V- Supply Current (Notes 5, 10)		-	40	-	µA
Power Dissipation Capacitance	Versus Clock Frequency (Notes 5, 8)	-	40	-	pF

NOTES:

4. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
5. All typical values have been characterized but not tested.
6. See "Parameters Definition" section.
7. Count is equal to one number change in the least significant digit of the display.
8. Parameter not tested on a production basis, guaranteed by design and/or characterization.
9. See "Differential Input" section.
10. 48kHz oscillator increases current by 20µA (Typ).

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**

  $f_{OSC} \approx 0.45/RC_{(OSC)}$
  $C_{OSC} \geq 50pF$
  $R_{OSC} > 50k\Omega$
  $C_{OSC} = 50pF$, $R_{OSC} = 180k\Omega$; f_{OSC} (Typ) = 48kHz

- **CLOCK FREQUENCY**

  $f_{CLOCK} = f_{OSC}/4$

- **CLOCK PERIOD**

  $t_{CLOCK} = 1/f_{CLOCK}$

- **CONVERSION CYCLE**

  $T_{CYC} = 4000 \times t_{CLOCK} = 16000 \times t_{OSC}$
  For f_{OSC} = 40kHz; T_{CYC} = 400ms

- **SIGNAL INTEGRATION PERIOD**

  $T_{INT} = 1000 \times t_{CLOCK}$

- **60/50Hz REJECTION CRITERIA**

  T_{INT} / t_{60Hz} or T_{INT} / t_{50Hz} = Integer

- **OPTIMUM FULL SCALE ANALOG INPUT RANGE**

  V_{INFS} = 200mV to 2V

- **INPUTS VOLTAGE RANGE**
  $(V- + 1V) < V_{IN\ LO}$ or $V_{IN\ HI} < (V+ - 1V)$

- **MAXIMUM INTEGRATION CURRENT**

  $I_{INT(MAX)} = V_{INFS} / R_{INT}$
  Maximum integration current should be the maximum buffer output current with no nonlinearity effect.
  Maximum Buffer Output Current = 1μA

- **INTEGRATOR MAXIMUM OUTPUT VOLTAGE SWING**

  $V_{INT(MAX)} = (T_{INT})\ (I_{INT(MAX)})/C_{INT}$
  $(V- + 0.5) < V_{INT(MAX)} < (V+ - 0.5)$
  (Typ) $V_{INT(MAX)}$ = 2V

- **INTEGRATING RESISTOR**

  $R_{INT} = V_{INFS} / I_{INT(MAX)}$

- **INTEGRATING CAPACITOR**

  $C_{INT} = (T_{INT})\ (I_{INT(MAX)}) / V_{INT(MAX)}$

- **AUTO-ZERO CAPACITOR VALUE**

  REFERENCE CAPACITOR VALUE
  $0.1\mu F < C_{REF} < 1\mu F$

- **REFERENCE INPUTS VOLTAGE RANGE**

  $V- < V_{REFLO}$ or $V_{REFHI} < V+$

- **REFERENCE VOLTAGE**

  $V_{REF} = V_{INFS}/2$

- **COMMON PIN VOLTAGE**

  $V_{COMMON} = V+ - 2.8$, (Typ), V_{COMMON} is regulated and can be used as a reference. It is biased between V+ and V- and regulation is lost at $(V+ - V-) < 6.8V$. V_{COMMON} pin does not have sink capability and can be externally pulled down to lower voltages.

- **DISPLAY TYPE**

  LCD, Non-Multiplexed

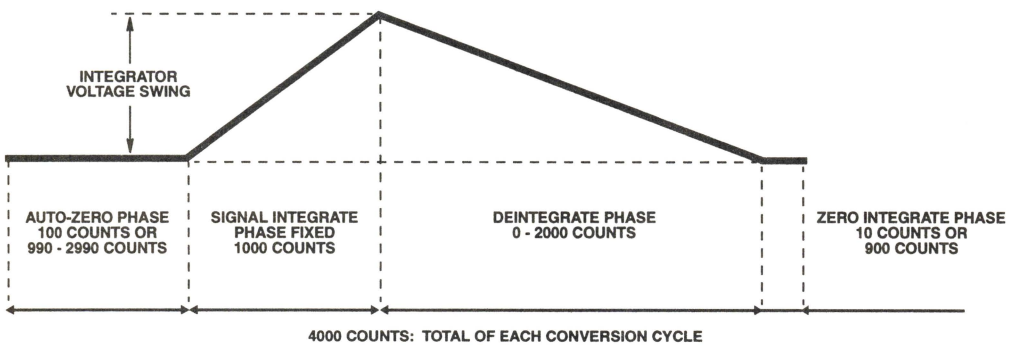
- **POWER SUPPLY, V+ TO V-**

  Single +9V or 5V Nominal, +5V to +12V Functional

- **DISPLAY READING**

  Reading = $1000 \times (V_{IN} / V_{REF})$
  Maximum Reading = 1999, for $V_{IN} = 1.999 \times V_{REF}$

Typical Integrator Amplifier Output Waveform (INT Pin)



NOTE: 1 Count = 1 Clock Cycle = 4 Oscillator Cycles.

Pin Descriptions

PIN NUMBER		NAME	FUNCTION	DESCRIPTION
40 PIN DIP	44 PIN FLATPACK			
1	8	V+	Supply	Power Supply.
2	9	D1	Output	Driver Pin for Segment "D" of the display units digit.
3	10	C1	Output	Driver Pin for Segment "C" of the display units digit.
4	11	B1	Output	Driver Pin for Segment "B" of the display units digit.
5	12	A1	Output	Driver Pin for Segment "A" of the display units digit.
6	13	F1	Output	Driver Pin for Segment "F" of the display units digit.
7	14	G1	Output	Driver Pin for Segment "G" of the display units digit.
8	15	E1	Output	Driver Pin for Segment "E" of the display units digit.
9	16	D2	Output	Driver Pin for Segment "D" of the display tens digit.
10	17	C2	Output	Driver Pin for Segment "C" of the display tens digit.
11	18	B2	Output	Driver Pin for Segment "B" of the display tens digit.
12	19	A2	Output	Driver Pin for Segment "A" of the display tens digit.
13	20	F2	Output	Driver Pin for Segment "F" of the display tens digit.
14	21	E2	Output	Driver Pin for Segment "E" of the display tens digit.
15	22	D3	Output	Driver pin for segment "D" of the display hundreds digit.
16	23	B3	Output	Driver pin for segment "B" of the display hundreds digit.
17	24	F3	Output	Driver pin for segment "F" of the display hundreds digit.
18	25	E3	Output	Driver pin for segment "E" of the display hundreds digit.
19	26	AB4	Output	Driver pin for both "A" and "B" segments of the display thousands digit.
20	27	POL	Output	Driver pin for the negative sign of the display.
21	28	BP/GND	Output	Driver pin for the LCD backplane/Power Supply Ground.
22	29	G3	Output	Driver pin for segment "G" of the display hundreds digit.
23	30	A3	Output	Driver pin for segment "A" of the display hundreds digit.
24	31	C3	Output	Driver pin for segment "C" of the display hundreds digit.
25	32	G2	Output	Driver pin for segment "G" of the display tens digit.
26	34	V-	Supply	Negative power supply.
27	35	INT	Output	Integrator amplifier output. To be connected to integrating capacitor.
28	36	BUFF	Output	Input buffer amplifier output. To be connected to integrating resistor.
29	37	A-Z	Input	Integrator amplifier input. To be connected to auto-zero capacitor.
30 31	38 39	IN LO IN HI	Input	Differential inputs. To be connected to input voltage to be measured. LO and HI designators are for reference and do not imply that LO should be connected to lower potential, e.g., for negative inputs IN LO has a higher potential than IN HI.
32	40	COMMON	Supply/ Output	Internal voltage reference output.
33 34	41 42	C_{REF-} C_{REF+}		Connection pins for reference capacitor.
35 36	43 44	REF LO REF HI	Input	Input pins for reference voltage to the device. REF HI should be positive reference to REF LO.
37	3	TEST	Input	Display test. Turns on all segments when tied to V+.
38 39 40	4 6 7	OSC3 OSC2 OSC1	Output Output Input	Device clock generator circuit connection pins.

Definition of Specifications

Count

A Count is equal to one number change in the least significant digit of the display. The analog size of a count referred to ADC input is:

$$\text{Analog Count Size} = \frac{\text{Full Scale Range}}{\text{Max Reading} + 1},$$

Max reading +1 for a $3^1/_2$ digit display is 2000 (1999+1).

Zero Input Reading

The reading of the ADC display when input voltage is zero and there is no common mode voltage, i.e., the inputs are shorted to COMMON pin.

Ratiometric Reading

The reading of the ADC display when input voltage is equal to reference voltage, i.e., IN HI tied to REF HI and IN LO tied to REF LO and COMMON pins. The accuracy of reference voltage is not important for this test.

Rollover Error

Difference in the absolute value reading of ADC display for equal magnitude but opposite polarity inputs. The input voltage should be close to full scale, which is the worst case condition.

Linearity

Deviation of the ADC transfer function (output reading versus input voltage transfer plot) from the best straight line fitted to ADC transfer plot.

Scale Factor Temperature Coefficient

The rate of change of the slope of ADC transfer function due to the change of temperature.

Equivalent Input Noise

The total random uncertainty of the ADC for converting a fixed input value to an output reading. This uncertainty is referred to input as a noise source which produces the equivalent effect. It is given for zero input and is expressed as Peak-to-Peak noise value and submultiples of Counts.

Overload Recovery Period

A measure of how fast the ADC will display an accurate reading when input changes from an overload condition to a value within the range. This is given as the number of conversion cycles required after the input goes within the range.

Theory of Operation

The HI7131 and HI7133 are dual-slope integrating type A/D converters. As the name implies, its output represents the integral or average of the input signal. A basic block diagram of a dual-slope integrating converter is shown in Figure 3. A conventional conversion cycle has two distinct phases:

First, the input signal is integrated for a fixed interval of time. This is called the signal integration phase. In this phase, the input of the integrator is connected to the input signal through the switch. During this time, charge builds up on C_{INT}, which is proportional to the input voltage.

The next phase is to discharge C_{INT}. This is called reference integration or deintegration phase, with the use of a fixed reference voltage. The time it takes to discharge the C_{INT} is directly proportional to the input signal. This time is converted to a digital readout by means of a BCD counter, driven by a clock oscillator. During this phase, the integrator input is connected to an opposite polarity reference voltage through the switch to discharge C_{INT}.

Notice that during the integration phase, the rate of charge built up on the capacitor is proportional to the level of the input signal, and there is a fixed period of time to integrate the input. However, during the discharge cycle the rate of discharge is fixed and there is a variable time period for complete discharge.

A $3^1/_2$ digit BCD counter is shown in the block diagram, the period of integration is determined by 1000 counts of this counter. Just prior to a measurement, the counter is reset to zero and C_{INT} has no charge. At the beginning of the measurement, the control logic enables the counter and the integrator input is connected to the input node. Charge begins accumulating on C_{INT} and the output of the integrator moves down or up respectively for positive or negative inputs. This process continues until the counter reaches 1000 counts. This will signal the control logic for the start of the deintegrating cycle. The control logic resets the counter and connects the integrator input to a reference voltage opposite to that of the input signal. The charge accumulated on C_{INT} is now starting to be removed and the counter starts to count up again. As soon as all the charge is removed, the output of the integrator reaches 0V. This is detected by the comparator and the control logic is signaled for the end of a measurement cycle. At this time the number accumulated in the counter is the representation of the input signal. This number will be stored on the latches and displayed until the end of the next measurement cycle.

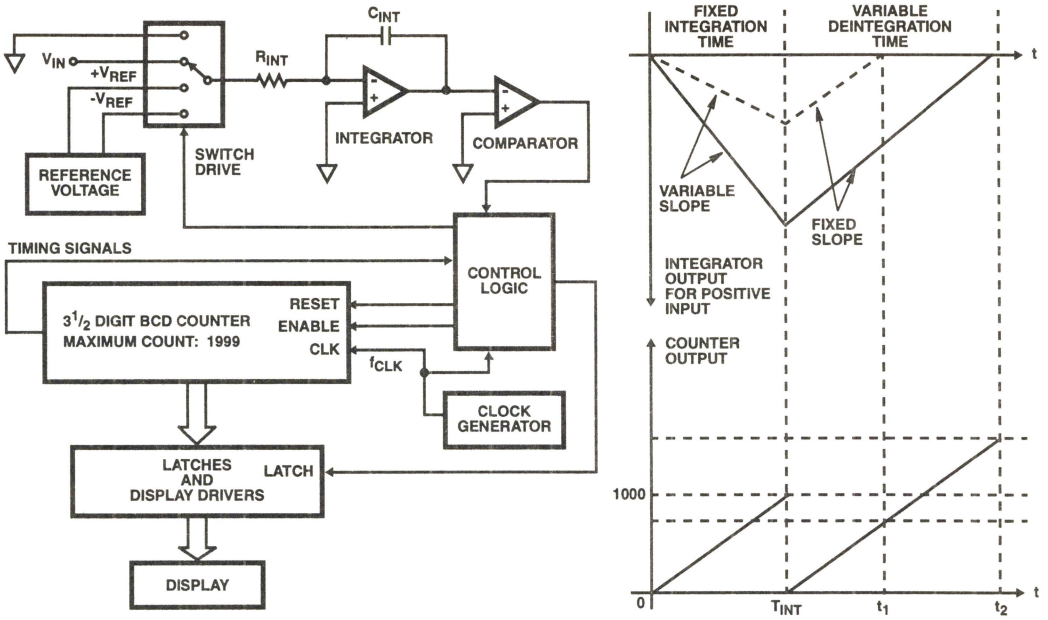


FIGURE 3. DUAL SLOPE INTEGRATING A/D CONVERTER

Figure 3 shows a typical waveform of the integrator output for 2 different positive input values and the associated representation of the counter output for those inputs. T_{INT} is the time period of integrating phase. t_1 and t_2 are the end of measurement for 2 different inputs.

The dual slope integrating technique puts the primary responsibility for accuracy on the reference voltage. The values of R_{INT} and C_{INT} and the clock frequency (f_{CLK}) are not important, provided they are stable during each conversion cycle. This can be expressed mathematically as follows:

$$\Delta V_{INT} = \frac{1}{R_{INT}C_{INT}} \int_0^{T_{INT}} V_{IN}dt = \frac{1}{R_{INT}C_{INT}} \int_0^{T_{DEINT}} V_{REF}dt$$

$$\Delta V_{INT} = \frac{\overline{V_{IN}}T_{INT}}{R_{INT}C_{INT}} = \frac{V_{REF}t_{DEINT}}{R_{INT}C_{INT}}$$

$\overline{V_{IN}}$: Input Average Value During Integration Time

$$T_{INT} = 1000\left(\frac{1}{f_{CLK}}\right)$$

$$t_{DEINT} = \text{Accumulated Counts}\left(\frac{1}{f_{CLK}}\right)$$

$$\text{Accumulated Counts} = 1000\frac{\overline{V_{IN}}}{V_{REF}} = \text{Display Reading}$$

It can be seen that the output reading of the ADC is only proportional to the ratio of V_{IN} over V_{REF}. The last equation also demonstrates that for the maximum display reading (i.e., 1999) we will have $V_{IN} = 1.999\ V_{REF}$. This implies that in this configuration the full scale range of the converter is twice its reference voltage.

The inherent advantages of integrating A/D converters are; very small nonlinearity error, no possibility of missing codes and good high frequency noise rejection.

Furthermore, the integrating converter has extremely high normal mode rejection of frequencies whose periods are an integral multiple of the integrating period (T_{INT}). This feature can be used to reject the line frequency related noises which are riding on input voltage by appropriate selection of clock frequency. This is shown in Figure 4.

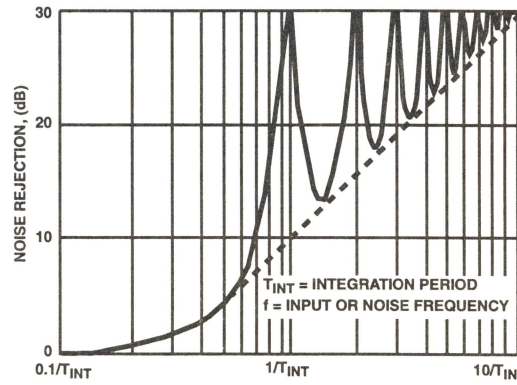


FIGURE 4. NOISE REJECTION FOR INTEGRATING TYPE A/D CONVERTER

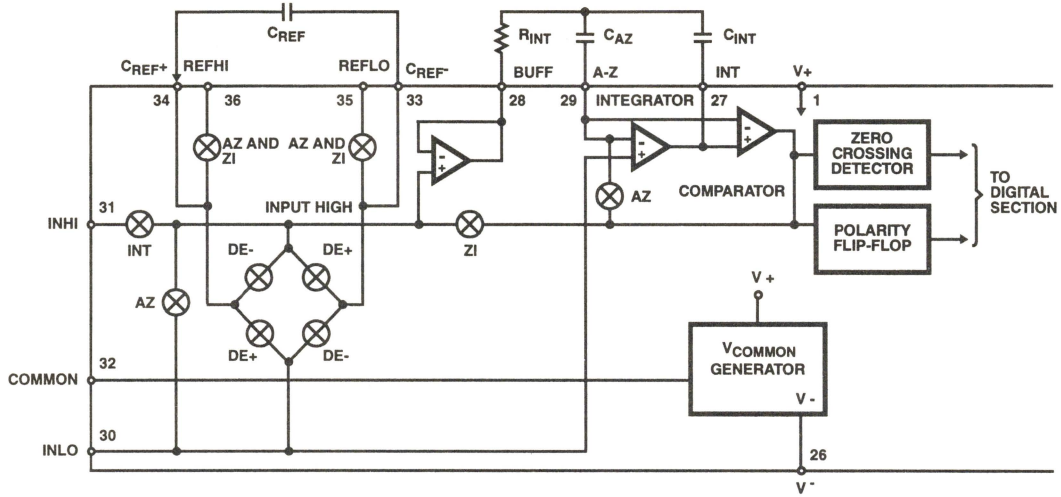


FIGURE 5A. HI7131 AND HI7133 ANALOG SECTION FUNCTIONAL DIAGRAM

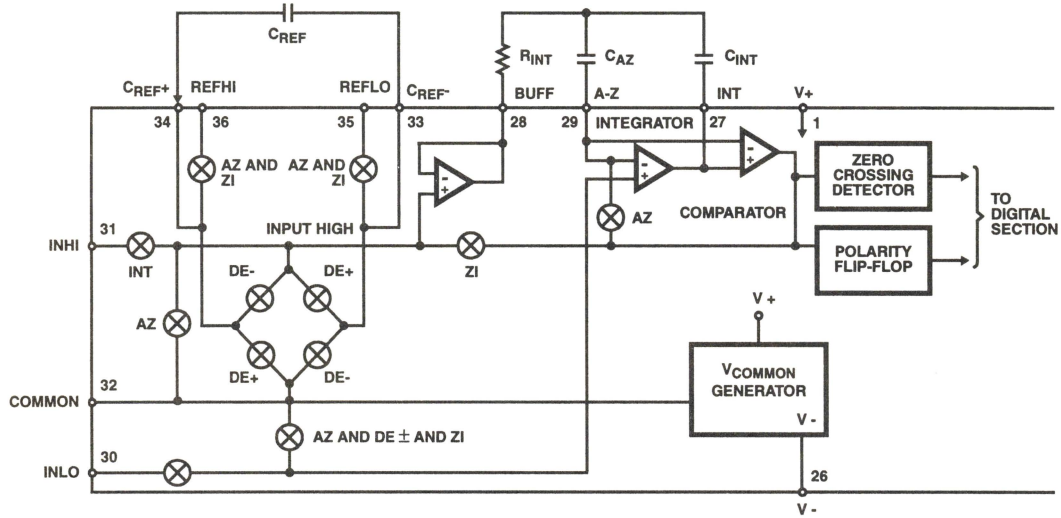


FIGURE 5B. ICL7136 AND ICL7137 ANALOG SECTION FUNCTIONAL DIAGRAM

FIGURE 5. HI7131, HI7133 vs ICL7136, ICL7137 ANALOG SECTIONS

HI7131/33 vs ICL7136/37

Figure 5 shows the analog front end block diagram of both HI7131/33 and ICL7136/37. The difference is the common reference voltage generator connection and 2 extra analog switches in the ICL7136. The HI7131 architecture uses the INLO as the reference point of the integrator (non-inverting input of the integrator amplifier) in all the phases of the conversion cycle. The ICL7136 uses INLO as a reference point only during integration cycle and COMMON pin is used as the integrator reference point during auto-zero, deintegrate, and zero integrate phases.

The circuit configuration of the HI7131 results in a superior 120dB rejection of DC common mode on the inputs. However, the HI7131 has reduced AC common mode noise rejection, since the noise on the INLO input can cause errors during the deintegration phase.

The circuit configuration of the ICL7136 is unaffected by the AC noise riding on the inputs, but the DC common mode rejection on the input is only 86dB.

Analog Section Description

Figure 5A shows a simplified diagram of the analog section of the HI7131 and HI7133. The circuit performs basic phases of dual slope integration. Furthermore, the device incorporates 2 additional phases called "Auto-Zero" and "Zero Integrate". The device accepts differential input signals and reference voltages. Also, there is a reference voltage generator which sets the COMMON pin 2.8V below the V+ supply. A complete conversion cycle is divided into the following four phases:

1. Auto-Zero (A/Z)
2. Signal Integrate (INT)
3. Deintegrate or Reference Integrate (DE±)
4. Zero Integrate (ZI)

Digitally controlled analog switches direct the appropriate signals for each phase of the conversion.

Auto-Zero Phase

During auto-zero three things occur. First, IN HI is disconnected from the device internal circuitry and internally shorted to IN LO. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} and integrating capacitor C_{INT} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A/Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

Signal Integrate Phase

During signal integrate the auto-zero loop is opened and the internal INPUT HIGH is connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide input common mode range: up to 1V from either supply. At the end of this phase, the polarity of the integrated signal is determined.

Deintegrate Phase

During this phase the IN LO and the internal INPUT HIGH are connected across the previously charged reference capacitor. The bridge type circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. As specified before, the digital reading displayed is:

$$\text{DIGITAL READING} = 1000\left(\frac{V_{INHI} - V_{INLO}}{V_{REFHI} - V_{REFLO}}\right).$$

Zero Integrate Phase

This phase is provided to eliminate overrange hangover and causes fast recovery from heavy overrange. During this phase a feedback loop is closed around the system by connecting comparator output to internal INPUT HIGH. This will discharge the integrator capacitor (C_{INT}), causing the integrator output return to zero. During this phase the reference capacitor is also connected to reference input, charging to the reference voltage.

A typical integrator output voltage during different phases is shown on the "Design Information Summary Sheet." This integrator output is for negative inputs and is referred to IN LO. For positive inputs the integrator output will go negative.

Digital Section Description

Figure 6 shows the block diagram of the digital section of the HI7131. The diagram shows the clock generator, control logic, counters, latches and display decoder drivers. An internal digital ground is generated from a 6V Zener diode and a large P-Channel source follower. This supply is capable of absorbing the relatively large capacitive currents when the LCD backplane (BP) and segment drivers are switched.

Display Drivers

A typical segment output driver consists of P-Channel and N-Channel MOSFETs.

An LCD consists of a backplane (BP) and segments. BP covers the whole area under the segments. Because of the nature of the LCDs, they should be driven by square waves. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square-wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

The HI7131 is a direct display drive (versus multiplexed) and each segment in each digit has its own segment driver. The display font and the segment assignment on the display are also shown in Figure 6.

Figure 6 shows the block diagram of the digital section of the HI7133. The diagram shows the clock generator, control logic, counters, latches and display decoder drivers. The supply rails of the digital circuitry are V+ and GND.

Display Drivers

A typical segment output consists of a P-Channel and an N-Channel MOSFET. This configuration is designed to drive common anode LED displays. The nominal sink current for each segment is 8mA, a typical value for instrument size common anode LED displays. The driver for the thousand digit is twice as big as other segments and can sink 16mA since it is actually driving 2 segments. The sink current for the polarity driver is 7mA. The polarity driver is on for negative inputs. The HI7133 is a direct display drive (versus multiplexed) and each segment in each digit has its own segment driver. The display font and the segment assignment on the display are also shown in Figure 7.

Clock Generator

The clock generator circuit basically includes 2 CMOS inverters and a divide-by-4 counter. It is designed to be used in 2 different basic configurations.

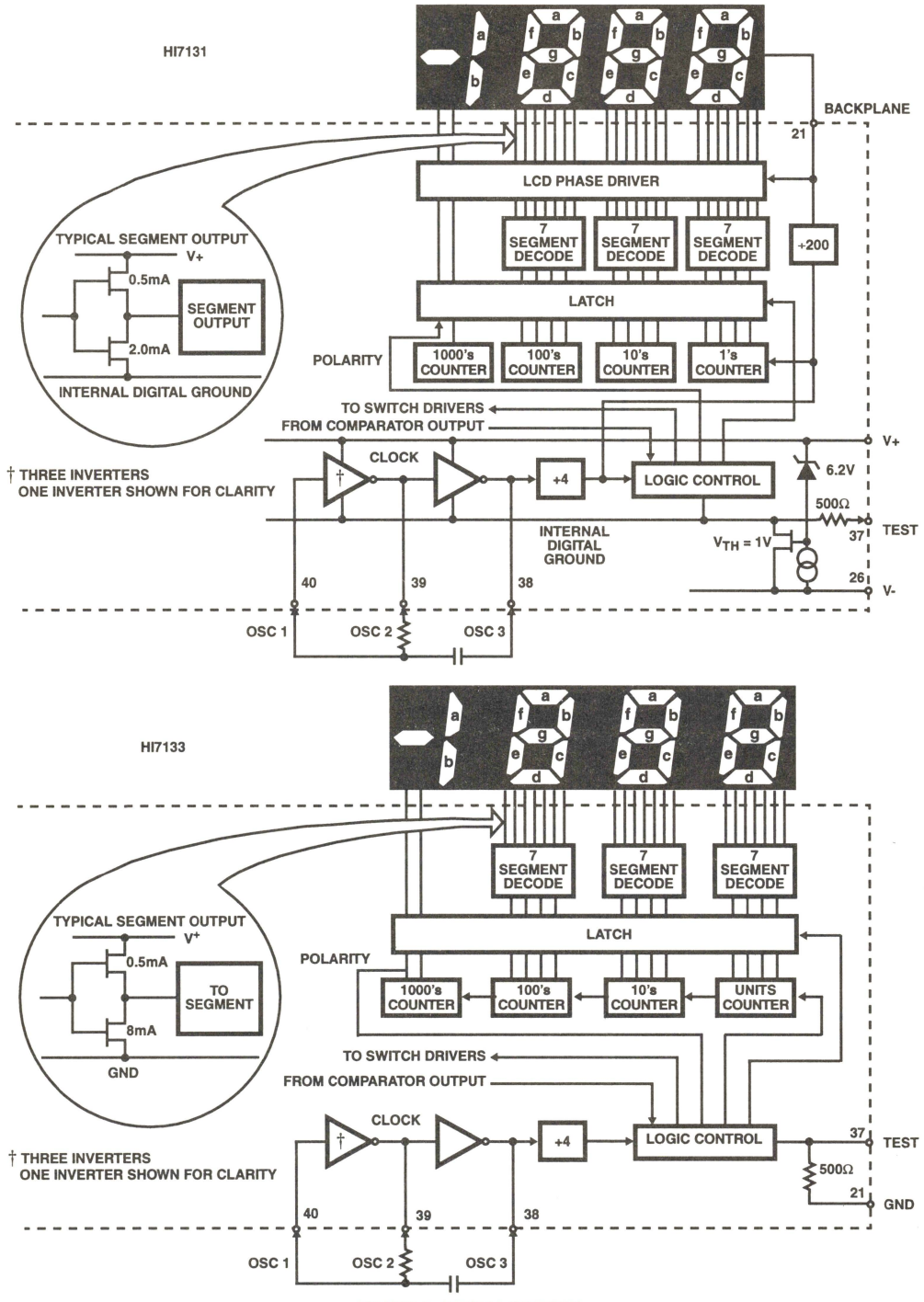


FIGURE 6. DIGITAL SECTION

1. Figure 7A, an External Oscillator Driving OSC 1.
2. Figure 7B, an RC Oscillator Using All 3 Oscillator Circuit Pins.

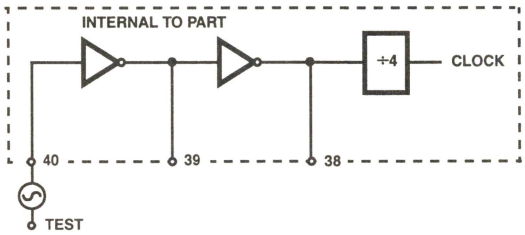


FIGURE 7A. EXTERNAL SIGNAL

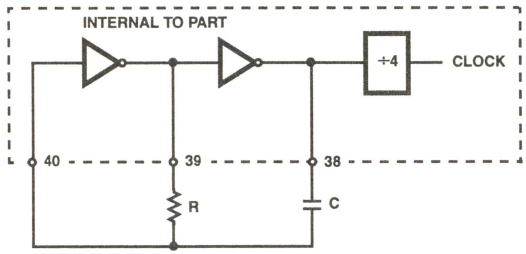


FIGURE 7B. RC OSCILLATOR

FIGURE 7. CLOCK CIRCUITS

The oscillator output frequency is divided by 4 before it clocks the rest of the digital section. Notice that there are 2 separate frequencies which are referred to as; oscillator frequency (f_{OSC}) and clock frequency (f_{CLK}) with the relation of:

$$f_{CLK} = \frac{f_{OSC}}{4}$$

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. For 60Hz, rejection oscillator frequencies of 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, $33^1/_3$kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of, 100kHz, $66^2/_3$kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/sec) will reject both 50Hz and 60Hz (also 400Hz and 440Hz).

For the RC oscillator configuration the relationship between oscillator frequency, R and C values are:

$$f_{OSC} \approx \frac{0.45}{R_{OSC}C_{OSC}}$$

(R in Ohms and C in Farads.)

System Timing

As it has been mentioned, the oscillator output is divided by 4 prior to clocking the digital section and specifically, the internal decade counters. The control logic looks at the counter outputs and comparator output (see analog section) to form the appropriate timing for 4 phases of conversion cycle.

The total length of a conversion cycle is equal to 4000 counts and is independent of the input signal magnitude or full scale range. Each phase of the conversion cycle has the following length:

Auto-Zero Phase

100 counts in case an overrange is detected. 990 to 2990 counts for normal conversion. For those inputs which are less than full scale, the deintegrate length is less than 2000 counts. Those extra counts on deintegrate phase are assigned to auto-zero phase to keep the conversion cycle constant.

Signal Integrate Phase

1000 counts, a fixed period of time. The time of integration can be calculated as:

$$T_{INT} = 1000\left(\frac{1}{f_{CLK}}\right) = 4000\left(\frac{1}{f_{OSC}}\right).$$

Deintegrate Phase

0 to 2000 counts, variable length phase depending on the input voltage.

Zero Integrate Phase

10 counts in case of normal conversion. 900 counts in case an overrange is detected.

Functional Considerations of Device Pins

COMMON Pin

The COMMON pin is the device internal reference generator output.

The COMMON pin sets a voltage that is about 2.8V less than the V+ supply rail. This voltage (V+ - V_{COMMON}) is the on-chip reference which can be used for setting converter reference voltage.

Within the IC, the COMMON pin is tied to an N-Channel transistor capable of sinking up to 3mA of current and still keeping COMMON voltage within the range. However, there is only 1µA of source current capability. The COMMON pin can be used as a virtual ground in single supply applications when the external analog signals need a reference point in between the supply rails. If higher sink and source current capability is needed for virtual ground a unity gain op-amp can be used as a buffer.

Differential Inputs (IN LO, IN HI)

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 1V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 120dB (Typ). However, care must be exercised to assure the integrator output does not saturate. This is illustrated in Figure 8, which shows how common mode voltage affects maximum swing on the integrator output. Figure 8 shows the circuit configuration during conversion. In this figure, common mode voltage is considered as a voltage on the IN LO pin referenced to (V+ - V-) / 2, which is usually the GND in a dual supply system.

A worst case condition would be a large positive common-mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

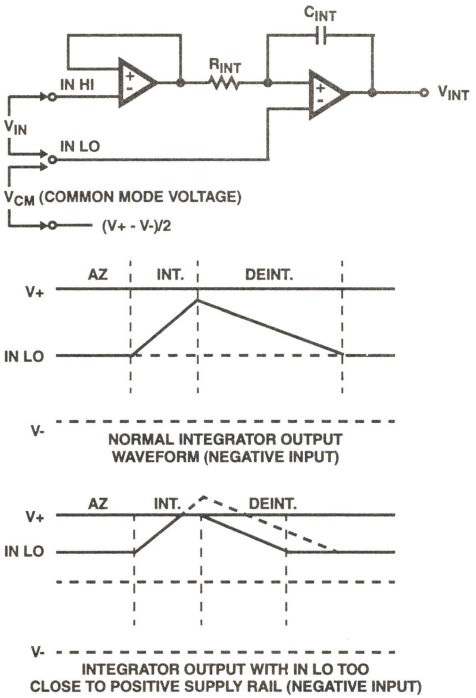


FIGURE 8. COMMON MODE VOLTAGE CONSIDERATION

Differential Reference (REF HI, REF LO) and Reference Capacitor Pins (C_{REF}+, C_{REF}-)

As was discussed in the analog section (Figure 5), the differential reference pins are connected across the reference capacitor (connected to pins C_{REF}+ and C_{REF}-) to charge it during the zero integrate and the auto-zero phase. Then the reference capacitor is used as either a positive or negative reference during the deintegrate phase. The reference capacitor acts as a flying capacitor between the reference voltage and integrator inputs in the deintegrate phase.

The common mode voltage range for the reference inputs is V+ to V-. The reference voltage can be generated anywhere within the power supply range of the converter. The main source of rollover error is reference common mode voltage caused by the reference capacitor losing or gaining charge to or from stray capacitance on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called upon to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This change in reference for positive or negative input voltage will give a rollover error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitances, this error can be held to less than 0.5 counts worst case. See the "Component Value Selection" section for auto-zero capacitor value.

TEST Pin

The TEST pin serves two functions. It is coupled to the internally generated digital ground through an effective 500Ω resistor. Thus, it can be used as the digital ground for external digital circuits such as segment drivers for decimal points or any other annunciator the user may want to include on the LCD display. For these applications the external digital circuit should be supplied between V+ and TEST pin. Figures 9 and 10 show such an application. In Figure 9 a MOSFET transistor is used to invert the BP signal to drive the decimal point. The MOSFET can be any general purpose type with a threshold voltage less than 3.5V and ON resistance less than 500Ω. Figure 10 uses an CMOS IC XOR gate to generate controllable decimal point drives. No more than a 1mA load should be applied to TEST pin by any external digital circuitry.

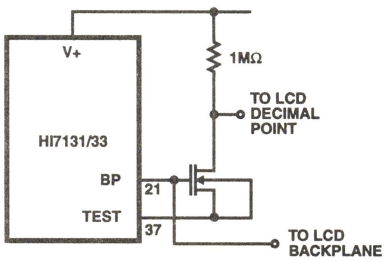


FIGURE 9. SIMPLE INVERTER FOR FIXED DECIMAL POINT DRIVE

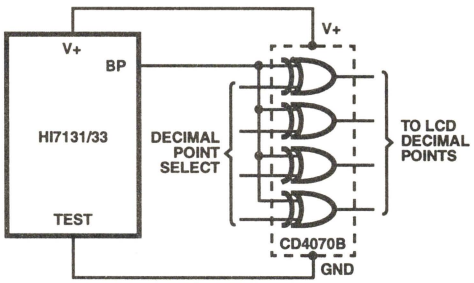


FIGURE 10. EXCLUSIVE "OR" GATE FOR DECIMAL POINTS AND ANNUNCIATORS DRIVE

The second function of the TEST pin is the "lamp test". When the TEST pin is pulled high (to V+) all segments will be turned on and the display should read -1888. The test pin will sink about 10mA under these conditions.

CAUTION: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

Component Selection

Integrating resistors and capacitors (R_{INT}, C_{INT}): A guideline to achieving the best performance from an integrating A/D converter is to try to reduce the value of R_{INT}, increase the value of C_{INT}, while having the highest possible voltage swing at the output of the integrator. This will reduce the sensitivity of the circuit to noise and leakage currents. In addition to these guidelines the circuit limitations should also be considered.

To determine R_{INT}, the imposed circuit limitation is the maximum output drive current of the buffer amplifier (see Figure 5) while maintaining its linearity. This current for the buffer amplifier is about 1μA. The R_{INT} resistor can be calculated from the expression:

$$R_{INT} = \frac{V_{IN}(\text{Full Scale})}{1\mu A}$$

The standard optimum values for R_{INT} are 180kΩ for 200mV full scale and 1.8MΩ for 2V full scale. Type of resistor and its absolute value is not critical to the accuracy of conversion, as was discussed previously.

The integrating capacitor should be selected to yield the maximum allowable voltage range to the integrator output (INT pin). The maximum allowable range does not saturate the integrator output. The integrator output can swing up or down to 0.3V from either supply rail and still maintain its linearity.

A nominal ±2V maximum range is optimum. The maximum range values are selected in order to leave enough room for all the component and circuit tolerances and for a reasonable common mode voltage range. The C_{INT} value can now be calculated as:

$$C_{INT} = \frac{T_{INT} I_{INT}}{V_{INTMAX}},$$

Where T_{INT} depends on clock frequency and was discussed before and I_{INT} is expressed as:

$$I_{INT} = \frac{V_{IN}(\text{Full Scale})}{R_{INT}}.$$

For 48kHz nominal oscillator frequency (12kHz clock internal frequency), R_{INT} equals 180kΩ for 1.8MΩ for the above mentioned swing, the optimum value for C_{INT} is 0.047μF.

An additional requirement of the integrating capacitor is to choose low dielectric absorption. This will minimize the converter's rollover, linearity and gain error. Furthermore, the integrating capacitor should also have low leakage current. Different types of capacitors are adequate for this application; polypropylene capacitors provide undetectable errors at reasonable cost and size. The absolute value of C_{INT} does not have any effect on accuracy.

Auto-Zero Capacitor (C_{AZ})

The value of the auto-zero capacitor has some influence on the noise of the converter. A larger value C_{AZ} has less sensitivity to noise. For 200mV full scale (resolution of 100μV), where noise is important, a 0.47μF or greater is recommended. On the 2V full scale, (resolution of 1mV), a 0.047μF capacitor is adequate for low noise.

The auto-zero capacitor should be a low leakage type to hold the voltage during conversion cycle. A mylar or polypropylene capacitor is recommended for C_{AZ}.

Reference Capacitor (C_{REF})

As discussed earlier, the input to the integrator during the deintegrate phase is the voltage at the reference capacitor. The sources of error related to the reference capacitor are stray capacitances at the C_{REF} terminals, and the leakage currents. Where a large common mode voltage exists for V_{REF}, the stray capacitances increase the rollover error by absorbing or pumping charge onto C_{REF} when positive or negative inputs are measured. Leakage of the capacitor itself or leakages through circuit boards will drop the voltage across C_{REF} and cause gain and rollover errors. The circuit boards should be designed to minimize stray capacitances and should be well cleaned to reduce leakage currents.

A 0.1μF capacitor for C_{REF} should work properly for most applications. When common mode voltage exists or at higher temperatures (where device leakage currents increase) a 1.0μF reference capacitor is recommended to reduce errors. The C_{REF} capacitor can be any low leakage type, a mylar capacitor is adequate.

Those applications which have variable reference voltage should also use a low dielectric absorption capacitor such as polypropylene, for example, a ratiometric measurement of resistance.

Oscillator Components

When an RC type of oscillator is desired, the oscillator frequency is approximately expressed by:

$$f_{OSC} = \frac{0.45}{RC},$$

(R in Ohms and C in Farads), where R > 50kΩ and C > 50pF. For 40kHz frequency which gives 2.5 readings per second, use 100K and 100pF or use 180kΩ and 50pF for lower power loss.

There is a typical variation of about 5% between oscillator frequencies of different parts. The oscillator frequency will decrease 1% for each 25°C rise. For those applications in which normal mode rejection of 60Hz or 50Hz line frequency is critical, a crystal or a precision external oscillator should be used.

Reference Voltage Selection

For a full scale reading the input signal is required to be twice the reference voltage. To be more precise, the full scale reading (±1999) takes place when the input is 1.999 times the V_{REF}. V_{REF} is the potential difference between REF HI and REF LO inputs. Thus, for the nominal 200mV and 2V ranges, V_{REF} should be 100mV and 1V respectively.

In many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and adjust the V_{REF} for 0.341V. Suitable values for integrating resistor and capacitor would be 620kΩ and 0.047μF. This makes the system slightly quieter and also avoids a divider network on the input.

The on-chip voltage reference (V+ - V_{COMMON}) is normally used to provide the converter reference voltage. However, some applications may desire to use an external reference generator. Various possible schemes exist for reference voltage settings. Figure 11 shows the normal way of using on-chip reference and also a way of using external reference. The value of resistors on both circuit depends on the converter input voltage range. Refer to "Typical Applications" section for various schemes.

Typical Applications

The HI7131 and HI7133 A/D Converters may be used in a wide variety of configurations. The following application circuits show some of the possibilities, and serves to illustrate the exceptional versatility of these devices.

The following application notes contain very useful information on understanding and applying these parts and are available from Harris Semiconductor.

Application Notes

NOTE #	DESCRIPTION	AnswerFAX DOC. #
AN016	"Selecting A/D Converters"	9016
AN017	"The Integrating A/D Converter"	9017
AN018	"Do's and Don'ts of Applying A/D Converters"	9018
AN032	"Understanding the Auto-Zero and Common Mode Performance of the ICL7136/7/9 Family"	9032
AN052	"Tips for Using Single Chip $3^1/_2$ Digit A/D Converters"	9052

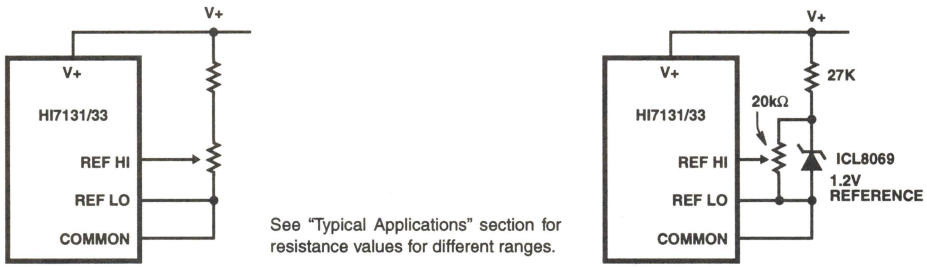
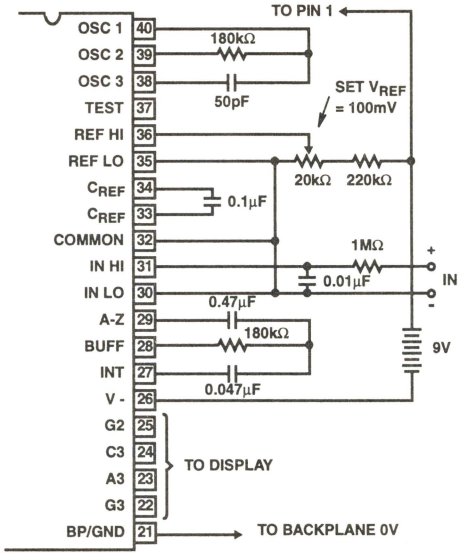


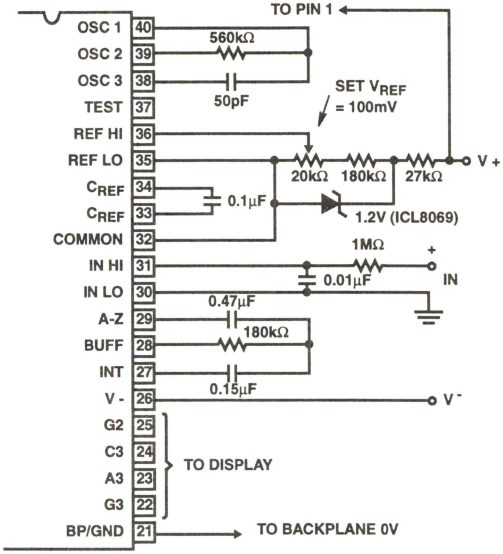
FIGURE 11. HI7131 TYPICAL REFERENCE CIRCUITS

Typical Applications



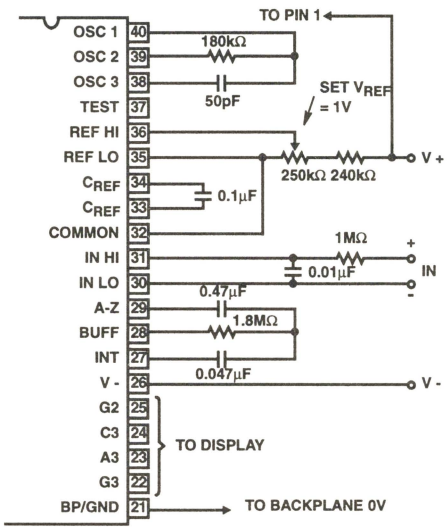
Values shown are for 200mV full-scale, 3 readings/sec., floating supply voltage (9V battery).

FIGURE 12. HI7131 AND HI7133 USING THE INTERNAL REFERENCE



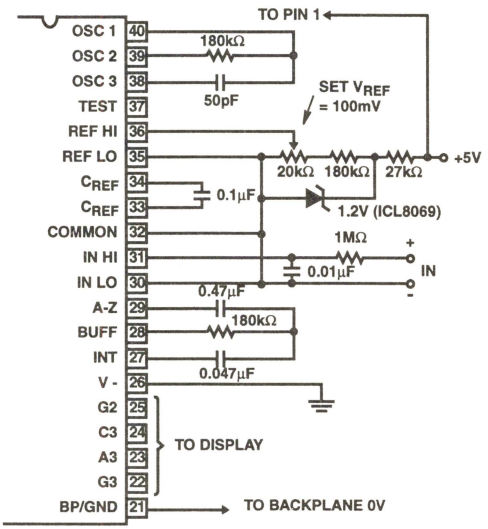
IN LO is tied to supply GND establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.

FIGURE 13. HI7131 AND HI7133 WITH AN EXTERNAL BAND-GAP REFERENCE (1.2V TYPE)



For 1 reading/sec., change C_{INT}, R_{OSC} to values of Figure 12.

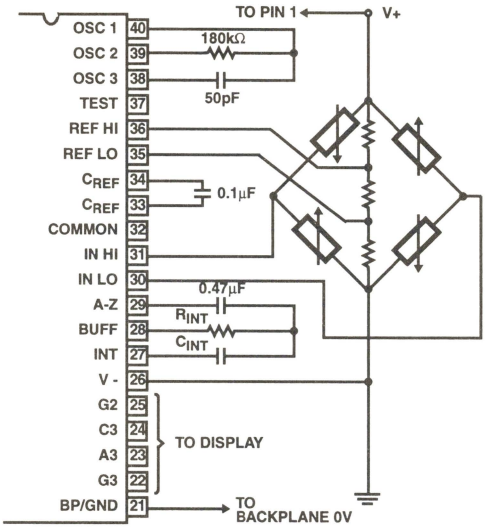
FIGURE 14. RECOMMENDED COMPONENT VALUES FOR 2.000V FULL-SCALE, 3 READINGS/SEC



An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference. COMMON holds the IN LO almost at the middle of the supply, ≈ 2.7V.

FIGURE 15. HI7131 AND HI7133 OPERATED FROM SINGLE +5V SUPPLY

Typical Applications (Continued)



The resistor values within the bridge are determined by the desired sensitivity.

FIGURE 16A. HI7131 AND HI7133 MEASURING RATIOMETRIC VALUES OF QUAD LOAD CELL

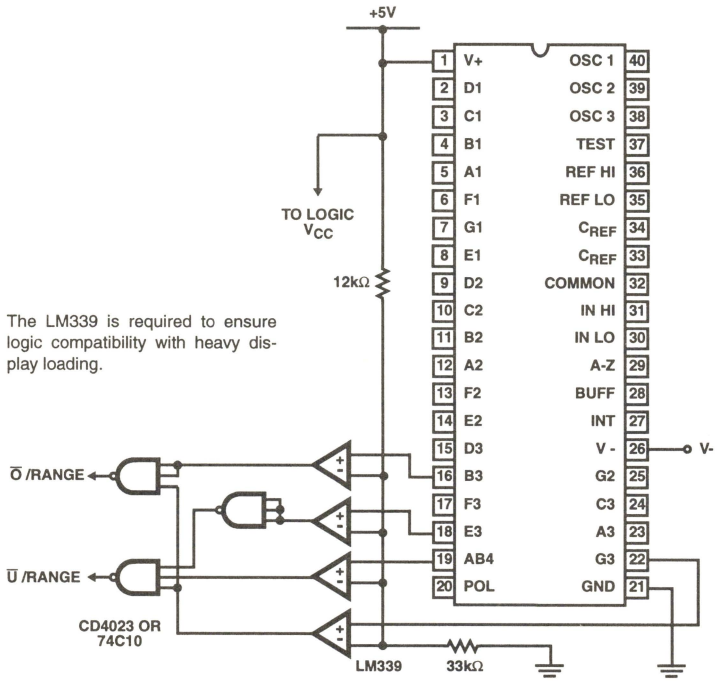
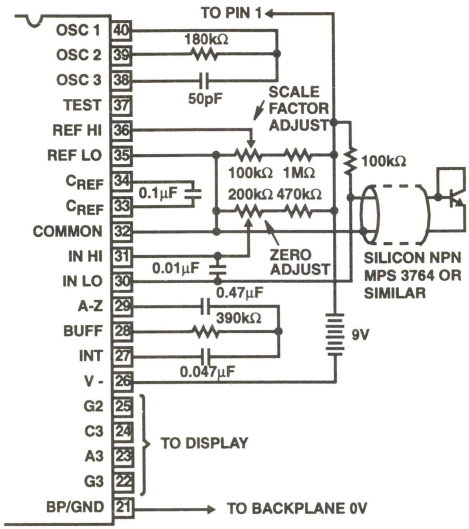


FIGURE 16B. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM HI7133 OUTPUTS

FIGURE 16.

Typical Applications (Continued)



A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading. See AD590 data sheets for alternative circuits.

FIGURE 17A. HI7131 AND HI7133 USED AS A DIGITAL CENTIGRADE THERMOMETER

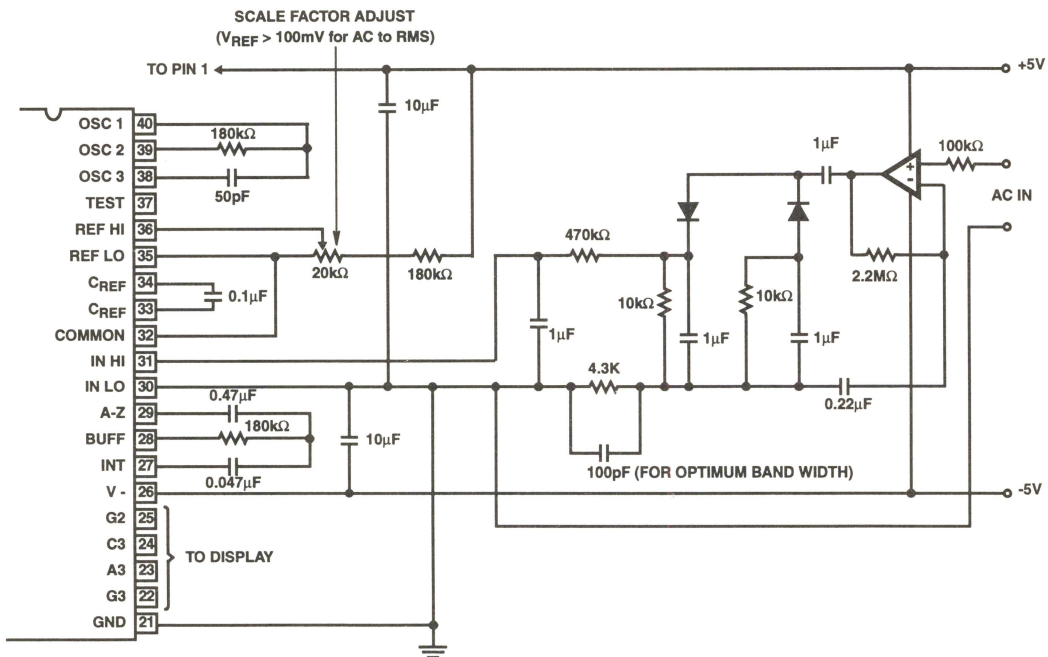
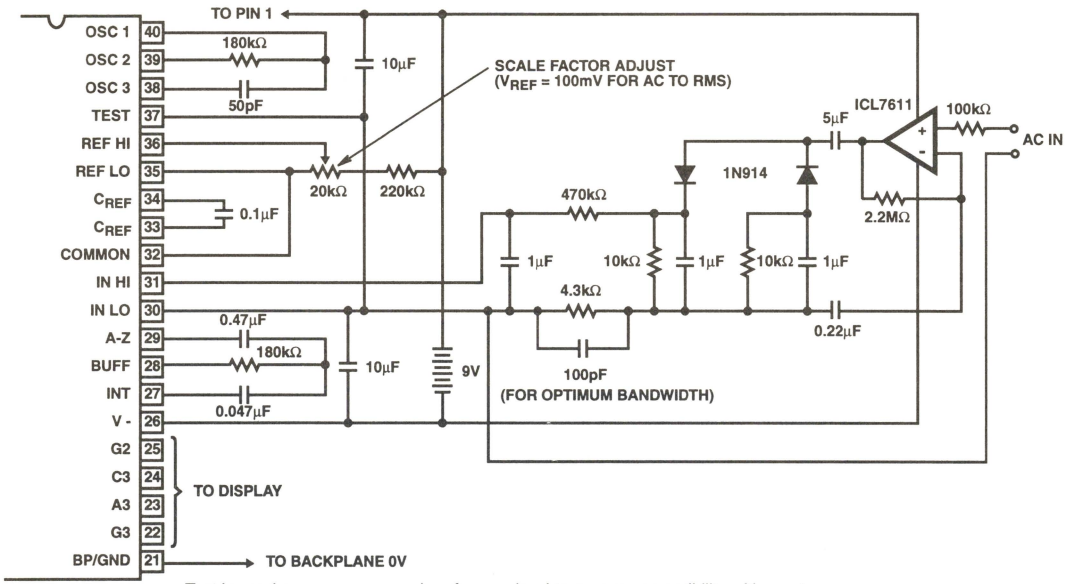


FIGURE 17B. AC TO DC CONVERTER AND HI7133 FOR RMS DISPLAY

FIGURE 17.

Typical Applications (Continued)



Test is used as a common-mode reference level to ensure compatibility with most op amps.

FIGURE 18. AC TO DC CONVERTER WITH HI7131 AND HI7133

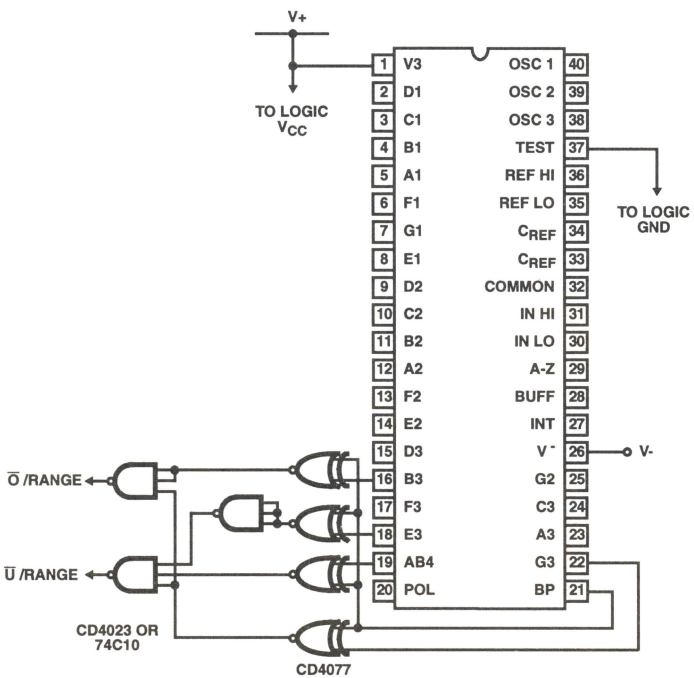


FIGURE 19. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM HI7131 OUTPUTS

Die Characteristics

DIE DIMENSIONS:

127 mils x 149 mils

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

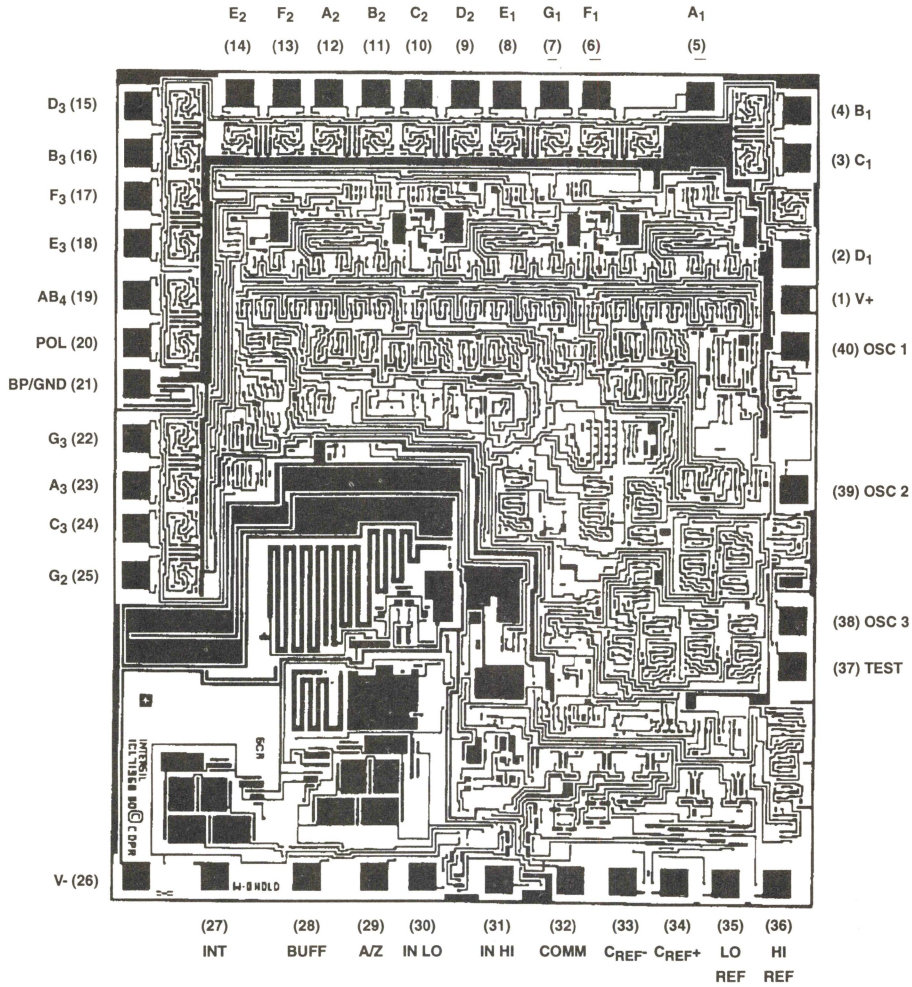
Type: PSG Nitride
Thickness: 15kÅ ±3kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

HI7131, HI7133



HARRIS SEMICONDUCTOR

ICL7106, ICL7107
ICL7106S, ICL7107S

$3^1/_2$ Digit, LCD/LED Display, A/D Converters

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

Features

- Guaranteed Zero Reading for 0V Input on All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference, Direct Display Drive - LCD ICL7106, LED ICL7107
- Low Noise - Less Than $15\mu V_{P-P}$
- On Chip Clock and Reference
- Low Power Dissipation - Typically Less Than 10mW
- No Additional Active Circuits Required
- Enhanced Display Stability (ICL7106S, ICL7107S)

Ordering Information

PART NO.	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
ICL7106CPL	0 to 70	40 Ld PDIP	E40.6
ICL7106RCPL	0 to 70	40 Ld PDIP (Note)	E40.6
ICL7106CM44	0 to 70	44 Ld MQFP	Q44.10x10
ICL7106SCPL	0 to 70	40 Ld PDIP	E40.6
ICL7107SCPL	0 to 70	40 Ld PDIP	E40.6
ICL7107CPL	0 to 70	40 Ld PDIP	E40.6
ICL7107RCPL	0 to 70	40 Ld PDIP (Note)	E40.6
ICL7107CM44	0 to 70	44 Ld MQFP	Q44.10x10

NOTE: "R" indicates device with reversed leads for mounting to PC board underside. "S" indicates enhanced stability.

Description

The Harris ICL7106 and ICL7107 are high performance, low power, $3^1/_2$ digit A/D converters. Included are seven segment decoders, display drivers, a reference, and a clock. The ICL7106 is designed to interface with a liquid crystal display (LCD) and includes a multiplexed backplane drive; the ICL7107 will directly drive an instrument size light emitting diode (LED) display.

The ICL7106 and ICL7107 bring together a combination of high accuracy, versatility, and true economy. It features autozero to less than $10\mu V$, zero drift of less than $1\mu V/^oC$, input bias current of 10pA (Max), and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge type transducers. Finally, the true economy of single power supply operation (ICL7106), enables a high performance panel meter to be built with the addition of only 10 passive components and a display.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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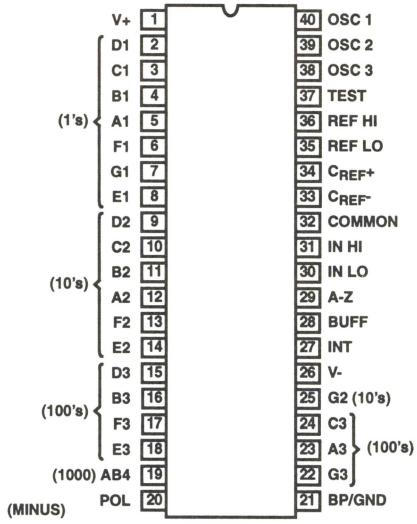
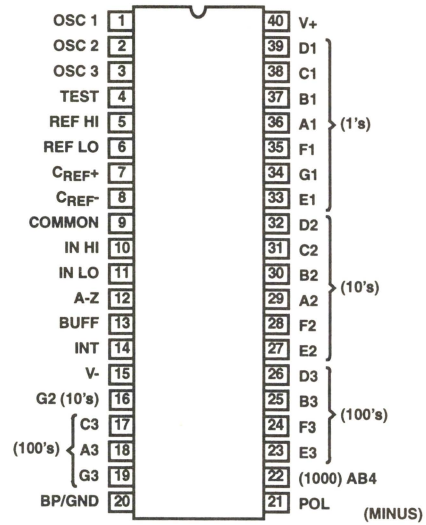
Pinouts

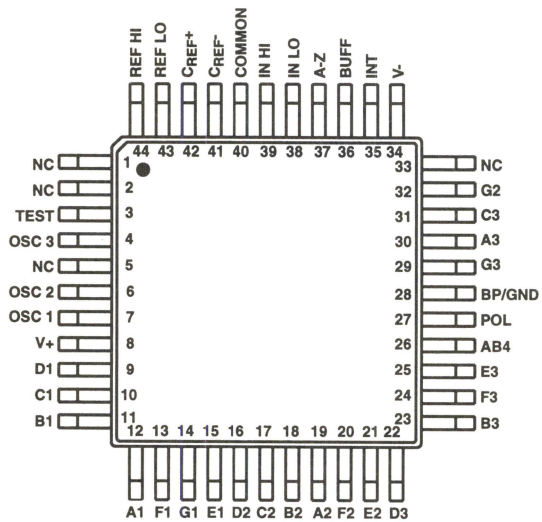
ICL7106, ICL7107 (PDIP)
TOP VIEW



ICL7106R, ICL7107R (PDIP)
TOP VIEW



ICL7106, ICL7107 (MQFP)
TOP VIEW



HARRIS SEMICONDUCTOR

ICL7116, ICL7117

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

$3\frac{1}{2}$ Digit, LCD/LED Display, A/D Converter with Display Hold

Features

- HOLD Reading Input Allows Indefinite Display Hold
- Guaranteed Zero Reading for 0V Input
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- Direct Display Drive
  - LCD ICL7116
  - LED ICL7117
- Low Noise - Less Than $15\mu V_{P-P}$ (Typ)
- On Chip Clock and Reference
- Low Power Dissipation - Typically Less Than 10mW
- No Additional Active Circuits Required
- Surface Mount Package Available

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
ICL7116CPL	0 to 70	40 Ld PDIP	E40.6
ICL7116CM44	0 to 70	44 Ld MQFP	Q44.10x10
ICL7117CPL	0 to 70	40 Ld PDIP	E40.6

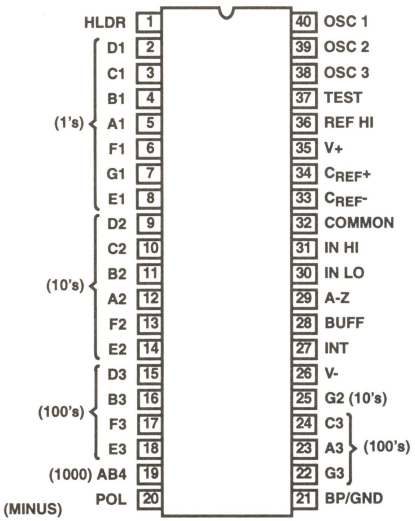
Description

The Harris ICL7116 and ICL7117 are high performance, low power, $3\frac{1}{2}$ digit, A/D converters. Included are seven segment decoders, display drivers, a reference, and a clock. The ICL7116 is designed to interface with a liquid crystal display (LCD) and includes a multiplexed backplane drive. The ICL7117 will directly drive an instrument size, light emitting diode (LED) display.

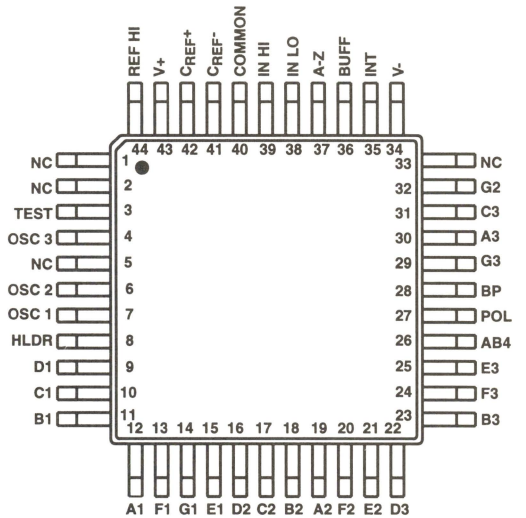
The ICL7116 and ICL7117 have all of the features of the ICL7106 and ICL7107 with the addition of a HOLD Reading input. With this input, it is possible to make a measurement and retain the value on the display indefinitely. To make room for this feature the reference low input has been connected to Common internally rather than being fully differential. These circuits retain the accuracy, versatility, and true economy of the ICL7106 and ICL7107. They feature auto-zero to less than $10\mu V$, zero drift of less than $1\mu V/^oC$, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally, the true economy of single power supply operation (ICL7116) enables a high performance panel meter to be built with the addition of only eleven passive components and a display.

Pinouts

ICL7116, ICL7117 (PDIP)
TOP VIEW



ICL7116 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3083.1**

HARRIS SEMICONDUCTOR

ICL7126

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

$3^1/_2$ Digit, Low Power, Single-Chip A/D Converter

Features

- 8,000 Hours Typical 9V Battery Life
- Guaranteed Zero Reading for 0V Input on All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference
- Direct LCD Display Drive - No External Components Required
- Pin Compatible With the ICL7106
- Low Noise - Less Than $15\mu V_{P-P}$
- On-Chip Clock and Reference
- Low Power Dissipation Guaranteed Less Than 1mW
- No Additional Active Circuits Required

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
ICL7126CPL	0 to 70	40 Ld PDIP	E40.6
ICL7126RCPL	0 to 70	40 Ld PDIP (Note)	E40.6

NOTE: "R" indicates device with reversed leads.

Description

The ICL7126 is a high performance, very low power $3^1/_2$-digit, A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven segment decoders, display drivers, reference, and clock. The ICL7126 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current of 100µA is ideally suited for 9V battery operation.

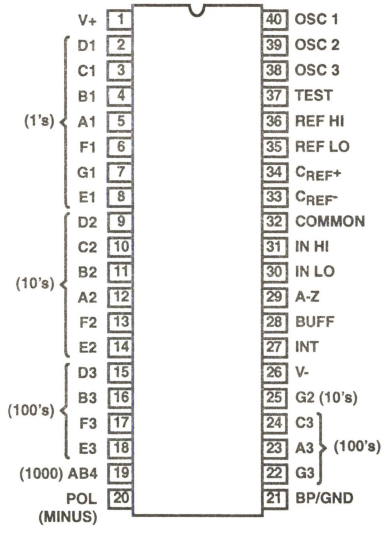
The ICL7126 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10µV, zero drift of less than $1\mu V/^oC$, input bias current of 10pA maximum, and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power operation allows a high performance panel meter or multi-meter to be built with the addition of only 10 passive components and a display.

The ICL7126 can be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

Pinout

NOT RECOMMENDED FOR NEW DESIGNS

ICL7126
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **3084.1**

HARRIS SEMICONDUCTOR

ICL7129

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

$4^1/_2$ Digit LCD, Single-Chip A/D Converter

Features

- ±19,999 Count A/D Converter Accurate to ±4 Count
- 10μV Resolution on 200mV Scale
- 110dB CMRR
- Direct LCD Display Drive
- True Differential Input and Reference
- Low Power Consumption
- Decimal Point Drive Outputs
- Overrange and Underrange Outputs
- Low Battery Detection and Indication
- 10:1 Range Change Input

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL7129CPL	0 to 70	40 Ld PDIP	E40.6
ICL7129RCPL	0 to 70	40 Ld PDIP	E40.6
ICL7129CM44	0 to 70	44 Ld MQFP	Q44.10x10

NOTE: "R" indicates device with reversed leads.

Description

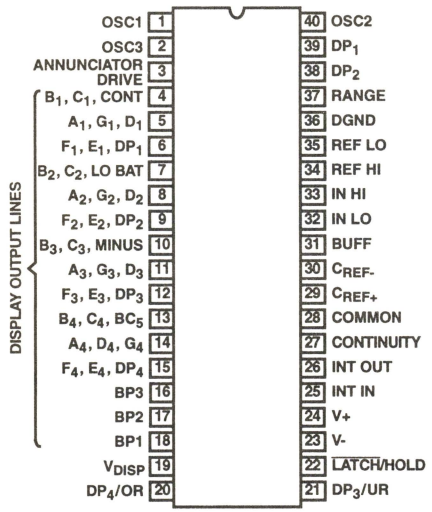
The Harris ICL7129 is a very high performance $4^1/_2$-digit, analog-to-digital converter that directly drives a multiplexed liquid crystal display. This single chip CMOS integrated circuit requires only a few passive components and a reference to operate. It is ideal for high resolution hand-held digital multimeter applications.

The performance of the ICL7129 has not been equaled before in a single chip A/D converter. The successive integration technique used in the ICL7129 results in accuracy better than 0.005% of full scale and resolution down to 10μV/count.

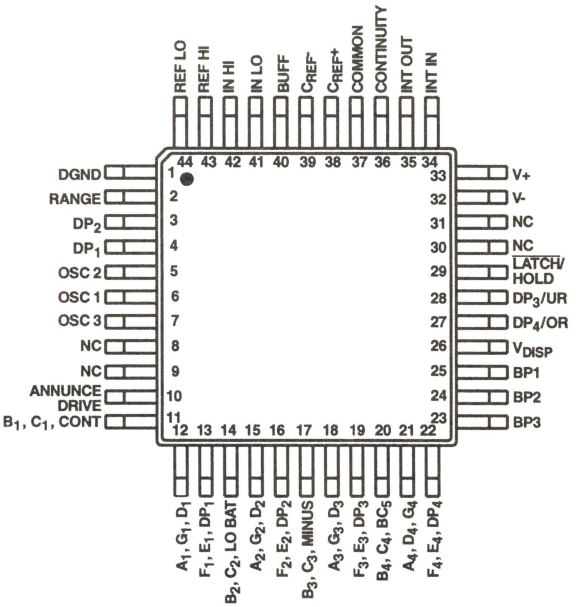
The ICL7129, drawing only 1mA from a 9V battery, is well suited for battery powered instruments. Provision has been made for the detection and indication of a "LOW/BATTERY" condition. Autoranging instruments can be made with the ICL7129 which provides overrange and underrange outputs and 10:1 range changing input. The ICL7129 instantly checks for continuity, giving both a visual indication and a logic level output which can enable an external audible transducer. These features and the high performance of the ICL7129 make it an extremely versatile and accurate instrument-on-a-chip.

Pinouts

ICL7129 (PDIP)
TOP VIEW



ICL7129 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3085.1**

HARRIS SEMICONDUCTOR

ICL7136, ICL7137

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

$3\frac{1}{2}$ Digit LCD/LED, Low Power Display, A/D Converters with Overrange Recovery

Features

- First Reading Overrange Recovery in One Conversion Period
- Guaranteed Zero Reading for 0V Input on All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference, Direct Display Drive
  - LCD ICL7136
  - LED ICL7137
- Low Noise - Less Than $15\mu V_{P-P}$
- On Chip Clock and Reference
- No Additional Active Circuits Required
- Low Power - Less Than 1mW
- Surface Mount Package Available
- Drop-In Replacement for ICL7126, No Changes Needed

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
ICL7136CPL	0 to 70	40 Ld PDIP	E40.6
ICL7136RCPL	0 to 70	40 Ld PDIP (Note)	E40.6
ICL7136CM44	0 to 70	44 Ld MQFP	Q44.10x10
ICL7137CPL	0 to 70	40 Ld PDIP	E40.6
ICL7137RCPL	0 to 70	40 Ld PDIP (Note)	E40.6
ICL7137CM44	0 to 70	44 Ld MQFP	Q44.10x10

NOTE: "R" indicates device with reversed leads.

Description

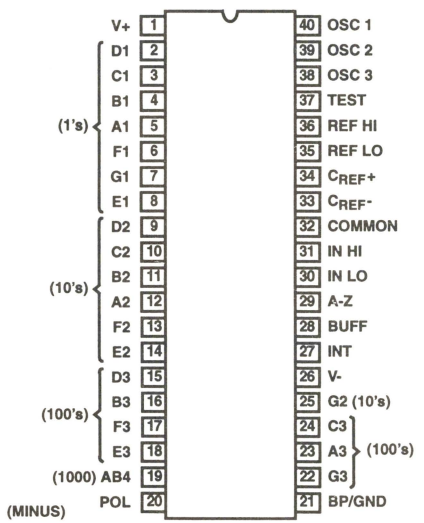
The Harris ICL7136 and ICL7137 are high performance, low power $3\frac{1}{2}$ digit, A/D converters. Included are seven segment decoders, display drivers, a reference, and a clock. The ICL7136 is designed to interface with a liquid crystal display (LCD) and includes a multiplexed backplane drive; the ICL7137 will directly drive an instrument size, light emitting diode (LED) display.

The ICL7136 and ICL7137 bring together a combination of high accuracy, versatility, and true economy. It features autozero to less than $10\mu V$, zero drift of less than $1\mu V/^oC$, input bias current of 10pA (Max), and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge type transducers. Finally, the true economy of single power supply operation (ICL7136), enables a high performance panel meter to be built with the addition of only 10 passive components and a display.

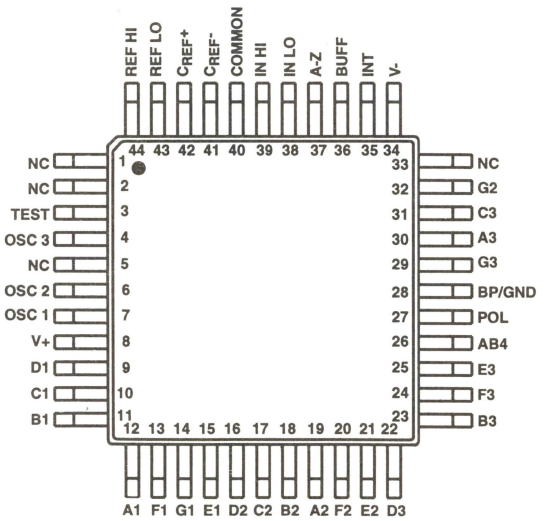
The ICL7136 and ICL7137 are improved versions of the ICL7126, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications. It can also be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

Pinouts

(PDIP)
TOP VIEW



(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3086.1**

ICL7139, ICL7149

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

$3^3/_4$ Digit, Autoranging Multimeter

Features

- 13 Ranges - ICL7139
  - 4 DC Voltage 400mV, 4V, 40V, 400V
  - 1 AC Voltage 400V
  - 4 DC Current 4mA, 40mA, 400mA, 4A
  - 4 Resistance 4kΩ, 40kΩ, 400kΩ, 4MΩ
- 18 Ranges - ICL7149
  - 4 DC Voltage 400mV, 4V, 40V, 400V
  - 2 AC Voltage with Optional AC Circuit
  - 4 DC Current 4mA, 40mA, 400mA, 4A
  - 4 AC Current with Optional AC Circuit
  - 4 Resistance 4kΩ, 40kΩ, 400kΩ, 4MΩ
- Autoranging - First Reading is Always on Correct Range
- On-Chip Duplex LCD Display Drive Including Three Decimal Points and 11 Annunciators
- No Additional Active Components Required
- Low Power Dissipation - Less than 20mW - 1000 Hour Typical Battery Life
- Display Hold Input
- Continuity Output Drives Piezoelectric Beeper
- Low Battery Annunciator with On-Chip Detection
- Guaranteed Zero Reading for 0V Input on All Ranges

Description

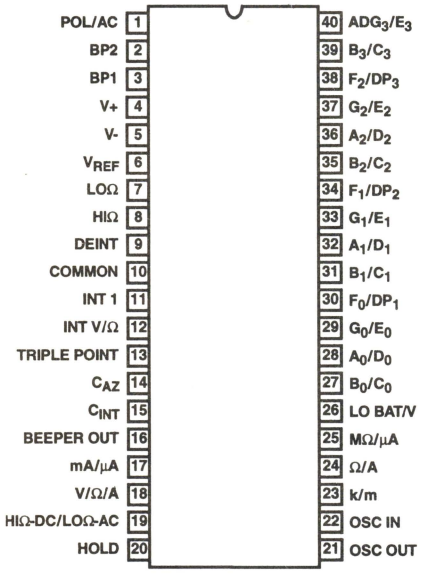
The Harris ICL7139 and ICL7149 are high performance, low power, auto-ranging digital multimeter ICs. Unlike other autoranging multimeter ICs, the ICL7139 and ICL7149 always display the result of a conversion on the correct range. There is no "range hunting" noticeable in the display. The unit will autorange between the four different ranges. A manual switch is used to select the 2 high group ranges. DC current ranges are 4mA and 40mA in the low current group, and 400mA and 4A in the high current group. Resistance measurements are made on 4 ranges, which are divided into two groups. The low resistance ranges are 4/40kΩ. The high resistance ranges are 0.4/4MΩ. Resolution on the lowest range is 1Ω.

Ordering Information

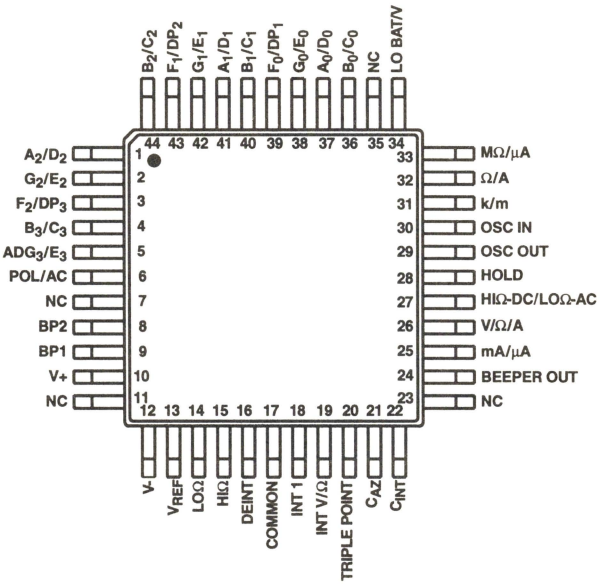
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL7139CPL	0 to 70	40 Ld PDIP	E40.6
ICL7149CPL	0 to 70	40 Ld PDIP	E40.6
ICL7149CM44	0 to 70	44 Ld MQFP	Q44.10x10

Pinouts

ICL7139, ICL7149 (PDIP)
TOP VIEW



ICL7149 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3088.1**

HARRIS SEMICONDUCTOR

ICL8052/ICL71C03, ICL8068/ICL71C03

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

Precision $4^1/_2$ Digit, A/D Converter

Features

- Typically Less Than $2\mu V_{P-P}$ Noise (200.00mV Full Scale, ICL8068)
- Accuracy Guaranteed to ±1 Count Over Entire ±20,000 Counts (2.0000V Full Scale)
- Guaranteed Zero Reading for 0V Input
- True Polarity at Zero Count for Precise Null Detection
- Single Reference Voltage Required
- Over-Range and Under-Range Signals Available for Auto-Ranging Capability
- All Outputs TTL Compatible
- Medium Quality Reference, 40ppm (Typ) on Board
- Blinking Display Gives Visual Indication of Over Range
- Six Auxiliary Inputs/Outputs are Available for Interfacing to UARTs, Microprocessors or Other Complex Circuitry
- 5pA Input Current (Typ) (8052A)

Description

The ICL8052 or ICL8068/ICL71C03 chip pairs with their multiplexed BCD output and digit drivers are ideally suited for the visual display DVM/DPM market. The outstanding $4^1/_2$ digit accuracy, 200.00mV to 2.0000V full scale capability, auto-zero and auto-polarity combine with true ratiometric operation, almost ideal differential linearity and time-proven dual slope conversion. Use of these chip pairs eliminates clock feedthrough problems, and avoids the critical board layout usually required to minimize charge injection.

When only 2000 counts of resolution are required, the 71C03 can be wired for $3^1/_2$ digits and give up to 30 readings/sec., making it ideally suited for a wide variety of applications.

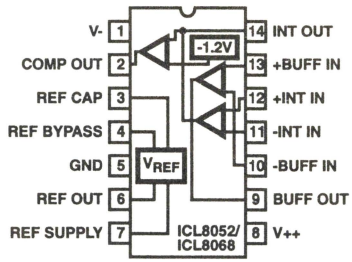
The ICL71C03 is an improved CMOS plug-in replacement for the ICL7103 and should be used in all new designs.

Ordering Information

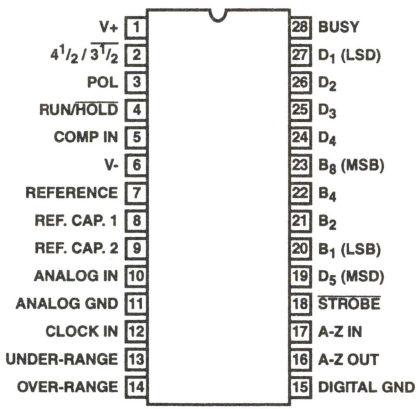
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL8052CPD	0 to 70	14 Ld PDIP	E14.3
ICL8052CDD	0 to 70	14 Ld CERDIP	F14.3
ICL8052ACPD	0 to 70	14 Ld PDIP	E14.3
ICL8052ACDD	0 to 70	14 Ld CERDIP	F14.3
ICL8068CDD	0 to 70	14 Ld CERDIP	F14.3
ICL8068ACDD	0 to 70	14 Ld CERDIP	F14.3
ICL8068ACJD	0 to 70	14 Ld CERDIP	F14.3
ICL71C03CPI	0 to 70	28 Ld PDIP	E28.6
ICL71C03ACPI	0 to 70	28 Ld PDIP	E28.6

Pinouts

ICL8052/ICL8068
(CERDIP, PDIP)
TOP VIEW



ICL71C03 (PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3081.1**

DATA ACQUISITION 4

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4-BIT HIGH SPEED A/D CONVERTER

DEVICE	SUFFIX CODE	OUTPUTS	CONV. TYPE	CONV. RATE (MSPS)	INPUT FPBW (MHz)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	DNL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI3304	JIP, JIB	Parallel, Binary, 4-Bit Latch, Three-State	Flash	25	40	CMOS, SOS	+3 to 7.5	2.0	±0.25	±0.25	IND	EXT	Low Power 25mW

6-BIT HIGH SPEED A/D CONVERTER

DEVICE	SUFFIX CODE	MIL SPEC	OUTPUTS	CONV. TYPE	CONV. RATE (MSPS)	INPUT FPBW (MHz)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	DNL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI3306	JIP/15, JIB/15	Y	Parallel, Binary, 6-Bit Latch, Three-State	Flash	15	30	CMOS, SOS	+3 to 7.5	4.8	±0.5	±0.5	IND	EXT	Low Power 70mW, Replaces Exar MP3306
	JIP/10, JIB/10	Y			10									
HI1172	JCP, JCB		TTL	2-Step	20	18	CMOS	+5		±0.5		COM	INT	Low Power 40mW
HI3-5701K	-5	Y	Parallel, Binary, 6-Bit Latch, Three-State	Flash	30	20	CMOS-JI	+5	4.0	±1.25	±0.6	COM	EXT	Low Cost MP7682 Second Source
HI9P5701K		Y											EXT	
HI3-5701B	-9	Y										IND	EXT	
HI9P5701B		Y											EXT	
HI1826	JCQ		ECL	Flash	140	250	ECL	-5.2	2.5	±0.25	±0.25	COM	EXT	
HI1866	JCQ		TTL/ECL		140	210	ECL	-	2.5	±0.2	±0.2	COM	EXT	1:2 De-Mux, TTL I/O
HI3086	JCQ		TTL/ECL		140	200	ECL	+5 or ±5	2.1	±0.2	±0.2	COM	EXT	1:2 De-Mux, TTL I/O

8-BIT HIGH SPEED A/D CONVERTER

DEVICE	SUFFIX CODE	OUTPUTS	CONV. TYPE	CONV. RATE (MSPS)	INPUT FPBW (MHz)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	DNL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI3318	JIP, JIB	Parallel, Binary, 3-Bit Latch, Three-State	Flash	15	5	CMOS, SOS	+5	6.4	±1.5	+1.0, -0.8	IND		Low Power 8-Bit Flash
HI2300	JCQ	TTL	2-Step	18	18	CMOS	+3.3	1.5	±1.3	±0.5	COM	INT	Low Power 18mW, DC Restore
HI1175	JCB, JCP	Parallel, Binary, 8-Bit Latch, Three-State	2-Step	20	18	CMOS	+5	2	±1.3	±0.5	IND	INT	Low Power 60mW
HI1176	JCQ		2-Step	20	18 (1db)		+5	2	±1.3	±0.5	IND	INT	Low Power 60mW, DC Restore
HI2301	JCQ	TTL	2-Step	30	20 (1db)	CMOS	$+5V_A$ / $+3.3V_D$	1.5	±1.3	±0.5	COM	INT	Low Power 125mW, DC Restore, Int Amp.
HI1179	JCQ	Parallel, Binary, 8-Bit Latch, Three-State	2-Step	35	60	CMOS	+5	2	+1.3 -1.0	±0.5	IND	INT	Low Power 80mW, DC Restore

8-BIT HIGH SPEED A/D CONVERTER (Continued)

DEVICE	SUFFIX CODE	OUTPUTS	CONV. TYPE	CONV. RATE (MSPS)	INPUT FPBW (MHz)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	DNL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI5714/4	CB	Parallel, Binary	2-Step Folding	40	15	HBC10	+5	2	±0.75	±0.5	COM	EXT	ENOB = 7.8 Bits at 4.43MHz
HI2302	JCQ	TTL	2-Step	50	100	CMOS		2	±0.5		COM	INT	Low Power 125mW, DC Restore
HI2303	JCQ	TTL	2-Step	3 x 50	100	CMOS	$+5V_A$ / $+3.3V_D$	2	±0.7	±0.3	IND	INT	Triple A/D, DC Restore
HI5714/6	CB	Parallel, Binary	2-Step Folding	60	15	HBC10	+5	2	±0.75	±0.5	COM	EXT	ENOB = 7.7 Bits at 4.43MHz
HI5662/6	IN	TTL	Pipeline	2 x 60	250	CMOS	$+5V_A$ / $+3V_D$	1	±1	±0.5	IND	EXT	Dual A/D
HI5714/7	CB	Parallel, Binary	2-Step Folding	75	15	HBC10	+5	2	±0.75	±0.5	COM	EXT	ENOB = 7.7 Bits at 4.43MHz
HI1386	JCP, AIL	Parallel, Binary, 8-Bit Latch	Flash	75	150	Bipolar	-5.2	2	±0.5	±0.5	IND, COM	EXT	Low Power 580mW
HI3026	JCQ	TTL, 1:2 Demux	Flash	120	150	Bipolar	+5 or ±5	2	±0.5	±0.5	COM	EXT	
HI1396	JCJ, AIL	Parallel, Binary, 8-Bit Latch	Flash	125	200	Bipolar	-5.2	2	±0.5	±0.5	IND, COM	EXT	Low Power 870mW
HI3026A	JCQ	TTL, 1:2 Demux	Flash	140	150	Bipolar	+5 or ±5	2	±0.5	±0.5	COM	EXT	
HI1166	AIL	Parallel, Binary, 8-Bit Latch	Flash	250	250	Bipolar	-5.2	2	±0.5	±0.5	IND	EXT	Low Power 1.4W
HI1276	AIL	Parallel, Binary, 8-Bit Latch	Flash	500	300	Bipolar	-5.2	2	±0.7	±0.5	IND	EXT	Low Power 2.8W

10-BIT HIGH SPEED A/D CONVERTER

DEVICE	SUFFIX CODE	OUTPUTS	CONV. TYPE	CONV. RATE (MSPS)	INPUT FPBW (MHz)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	DNL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI5710A	JCQ	Offset Binary, 2's Complement	2 Step Flash	20	100	CMOS	$+5V_A$ / $+3.3V_D$	2	±1.3	±0.5	COM	EXT	Low Power 150mW
HI5767/2	CB	Offset Binary, 2's Complement	Pipeline	20	250	CMOS	$+5V_A$ / $+3V_D$	1	±1.0	±0.5	COM	INT	
HI5702	JCB	Offset Binary, 2's Complement	Pipeline	36	250	BiCMOS	+5	1.25	±1.0	±0.5	COM	EXT	9+ ENOB at 10MHz Input
HI5702	KCB		Pipeline	40	250	BiCMOS	+5						
HI5703	KCB	Offset Binary, 2's Complement	Pipeline	40	250	BiCMOS	$+5V_A$ / $+3V_D$	1.25	±1.0	±0.5	COM	EXT	9+ ENOB at 10MHz Input
HI5746	KCB	Offset Binary, 2's Complement	Pipeline	40	250	CMOS	$+5V_A$ / $+3V_D$	1	±1.0	±0.5	COM	EXT	Low Power 225mW, 8.8 ENOB at 10MHz

10-BIT HIGH SPEED A/D CONVERTER (Continued)

DEVICE	SUFFIX CODE	OUTPUTS	CONV. TYPE	CONV. RATE (MSPS)	INPUT FPBW (MHz)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	DNL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI5767/4	CB	Offset Binary, 2's Complement	Pipeline	40	250	CMOS	$+5V_A$ / $+3V_D$	1	±1.0	±0.5	COM	INT	
HI5767/6	CB	Offset Binary, 2's Complement	Pipeline	60	250	CMOS	$+5V_A$ / $+3V_D$	1	±1.0	±0.5	COM	INT	
HI5766	KCB	Offset Binary, 2's Complement	Pipeline	60	250	CMOS	$+5V_A$ / $+3V_D$	1	±1.0	±0.5	COM	EXT	Low Power 315mW, 8.3 ENOB at 10MHz Input
HI5762/6	IN	Offset Binary, 2's Complement	Pipeline	2 x 60	250	CMOS	$+5V_A$ / $+3V_D$	1	±1.0	±0.5	COM	IND	Dual A/D

12-BIT HIGH SPEED A/D CONVERTER

DEVICE	SUFFIX CODE	OUTPUTS	CONV. TYPE	CONV. RATE (MSPS)	INPUT FPBW (MHz)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	DNL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI5800	BID, KCD	Parallel, Binary, Three-State, 8-Bit Bus, 12-Bit Bus and 16-Bit Bus	Two-Step	3	20	BiCMOS	±5V	5	±1.0		COM, IND	INT	High Performance Sampling A/D System, +11.5 ENOB
HI5800	JCD						±5V		±2.0		COM		
HI5804	KCB	Offset Binary	Pipeline	5	100	BiCMOS	$+5V_A$ / $+3V_D$	4	±2.0	±0.5	COM	INT	10.3 ENOB at 1MHz Input, 300mW
HI5805	BIB			5		BiCMOS	$+5V_A$ / $+3V_D$	4	±1.0	±0.5	IND	INT	11 ENOB at 1MHz Input, 300mW
HI5808	BIB			10		BiCMOS	$+5V_A$ / $+3V_D$	4	±1.0	±0.5	IND	INT	10.8 ENOB at 1MHz Input, 325mW

14-BIT HIGH SPEED A/D CONVERTER

DEVICE	SUFFIX CODE	MIL SPEC	OUTPUTS	CONV. TYPE	CONV. RATE (MSPS)	INPUT FPBW (MHz)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	DNL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI5905	IN	Y	2's Complement	Pipeline	5	100	BiCMOS	$+5V_A$	4	±1.0	±0.5	IND	INT	350mW

CA3304, CA3304A

HARRIS SEMICONDUCTOR

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

4-Bit, 25 MSPS, Flash A/D Converters

Features

- CMOS/SOS Low Power with Video Speed (Typ) . . 25mW
- Parallel Conversion Technique
- Single Power Supply Voltage . . . . . 3V to 7.5V
- 25MHz Sampling Rate (40ns Conversion Time) at 5V Supply
- 4-Bit Latched Three-State Output with Overflow and Data Change Outputs
- $^1/_8$ LSB Maximum Nonlinearity (A Version)
- Inherent Resistance to Latch-Up Due to SOS Process
- Bipolar Input Range with Optional Second Supply
- Wide Input Bandwidth (Typ) 25MHz

Applications

- High Speed A/D Conversion
- Ultrasound Signature Analysis
- Transient Signal Analysis
- High Energy Physics Research
- General-Purpose Hybrid ADCs
- Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- Robot Vision
- RSSI Circuits

Description

The Harris CA3304 is a CMOS parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high speed digitization. Digitizing at 25MHz, for example, requires only about 35mW.

The CA3304 operates over a wide, full-scale signal input voltage range of 0.5V up to the supply voltage. Power consumption is as low as 10mW, depending upon the clock frequency selected.

The intrinsic high conversion rate makes the CA3304 types ideally suited for digitizing high speed signals. The overflow bit makes possible the connection of two or more CA3304s in series to increase the resolution of the conversion system. A series connection of two CA3304s may be used to produce a 5-bit, 25MHz converter. Operation of two CA3304s in parallel doubles the conversion speed (i.e., increases the sampling rate from 25MHz to 50MHz). A data change pin indicates when the present output differs from the previous, thus allowing compaction of data storage.

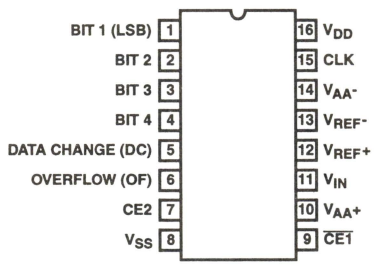
Sixteen paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3304. Fifteen comparators are required to quantize all input voltage levels in this 4-bit converter, and the additional comparator is required for the overflow bit.

Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	SAMPLING RATE	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3304E	±0.25 LSB	25MHz (40ns)	-40 to 85	16 Ld PDIP	E16.3
CA3304AE	±0.125 LSB	25MHz (40ns)	-40 to 85	16 Ld PDIP	E16.3
CA3304M	±0.25 LSB	25MHz (40ns)	-40 to 85	16 Ld SOIC (W)	M16.3
CA3304AM	±0.125 LSB	25MHZ (40ns)	-40 to 85	16 Ld SOIC (W)	M16.3
CA3304D	±0.25 LSB	25MHz (40ns)	-55 to 125	16 Ld SBDIP	D16.3
CA3304AD	±0.125 LSB	25MHz (40ns)	-55 to 125	16 Ld SBDIP	D16.3

Pinout

CA3304 (SBDIP, PDIP, SOIC)
TOP VIEW



4 A/D CONVERTERS HIGH SPEED

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 1790.2

HARRIS SEMICONDUCTOR

CA3306, CA3306A, CA3306C

6-Bit, 15 MSPS, Flash A/D Converters

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

Features

- CMOS Low Power with Video Speed (Typ) 70mW
- Parallel Conversion Technique
- Signal Power Supply Voltage . . . . . 3V to 7.5V
- 15MHz Sampling Rate with Single 5V Supply
- 6-Bit Latched Three-State Output with Overflow Bit
- Pin-for-Pin Retrofit for the CA3300

Applications

- TV Video Digitizing
- Ultrasound Signature Analysis
- Transient Signal Analysis
- High Energy Physics Research
- High Speed Oscilloscope Storage/Display
- General Purpose Hybrid ADCs
- Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- Robot Vision

Description

The CA3306 family are CMOS parallel (FLASH) analog-to-digital converters designed for applications demanding both low power consumption and high speed digitization. Digitizing at 15MHz, for example, requires only about 50mW.

The CA3306 family operates over a wide, full scale signal input voltage range of 1V up to the supply voltage. Power consumption is as low as 15mW, depending upon the clock frequency selected. The CA3306 types may be directly retrofitted into CA3300 sockets, offering improved linearity at a lower reference voltage and high operating speed with a 5V supply.

The intrinsic high conversion rate makes the CA3306 types ideally suited for digitizing high speed signals. The overflow bit makes possible the connection of two or more CA3306s in series to increase the resolution of the conversion system. A series connection of two CA3306s may be used to produce a 7-bit high speed converter. Operation of two CA3306s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15MHz to 30MHz).

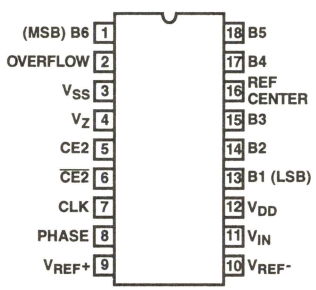
Sixty-four paralleled auto balanced comparators measure the input voltage with respect to a known reference to produce the parallel bit outputs in the CA3306. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

Ordering Information

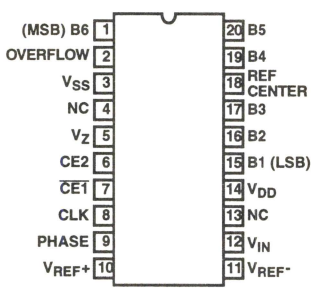
PART NUMBER	LINEARITY (INL, DNL)	SAMPLING RATE	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3306E	±0.5 LSB	15MHz (67ns)	-40 to 85	18 Ld PDIP	E18.3
CA3306CE	±0.5 LSB	10MHz (100ns)	-40 to 85	18 Ld PDIP	E18.3
CA3306M	±0.5 LSB	15MHz (67ns)	-40 to 85	20 Ld SOIC	M20.3
CA3306CM	±0.5 LSB	10MHz (100ns)	-40 to 85	20 Ld SOIC	M20.3
CA3306D	±0.5 LSB	15MHz (67ns)	-55 to 125	18 Ld SBDIP	D18.3
CA3306CD	±0.5 LSB	10MHz (100ns)	-55 to 125	18 Ld SBDIP	D18.3
CA3306J3	±0.5 LSB	15MHz (67ns)	-55 to 125	20 Ld CLCC	J20.B
CA3306J3	±0.5 LSB	10MHz (100ns)	-55 to 125	20 Ld CLCC	J20.B

Pinouts

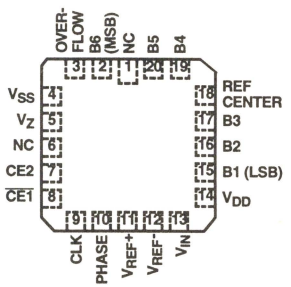
CA3306 (PDIP, SBDIP)
TOP VIEW



CA3306 (SOIC)
TOP VIEW



CA3306 (CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3102.1**

HARRIS SEMICONDUCTOR

CA3318

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

CMOS Video Speed, 8-Bit, Flash A/D Converter

Features

- CMOS Low Power with SOS Speed (Typ)..... 150mW
- Parallel Conversion Technique
- 15MHz Sampling Rate (Conversion Time).....67ns
- 8-Bit Latched Three-State Output with Overflow Bit
- Accuracy (Typ)..... ±1 LSB
- Single Supply Voltage..... 4V to 7.5V
- 2 Units in Series Allow 9-Bit Output
- 2 Units in Parallel Allow 30MHz Sampling Rate

Applications

- TV Video Digitizing (Industrial/Security/Broadcast)
- High Speed A/D Conversion
- Ultrasound Signature Analysis
- Transient Signal Analysis
- High Energy Physics Research
- General-Purpose Hybrid ADCs
- Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- µP Data Acquisition Systems

Description

The CA3318 is a CMOS parallel (FLASH) analog-to-digital converter designed for applications demanding both low power consumption and high speed digitization.

The CA3318 operates over a wide full scale input voltage range of 4V up to 7.5V with maximum power consumption depending upon the clock frequency selected. When operated from a 5V supply at a clock frequency of 15MHz, the typical power consumption of the CA3318 is 150mW.

The intrinsic high conversion rate makes the CA3318 ideally suited for digitizing high speed signals. The overflow bit makes possible the connection of two or more CA3318s in series to increase the resolution of the conversion system. A series connection of two CA3318s may be used to produce a 9-bit high speed converter. Operation of two CA3318s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15MHz to 30MHz).

256 paralleled auto balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel bit outputs in the CA3318.

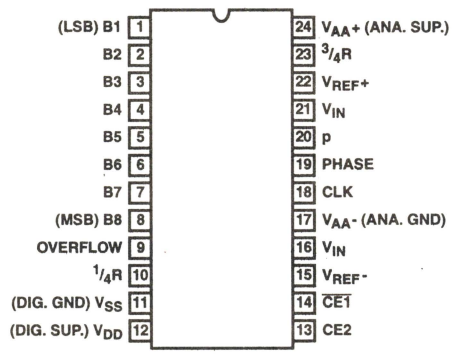
255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	SAMPLING RATE	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3318CE	±1.5 LSB	15MHz (67ns)	-40 to 85	24 Ld PDIP	E24.6
CA3318CM	±1.5 LSB	15MHz (67ns)	-40 to 85	24 Ld SOIC	M24.3
CA3318CD	±1.5 LSB	15MHz (67ns)	-40 to 85	24 Ld SBDIP	D24.6

Pinout

CA3318
(PDIP, SBDIP, SOIC)
TOP VIEW



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File Number 3103.1

HARRIS SEMICONDUCTOR

HI1166

August 1997

8-Bit, 250 MSPS, Flash A/D Converter

Features

- Differential Linearity Error . . . . . ±0.5 LSB or Less
- Integral Linearity Error . . . . . ±0.5 LSB or Less
- Built-In Integral Linearity Compensation Circuit
- Ultra High Speed Operation with Maximum Conversion Rate (Min) . . . . . 250 MSPS
- Low Input Capacitance 18pF (Typ)
- Wide Analog Input Bandwidth (Min for Full Scale Input) 250MHz
- Single Power Supply . . . . . -5.2V
- Low Power Consumption . . . . . 1.4W (Typ)
- Low Error Rate
- Capable of Driving 50Ω Loads
- Evaluation Board Available
- Direct Replacement for Sony CXA1166K

Description

The HI1166 is an 8-bit, ultra high speed, flash Analog-to-Digital converter IC capable of digitizing analog signals at a maximum rate of 250 MSPS. The digital I/O levels of the converter are compatible with ECL 100K/10KH/10K.

Applications

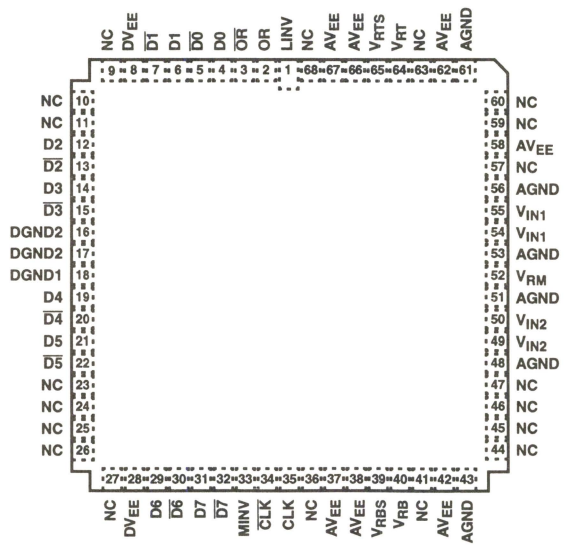
- Spectrum Analyzers
- Radar Systems
- Direct RF Down-Conversion
- Video Digitizing
- Communication Systems
- Digital Oscilloscopes

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1166AIL	-20 to 100	68 Ld CLCC	J68.A
HI1166-EV	25	Evaluation Board	

Pinout

HI1166
(CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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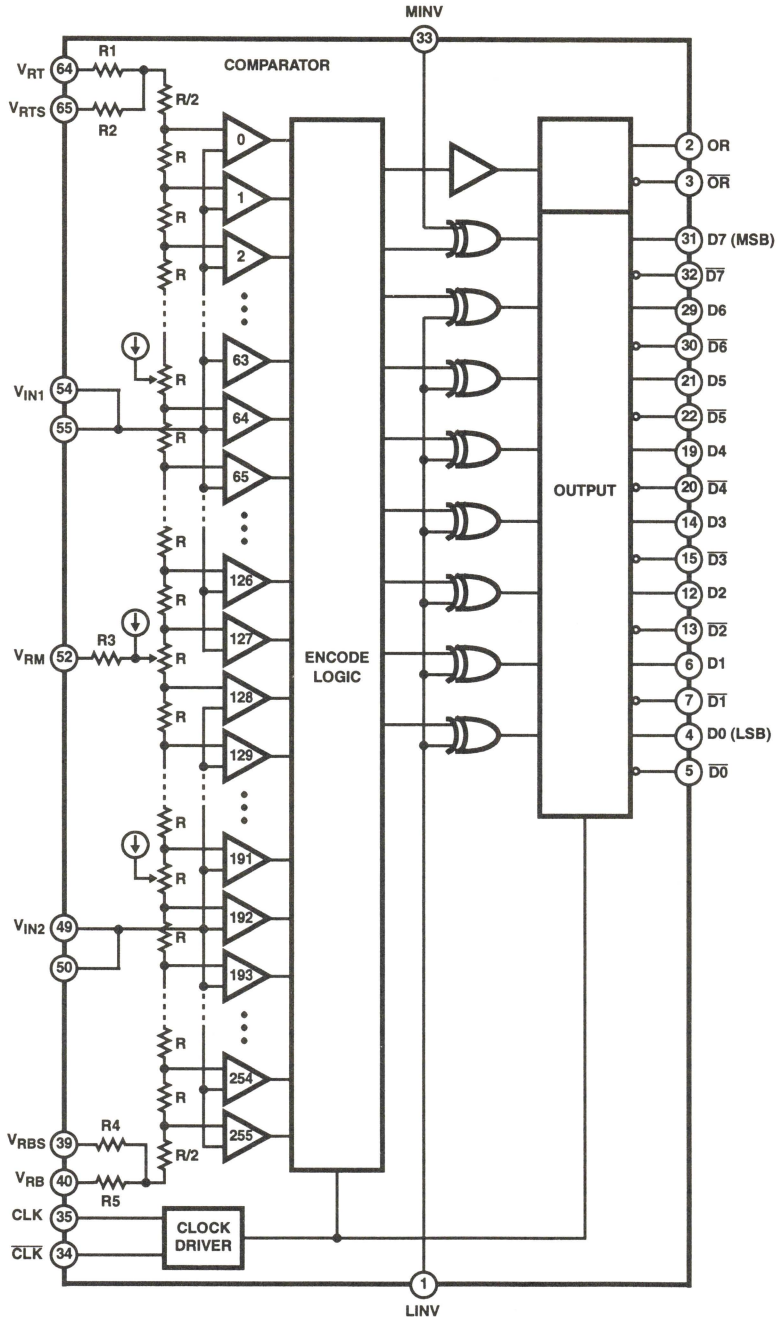
File Number **3579.3**

Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{EE}, DV_{EE}) . . . . . -7V to +0.5V
Analog Input Voltage (V_{IN}) . . . . . -2.7V to +0.5V
Reference Input Voltage
V_{RT}, V_{RB}, V_{RM} . . . . . -2.7V to +0.5V
$|V_{RT} - V_{RB}|$ 2.5V
Digital Input Voltage
MINV, LINV, CLK, $\overline{CLK}$ . . . . . -4V to +0.5V
|CLK-$\overline{CLK}$| 2.7V
V_{RM} Pin Input Current (I_{VRM}) . . . . . -3mA to +3mA
Digital Output Current
(ID0 to ID7, IOR, $\overline{ID0}$ to $\overline{ID7}$, $\overline{IOR}$) . . . . . -30mA to 0mA
Temperature Range, T_A (Note 5) . . . . . -20^oC to 100^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	$\theta_{JA}{}^oC/W$	$\theta_{JC}{}^oC/W$
CLCC Package	38	10

Maximum Power Dissipation 2.1W
Maximum Junction Temperature . . . . . 175^oC
Maximum Storage Temperature Range (T_{STG}) . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC

Operating Conditions (Note 1)

Supply Voltage	MIN	TYP	MAX
AV_{EE}, DV_{EE}	-5.5V	-5.2	-4.95V
AV_{EE} - DV_{EE}	-0.05V	0	0.05V
AGND - DGND	-0.05V	0	0.05V

Reference Input Voltage	MIN	TYP	MAX
V_{RT}	-0.1V	-2	0.1V
V_{RB}	-2.2V	-2	-1.8V

Analog Input Voltage, V_{IN} . . . . . V_{RB} to V_{RT}

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, V_{RT}, $V_{RTS} = 0V$, V_{RB}, $V_{RBS} = -2V$ (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Resolution		-	8	-	Bits
Integral Linearity Error, INL	f_C = 250 MSPS	-	±0.3	±0.5	LSB
Differential Linearity Error, DNL	f_C = 250 MSPS	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Signal to Noise Ratio, SINAD = $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	Input = 1kHz, Full Scale, f_C = 250MHz	44	46	-	dB
	Input = 60kHz, Full Scale, f_C = 250MHz	-	37	-	dB
Error Rate	Input = 50MHz, Full Scale, Error > 16 LSB, f_C = 250MHz	-	-	10^{-9}	TPS (Note 3)
	Input = 62.499MHz, Full Scale, Error > 16 LSB, f_C = 250MHz	-	10^{-8}	10^{-6}	TPS (Note 3)
Differential Gain Error, DG	NTSC 40 IRE Mod. Ramp, f_C = 250 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Overrange Recovery Time		-	1.0	-	ns
Maximum Conversion Rate, f_C		250	-	-	MSPS
Aperture Jitter, t_{AJ}		-	9	-	ps
Sampling Delay, t_{DS}		0.4	1.4	2.4	ns
ANALOG INPUT					
Analog Input Capacitance, C_{IN}	V_{IN} - 1V + $0.07V_{RMS}$	-	18	-	pF
Analog Input Resistance, R_{IN}		50	120	-	kΩ
Input Bias Current, I_{IN}	V_{IN} = -1V	20	-	450	µA
Full Scale Input Bandwidth	$V_{IN} = 2V_{P-P}$	200	250	-	MHz
REFERENCE INPUTS					
Reference Resistance, R_{REF}		83	125	182	Ω

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, V_{RT}, $V_{RTS} = 0V$, V_{RB}, $V_{RBS} = -2V$ (Note 1) **(Continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Residual Resistance	R1	Note 2	0.1	0.6	2.0	Ω
	R2		300	500	700	Ω
	R3		0.5	2.0	5.0	Ω
	R4		300	500	700	Ω
	R5		0.1	0.6	2.0	Ω
DIGITAL INPUTS						
Logic H Level, V_{IH}			-1.13	-	-	V
Logic L Level, V_{IL}			-	-	-1.5	V
Logic H Current, I_{IH}		Input Connected to GND	0	-	70	µA
Logic L Current, I_{IL}		Input Connected to -2V	-50	-	50	µA
Input Capacitance			-	4	-	pF
DIGITAL OUTPUTS						
Logic H Level, V_{OH}		$R_L = 50Ω$	-1.0	-	-	V
Logic L Level, V_{OL}		$R_L = 50Ω$	-	-	-1.6	V
TIMING CHARACTERISTICS						
H Pulse Width of Clock, t_{PW1}			1.8	-	-	ns
L Pulse Width of Clock, t_{PW0}			1.8	-	-	ns
Output Rise Time, t_r		$R_L = 50Ω$	-	0.6	1.5	ns
Output Fall Time, t_f		$R_L = 50Ω$	-	0.6	1.5	ns
Output Delay, t_{OD}		$R_L = 50Ω$	1.8	2.5	3.2	ns
POWER SUPPLY CHARACTERISTICS						
Supply Current, I_{EE}			-360	-270	-	mA
Power Consumption, P_D		Note 4	-	1.4	1.9	W

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. See Functional Block Diagram.
3. TPS: Times Per Sample.
4. $PD = I_{EEA} \bullet AV_{EE} + I_{EED} \bullet DV_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$
5. T_A is specified in still air and without heat sink. To extend temperature range, appropriate heat management techniques must be employed (See Figure 2).

Timing Diagram

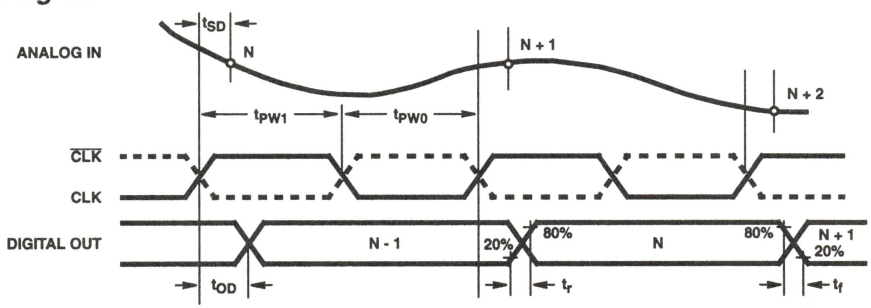


FIGURE 1.

Typical Performance Curves

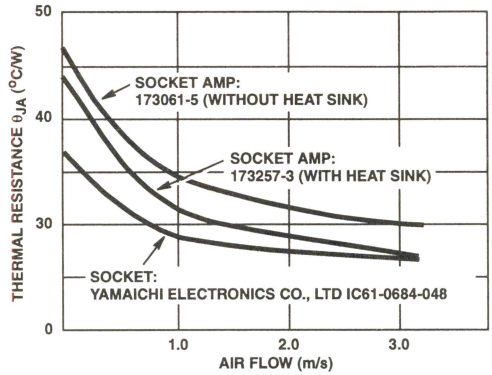


FIGURE 2. THERMAL RESISTANCE OF THE CONVERTER MOUNTED ON A BOARD

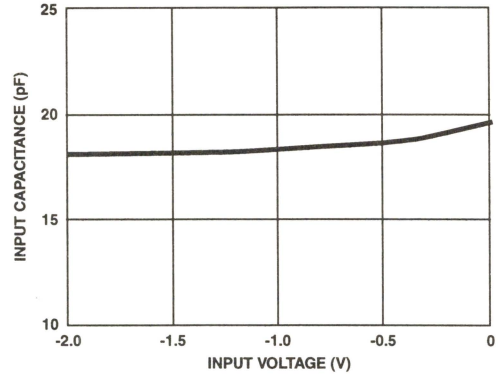


FIGURE 3. V_{IN} PIN CAPACITANCE vs VOLTAGE CHARACTERISTICS

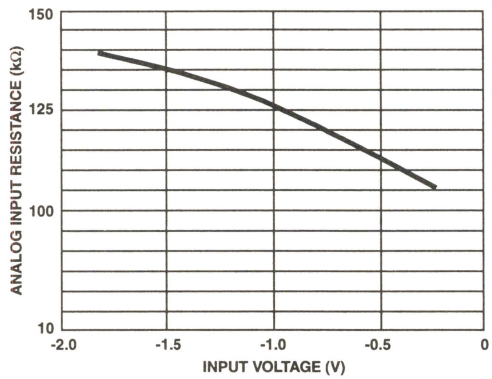


FIGURE 4. V_{IN} PIN INPUT RESISTANCE vs VOLTAGE CHARACTERISTICS

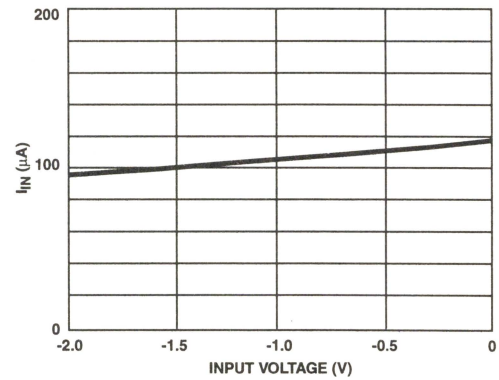


FIGURE 5. V_{IN} PIN INPUT CURRENT vs VOLTAGE CHARACTERISTICS

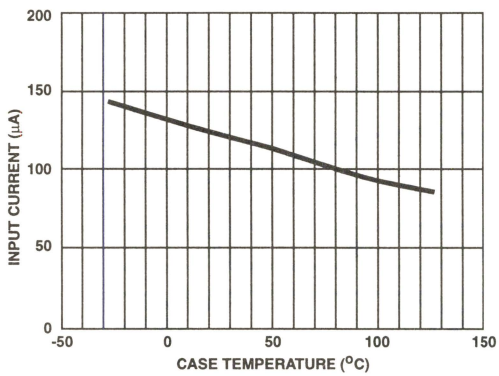


FIGURE 6. V_{IN} PIN INPUT CURRENT vs TEMPERATURE CHARACTERISTICS

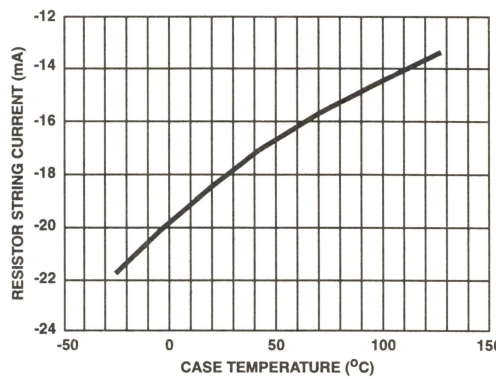


FIGURE 7. RESISTOR STRING CURRENT vs TEMPERATURE CHARACTERISTICS

Typical Performance Curves (Continued)

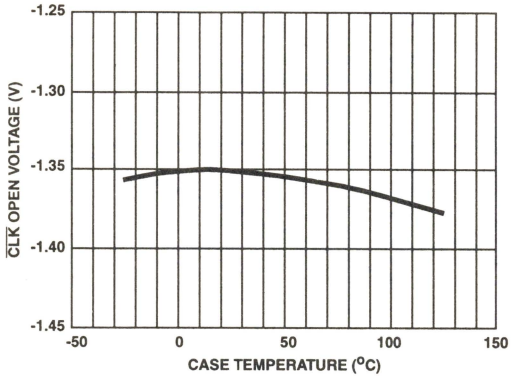


FIGURE 8. $\overline{CLK}$ OPEN VOLTAGE vs TEMPERATURE CHARACTERISTICS

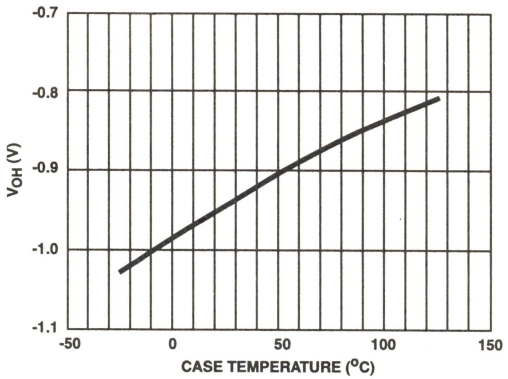


FIGURE 9. V_{OH} vs TEMPERATURE CHARACTERISTICS

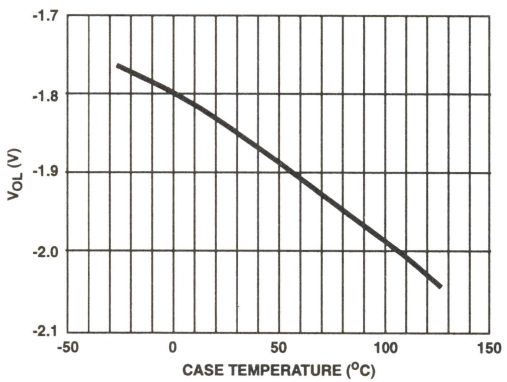


FIGURE 10. V_{OL} vs TEMPERATURE CHARACTERISTICS

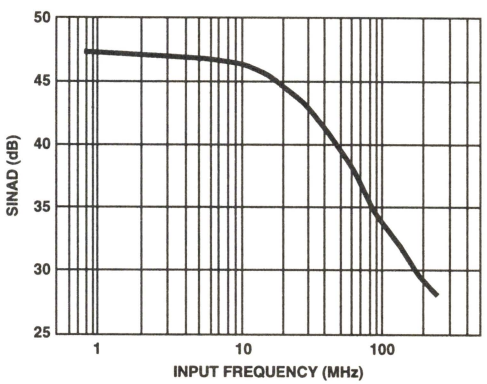


FIGURE 11. SINAD vs INPUT FREQUENCY RESPONSE CHARACTERISTICS

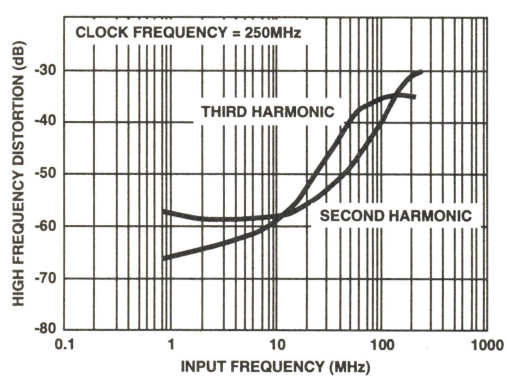


FIGURE 12. HARMONIC DISTORTION vs INPUT FREQUENCY RESPONSE CHARACTERISTICS

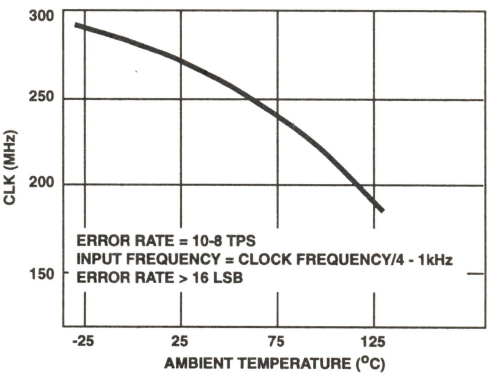


FIGURE 13. MAXIMUM CONVERSION RATE vs TEMPERATURE CHARACTERISTICS

Typical Performance Curves (Continued)

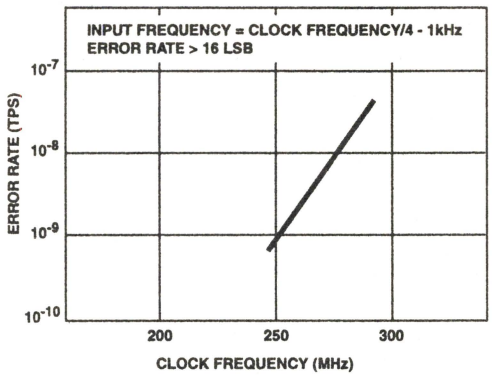


FIGURE 14. ERROR RATE vs CONVERSION RATE

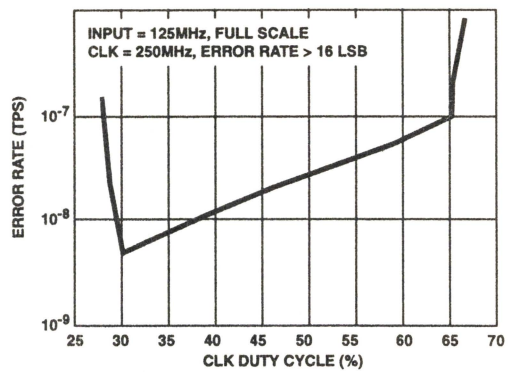


FIGURE 15. ERROR RATE vs CLOCK DUTY CYCLE

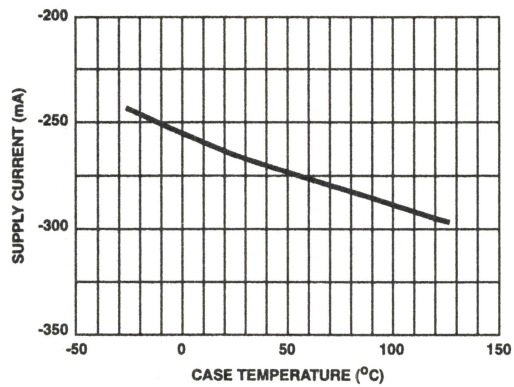
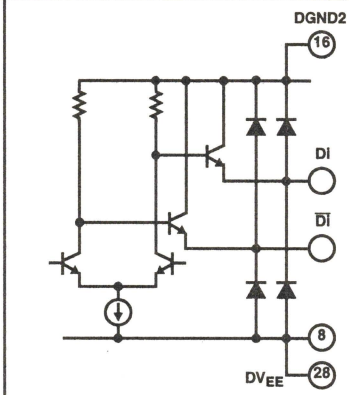
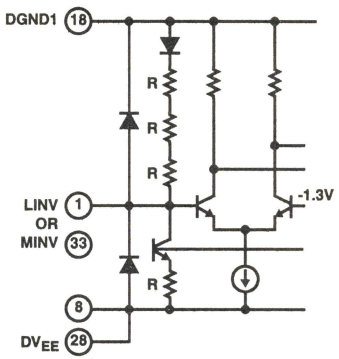
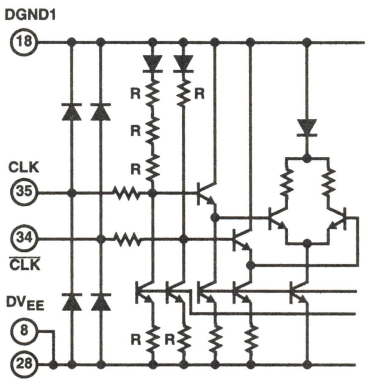


FIGURE 16. SUPPLY CURRENT vs TEMPERATURE CHARACTERISTICS

Pad Descriptions

PAD NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
4, 5	D0, $\overline{D0}$	O	ECL		LSB and complementary LSB output.
6, 7	D1, $\overline{D1}$				D1 to D6: Data Output. $\overline{D1}$ to $\overline{D6}$: Complementary Data Output.
12, 13	D2, $\overline{D2}$				
14, 15	D3, $\overline{D3}$				
19, 20	D4, $\overline{D4}$				
21, 22	D5, $\overline{D5}$				
29, 30	D6, $\overline{D6}$				
31, 32	D7, $\overline{D7}$				MSB Complementary MSB Data Output.
2, 3	OR, $\overline{OR}$				Overrange and Complementary Overrange Output.
1	LINV	I	ECL		Polarity selection for LSBs (refer to the A/D Output Code Table.) Pulled low when left open.
33	MINV	I	ECL		Polarity selection for MSB (refer to the A/D Output Code Table). Pulled low when left open.
35	CLK	I	ECL		CLK Input.
34	$\overline{CLK}$	I	ECL		Complementary CLK Input. Pulled down to -1.3V when left open.

Pad Descriptions (Continued)

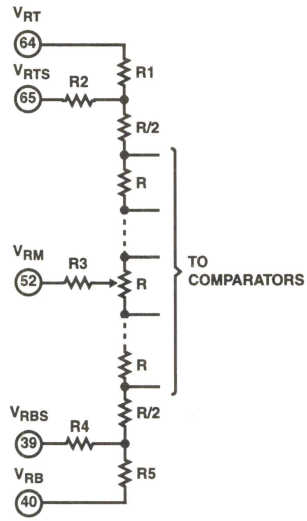
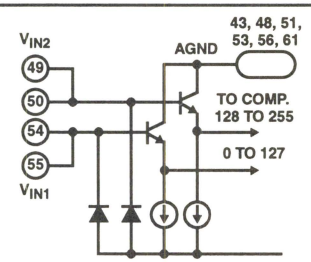
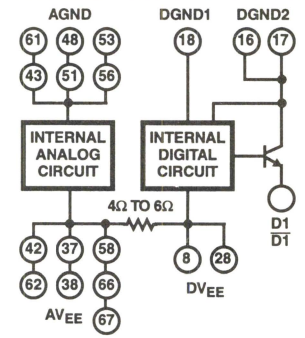
PAD NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
64	V_{RT}	I	0V		Analog Reference Voltage (Top) (0V Typ).
65	V_{RTS}	O	0V		Reference Voltage Sense (Top).
52	V_{RM}	I	$V_{RB/2}$		Reference Voltage Mid Point. Can be used for linearity compensation.
39	V_{RBS}	O	-2V		Reference Voltage Sense (Bottom).
40	V_{RB}	I	-2V		Analog Reference Voltage (Bottom).
49, 50	V_{IN2}	I	V_{RTS} to V_{RBS}		Analog Input. All of the pins must be wired externally.
54, 55	V_{IN1}				
43, 48, 51, 53, 56, 61	AGND		0V		Analog ground.
37, 38, 42, 58, 62, 66, 67	AV_{EE}		-5.2V		Analog supply. Internally connected to DV_{EE} (resistance: 4Ω to 6Ω).
18	DGND1		0V		Digital ground.
16, 17	DGND2		0V		Digital ground for output drive.
8, 28	DV_{EE}		-5.2V		Digital supply. Internally connected to AV_{EE} (resistance: 4Ω to 6Ω).

TABLE 1. A/D OUTPUT CODE

V_{IN} (NOTE 1)	STEP	MINV 1, LINV 1			0, 1			1, 0			0, 0		
		OR	D7	D0	OR	D7	D0	OR	D7	D0	OR	D0	D7
0V		0	000•••••00		0	100•••••00		0	011•••••11		0	111•••••11	
	0	1	000•••••00		1	100•••••00		1	011•••••11		1	111•••••11	
	1	1	000•••••01		1	100•••••01		1	011•••••10		1	111•••••10	
			•			•			•			•	
			•			•			•			•	
			•			•			•			•	
-1V	127	1	011•••••11		1	111•••••11		1	000•••••00		1	100•••••00	
	128	1	100•••••00		1	000•••••00		1	111•••••11		1	011•••••11	
			•			•			•			•	
			•			•			•			•	
			•			•			•			•	
	254	1	111•••••10		1	011•••••10		1	100•••••01		1	000•••••01	
	255	1	111•••••11		1	011•••••11		1	100•••••00		1	000•••••00	
-2V		1	111•••••11		1	011•••••11		1	100•••••00		1	000•••••00	

NOTE:

1. $V_{RT} = V_{RTS} = 0V$, $V_{RM} = -1V$ or open, $V_{RB} = V_{RBS} = -2V$.

Test Circuits and Waveforms

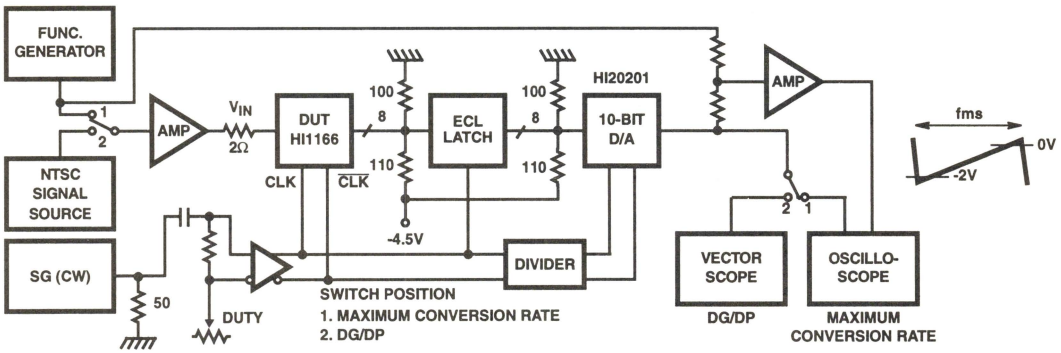


FIGURE 17. MAXIMUM CONVERSION RATE TEST CIRCUIT

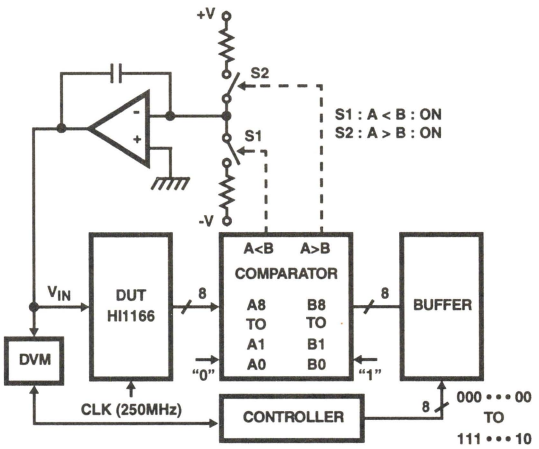


FIGURE 18. INTEGRAL AND DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits and Waveforms (Continued)

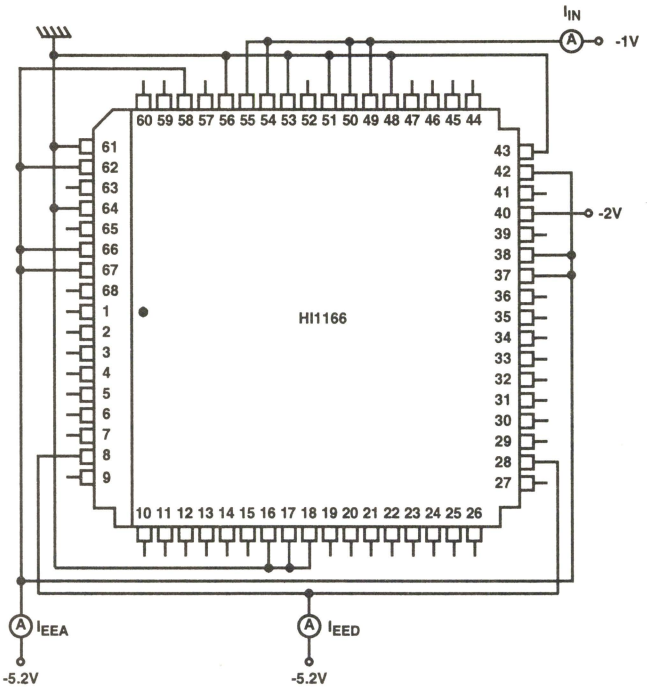


FIGURE 19. POWER SUPPLY AND ANALOG INPUT BIAS CURRENT TEST CIRCUIT

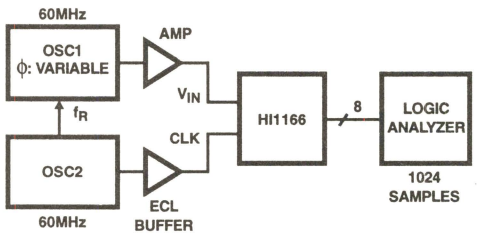
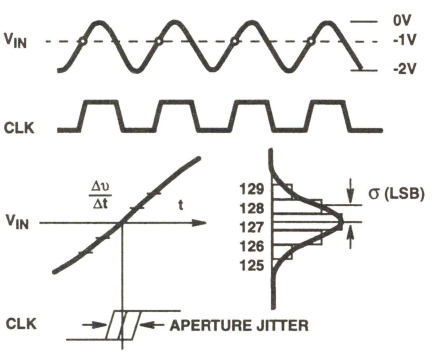


FIGURE 20A.



Aperture jitter is defined as follows:

$$t_{AJ} = \sigma / \frac{\Delta v}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f \right),$$

Where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

FIGURE 20B. APERTURE JITTER TEST METHOD

FIGURE 20. SAMPLING DELAY AND APERTURE JITTER TEST CIRCUIT

HARRIS SEMICONDUCTOR

HI1172

6-Bit, 20 MSPS, Video A/D Converter (CMOS)

August 1997

Features

- Resolution 6-Bit
- Maximum Sampling Frequency . . . . . 20 MSPS
- Low Power Consumption at 20 MSPS (Typ) (Reference Current Excluded) 40mW
- Built-In Sample and Hold Circuit
- Three-State TTL Compatible Output
- Power Supply . . . . . 5V Single
- Low Input Capacitance 4pF
- Reference Impedance . . . . . 250Ω (Typ)

Applications

- Video Digitizing
- Wireless Communications

Description

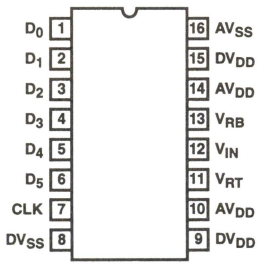
HI1172 is a 6-bit, CMOS A/D converter for video use. The adoption of a 2-step parallel conversion achieves speeds of 20 MSPS minimum, 35 MSPS typical.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1172JCP	-20 to 75	16 Ld PDIP	E16.3A-S
HI1172JCB	-20 to 75	16 Ld SOIC	M16.2-S

Pinout

HI1172
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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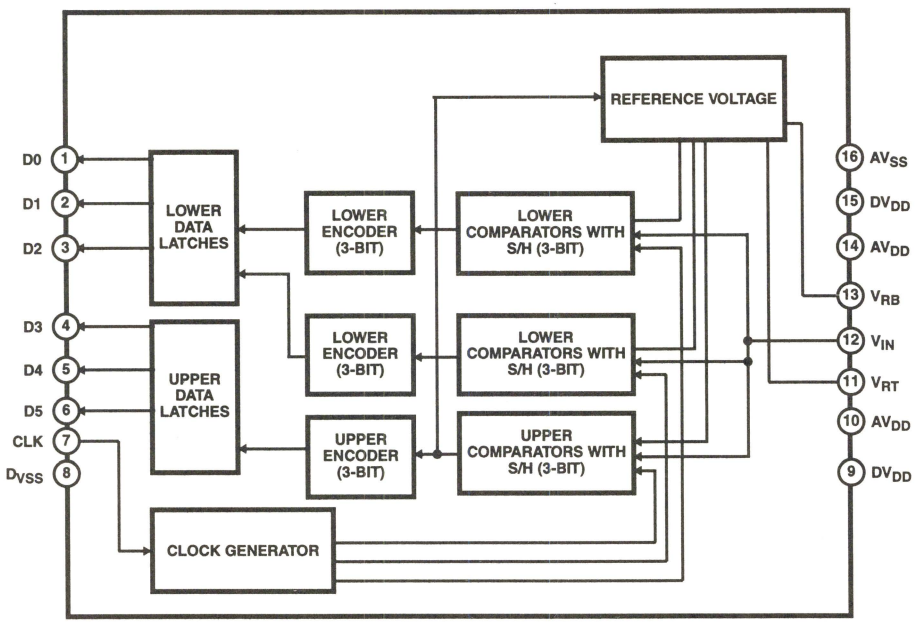
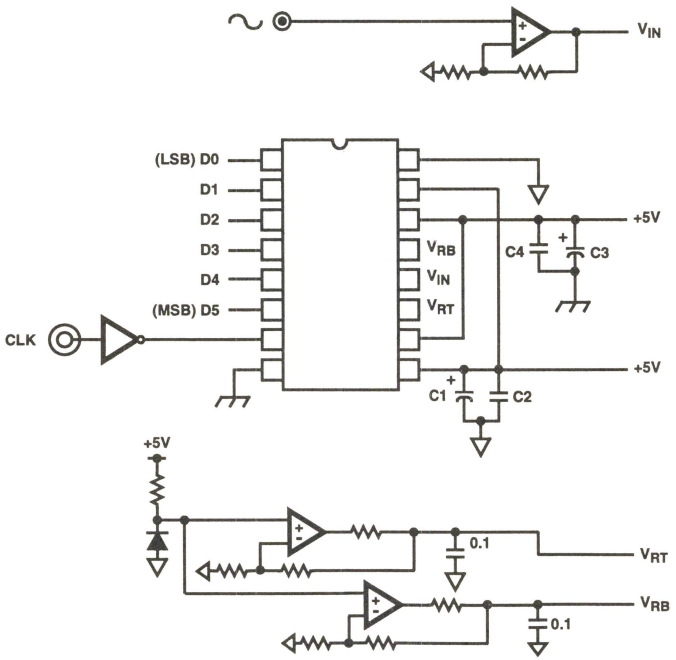
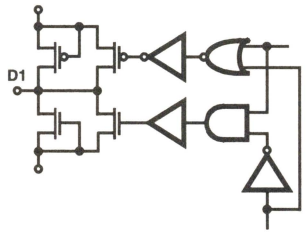
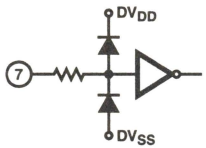
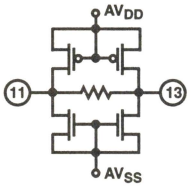
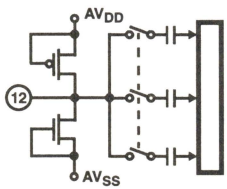
Functional Block Diagram



Typical Application Circuit



Pin Descriptions

NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 6	D0 to D5		D0 (LSB) to D5 (MSB) Output.
7	CLK		Clock Input.
8	DV_{SS}		Digital GND.
9, 15	DV_{DD}		Digital +5V.
10, 14	AV_{DD}		Analog +5V.
11	V_{RT}		Reference Voltage (Top).
13	V_{RB}		Reference Voltage (Bottom).
12	V_{IN}		Analog Input.
16	AV_{SS}		Analog GND.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Reference Voltage (V_{RT}, V_{RB}) . . . . . V_{DD} to V_{SS}
Analog Input Voltage (V_{IN}) . . . . . V_{DD} to V_{SS}
Digital Input Voltage (CLK) . . . . . V_{DD} to V_{SS}
Digital Output Voltage (V_{OH}, V_{OL}) . . . . . V_{DD} to V_{SS}

Operating Conditions

Supply Voltage Range, AV_{DD}, AV_{SS} . . . . . 4.75V to 5.25V
Reference Voltage, DV_{DD}, DV_{SS}
V_{RT} . . . . . 0.9V to 5V
V_{RB} . . . . . 0V to 4.1V
V_{RT} - V_{RB} . . . . . 0.9V to AV_{DD}
Analog Input Voltage (V_{IN}) . . . . . V_{RB} to V_{RT}
Clock Pulse Width
t_{PW1} . . . . . 25ns (Min)
t_{PW0} . . . . . 25ns (Min)
Temperature Range . . . . . -20^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	120
PDIP Package	94

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{DD} = +5V$, $V_{RB} = 1V$, $V_{RT} = 2V$, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Speed, f_C	f_C	V_{IN} = 1V to 2V f_{IN} = 1kHz Ramp		0.5	-	20	MSPS
Integral Non-Linearity	E_L	f_C = 20 MSPS V_{IN} = 1V to 2V		-	±0.3	±0.5	LSB
Differential Non-Linearity	E_D	f_C = 20 MSPS V_{IN} = 1V to 2V		-	±0.3	±0.5	LSB
Supply Current	I_{DD}	f_C = 20 MSPS NTSC Ramp Wave Input		-	7	12	mA
Reference Pin Current	I_{REF}			3	4	5.7	mA
Analog Input (-1dB)	BW			-	18	-	MHz
Analog Input Capacitance	C_{IN}	V_{IN} = 1.5V + 0.07V_{RMS}		-	4	-	pF
Reference Resistance (V_{RT} to V_{RB})	R_{REF}			175	250	325	Ω
Offset Voltage	E_{OT}			0	-20	-40	mV
	E_{OB}			15	35	55	mV
Digital Input Voltage	V_{IH}			4.0	-	-	V
	V_{IL}			-	-	1.0	V
Digital Input Current	I_{IH}	V_{DD} = Max	$V_{IH} = V_{DD}$	-	-	5	µA
	I_{IL}		V_{IL} = 0V	-	-	5	µA
Digital Output Current	I_{OH}	V_{DD} = Min	$V_{OH} = V_{DD} - 0.5V$	-1.1	-	-	mA
	I_{OL}		V_{OL} = 0.4V	3.7	-	-	mA
Output Data Delay	T_{DL}	With TTL 1 Gate and 10pF Load		-	18	30	ns
Differential Gain Error	DG	NTSC 40 IRE Mod		-	1.0	-	%
Differential Phase Error	DP	Ramp, f_C = 14.3 MSPS		-	1.0	-	deg
Aperture Jitter	t_{AJ}			-	40	-	ps
Sampling Delay	t_{SD}			-	4	-	ns

Test Circuits

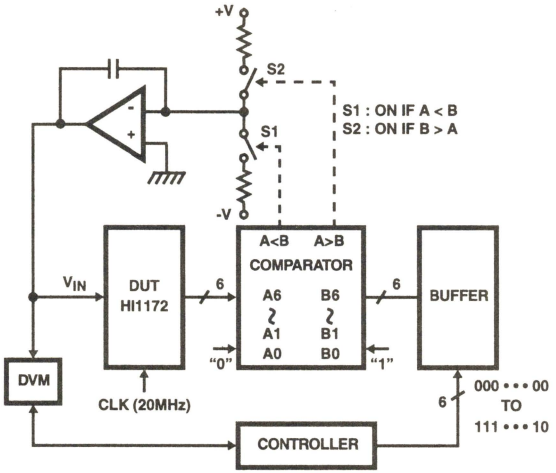


FIGURE 1. INTEGRAL NON-LINEARITY ERROR, DIFFERENTIAL NON-LINEARITY, OFFSET VOLTAGE

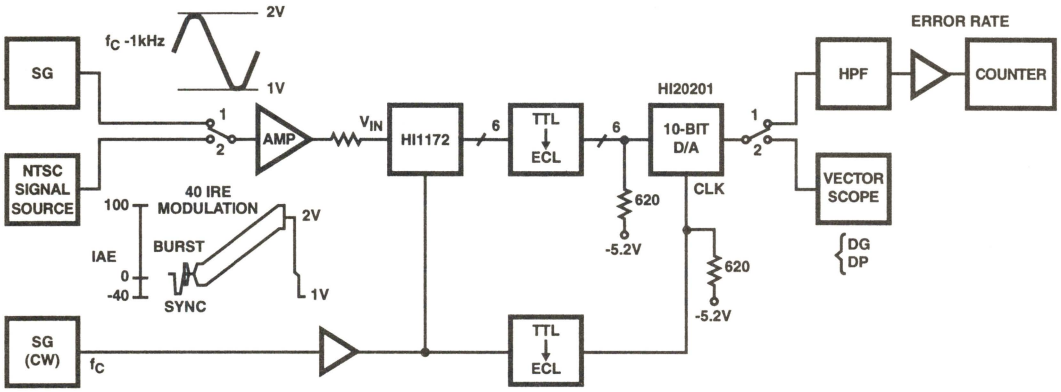


FIGURE 2. MAXIMUM OPERATIONAL SPEED, DIFFERENTIAL GAIN ERROR, DIFFERENTIAL PHASE ERROR

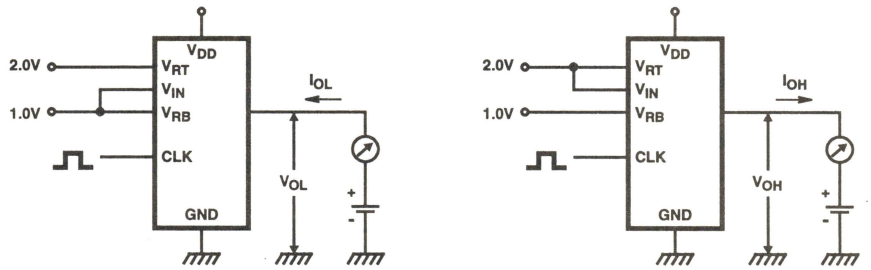


FIGURE 3. DIGITAL OUTPUT CURRENT TEST CIRCUIT

Timing Diagrams

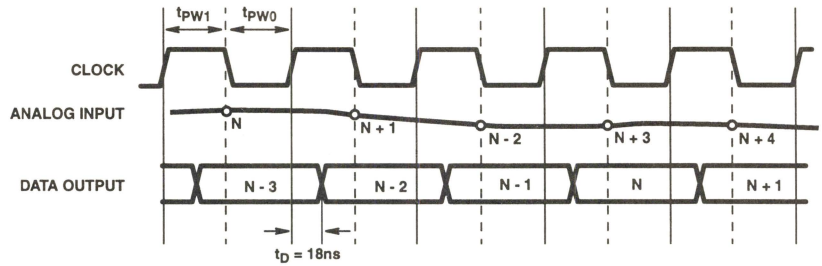


FIGURE 4. TIMING CHART 1

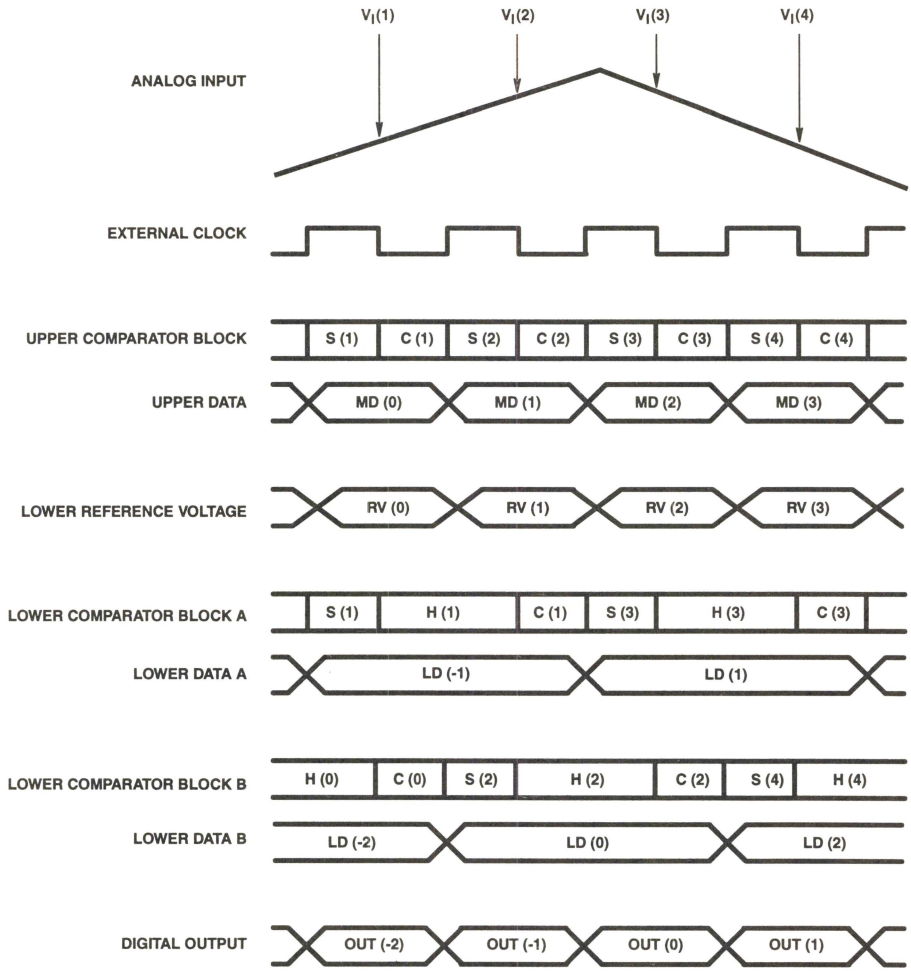


FIGURE 5. TIMING CHART 2

Digital Output

Compatibility between analog input voltage and the digital output code is indicated in the chart below.

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE					
		MSB					LSB
V_{RT}	0	1	1	1	1	1	1
•	•			•			
•	•			•			
•	•			•			
•	31	1	0	0	0	0	1
•	32	0	1	1	1	1	1
•	•			•			
•	•			•			
•	•			•			
V_{RB}	63	0	0	0	0	0	0

Operation (See Block Diagram and Waveform)

The HI1172 is a 2-step parallel system A/D converter featuring a 3-bit upper comparators group and 2 lower comparators groups of 3-bit each. The reference voltage that is equal to the voltage between V_{RT}-V_{RB}/8 is constantly applied to the upper 3-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data.

This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols, i.e., input sampling (auto zero) mode, input hold mode and comparison mode.

The operation of respective parts is as indicated in the chart. Input voltage Vi (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.

The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Notes On Operation

- V_{DD}, V_{SS} - To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1µF set as close as possible to the pin to bypass to the respective GNDs.
- Analog Input - Compared with a flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to drive with an amplifier featuring sufficient bandwidth and drive capability. When driving with an amplifier of low output impedance, parasitic oscillation may occur. That may be prevented by inserting a resistance of about 100Ω in series between the amplifier output and A/D input.
- Clock Input - The clock line wiring should be as short as possible. Also, to avoid any interference with other signals, separate it from the other circuits.
- Reference Input - Voltage between V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. By bypassing V_{RT} and V_{RB} pins to GND with a capacitor of about 0.1µF, stable characteristics are obtained.
- Timing - Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.
- About Latch Up - It is necessary that AV_{DD} and DV_{DD} pins to be the common source of power supply. This is to avoid latch up due to the voltage difference between AV_{DD} and DV_{DD} pins when power is ON.

HARRIS SEMICONDUCTOR

HI1175

August 1997

8-Bit, 20 MSPS, Flash A/D Converter

Features

- Resolution ..... 8-Bit ±0.3 LSB (DNL)
- Maximum Sampling Frequency ..... 20 MSPS
- Low Power Consumption ....60mW (at 20 MSPS Typ) (Reference Current Excluded)
- Built-In Sample and Hold Circuit
- Built-In Reference Voltage Self Bias Circuit
- Three-State TTL Compatible Output
- Single +5V Power Supply
- Low Input Capacitance ..... 11pF (Typ)
- Reference Impedance .....300Ω (Typ)
- Evaluation Board Available (HI1175-EV)
- Low Cost
- Direct Replacement for the Sony CXD1175

Applications

- Video Digitizing
- Image Scanners
- Multimedia
- PC Video Capture
- TV Set Top Boxes
- Personal Communication Systems (PCS)

Description

The HI1175 is an 8-bit, analog-to-digital converter built in a 1.4μm CMOS process. The low power, low differential gain and phase, high sampling rate, and single 5V supply make the HI1175 ideal for video and imaging applications.

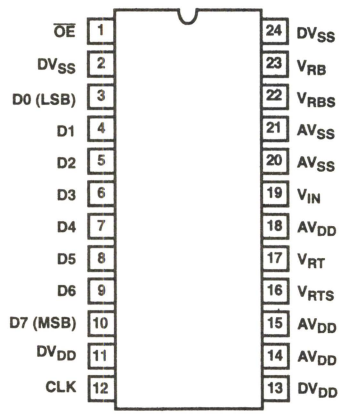
The adoption of a 2-step flash architecture achieves low power consumption (60mW) at a maximum conversion speed of 20 MSPS (Min), 35 MSPS typical with only a 2.5 clock cycle data latency. The HI1175 also features digital output enable/disable and a built in voltage reference. The HI1175 can be configured to use the internal reference or an external reference if higher precision is required.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1175JCP	-40 to 85	24 Ld PDIP	E24.4-S
HI1175JCB	-40 to 85	24 Ld SOIC	M24.2-S
HI1175-EV	25	Evaluation Board	

Pinout

HI1175 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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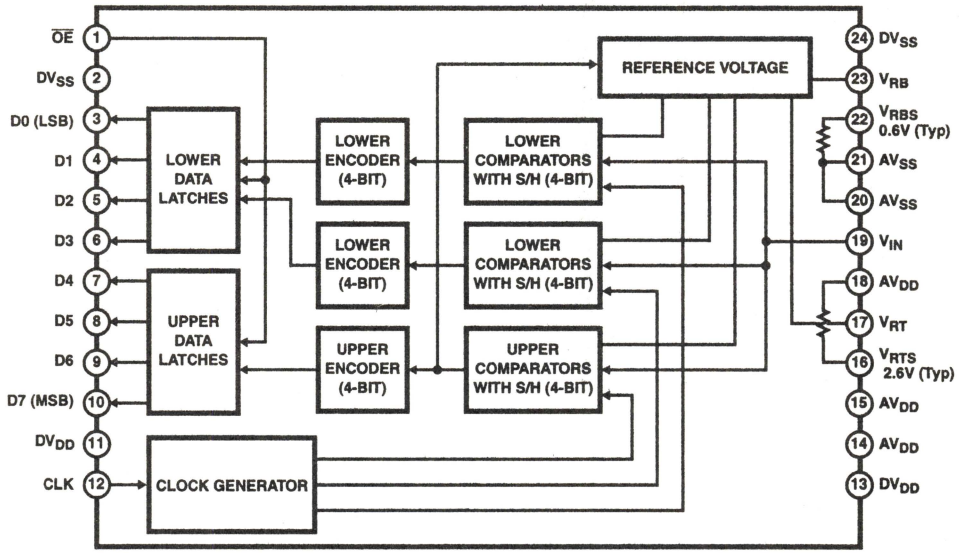
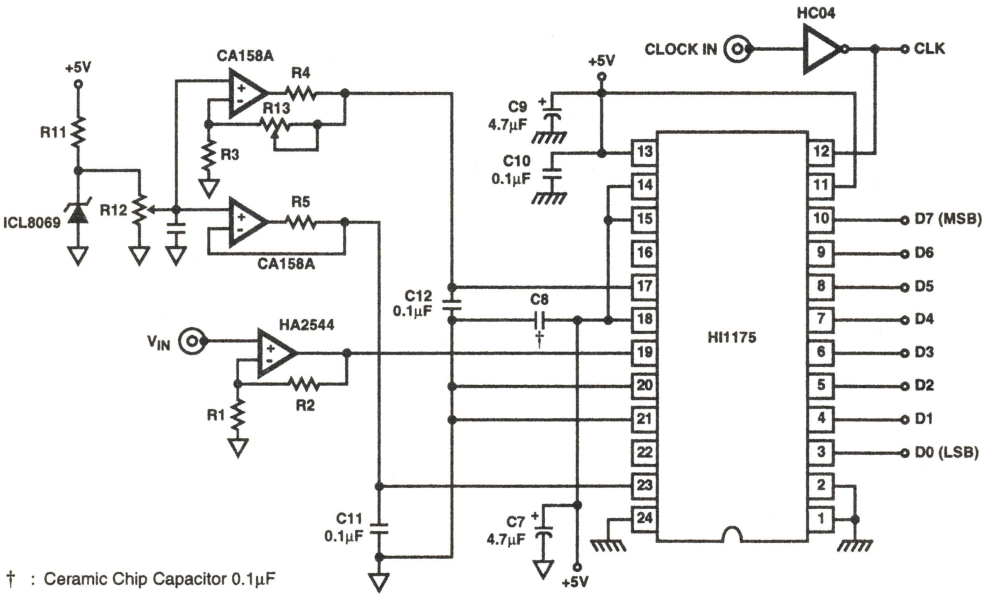
File Number **3577.6**

Functional Block Diagram



Typical Application Schematic



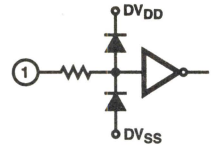
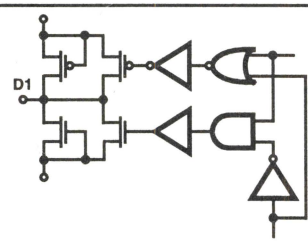
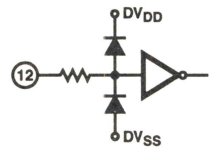
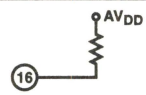
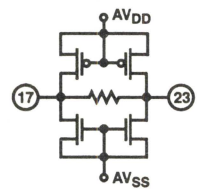
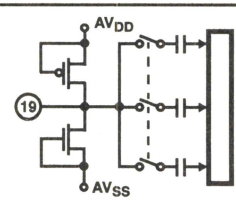
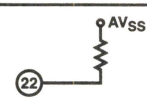
† : Ceramic Chip Capacitor 0.1µF

: Analog GND

: Digital GND

NOTE: It is necessary that AV_{DD} and DV_{DD} pins be driven from the same supply. The gain of analog input signal can be changed by adjusting the ratio of R2 to R1.

Pin Descriptions and Equivalent Circuits

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1	$\overline{OE}$		When $\overline{OE}$ = Low, Data is valid. When $\overline{OE}$ = High, D0 to D7 pins high impedance.
2, 24	DV_{SS}		Digital GND.
3-10	D0 to D7		D0 (LSB) to D7 (MSB) Output.
11, 13	DV_{DD}		Digital +5V.
12	CLK		Clock Input.
16	V_{RTS}		Shorted with V_{RT} generates, +2.6V.
17	V_{RT}		Reference Voltage (Top).
23	V_{RB}		Reference Voltage (Bottom).
14, 15, 18	AV_{DD}		Analog +5V.
19	V_{IN}		Analog Input.
20, 21	AV_{SS}		Analog GND.
22	V_{RBS}		Shorted with V_{RB} generates +0.6V.

Absolute Maximum Ratings

Supply Voltage, V_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} . . . . . V_{DD} to V_{SS}
Analog Input Voltage, V_{IN} . . . . . V_{DD} to V_{SS}
Digital Input Voltage, CLK . . . . . V_{DD} to V_{SS}
Digital Output Voltage, V_{OH}, V_{OL} . . . . . V_{DD} to V_{SS}

Operating Conditions (Note 1)

Temperature Range, T_A . . . . . -40°C to 85°C
Supply Voltage
AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS} . . . . . +4.75V to +5.25V
|DGND-AGND| . . . . . 0mV to 100mV
Reference Input Voltage
V_{RB} . . . . . 0V and Above
V_{RT} . . . . . 2.8V and Below
Analog Input Range, V_{IN} . . . . . V_{RB} to V_{RT} ($1.8V_{P-P}$ to $2.8V_{P-P}$)
Clock Pulse Width
t_{PW1} . . . . . 25ns (Min)
t_{PW0} . . . . . 25ns (Min)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	78
SOIC Package	98

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range, T_{STG} . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

f_C = 20 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Offset Voltage E_{OT}		-60	-35	-10	mV
E_{OB}		0	+15	+45	mV
Integral Non-Linearity, INL	f_C = 20 MSPS, V_{IN} = 0.6V to 2.6V	-	±0.5	±1.3	LSB
Differential Non-Linearity, DNL	f_C = 20 MSPS, V_{IN} = 0.6V to 2.6V	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Effective Number of Bits, ENOB	f_{IN} = 1MHz	-	7.6	-	Bits
Spurious Free Dynamic Range	f_{IN} = 1MHz	-	51	-	dB
Signal to Noise Ratio, SINAD	f_C = 20MHz, f_{IN} = 1MHz	-	46	-	dB
$= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_C = 20MHz, f_{IN} = 3.58MHz	-	46	-	dB
Maximum Conversion Speed, f_C	V_{IN} = 0.6V to 2.6V, f_{IN} = 1kHz Ramp	20	35	-	MSPS
Minimum Conversion Speed		-	-	0.5	MSPS
Differential Gain Error, DG	NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Aperture Jitter, t_{AJ}		-	30	-	ps
Sampling Delay, t_{DS}		-	4	-	ns
Data Latency, t_{LAT}		-	-	2.5	Cycles
ANALOG INPUTS					
Analog Input Bandwidth (-1dB), BW		-	18	-	MHz
Analog Input Capacitance, C_{IN}	V_{IN} = 1.5V + $0.07V_{RMS}$	-	11	-	pF

Electrical Specifications f_C = 20 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE INPUT						
Reference Pin Current, I_{REF}			4.5	6.6	8.7	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}			230	300	450	Ω
INTERNAL VOLTAGE REFERENCE						
Self Bias Mode 1						
V_{RB}	Short V_{RB} and V_{RBS}, Short V_{RT} and V_{RTS}		0.60	0.64	0.68	V
V_{RT} - V_{RB}			1.96	2.09	2.21	V
Self Bias Mode 2, V_{RT}	V_{RB} = AGND, Short V_{RT} and V_{RTS}		2.25	2.39	2.53	V
DIGITAL INPUTS						
Digital Input Voltage						
V_{IH}			4.0	-	-	V
V_{IL}			-	-	1.0	V
Digital Input Current						
I_{IH}	V_{DD} = Max	V_{IH} = V_{DD}	-	-	5	µA
I_{IL}		V_{IL} = 0V	-	-	5	µA
DIGITAL OUTPUTS						
Digital Output Current						
I_{OH}	$\overline{OE}$ = V_{SS}, V_{DD} = Min	V_{OH} = V_{DD} -0.5V	-1.1	-	-	mA
I_{OL}		V_{OL} = 0.4V	3.7	-	-	mA
Digital Output Current						
I_{OZH}	$\overline{OE}$ = V_{DD}, V_{DD} = Max	V_{OH} = V_{DD}	-	0.01	16	µA
I_{OZL}		V_{OL} = 0V	-	0.01	16	µA
TIMING CHARACTERISTICS						
Output Data Delay, t_{DL}			-	18	30	ns
POWER SUPPLY CHARACTERISTIC						
Supply Current, I_{DD}	f_C = 20 MSPS, NTSC Ramp Wave Input		-	12	17	mA

NOTE:

2. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams

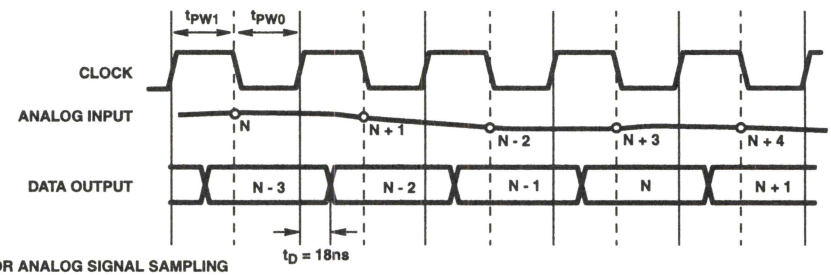


FIGURE 1.

Timing Diagrams

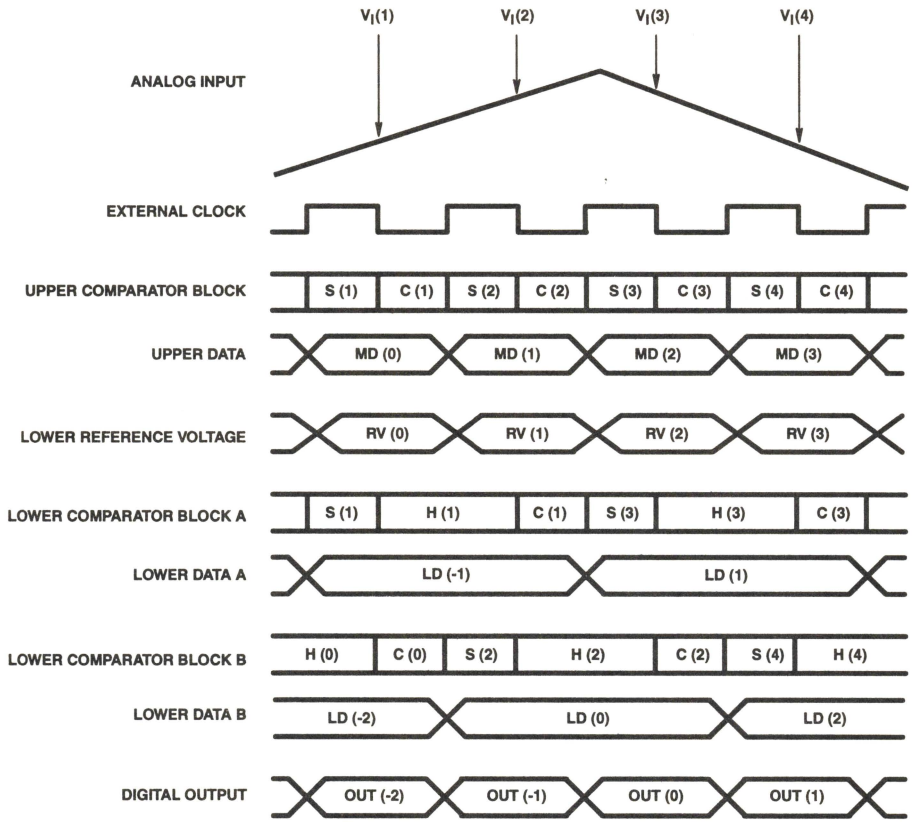


FIGURE 2.

Typical Performance Curves

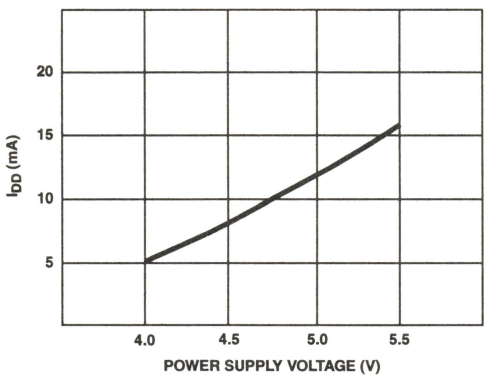


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

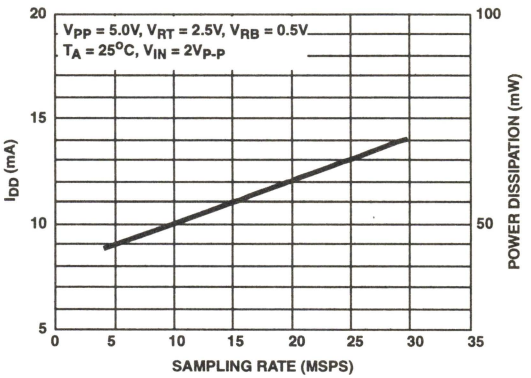


FIGURE 4. SUPPLY CURRENT AND POWER vs SAMPLING RATE

Typical Performance Curves (Continued)

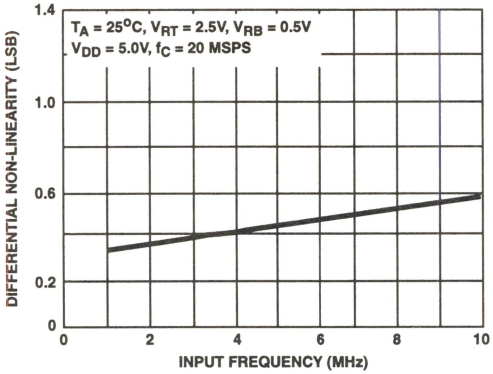


FIGURE 5. DIFFERENTIAL NON-LINEARITY vs INPUT FREQUENCY

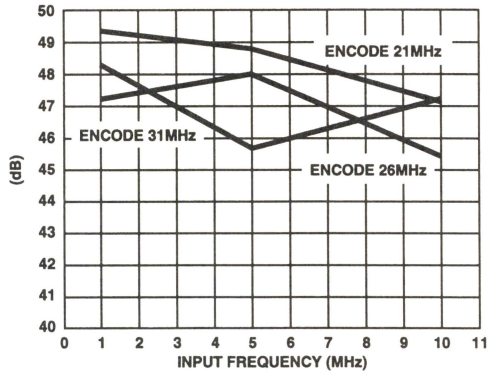


FIGURE 6. HI1175JCP SNR vs INPUT FREQUENCY

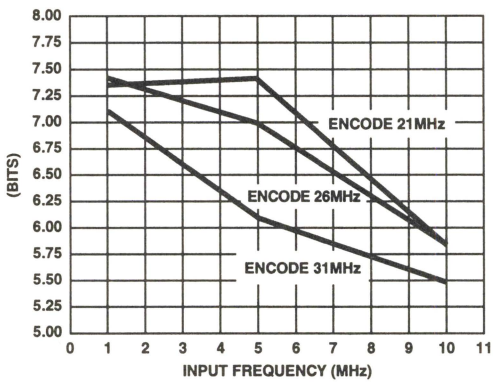


FIGURE 7. HI1175JCP ENOB vs INPUT FREQUENCY

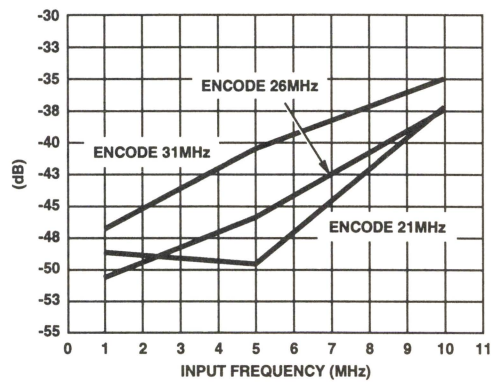


FIGURE 8. HI1175JCP THD vs INPUT FREQUENCY

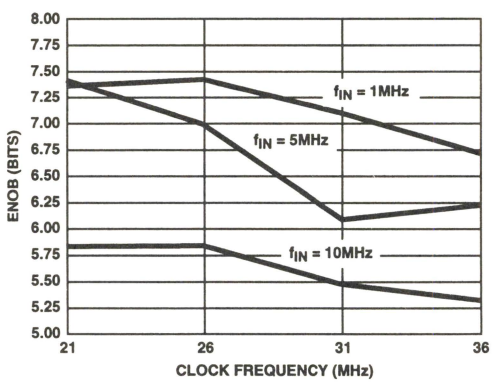


FIGURE 9. ENOB vs CLOCK FREQUENCY

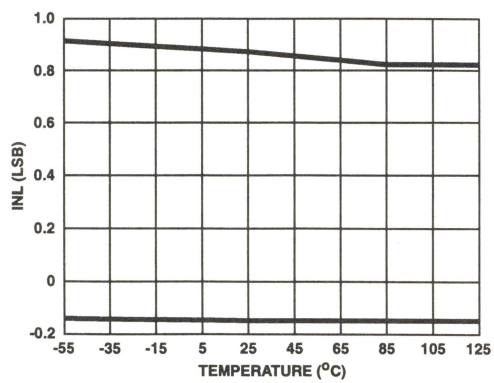


FIGURE 10. INL vs TEMPERATURE

Typical Performance Curves (Continued)

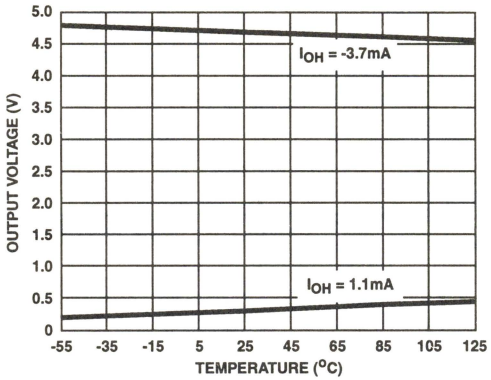


FIGURE 11. DIGITAL OUTPUT VOLTAGE vs TEMPERATURE

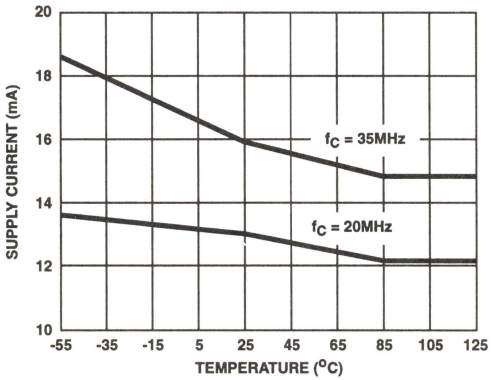


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

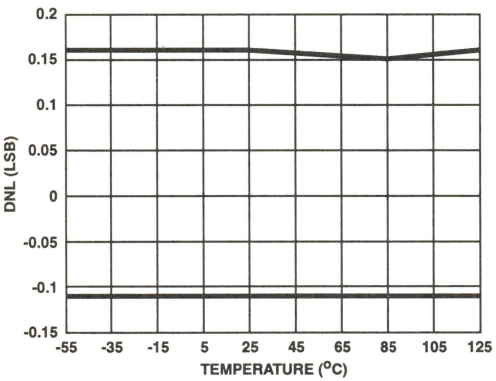


FIGURE 13. DNL vs TEMPERATURE

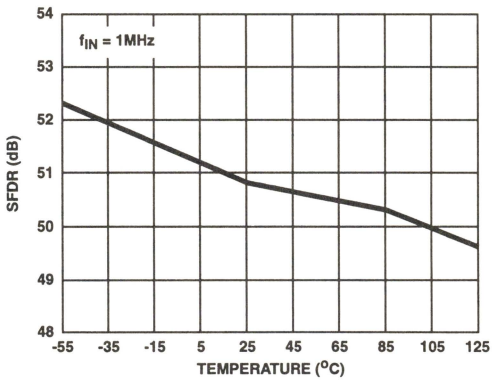


FIGURE 14. SFDR vs TEMPERATURE

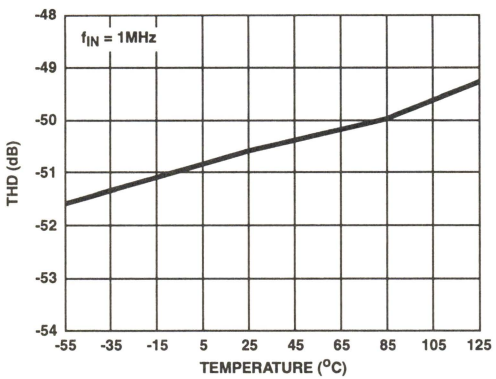


FIGURE 15. THD vs TEMPERATURE

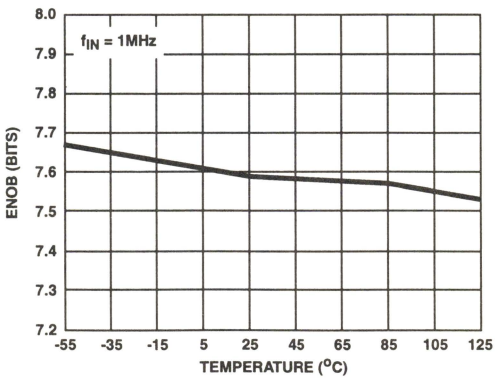


FIGURE 16. ENOB vs TEMPERATURE

Typical Performance Curves (Continued)

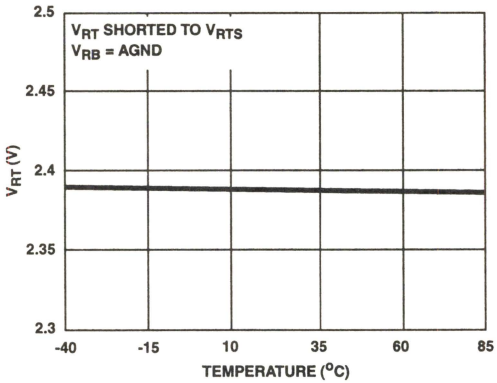


FIGURE 17. V_{RT} vs TEMPERATURE

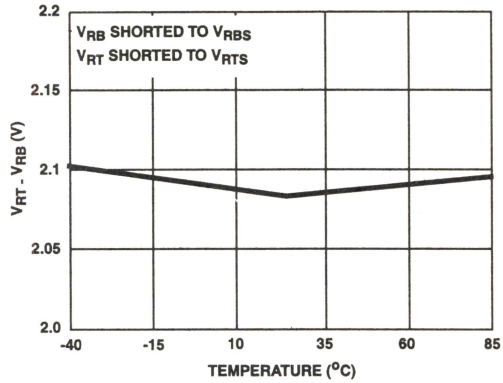


FIGURE 18. V_{RT} - V_{RB} vs TEMPERATURE

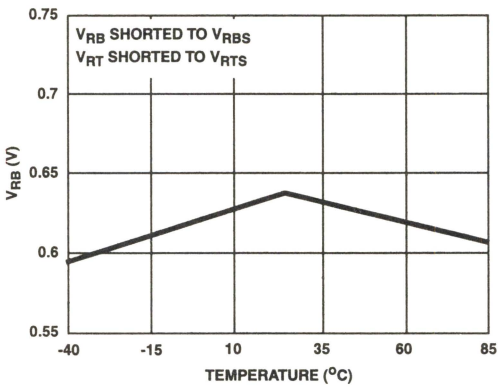


FIGURE 19. V_{RB} vs TEMPERATURE

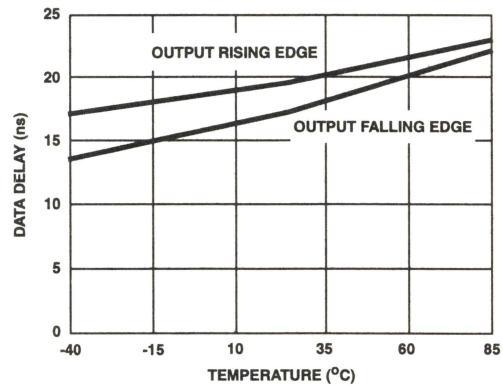


FIGURE 20. OUTPUT DATA DELAY vs TEMPERATURE

A/D OUTPUT CODE TABLE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB	D6	D5	D4	D3	D2	D1	LSB
V_{RT}	255	1	1	1	1	1	1	1	1
	•					•			
•	•					•			
•	•					•			
•									
•	128	1	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1
•									
•	•					•			
•	•					•			
	•					•			
V_{RB}	0	0	0	0	0	0	0	0	0

Detailed Description

The HI1175 is a 2-step A/D converter featuring a 4-bit upper comparator group and two lower comparator groups of 4 bits each. The reference voltage can be obtained from the onboard bias generator or be supplied externally. This IC uses an offset canceling type comparator that operates synchronously with an external clock. The operating modes of the part are input sampling (S), hold (H), and compare (C).

The operation of the part is illustrated in Figure 2. A reference voltage that is between V_{RT}-V_{RB} is constantly applied to the upper 4-bit comparator group. $V_I(1)$ is sampled with the falling edge of the first clock by the upper comparator block. The lower block A also samples $V_I(1)$ on the same edge. The upper comparator block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates a reference voltage RV(1) that corresponds to the upper results and applies it to the lower comparator block A. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as OUT(1) with the rising edge of the third clock. There is a 2.5 cycle clock delay from the analog input sampling point to the corresponding digital output data. Notice how the lower comparator blocks A and B alternate generating the lower data in order to increase the overall A/D sampling rate.

Power, Grounding, and Decoupling

To reduce noise effects, separate the analog and digital grounds.

In order to avoid latchup at power up, it is necessary that AV_{DD} and DV_{DD} be driven from the same supply.

Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1µF capacitor close to the pin.

Analog Input

The input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with an amplifier with sufficient bandwidth and drive capability. In order to prevent parasitic oscillation, it may be necessary to insert a low value (i.e., 0.24Ω) resistor between the output of the amplifier and the A/D input.

Reference Input

The range of the A/D is set by the voltage between V_{RT} and V_{RB}. The internal bias generator will set V_{RTS} to 2.6V and V_{RBS} to 0.6V. These can be used as the part reference by shorting V_{RT} and V_{RTS} and V_{RB} to V_{RBS}. The analog input range of the A/D will now be from 0.6V to 2.6V and is referred to as Self Bias Mode 1. Self Bias Mode 2 is where V_{RB} is connected to AGND and V_{RT} is shorted to V_{RTS}. The analog input range will now be from 0V to 2.4V.

Test Circuits

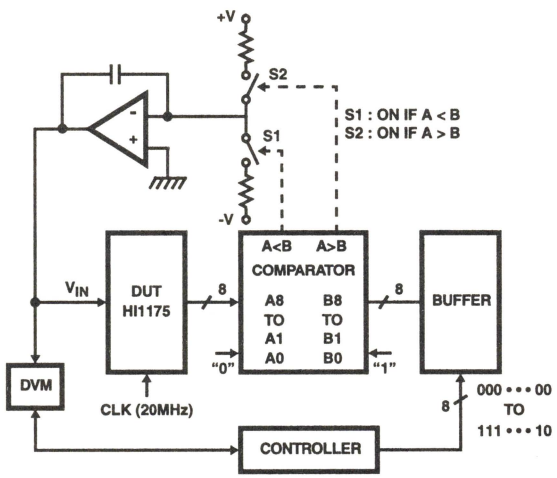


FIGURE 21. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

Test Circuits (Continued)

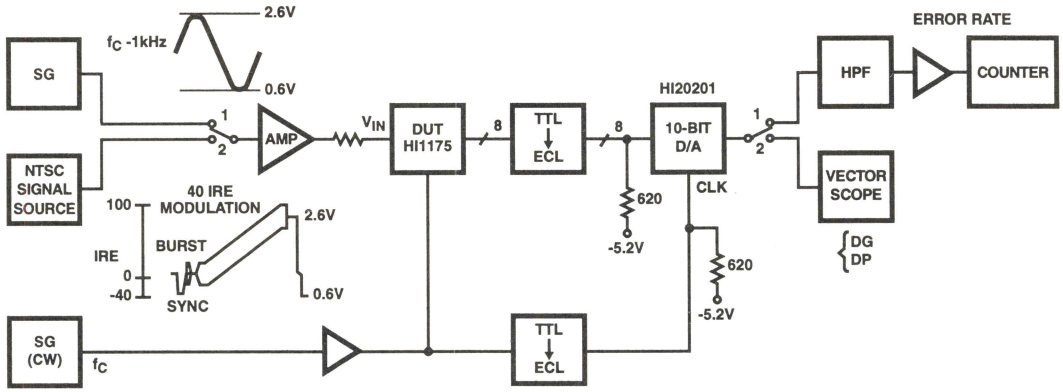


FIGURE 22. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

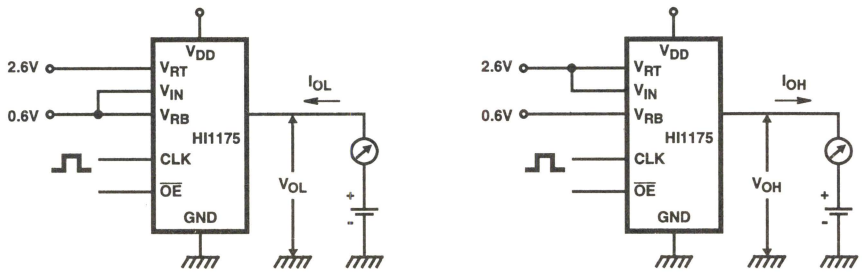
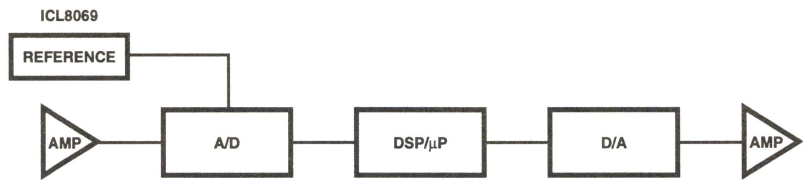


FIGURE 23. DIGITAL OUTPUT CURRENT TEST CIRCUIT



HA5020 (Single) HA5022(Dual) HA5024 (Quad) HA5013 (Triple)	HI1175 (8-Bit)	HSP9501 HSP48901 HSP43881 HSP43168	HI3338 (8-Bit) HI1171 (8-Bit)	HA5020 (Single)

HSP9501: Programmable Data Buffer
HSP48901: 3 x 3 Image Filter, 30MHz, 8-Bit
HSP43881: Digital Filter, 30MHz, 1-D and 2-D FIR Filters
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz

CMOS Logic Available in HC, HCT, AC, ACT and FCT.

HA5013: Triple, 125MHz, I_{OUT} = 20mA
HA5020: Single, 100MHz, I_{OUT} = 30mA, Output Enable/Disable
HA5022: Dual, 125MHz, I_{OUT} = 20mA, Output Enable/Disable
HA5024: Quad, 125MHz, I_{OUT} = 20mA, Output Enable/Disable

FIGURE 24. 8-BIT SYSTEM COMPONENTS

Static Performance Definitions

Offset, full scale, and gain all use a measured value of the internal voltage reference to determine the ideal plus and minus full scale values. The results are all displayed in LSBs.

Offset Error (E_{OB})

The first code transition should occur at a level $^1/_2$ LSB above the bottom reference voltage. Offset is defined as the deviation of the actual code transition from this point. Note that this is adjustable to zero.

Full Scale Error (E_{OT})

The last code transition should occur for a analog input that is $1^1/_2$ LSBs below full scale. Full scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed to have no missing codes.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI1175. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 1024 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from fullscale for all these tests. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to fullscale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02,$$

where: $V_{CORR} = 0.5dB$.

Total Harmonic Distortion

This is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the 2nd and 3rd harmonic component respectively to the RMS value of the measured input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

Full Power Input Bandwidth

Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Timing Definitions

Sampling Delay (t_{SD})

Sampling delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

This is the RMS variation in the sampling delay due to variation of internal clock path delays.

Data Latency (t_{LAT})

After the analog sample is taken, the data on the bus is available after 2.5 cycles of the clock. This is due to the architecture of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 2.5 cycles.

Output Data Delay (t_D)

Output Data Delay is the delay time from when the data is valid (rising clock edge) to when it shows up at the output bus. This is due to internal delays at the digital output.

HARRIS SEMICONDUCTOR

HI1176

August 1997

8-Bit, 20 MSPS, Flash A/D Converter

Features

- Resolution ±0.5 LSB (DNL) 8-Bit
- Maximum Sampling Frequency . . . . . 20 MSPS
- Low Power Consumption at 20 MSPS (Typ) (Reference Current Excluded) 60mW
- Built-In Sync Clamp Function
- Built-In Monostable Multivibrator for Clamp Pulse Generation
- Built-In Sync Pulse Polarity Selection Function
- Clamp Pulse Direct Input Possible
- Built-In Clamp ON/OFF Function
- Built-In Reference Voltage Self Bias Circuit
- Input CMOS Compatible
- Three-State TTL Compatible Output
- Single +5V Power Supply
- Low Input Capacitance (Typ) 11pF
- Reference Impedance (Typ) 300Ω
- Direct Replacement for the Sony CXD1176

Description

The HI1176 is an 8-bit, CMOS analog-to-digital converter for video use that features a sync clamp function. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 20 MSPS. For higher sampling rates, refer to the pin-for-pin compatible HI1179 data sheet, AnswerFAX document number 3666.

Applications

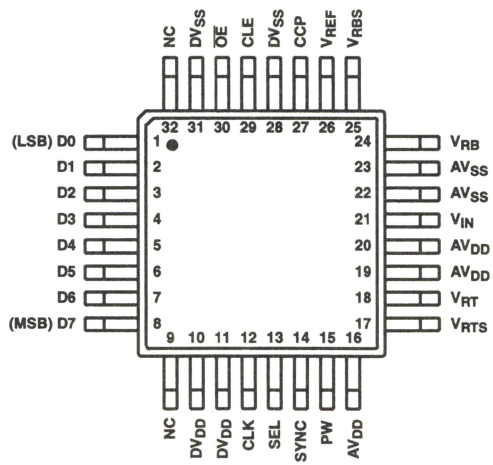
- Video Digitizing
- Image Scanners
- Low Cost High Speed Data Acquisition Systems
- Multimedia

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1176JCQ	-40 to 85	32 Ld MQFP	Q32.7x7-S
HI1176-EV	25	Evaluation Board	

Pinout

HI1176
(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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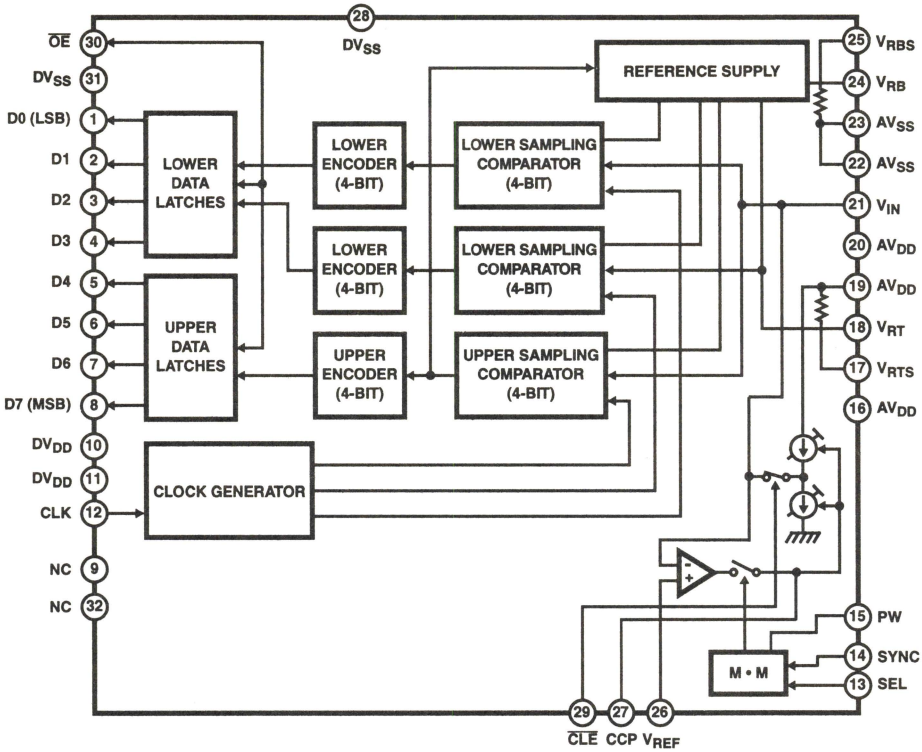
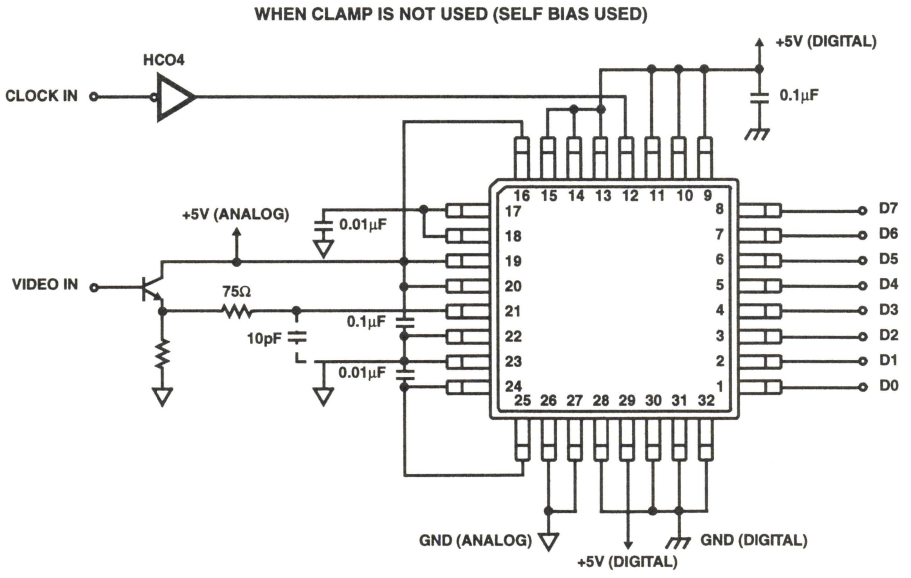
File Number **3582.4**

Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage, V_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Analog Input Voltage, V_{IN} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Digital Input Voltage, CLK . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Digital Output Voltage, V_{OH}, V_{OL} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V

Operating Conditions (Note 1)

Temperature Range, T_A . . . . . -40°C to 85°C
Supply Voltage
AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS} . . . . . +4.75V to +5.25V
IDGND-AGNDI . . . . . .0mV to 100mV
Reference Input Voltage
V_{RB} . . . . . 0V and Above
V_{RT} . . . . . 2.8V and Below
Analog Input Voltage, V_{IN} . . . . . V_{RB} to V_{RT} ($1.8V_{P-P}$ to AV_{DD})
Clock Pulse Width
t_{PW1} . . . . . 25ns (Min)
t_{PW0} . . . . . 25ns (Min)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
MQFP Package	122

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

f_C = 20 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Offset Voltage E_{OT}		-60	-40	-20	mV
E_{OB}		+20	+40	+60	mV
Integral Non-Linearity, INL	f_C = 20 MSPS, V_{IN} = 0.5V to 2.5V	-	±0.5	±1.3	LSB
Differential Non-Linearity, DNL	f_C = 20 MSPS, V_{IN} = 0.5V to 2.5V	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Signal to Noise Ratio, SINAD	f_S = 20MHz, f_{IN} = 1MHz	-	46	-	dB
$\frac{\text{RMS Signal}}{\text{Signal-To-Noise + Distortion Ratio, SINAD}}$	f_S = 20MHz, f_{IN} = 3.58MHz	-	46	-	dB
Maximum Conversion Speed, f_C	V_{IN} = 0.5V to 2.5V, f_{IN} = 1kHz Ramp	20	35	-	MSPS
Minimum Conversion Speed		-	-	0.5	MSPS
Differential Gain Error, DG	NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Aperture Jitter, t_{AJ}		-	30	-	ps
Sampling Delay, t_{DS}		-	4	-	ns
ANALOG INPUTS					
Analog Input Bandwidth (-1dB), BW		-	18	-	MHz
Analog Input Capacitance, C_{IN}	$V_{IN} = 1.5V + 0.07V_{RMS}$	-	11	-	pF

Electrical Specifications f_C = 20 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE INPUT						
Reference Pin Current, I_{REF}			4.5	6.6	8.7	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}			230	300	450	Ω
INTERNAL VOLTAGE REFERENCES						
Self Bias						
V_{RB}	Short V_{RB} and V_{RBS}, Short V_{RT} and V_{RTS}		0.48	0.52	0.56	V
V_{RT} - V_{RB}			1.96	2.08	2.22	V
DIGITAL INPUTS						
Digital Input Voltage						
V_{IH}			4.0	-	-	V
V_{IL}			-	-	1.0	V
Digital Input Current						
I_{IH}	V_{DD} = Max	V_{IH} = V_{DD}	-	-	5	µA
I_{IL}		V_{IL} = 0V	-	-	5	µA
DIGITAL OUTPUTS						
Digital Output Current						
I_{OH}	$\overline{OE}$ = V_{SS}, V_{DD} = Min	V_{OH} = V_{DD} -0.5V	-1.1	-	-	mA
I_{OL}		V_{OL} = 0.4V	3.7	-	-	mA
Digital Output Current						
I_{OZH}	$\overline{OE}$ = V_{DD}, V_{DD} = Max	V_{OH} = V_{DD}	-	-	16	µA
I_{OZL}		V_{OL} = 0V	-	-	16	µA
TIMING CHARACTERISTICS						
Output Data Delay, t_{DL}			-	18	30	ns
POWER SUPPLY CHARACTERISTIC						
Supply Current, I_{DD}	f_C = 20 MSPS, NTSC Ramp Wave Input		-	12	18	mA
CLAMP CHARACTERISTICS						
Clamp Offset Voltage, E_{OC}	V_{IN} = DC, PWS = 3µs	V_{REF} = 0.5V	0	+20	+40	mV
		V_{REF} = 2.5V	-50	-30	-10	mV
Clamp Pulse Width (Sync Pin Input), t_{CPW}	C = 100pF, R = 130kΩ on Pin 15		1.75	2.75	3.75	µs
Clamp Pulse Delay, t_{CPD}			-	25	-	ns

NOTE:

1. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams

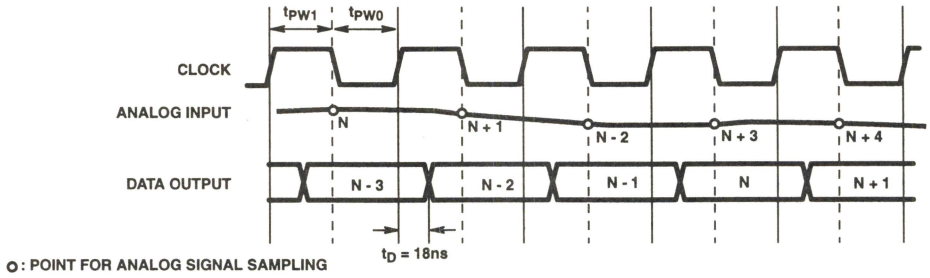


FIGURE 1.

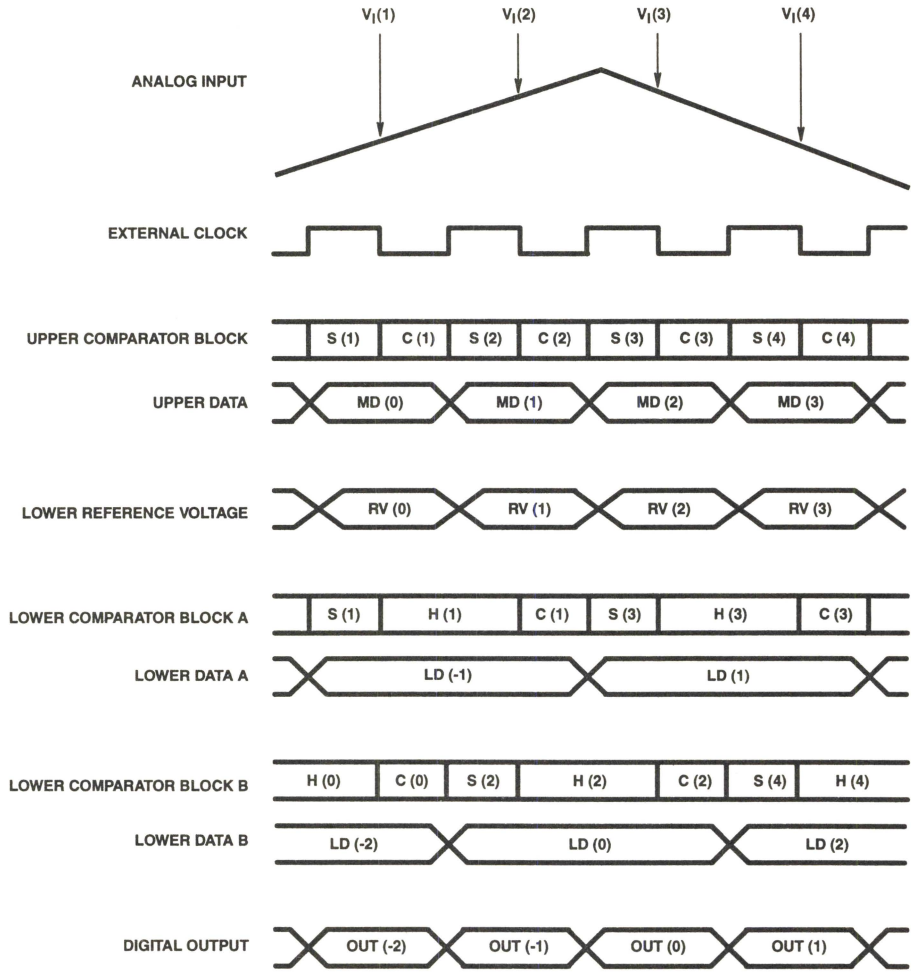


FIGURE 2.

Typical Performance Curves

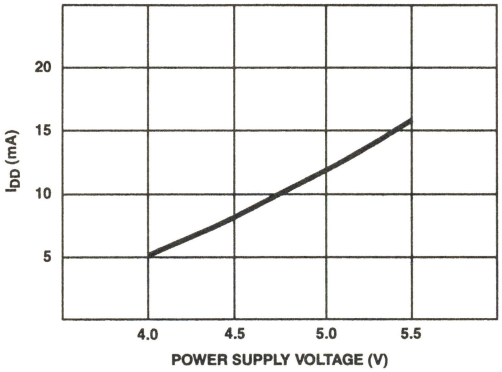


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

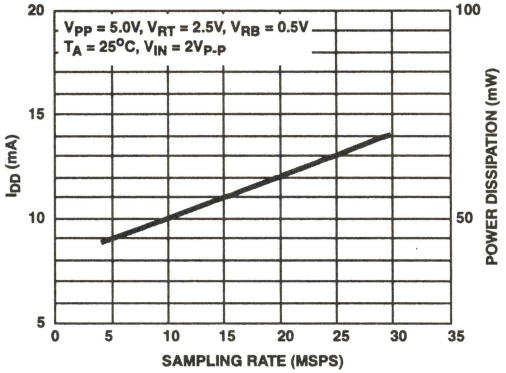


FIGURE 4. SUPPLY CURRENT AND POWER vs SAMPLING RATE

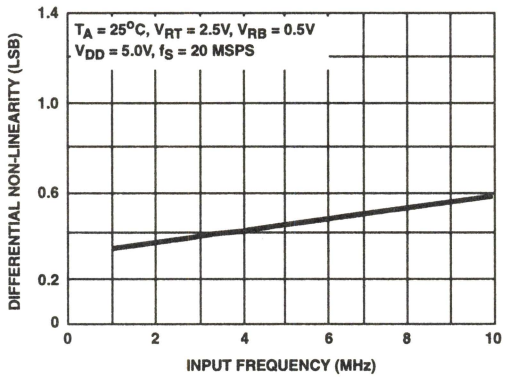
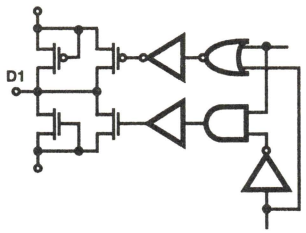
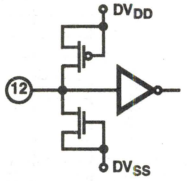
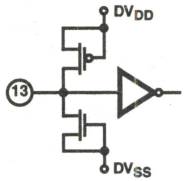
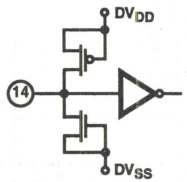
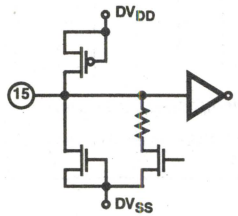
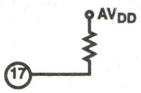
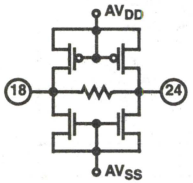


FIGURE 5. DIFFERENTIAL NON-LINEARITY vs INPUT FREQUENCY

Pin Descriptions

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1-8	D0 to D7		D0 (LSB) to D7 (MSB) Output.
10, 11	DV_{DD}		Digital +5V.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
12	CLK		Clock Input.
13	SEL		When SEL is low, the falling edge of Pin 14 (sync) triggers the monostable. When SEL is high, the rising edge of Pin 14 (sync) triggers the monostable.
14	SYNC		Trigger pulse input to the monostable multivibrator. Trigger polarity can be controlled by Pin 13 (SEL).
15	PW		When a clamp pulse is generated by the monostable, the pulse width is determined by the external R and C. When the clamp pulse is directly input, it is input to Pin 15 (PW).
16, 19, 20	AV_{DD}		Analog +5V.
17	V_{RTS}		When shorted with V_{RT}, generates approx. +2.6V.
18	V_{RT}		Reference Voltage (Top).
24	V_{RB}		Reference Voltage (Bottom).

Pin Descriptions (Continued)

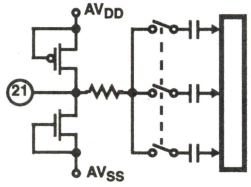
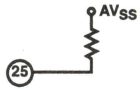
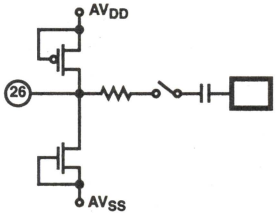
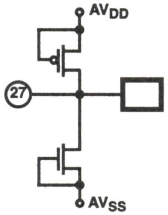
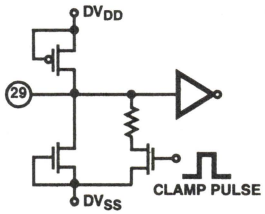
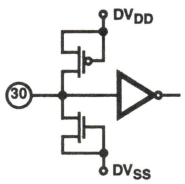
PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
21	V_{IN}		Analog Input.
22, 23	AV_{SS}		Analog Ground.
25	V_{RBS}		When shorted with V_{RB}, generates approx. +0.5V.
26	V_{REF}		Clamp Reference Voltage Input.
27	CCP		Integrates the voltage for clamp control.
28, 31	DV_{SS}		Digital GND.
29	$\overline{CLE}$		When $\overline{CLE}$ is low, clamp function is activated. When $\overline{CLE}$ is high, clamp function is OFF and only the usual A/D converter function is active. By connecting $\overline{CLE}$ pin to DV_{DD} via a several hundred Ω resistance, the clamp pulse can be tested.
30	$\overline{OE}$		When $\overline{OE}$ is low, data is valid. When $\overline{OE}$ is high, D0 to D7 pins are high impedance.

TABLE 1. A/D OUTPUT CODE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
V_{RT}	255	1	1	1	1	1	1	1	1
	•					•			
	•					•			
	•					•			
	•								
	128	1	0	0	0	0	0	0	0
	127	0	1	1	1	1	1	1	1
	•					•			
	•					•			
	•					•			
	•								
V_{RB}	0	0	0	0	0	0	0	0	0

Detailed Description

The HI1176 is a 2-step A/D converter featuring a 4-bit upper comparator group and two lower comparator groups of 4 bits each. The reference voltage can obtained from the onboard bias generator or be supplied externally. This IC uses an offset canceling type comparator that operates synchronously with an external clock. The operating modes of the part are input sampling/autozero (S), hold (H), and compare (C).

The operation of the part is illustrated in Figure 2. A reference voltage that is between V_{RT}-V_{RB} is constantly applied to the upper 4-bit comparator group. $V_I(1)$ is sampled with the falling edge of the first clock by the upper comparator block. The lower block A also samples $V_I(1)$ on the same edge. The upper comparator block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates a reference voltage RV(1) that corresponds to the upper results and applies it to the lower comparator block A. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as OUT(1) with the rising edge of the third clock. There is a 2.5 cycle clock delay from the analog input sampling point to the corresponding digital output data. Notice how the lower comparator blocks A and B alternate generating the lower data in order to increase the overall A/D sampling rate.

Power, Grounding, and Decoupling

To reduce noise effects, separate the analog and digital grounds.

Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1µF capacitor close to the pin.

Analog Input

The input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with an amplifier with sufficient bandwidth and drive capability. In order to prevent parasitic oscillation, it may be necessary to insert a resistor between the output of the amplifier and the A/D input.

Reference Input

The range of the A/D is set by the voltage between V_{RT} and V_{RB}. The internal bias generator will set V_{RTS} to 2.5V and V_{RBS} to 0.5V. These can be used as the part reference by shorting V_{RT} and V_{RTS} and V_{RB} to V_{RBS}. The analog input range of the A/D will now be from 0.5V to 2.5V. If a V_{RB} below +0.5V is used the linearity of the part will be degraded.

Bypass V_{RT} and V_{RB} to analog ground with a 0.1µF capacitor.

Clamp Operation

The HI1176 provides a clamp option that allows the user to clamp a portion of the analog input to a voltage set by the V_{REF} pin. The clamp function is enabled by bringing $\overline{CLE}$ low. An internal monostable multivibrator is provided that can be used to generate the clamp pulses. The monostable pulse width is determined by the external R and C connected to the PW pin. The trigger to the monostable is applied on the SYNC pin. The edge that triggers the monostable is determined by the SEL pin. When SEL is low the falling edge will trigger the monostable and when SEL is high the rising edge will trigger the monostable. Figure 6 shows the HI1176 configured for this mode of operation. The clamp pulse is latched by the ADC sampling clock. This is not necessary to the operation of the clamp function but if this is not done then a slight beat might be generated as vertical sag according to the relation between the sampling frequency and the clamp frequency.

The HI1176 can also be configured to operate with an external clamp pulse. In this case a negative going pulse is input to the PW pin. V_{IN} will now be clamped during the low period of the clamp pulse to the voltage on the V_{REF} pin. Figure 7 shows the HI1176 configured for this mode of operation.

Figure 1 illustrates the operation of HI1176 when the clamp function is not used.

Typical Application Circuits

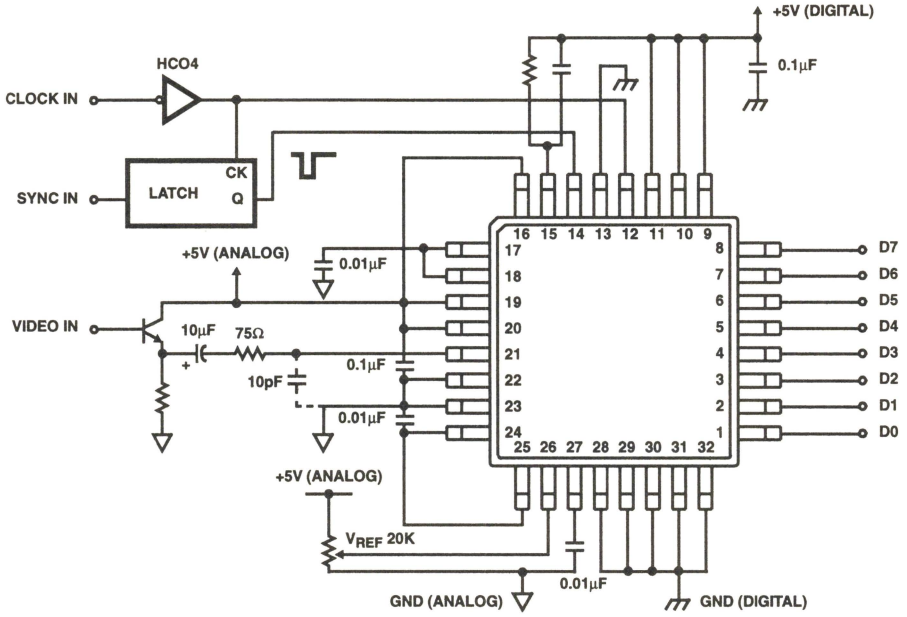


FIGURE 6. PEDESTAL CLAMP IS EXECUTED BY SYNC PULSE (SELF BIAS USED)

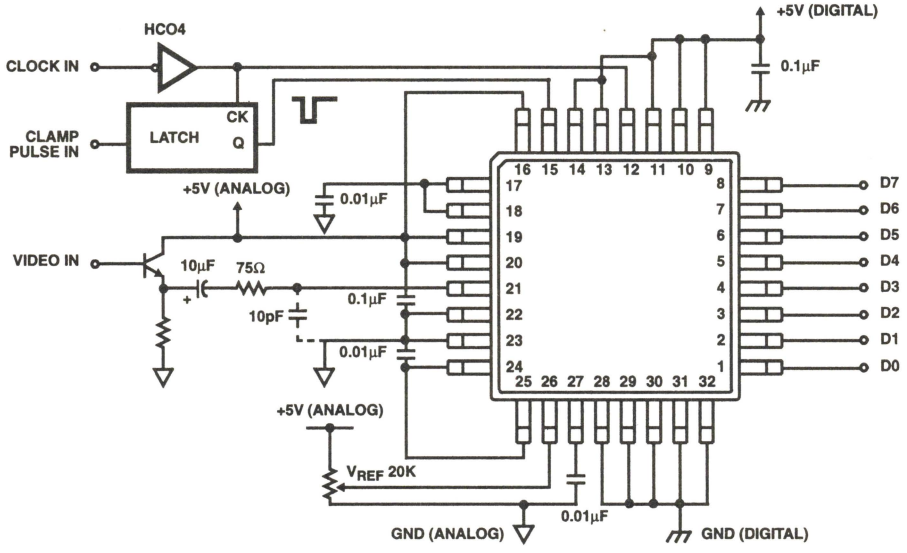


FIGURE 7. CLAMP PULSE IS DIRECTLY INPUT (SELF BIAS USED)

Test Circuits

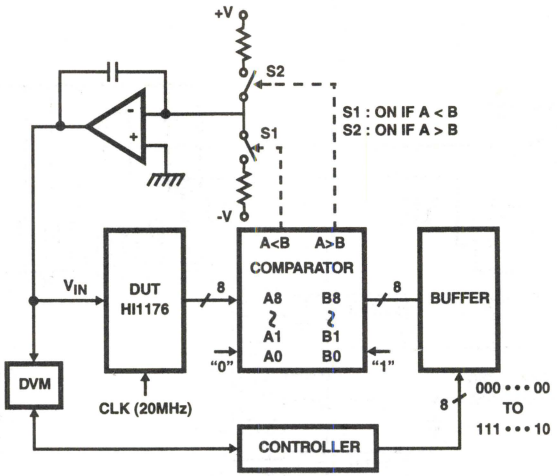


FIGURE 8. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

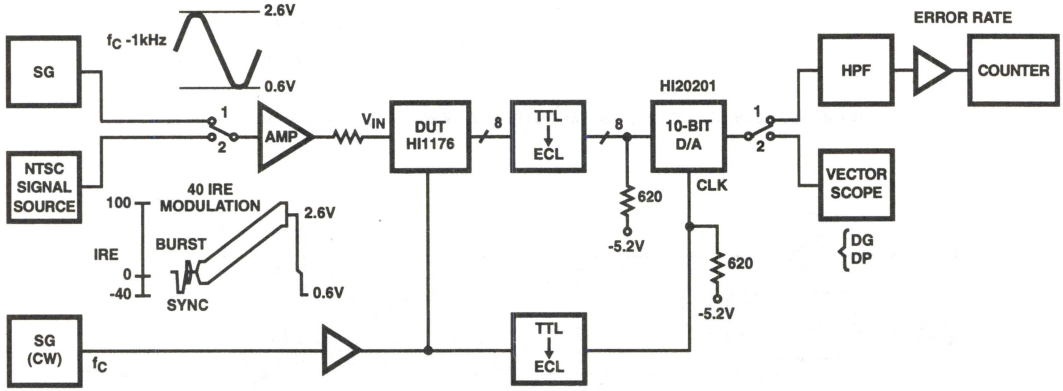


FIGURE 9. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

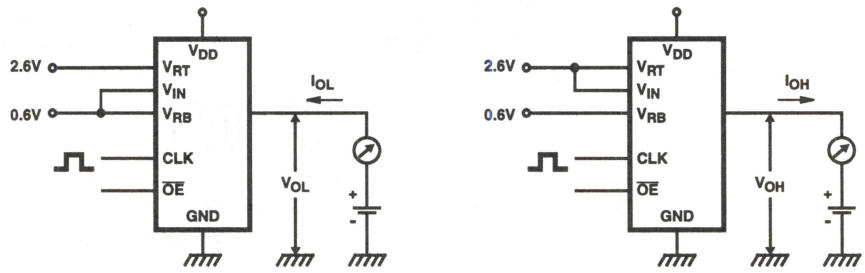


FIGURE 10. DIGITAL OUTPUT CURRENT TEST CIRCUIT

8-Bit, 35 MSPS, Video A/D Converter

Features

- Resolution 8-Bit . . . . . ±0.5 LSB (DNL)
- ENOB at f_{IN} = 1MHz . . . . . 7.6 Bits
- Maximum Sampling Frequency . . . . . 35 MSPS
- Low Power Consumption 80mW (at 35 MSPS Typ) (Reference Current Excluded)
- Built-In Input Clamp Function (DC Restore)
- No Sample/Hold Required
- Internal Voltage Reference
- Input CMOS Compatible
- Three-State TTL Compatible Output
- Single Power Supply . . . . . +5V
- Low Input Capacitance (Typ) 8pF
- Reference Impedance (Typ) 330Ω
- Direct Replacement for Sony CXD1179

Applications

- Desktop Video
- Multimedia
- Video Digitizing
- Image Scanners
- Low Cost High Speed Data Acquisition Systems

Description

The HI1179 is an 8-bit CMOS analog-to-digital converter for video use that features a sync clamp function. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 35 MSPS, allowing up to 8x over sampling of NTSC and PAL signals.

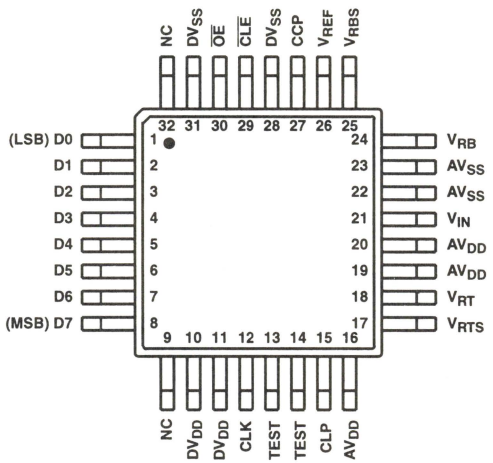
The HI1179 is available in the Industrial temperature range and is supplied in 32 lead Plastic Metric Quad Flatpack (MQFP) package. For lower sampling rates, refer to the HI1176 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1179JCQ	-40 to 85	32 Ld MQFP	Q32.7x7-S
HI1179-EV	25	Evaluation Board	

Pinout

HI1179 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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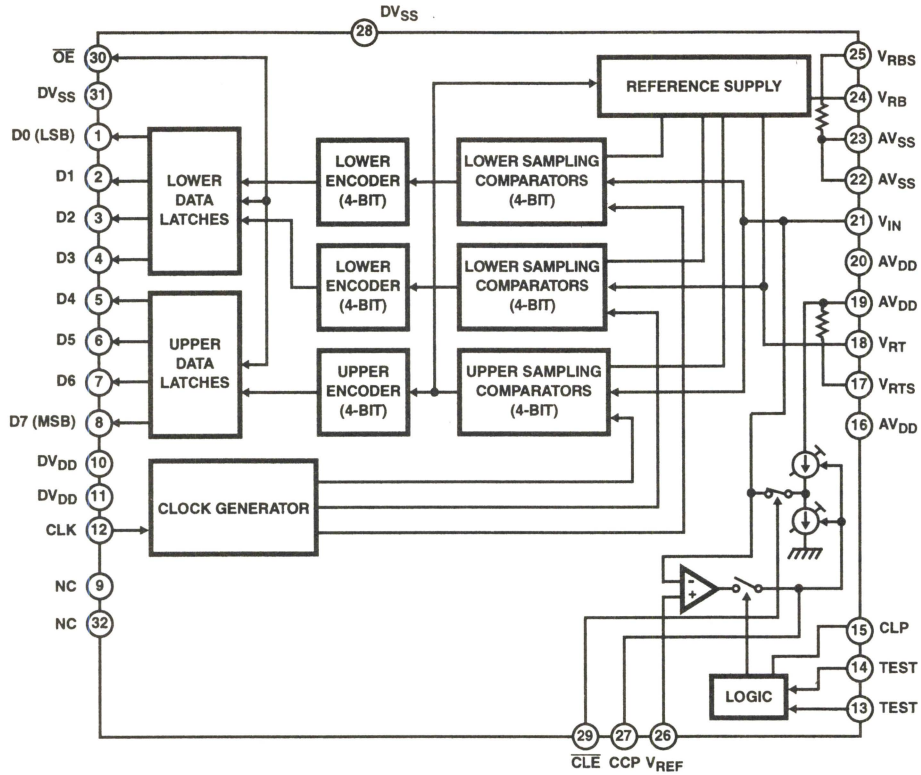
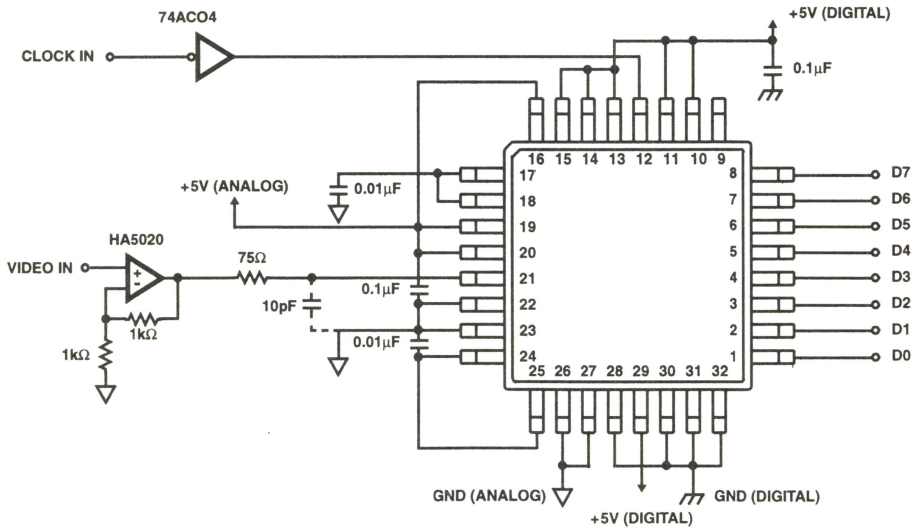
Functional Block Diagram



Typical Application Schematic



NON-CLAMP APPLICATION (INTERNAL REFERENCE USED)

Absolute Maximum Ratings

Supply Voltage, V_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} . . . . . V_{DD} to V_{SS}
Analog Input Voltage, V_{IN} . . . . . V_{DD} to V_{SS}
Digital Input Voltage . . . . . V_{DD} to V_{SS}
Digital Output Voltage, V_{OH}, V_{OL} . . . . . V_{DD} to V_{SS}

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} °C/W
MQFP Package 122
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range, T_{STG} . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(MQFP - Lead Tips Only)

Recommended Operating Conditions (Note 2)

Supply Voltage
AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS} . . . . . +4.75V to +5.25V
IDGND-AGNDI . . . . . .0mV to 100mV
Reference Input Voltage
V_{RB} . . . . . 0V and Above
V_{RT} . . . . . 2.7V and Below
Temperature Range, T_A . . . . . -40°C to 85°C

Analog Input Voltage, V_{IN} . . . . . V_{RB} to V_{RT} ($1.8V_{P-P}$ to AV_{DD})
Clock Pulse Width
t_{PW1} . . . . . .14ns (Min)
t_{PW0} . . . . . .14ns (Min)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

f_C = 35 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C (Note 2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Maximum Conversion Speed, f_C	V_{IN} = 0.5V to 2.5V, f_{IN} = 1kHz Ramp	35	40	-	MSPS
Minimum Conversion Speed, f_C	V_{IN} = 0.5V to 2.5V, f_{IN} = 1kHz Ramp	-	-	0.5	MSPS
Integral Non-Linearity, INL	f_C = 35 MSPS, V_{IN} = 0.5V to 2.5V	-1.0	±0.5	+1.3	LSB
Differential Non-Linearity, DNL	f_C = 35 MSPS, V_{IN} = 0.5V to 2.5V	-0.5	±0.3	+0.5	LSB
DYNAMIC CHARACTERISTICS					
ENOB	f_{IN} = 1MHz	-	7.6	-	Bits
	f_{IN} = 5MHz	-	7.3	-	Bits
Differential Gain Error, DG	NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Aperture Jitter, t_{AJ}		-	30	-	ps
Offset Voltage					
E_{OT}		-60	-40	-20	mV
E_{OB}		+55	+75	+95	mV
Sampling Delay, t_{SD}		-	2	-	ns
ANALOG INPUTS					
Analog Input Bandwidth, BW	-1dB	-	25	-	MHz
	-3dB	-	60	-	MHz
Analog Input Capacitance, C_{IN}	V_{IN} = 1.5V + $0.07V_{RMS}$	-	8	-	pF
REFERENCE INPUT					
Reference Pin Current, I_{REF}		4.5	6.1	8.7	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}		230	330	440	Ω

Electrical Specifications f_C = 35 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C (Note 2) **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REFERENCES						
Self Bias						
V_{RB}	Short V_{RB} to V_{RBS}, Short V_{RT} to V_{RTS}		0.52	0.56	0.60	V
V_{RT} - V_{RB}			1.96	2.10	2.24	V
V_{RT} - V_{RB}	Short V_{RT} to V_{RTS}, Short V_{RB} to AV_{SS}		2.13	2.33	2.53	V
DIGITAL INPUTS						
Digital Input Voltage						
V_{IH}			3.5	-	-	V
V_{IL}			-	-	0.5	V
Digital Input Current						
I_{IH}	V_{DD} = Max	$V_{IH} = V_{DD}$	-	-	5	µA
I_{IL}		V_{IL} = 0V	-	-	5	µA
DIGITAL OUTPUTS						
Digital Output Current						
I_{OH}	$\overline{OE} = V_{SS}$, V_{DD} = Min	$V_{OH} = V_{DD}$ -0.5V	-1.1	-2.5	-	mA
I_{OL}		V_{OL} = 0.4V	3.7	6.5	-	mA
Digital Output Leakage Current						
I_{OZH}	$\overline{OE} = V_{DD}$, V_{DD} = Max	$V_{OH} = V_{DD}$	-	-	16	µA
I_{OZL}		V_{OL} = 0V	-	-	16	µA
TIMING CHARACTERISTICS						
Output Data Delay, t_D	Load is One TTL Gate and 10pF Load		7	13	18	ns
Output Enable/Disable Delay	t_{PZH}, t_{PZL}	R_L = 1K, C_L = 15pF, $\overline{OE}$ = 5V → 0V	5	8	14	ns
	t_{PHZ}, t_{PLZ}	R_L = 1K, C_L = 15pF, $\overline{OE}$ = 0V → 5V	4	6.5	11	ns
POWER SUPPLY CHARACTERISTIC						
Supply Current, I_{DD}	f_C = 35 MSPS, NTSC Ramp Wave Input		-	16	22	mA
CLAMP CHARACTERISTICS						
Clamp Offset Voltage, E_{OC}	V_{IN} = DC, PWS = 3µs	V_{REF} = 0.5V	-20	0	+20	mV
		V_{REF} = 2.5V	-30	-10	+10	mV
Clamp Pulse Delay, t_{CPD}			-	25	-	ns

NOTE:

2. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams

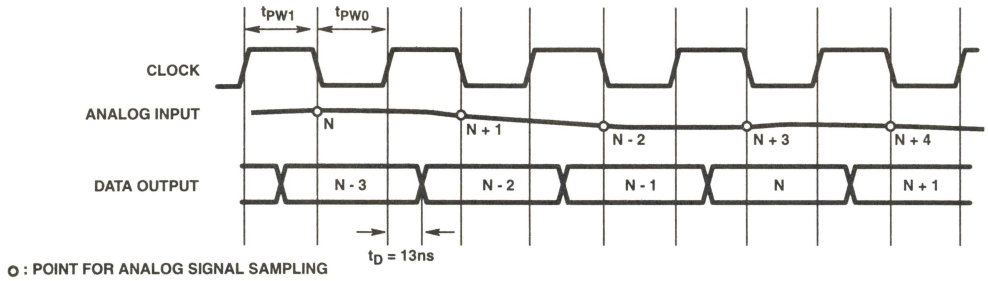


FIGURE 1.

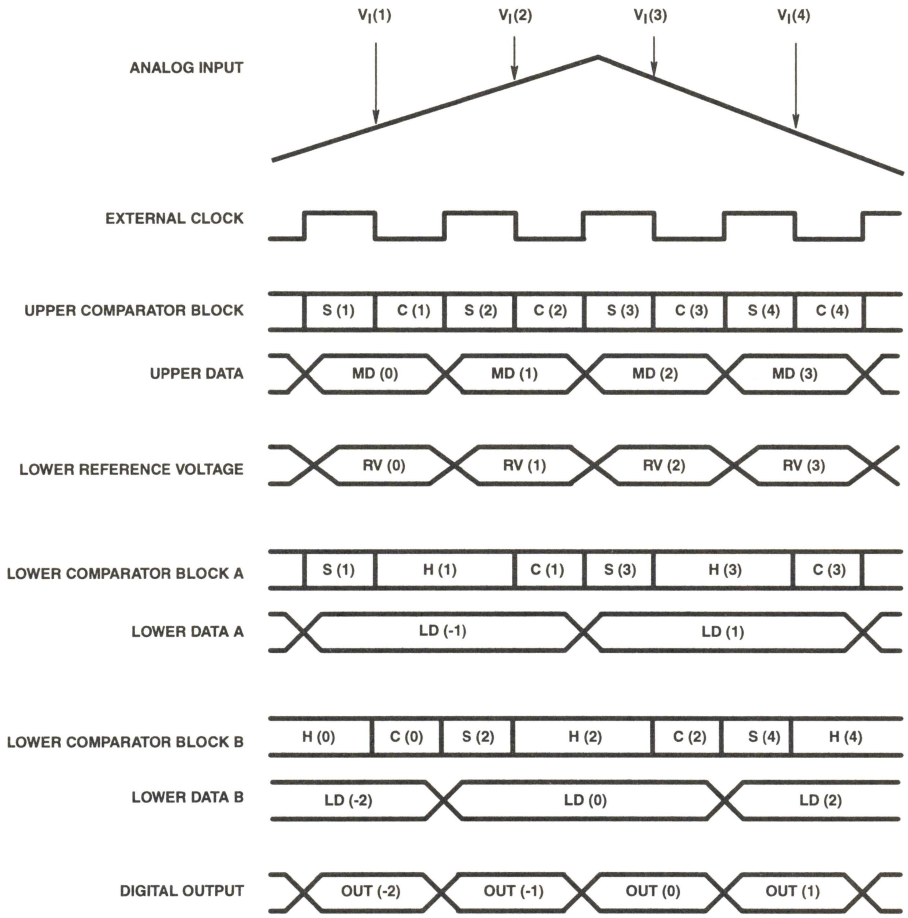


FIGURE 2.

Timing Diagrams (Continued)

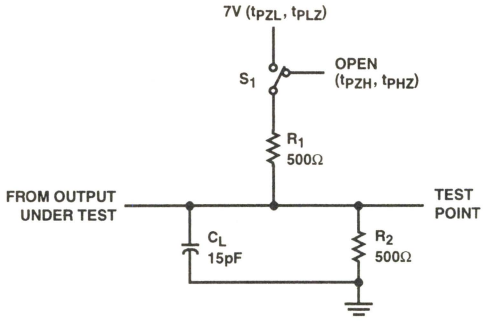


FIGURE 3A. THREE-STATE LOAD CIRCUIT

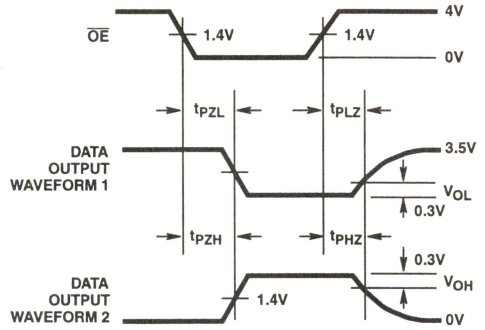


FIGURE 3B. THREE-STATE OUTPUT ENABLE/DISABLE TIMES

Typical Performance Curves f_C = 35 MSPS, T_A = 25°C, Unless Otherwise Specified

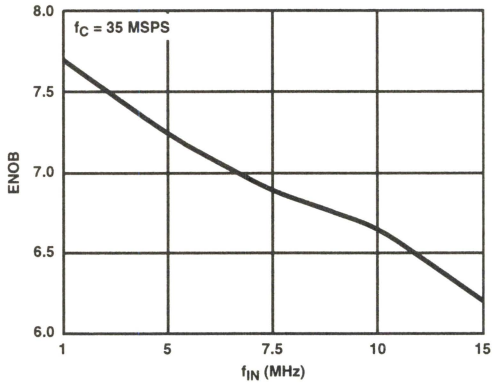


FIGURE 4. ENOB vs INPUT FREQUENCY

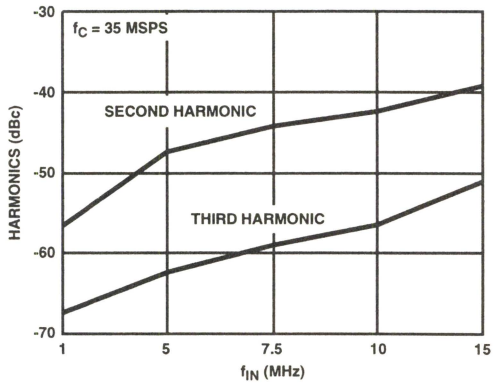


FIGURE 5. HARMONICS vs INPUT FREQUENCY

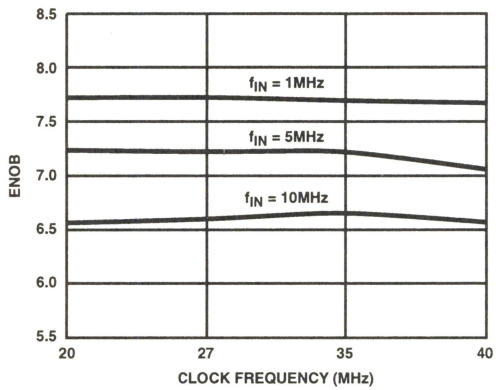


FIGURE 6. ENOB vs CLOCK FREQUENCY

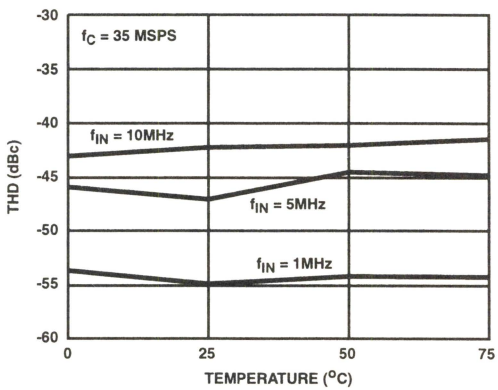


FIGURE 7. THD vs TEMPERATURE

Typical Performance Curves f_C = 35 MSPS, T_A = 25°C, Unless Otherwise Specified (Continued)

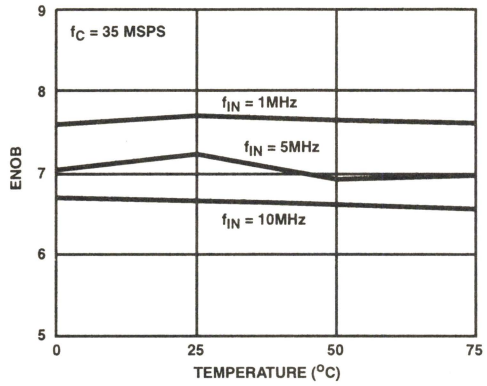


FIGURE 8. ENOB vs TEMPERATURE

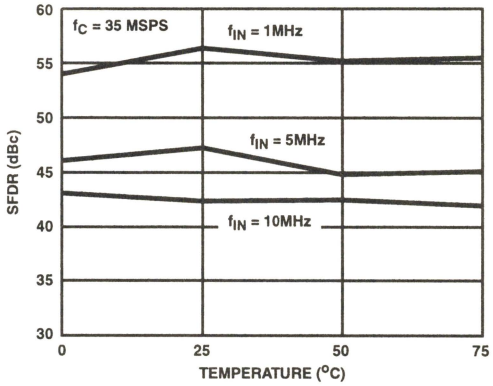


FIGURE 9. SFDR vs TEMPERATURE

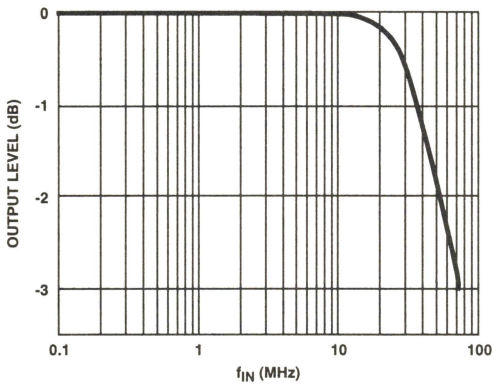


FIGURE 10. OUTPUT LEVEL vs INPUT FREQUENCY

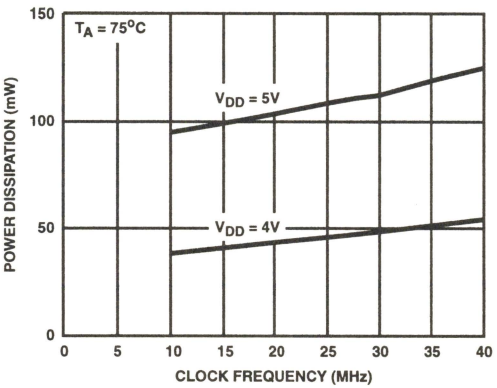
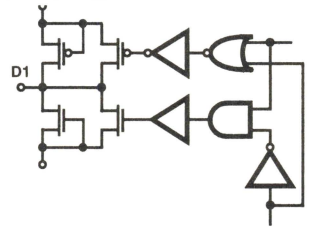
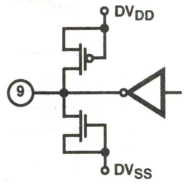
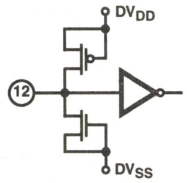
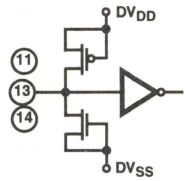
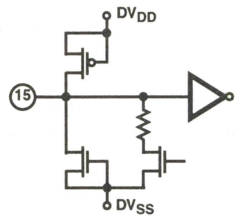
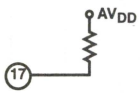
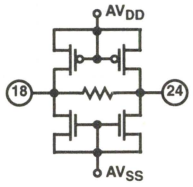


FIGURE 11. POWER DISSIPATION vs CLOCK FREQUENCY

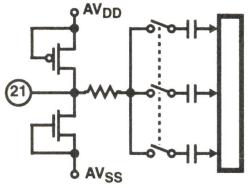
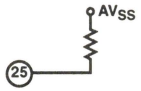
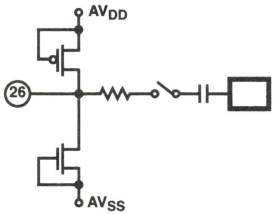
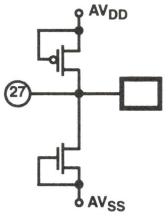
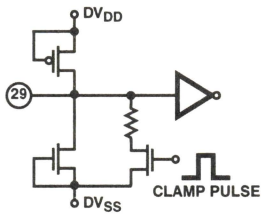
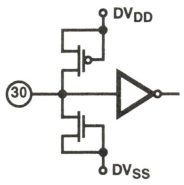
Pin Descriptions

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1-8	D0 to D7		D0 (LSB) to D7 (MSB) output.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
9	NC		This pin must be left open. Used for test purposes only.
10	DV_{DD}		Digital +5V.
12	CLK		Clock Input.
11, 13, 14	TEST		Pin 11 must be connected to DV_{DD}. Pin 13, and Pin 14 must be connected to DV_{DD} or DV_{SS}. Used for test purposes only.
15	CLP		Clamp Pulse Input. The input signal voltage is clamped to V_{REF} while the clamp pulse is low.
16, 19, 20	AV_{DD}		Analog +5V.
17	V_{RTS}		When shorted with V_{RT}, generates approximately +2.6V.
18	V_{RT}		Reference Voltage (Top).
24	V_{RB}		Reference Voltage (Bottom).

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
21	V_{IN}		Analog Input.
22, 23	AV_{SS}		Analog Ground.
25	V_{RBS}		When shorted with V_{RB}, generates approximately +0.5V.
26	V_{REF}		Clamp Reference Voltage Input.
27	CCP		Integrates the voltage for clamp control. CCP and V_{IN} voltage changes are in phase.
28, 31	DV_{SS}		Digital ground.
29	$\overline{CLE}$		When $\overline{CLE}$ is low, clamp function is activated. When $\overline{CLE}$ is high, clamp function is OFF and only the usual A/D converter function is active. By connecting $\overline{CLE}$ pin to DV_{DD} via a several hundred Ω resistance, the clamp pulse can be tested.
30	$\overline{OE}$		When $\overline{OE}$ is low, data is valid. When $\overline{OE}$ is high, D0 to D7 pins are high impedance.

A/D OUTPUT CODE TABLE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
V_{RT}	255	1	1	1	1	1	1	1	1
	•					•			
•	•					•			
•	•					•			
•									
•	128	1	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1
•									
•	•					•			
•	•					•			
	•					•			
V_{RB}	0	0	0	0	0	0	0	0	0

Detailed Description

The HI1179 is a 2-step A/D converter featuring a 4-bit upper comparator group and two lower comparator groups of 4 bits each. The reference voltage can be obtained from the onboard bias generator or be supplied externally. This IC uses an offset canceling type comparator that operates synchronously with an external clock. The operating modes of the part are input sampling/autozero (S), hold (H), and compare (C).

The operation of the part is illustrated in Figure 2. A reference voltage that is between VRT-VRB is constantly applied to the upper 4-bit comparator group. VI(1) is sampled with the falling edge of the first clock by the upper comparator block. The lower block A also samples VI(1) on the same edge. The upper comparator block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates a reference voltage RV(1) that corresponds to the upper results and applies it to the lower comparator block A. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as OUT(1) with the rising edge of the third clock. There is a 2.5 clock cycle delay from the analog input sampling point to the corresponding digital output data. Notice how the lower comparator blocks A and B alternate generating the lower data in order to increase the overall A/D sampling rate.

Power, Grounding, and Decoupling

Separate analog and digital grounds to reduce noise effects, connecting them at a single point near the HI1179. Analog and digital power should also be separated for optimum performance. If a single 5V supply is used, isolate the analog and digital power with an inductor or ferrite bead to minimize the digital noise on the analog supply.

Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1µF capacitor close to the pin.

Analog Input

The analog input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with a low impedance source with sufficient bandwidth and drive capability.

Op amps such as the HA-2544, the HA5020 and the HFA1100 family should make excellent input amplifiers depending on the applications requirements. In order to prevent parasitic oscillation, it may be necessary to insert a resistor between the output of the amplifier and the A/D input.

The input can be AC or DC coupled. If AC coupled the input will float to about $^1/_2(V_{RT} + V_{RB})$. The other option is to use the internal clamp, which will be discussed later. When DC coupling the input be sure to disable the clamp function ($\overline{CLE}$, pin 29).

Reference Input

The HI1179 has an internal reference with the option to use an external reference if more accuracy is desired.

The analog input range of the A/D is set by the voltage between V_{RT} and V_{RB}. The internal reference can be used by shorting V_{RT} to V_{RTS} and V_{RB} to V_{RBS}. The internal bias generator will set V_{RT} to about 2.6V and V_{RB} to about 0.6V. The analog input range of the A/D will now be from 0.6V to 2.6V. The internal reference may be subjected to power supply variations since the internal reference resistor ladder is connected directly to V_{DD} and V_{SS}. Any supply variations can be minimized by good decoupling of V_{RT} and V_{RB}.

An external reference can be used for increased accuracy, by connecting the reference voltage to V_{RT} and V_{RB}. If an external reference is used, V_{RT} should be keep below 2.8V and (V_{RT} - V_{RB}) should be less than 2.8V and greater than 1.8V. If a V_{RB} below +0.6V is used the linearity of the part may degrade. An ICL8069 reference and a dual op amp, with outputs connect to V_{RT} and V_{RB}, makes a good, low cost external reference.

Bypass V_{RT} and V_{RB} to analog ground with a 0.1µF capacitor when using either internal or external references.

Clamp Operation

The HI1179 provides a clamp (DC restore) option that allows the user to clamp a portion of the analog input to a voltage set by the V_{REF} pin before the signal is digitized. The clamp

function is enabled by tying $\overline{CLE}$ low. In this case a negative going pulse is sent to the CLP pin. V_{IN} will now be clamped during the low period of the clamp pulse to the voltage on the V_{REF} pin. Figure 15 shows the HI1179 configured for this mode of operation.The clamp pulse is latched by the ADC sampling clock through an external latch. This is not necessary to the operation of the clamp function but in video applications, if this is not done, then a slight beat might be generated as vertical sag according to the relation between the sampling frequency and the clamp frequency. The pulse width of the input clamp pulse will depend on the input signal. For example, a 1µs pulse width will allow the user to clamp the back porch of an NTSC input signal to the reference voltage, V_{REF}.

The clamp can be disabled by tying $\overline{CLE}$ high and then the HI1179 acts like a normal A/D converter, accepting a DC coupled input. The Typical Application Schematic illustrates the operation of HI1179 when the clamp function is not used.

Additional information on the HI1179 is available in Application Note 9407, "Using the HI1176/HI1179 Evaluation Board".

Test Circuits

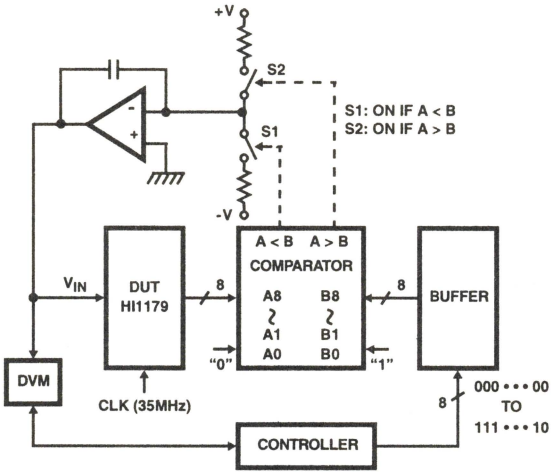


FIGURE 12. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

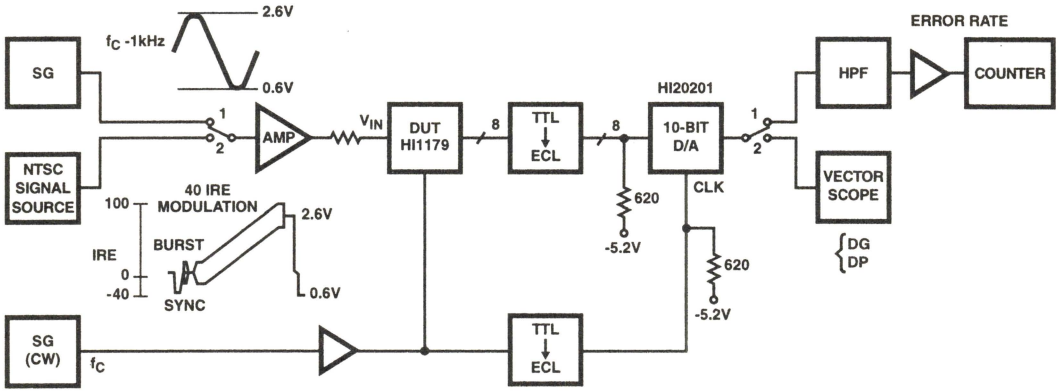


FIGURE 13. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

Test Circuits (Continued)

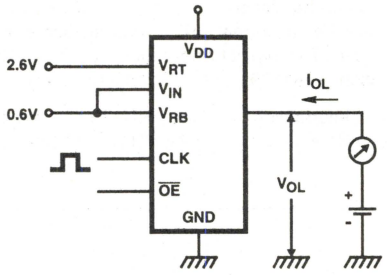


FIGURE 14A.

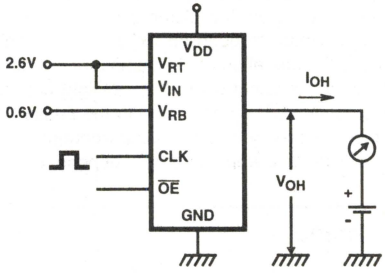


FIGURE 14B.

FIGURE 14. DIGITAL OUTPUT CURRENT TEST CIRCUIT

Typical Application Circuits

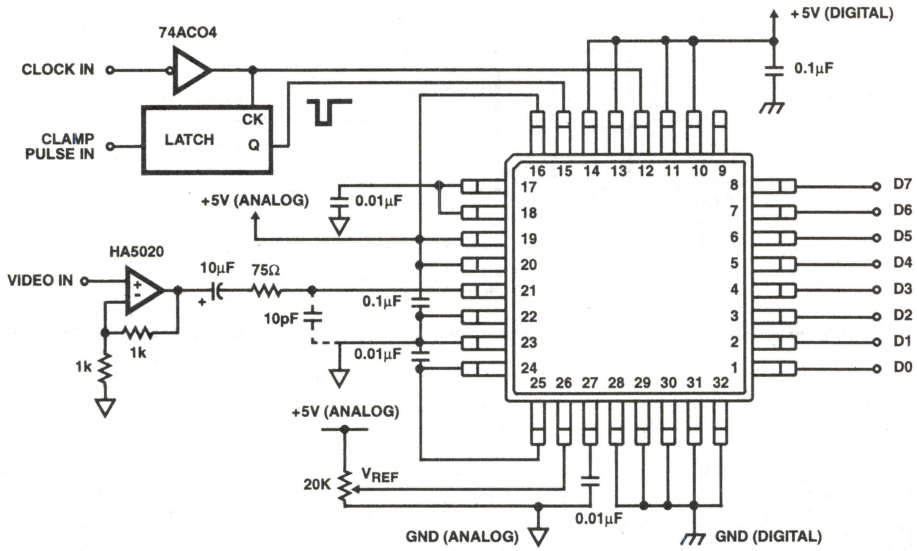
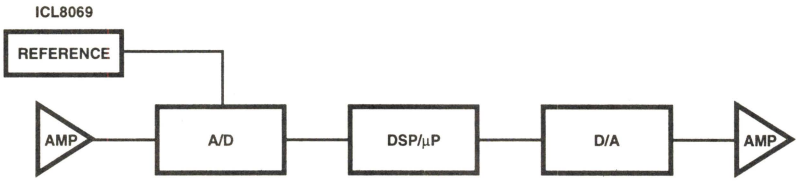


FIGURE 15. INPUT CLAMP APPLICATION (INTERNAL REFERENCE USED)

Typical Application Circuits (Continued)



HA5020 (Single)	HI1179 (8-Bit)	HSP9501	HI1171 (8-Bit)	HA5020 (Single)
HA5022 (Dual)		HSP48410	CA3338 (8-Bit)	HA2842 (Single)
HA5024 (Quad)		HSP48908		HFA1115 (Single)
HA5013 (Triple)		HSP48901		HFA1212 (Dual)
HFA1105 (Single)		HSP48212		HFA1412 (Quad)
HFA1205 (Dual)		HSP43881		
HFA1405 (Quad)		HSP43168		

HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution, 4K x 4K Frame Size
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48901: 3 x 3 Image Filter, 30MHz, 8-Bit
HSP48212: Video Mixer
HSP43881: Digital Filter, 30MHz, 1-D and 2-D FIR Filters
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz

CMOS Logic Available in HC, HCT, AC, ACT and FCT.

FIGURE 16. 8-BIT VIDEO COMPONENTS

Static Performance Definitions

Offset, full-scale, and gain all use a measured value of the internal voltage reference to determine the ideal plus and minus full-scale values. The results are all displayed in LSBs.

Offset Error (VOS)

The first code transition should occur at a level $^1/_2$ LSB above the negative full-scale. Offset is defined as the deviation of the actual code transition from this point. Note that this is adjustable to zero.

Full-Scale Error (FSE)

The last code transition should occur for a analog input that is $1^1/_2$ LSBs below positive full scale. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed to have no missing codes.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI1179. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 1024 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02,$$

where: $V_{CORR} = 0.5dB$.

Total Harmonic Distortion

This is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the 2nd and 3rd harmonic component respectively to the RMS value of the measured input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

Full Power Input Bandwidth

Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Timing Definitions

Sampling Delay (t_{SD})

Sampling delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

This is the RMS variation in the sampling delay due to variation of internal clock path delays.

Data Latency (t_{LAT})

After the analog sample is taken, the data on the bus is available after 2.5 cycles of the clock. This is due to the architecture of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 2.5 cycles.

Output Data Delay (t_D)

Output Data Delay is the delay time from when the data is valid (rising clock edge) to when it shows up at the output bus. This is due to internal delays at the digital output.

August 1997

8-Bit, 500 MSPS, Flash A/D Converter

Features

- Differential Linearity Error ..... ±0.5 LSB
- Integral Linearity Error ..... ±0.7 LSB
- Built-In Integral Linearity Compensation Circuit
- Ultra High Speed Operation with Maximum Conversion Rate (Min)..... 500 MSPS
- Low Input Capacitance (Typ) 20pF
- Wide Analog Input Bandwidth (Min for Full Scale Input)..... 300MHz
- Single Power Supply ..... -5.2V
- Low Power Consumption (Typ) 2.8W
- Low Error Rate
- Capable of Driving 50Ω Loads
- Direct Replacement for Sony CXA1276K

Applications

- Radar Systems
- Communication Systems
- Digital Oscilloscopes
- Direct RF Down-Conversion

Description

The HI1276 is an 8-bit, ultra-high-speed, flash Analog-to-Digital converter IC capable of digitizing analog signals at a maximum rate of 500 MSPS. The digital I/O levels of this A/D converter are compatible with ECL 100K/10KH/10K.

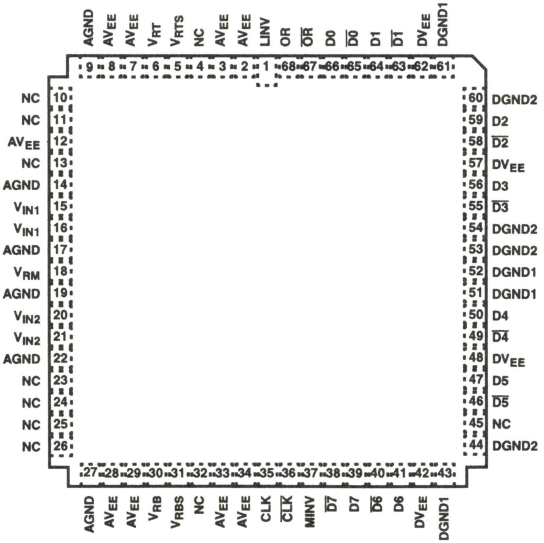
The HI1276 is available in the Industrial temperature range and is supplied in a 68 lead ceramic LCC package.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1276AIL	-20 to 100	68 Ld CLCC	J68.B
HI1276-EV	25	Evaluation Board	

Pinout

HI1276 (CLCC)
HEAT SINK UP, RECESSED CAVITY DOWN



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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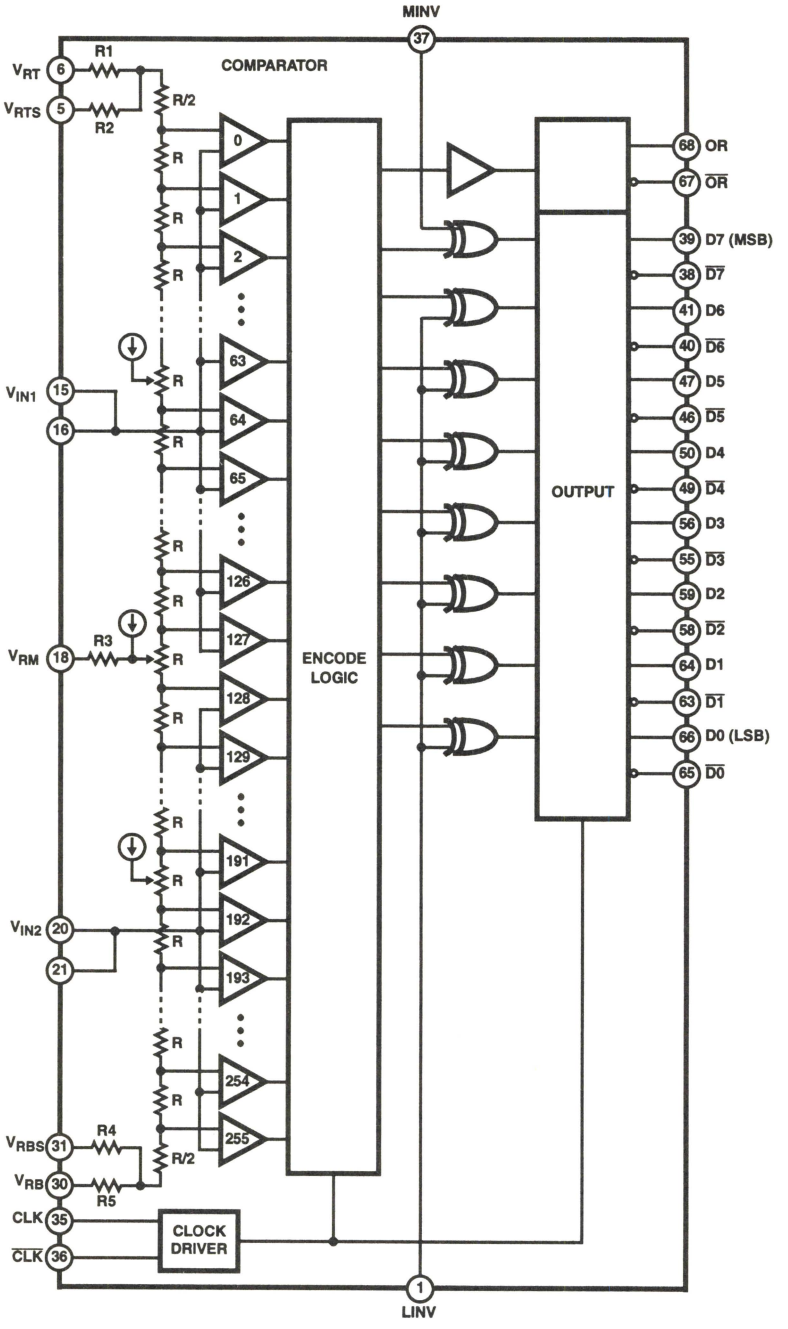
File Number 3578.4

Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{EE}, DV_{EE}) . . . . . -7V to +0.5V
Analog Input Voltage (V_{IN}) . . . . . -2.7 to +0.5V
Reference Input Voltage
V_{RT}, V_{RB}, V_{RM} . . . . . AV_{EE} to +0.5V
$|V_{RT} - V_{RB}|$ 2.5V
Digital Input Voltage
MINV, LINV . . . . . -4V to +0.5V
CLK, $\overline{CLK}$, ... DV_{EE} to +0.5V
$|CLK-\overline{CLK}|$ 2.7V
V_{RM} Pin Input Current (I_{VRM}) . . . . . -3mA to +3mA
Digital Output Current
(ID0 to ID7, IOR, $\overline{ID0}$ to $\overline{ID7}$, $\overline{IOR}$) . . . . . -30mA to 0mA

Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}{}^oC/W$	$\theta_{JC}{}^oC/W$
CLCC Package	18	4

Maximum Junction Temperature . . . . . 175^oC
Maximum Storage Temperature Range (T_{STG}) . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Operating Conditions (Note 1)

Supply Voltage	MIN	TYP	MAX
AV_{EE}, DV_{EE}	-5.5V	-5.2V	-4.95V
AV_{EE} - DV_{EE}	-0.05V	0V	0.05V
AGND - DGND	-0.05V	0V	0.05V
Temperature Range (Note 5)			
T_C	-20^oC	-	100^oC

Reference Input Voltage	MIN	TYP	MAX
V_{RT}	-0.1V	-2	0.1V
V_{RB}	-2.2V	-2	-1.8V
Analog Input Voltage, V_{IN}	V_{RB}	-	V_{RT}

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, V_{RT}, $V_{RTS} = 0V$, V_{RB}, $V_{RBS} = -2V$ (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		-	8	-	Bits
Integral Linearity Error, INL	f_C = 500 MSPS	-	±0.3	±0.7	LSB
Differential Linearity Error, DNL	f_C = 500 MSPS	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	Input = 1kHz, Full Scale, f_C = 500 MSPS	-	46	-	dB
	Input = 100MHz, Full Scale, f_C = 500 MSPS	-	37	-	dB
Error Rate	Input = 100MHz, Full Scale, Error > 16 LSB, f_C = 400 MSPS	-	10^{-11}	10^{-9}	TPS (Note 3)
	Input = 125MHz, Full Scale, Error > 16 LSB, f_C = 500 MSPS	-	10^{-8}	10^{-6}	TPS (Note 3)
Differential Gain Error, DG	NTSC 40 IRE Mod. Ramp, f_C = 500 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Overrange Recovery Time		-	1.0	-	ns
Maximum Conversion Rate, f_C		500	-	-	MSPS
Aperture Jitter, t_{AJ}	Input = 150MHz	-	11	-	ps
Sampling Delay, t_{DS}	Input = 150MHz	0.2	0.8	1.5	ns
ANALOG INPUT					
Analog Input Capacitance, C_{IN}	$V_{IN} = 1V + 0.07V_{RMS}$	-	20	-	pF
Analog Input Resistance, R_{IN}		30	70	-	kΩ
Input Bias Current, I_{IN}	V_{IN} = -1V	-	-	850	µA
Full Scale Input Bandwidth	$V_{IN} = 2V_{P-P}$	300	-	-	MSPS
REFERENCE INPUTS					
Reference Resistance, R_{REF}		70	110	160	Ω

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, V_{RT}, $V_{RTS} = 0V$, V_{RB}, $V_{RBS} = -2V$ (Note 1) **(Continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Residual Resistance	R1	Note 2	0.1	0.5	2.0	Ω
	R2		0.5	5.2	10	Ω
	R3		0.5	1.6	5.0	Ω
	R4		0.5	8.7	20	Ω
	R5		0.1	0.5	2.0	Ω
DIGITAL INPUTS						
Logic H Level, V_{IH}			-1.10	-	-	V
Logic L Level, V_{IL}			-	-	-1.55	V
Logic H Current, I_{IH}		Input Connected to -0.8V	0	-	70	µA
Logic L Current, I_{IL}		Input Connected to -1.6V	-50	-	60	µA
Input Capacitance			-	6	-	pF
DIGITAL OUTPUTS						
Logic H Level, V_{OH}		$R_L = 50Ω$	-1.03	-	-	V
Logic L Level, V_{OL}		$R_L = 50Ω$	-	-	-1.58	V
TIMING CHARACTERISTICS						
Clock Duty Cycle			45	50	55	%
Output Rise Time, t_r		$R_L = 50Ω$, 20% to 80%	0.5	0.7	1.0	ns
Output Fall Time, t_f		$R_L = 50Ω$, 80% to 20%	0.5	0.7	1.0	ns
Output Delay, t_{OD}			1.5	1.9	2.3	ns
POWER SUPPLY CHARACTERISTICS						
Supply Current, I_{EE}			-680	-520	-	mA
Power Consumption, P_D		Note 4	-	2.8	3.6	W

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. See Functional Block Diagram.
3. TPS: Times Per Sample.
4. $P_D = I_{EEA} \bullet AV_{EE} + I_{EED} \bullet DV_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$.
5. T_A is specified in still air and without heatsink. To extend temperature range, appropriate heat management techniques must be employed (See Figure 2).

Timing Diagram

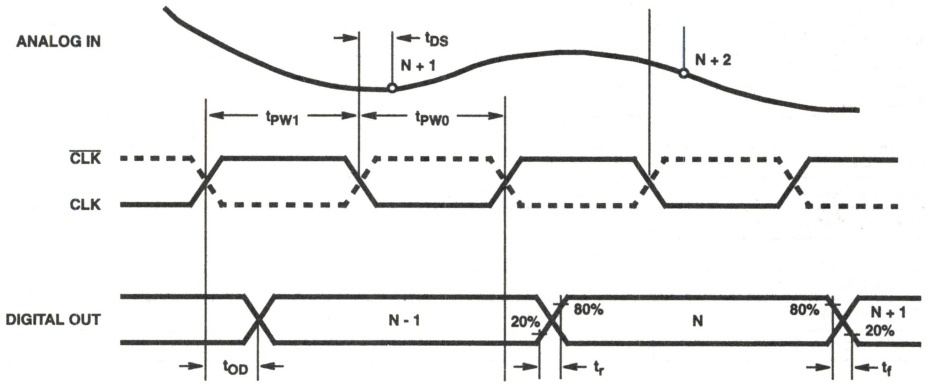


FIGURE 1.

Typical Performance Curves

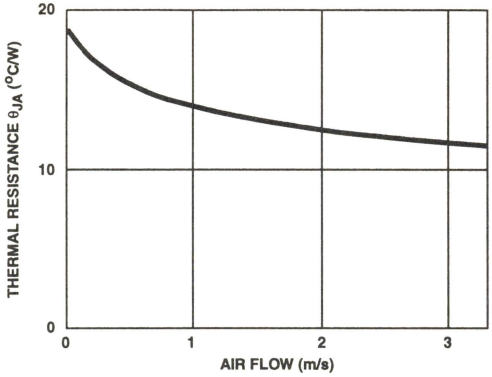


FIGURE 2. THERMAL RESISTANCE MOUNTED ON-BOARD

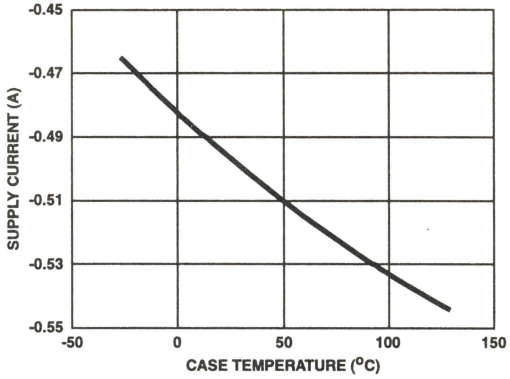


FIGURE 3. SUPPLY CURRENT vs TEMPERATURE CHARACTERISTICS

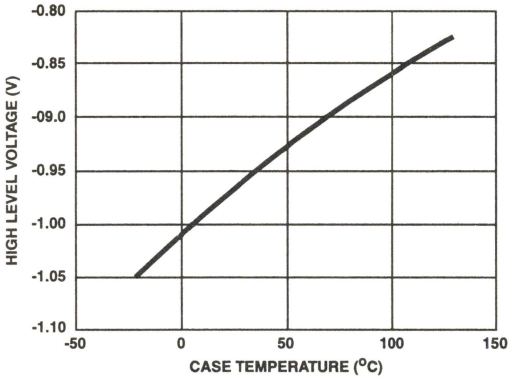


FIGURE 4. DO PIN HIGH LEVEL VOLTAGE vs TEMPERATURE CHARACTERISTICS

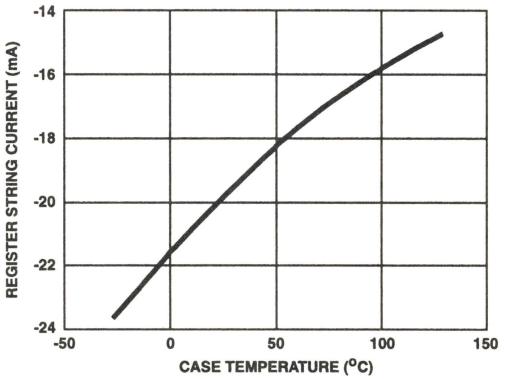


FIGURE 5. REGISTER STRING CURRENT vs TEMPERATURE CHARACTERISTICS

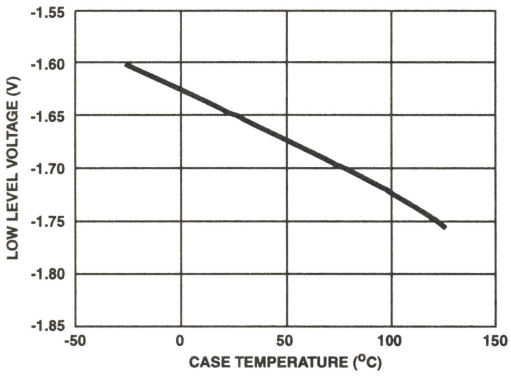


FIGURE 6. D0 PIN LEVEL VOLTAGE vs TEMPERATURE CHARACTERISTICS

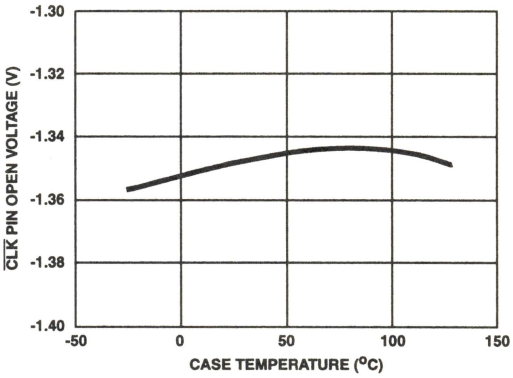


FIGURE 7. $\overline{CLK}$ PIN OPEN VOLTAGE vs TEMPERATURE CHARACTERISTICS

Typical Performance Curves (Continued)

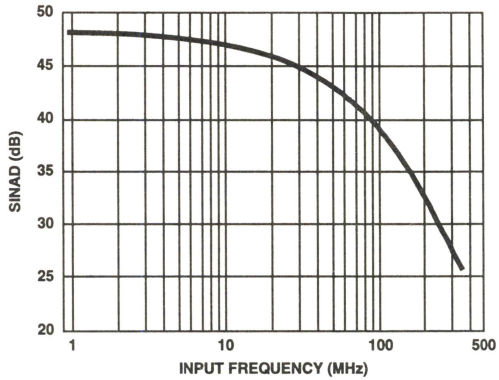


FIGURE 8. SINAD vs INPUT FREQUENCY CHARACTERISTICS

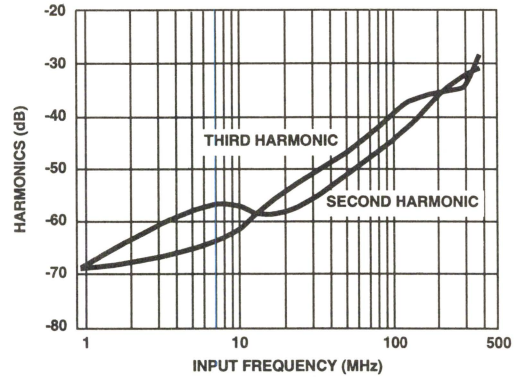


FIGURE 9. HARMONIC DISTORTION vs INPUT FREQUENCY CHARACTERISTICS

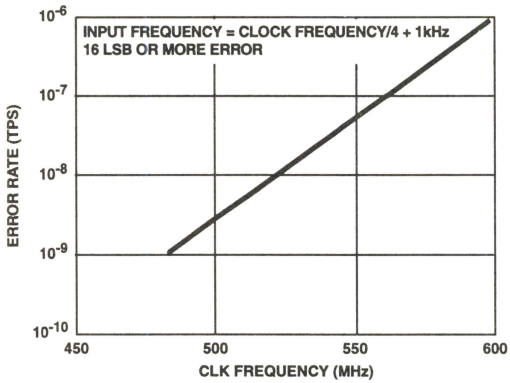


FIGURE 10. ERROR RATE vs CONVERSION FREQUENCY CHARACTERISTICS

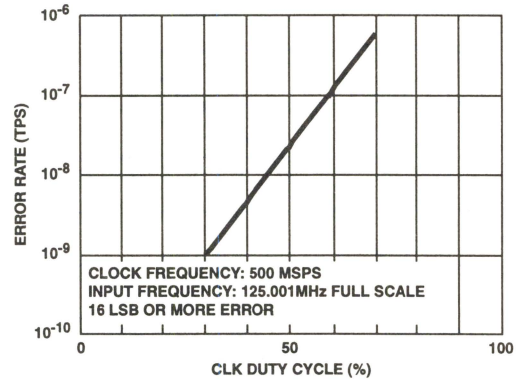


FIGURE 11. ERROR RATE vs CLOCK DUTY CYCLE CHARACTERISTICS

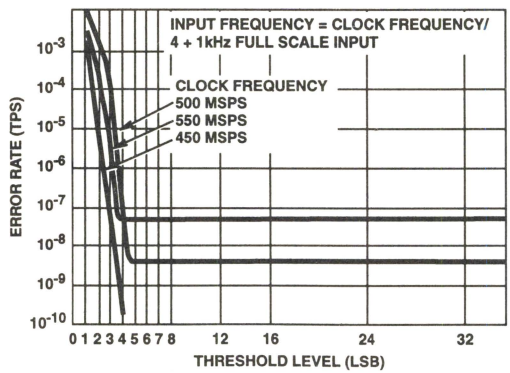
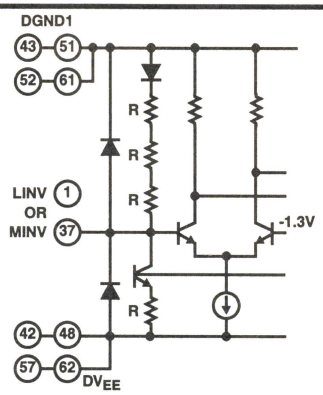
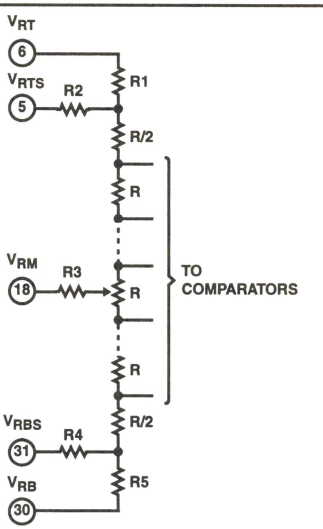
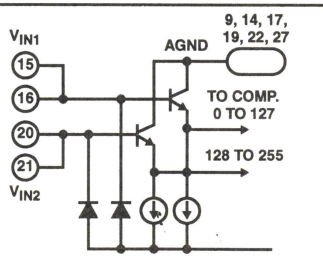
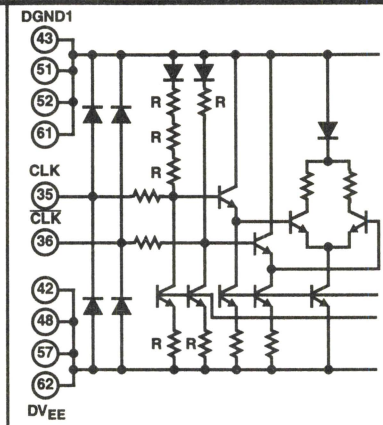
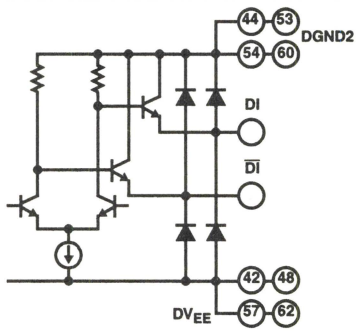
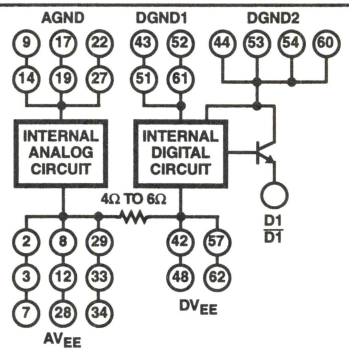


FIGURE 12. ERROR RATE vs THRESHOLD LEVEL CHARACTERISTICS

Pin Descriptions

PIN NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
1	LINV	I	ECL		Polarity Selection for LSBs (refer to the A/D Output Code Table.) Pulled low when left open.
37	MINV				Polarity Selection for MSB (refer to the A/D Output Code Table). Pulled low when left open.
6	V_{RT}	I	0V		Analog Reference Voltage (Top) (0V Typ).
5	V_{RTS}	O	0V		Reference Voltage Sense (Top).
18	V_{RM}	I	$V_{RB/2}$		Reference Voltage Mid Point. Can be used for linearity compensation.
31	V_{RBS}	O	-2V		Reference Voltage Sense (Bottom).
30	V_{RB}	I	-2V		Analog Reference Voltage (Bottom).
15, 16	V_{IN1}	I	V_{RTS} to V_{RBS}		Analog Input. All of the pins must be wired externally.
20, 21	V_{IN2}				

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
35	CLK	I	ECL		CLK Input.
36	$\overline{CLK}$				Complementary CLK Input. Pulled down to -1.3V when left open.
38, 39	$\overline{D7}$, D7	O	ECL		MSB and Complementary Msb Data Output.
40, 41	$\overline{D6}$, D6				D1 to D6: Data output D1 to D6: Complementary data output
46, 47	$\overline{D5}$, D5				
49, 50	$\overline{D4}$, D4				
55, 56	$\overline{D3}$, D3				
58, 59	$\overline{D2}$, D2				
63, 64	$\overline{D1}$, D1				
65, 66	$\overline{D0}$, D0				LSB Data Complementary Output LSB Data Output.
67, 68	$\overline{OR}$, OR				Overrange and Complementary Overrange Output.
2, 3, 7, 8, 12, 28, 29, 33, 34	AV_{EE}	-	-5.2V		Analog Supply. Internally connected to DV_{EE} (resistance: 4Ω to 6Ω).
9, 14, 17, 19, 22, 27	AGND		0V		Analog Ground.
42, 48, 57, 62	DV_{EE}		-5.2V		Digital Supply. Internally connected to AV_{EE} (resistance: 4Ω to 6Ω).
43, 51, 52, 61	DGND1		0V		Digital Ground.
44, 53, 54, 60	DGND2 (Note 6)		0V		Digital Ground for Output Drive.
4, 10, 11, 13, 23, 24, 25, 26, 32	NC				No-Connect pins. It is recommended to wire these pins to AGND.
45	NC				No-Connect pin. It is recommended to wire these pins to DGND.

NOTE:

6. $V_{RT} = V_{RTS} = 0V$, $V_{RM} = -1V$ or open, $V_{RB} = V_{RBS} = -2V$

A/D OUTPUT CODE TABLE

(NOTE 1) V_{IN}	STEP	MINV 1, LINV 1			0, 1			1, 0			0, 0		
		OR	D7	D0	OR	D7	D0	OR	D7	D0	OR	D0	D7
0V		1	000•••••00		1	100•••••00		1	011•••••11		1	111•••••11	
	0	0	000•••••00		0	100•••••00		0	011•••••11		0	111•••••11	
	1	0	000•••••01		0	100•••••01		0	011•••••10		0	111•••••10	
			•			•			•			•	
			•			•			•			•	
			•			•			•			•	
-1V	127	0	011•••••11		0	111•••••11		0	000•••••00		0	100•••••00	
	128	0	100•••••00		0	000•••••00		0	111•••••11		0	011•••••11	
			•			•			•			•	
			•			•			•			•	
			•			•			•			•	
	254	0	111•••••10		0	011•••••10		0	100•••••01		0	000•••••01	
	255	0	111•••••11		0	011•••••11		0	100•••••00		0	000•••••00	
-2V		0	111•••••11		0	011•••••11		0	100•••••00		0	000•••••00	

Test Circuits

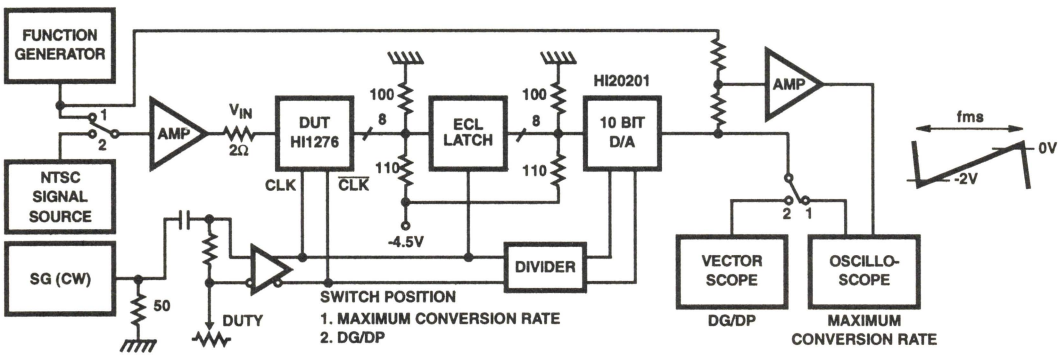


FIGURE 13. MAXIMUM CONVERSION RATE AND DIFFERENTIAL GAIN/PHASE ERROR TEST CIRCUIT

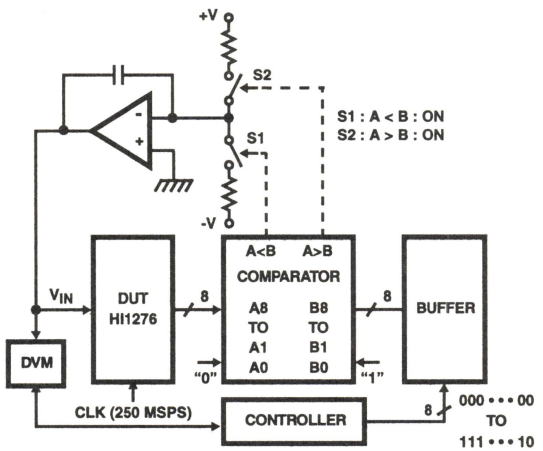


FIGURE 14. INTEGRAL AND DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits (Continued)

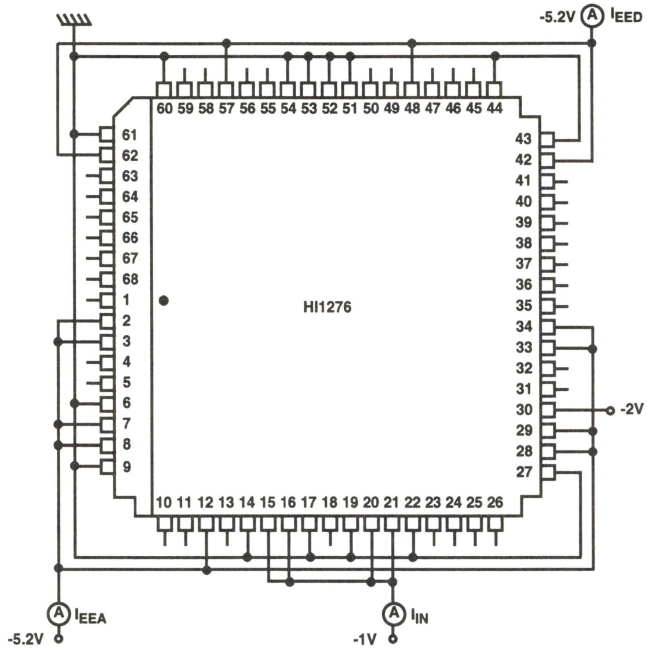


FIGURE 15. POWER SUPPLY AND ANALOG INPUT BIAS CURRENT TEST CIRCUIT

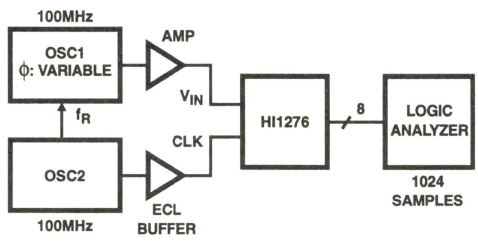
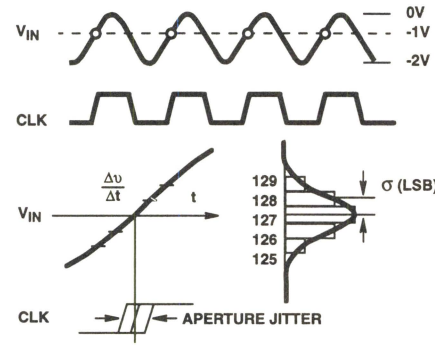


FIGURE 16A.



Aperture jitter is defined as follows:

$$t_{AJ} = \sigma / \frac{\Delta \upsilon}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f \right),$$

Where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

FIGURE 16B. APERTURE JITTER TEST METHOD

FIGURE 16. SAMPLING DELAY AND APERTURE JITTER TEST CIRCUIT

HARRIS SEMICONDUCTOR

HI1386

August 1997

8-Bit, 75 MSPS, Flash A/D Converter

Features

- Differential Linearity Error ±0.5 LSB or Less
- Integral Linearity Error ±0.5 LSB or Less
- Built-In Integral Linearity Compensation Circuit
- High-Speed Operation with Maximum Conversion Rate (Min) . . . . . 75 MSPS
- Low Input Capacitance (Typ) 17pF
- Wide Analog Input Bandwidth (Min for Full Scale Input) 150MHz
- Single Power Supply . . . . . -5.2V
- Low Power Consumption (Typ) 580mW
- Low Error Rate
- Operable at 50% Clock Duty Cycle
- Capable of Driving 50Ω Loads
- Direct Replacement for CXA1386

Applications

- Video Digitizing
- RGB Graphics Processing
- HDTV (High Definition TV)
- Radar Systems
- Communication Systems
- Direct RF Down-Conversion
- Digital Oscilloscopes

Description

The HI1386 is an 8-bit, high-speed flash analog-to-digital converter IC capable of digitizing analog signals at a maximum rate of 75 MSPS. The digital I/O levels of this A/D converter are compatible with ECL 100K/10KH/10K.

The HI1386 is available in the commercial and industrial temperature range and is supplied in 28 lead plastic DIP and 44 lead ceramic LCC packages.

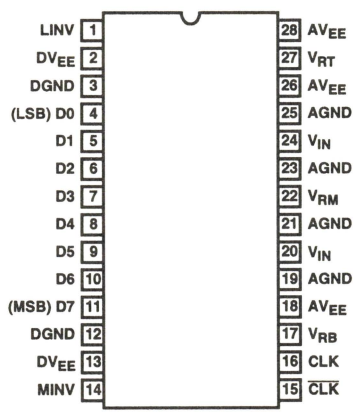
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1386JCP	-20 to 75	28 Ld PDIP	E28.6A-S
HI1386AIL	-20 to 100	44 Ld CLCC	J44.B

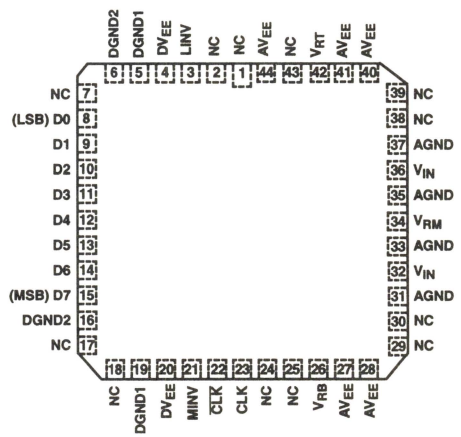
4 A/D CONVERTERS HIGH SPEED

Pinouts

HI1386 (PDIP)
TOP VIEW



HI1386 (CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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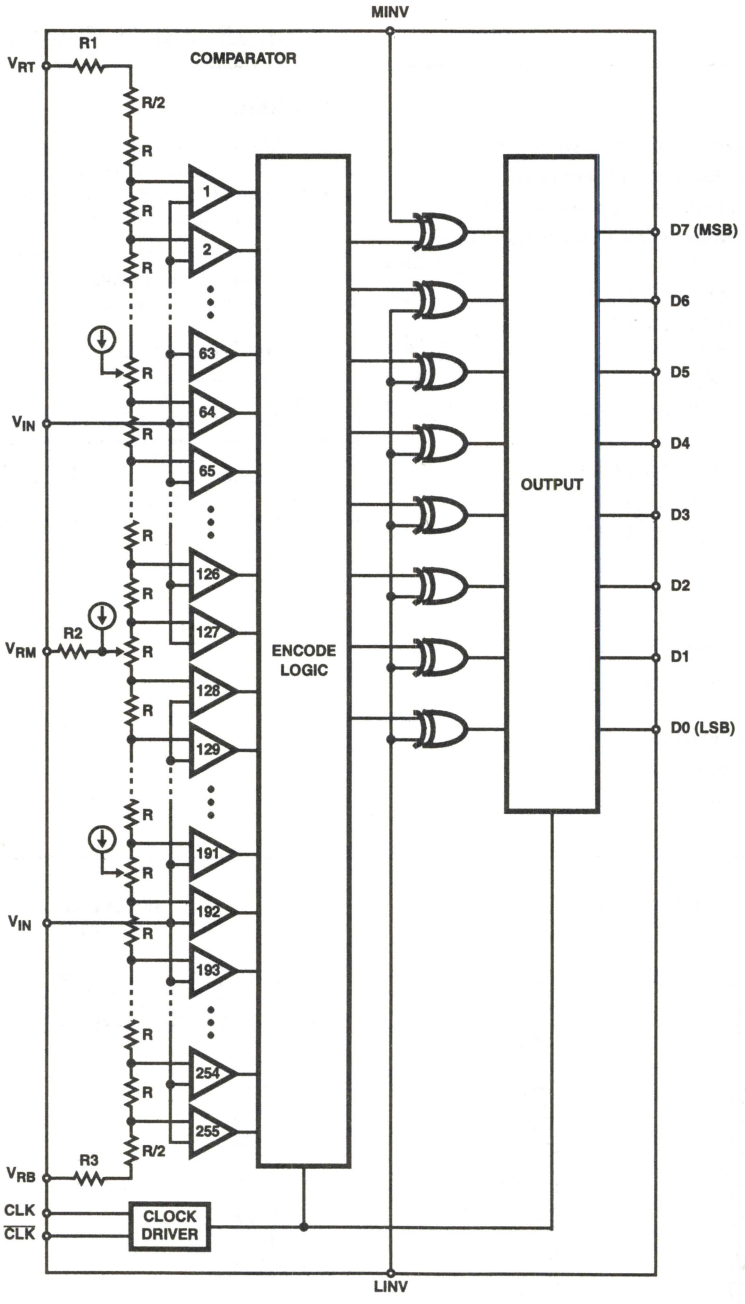
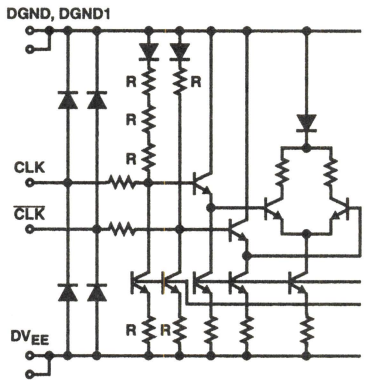
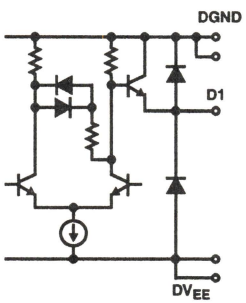
File Number 3583.4

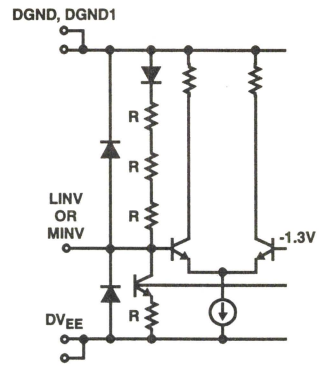
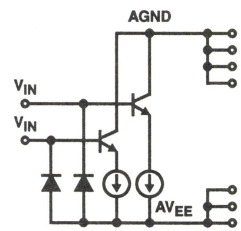
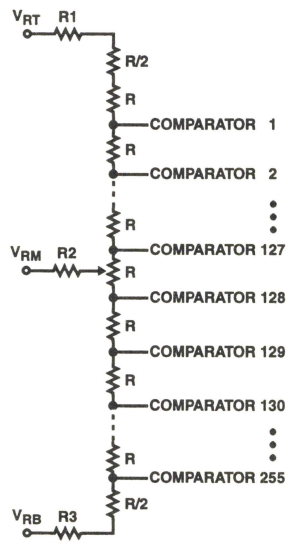
Functional Block Diagram



Pin Descriptions

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
19, 21, 23, 25	31, 33, 35, 37	AGND	-	0V		Analog GND. Used as GND for input buffers and latches of comparators. Isolated from DGND, DGND1, and DGND2.
18, 26, 28	27, 28, 40, 41, 44	AV_{EE}	-	-5.2V		Analog V_{EE} -5.2V (Typ). Internally connected to DV_{EE} (Resistance: 4Ω to 6Ω). Bypass with 0.1µF to AGND.
16	23	CLK	I	ECL		CLK Input.
15	22	$\overline{CLK}$				Input Complementary to CLK. When open pulled down to -1.3V. Device is operable without $\overline{CLK}$ input, but use of complementary inputs of CLK and $\overline{CLK}$ is recommended to obtain stable high speed operation.
3, 12	-	DGND	-	0V		Digital GND (used for internal circuits and output transistors).
-	5, 19	DGND1	-	0V		Digital GND (used for internal circuits and output transistors).
-	6, 16	DGND2	-	0V		Digital GND (used for output buffers).
2, 13	4, 20	DV_{EE}	-	-5.2V		Digital V_{EE}. Internally connected to AV_{EE} (resistance: 4Ω to 6Ω). Bypass with 0.1µF to DGND
4	8	D0	O	ECL		LSB of Data Outputs. External pull-down resistor is required.
5	9	D1				Data Outputs. External pull-down resistors are required.
6	10	D2				
7	11	D3				
8	12	D4				
9	13	D5				
10	14	D6				
11	15	D7				MSB of Data Outputs. External pull-down resistor is required.

Pin Descriptions (Continued)

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
1	3	LINV	I	ECL		Input Pin for D0 (LSB) to D6 Output Polarity Inversion (see A/D Output Code Table). Pulled low when left open.
14	21	MINV	I	ECL		Input Pin for D7 (MSB) Output Polarity Inversion (see A/D Output Code Table). Pulled low when left open.
20, 24	32, 36	V_{IN}	I	V_{RT} to V_{RB}		Analog Input Pins. These two pins must be connected externally, since they are not internally connected. See Application Note for precautions.
17	26	V_{RB}	I	-2V		Reference Voltage (Bottom). Typically -2V. Bypass with a 0.1µF and 10µF to AGND.
22	34	V_{RM}	I	$V_{RB}/2$		Reference Voltage Mid Point. Can be used as a pin for integral linearity compensation.
27	42	V_{RT}	I	0V		Reference Voltage (Top) Typically 0V.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{EE}, DV_{EE}) . . . . . -7V to +0.5V
Analog Input Voltage (V_{IN}) . . . . . -2.7V to +0.5V
Reference Input Voltage
V_{RT}, V_{RB}, V_{RM} . . . . . -2.7V to +0.5V
$|V_{RT} - V_{RB}|$ 2.5V
Digital Input Voltage
CLK, $\overline{CLK}$, MINV, LINV . . . . . -4V to +0.5V
$|CLK-\overline{CLK}|$ 2.7V
V_{RM} Pin Input Current (I_{VRM}) . . . . . -3mA to +3mA
Digital Output Current (ID0 to ID7) . . . . . -30mA to 0mA

Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}{}^oC/W$	$\theta_{JC}{}^oC/W$
PDIP Package	58	N/A
CLCC Package	45	11

Maximum Junction Temperature
CLCC Package . . . . . 175^oC
PDIP Package . . . . . 150^oC
Maximum Storage Temperature Range (T_{STG}) . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Operating Conditions

Temperature Ranges (Note 4)
PDIP Package (T_A) . . . . . -20^oC to 75^oC
CLCC Package (T_C) . . . . . -20^oC to 100^oC
Supply Voltage
AV_{EE}, DV_{EE} . . . . . -5.5V to -4.95V
AV_{EE} - DV_{EE} . . . . . -0.05V to 0.05V
AGND - DGND . . . . . -0.05V to 0.05V
Reference Input Voltage
V_{RT} . . . . . -0.1V to 0.1V
V_{RB} . . . . . -2.2V to -1.8V

Analog Input Voltage, V_{IN} . . . . . V_{RB} to V_{RT}
Pulse Width of Clock
t_{PW1} . . . . . 6.6ns (Min)
t_{PW0} . . . . . 6.6ns (Min)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, $V_{RT} = 0V$, $V_{RB} = -2V$ (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Resolution		-	8	-	Bits
Integral Linearity Error, INL	f_C = 75MHz	-	±0.3	±0.5	LSB
Differential Linearity Error, DNL	f_C = 75MHz	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Signal to Noise and Distortion Ratio, SINAD = $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	Input = 1MHz, Full Scale, f_C = 75MHz	-	46	-	dB
	Input = 18.75MHz, Full Scale, f_C = 75MHz	-	40	-	dB
Error Rate	Input = 18.749MHz, Full Scale, Error > 16 LSB, f_C = 75MHz	-	-	10^{-9}	TPS (Note 2)
Differential Gain Error, DG	NTSC 40 IRE Mod. Ramp, f_C = 75 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Maximum Conversion Rate, f_C	Error Rate of 10^{-9} TPS (Note 2)	75	-	-	MSPS
Aperture Jitter, t_{AJ}		-	10	-	ps
Sampling Delay, t_{DS}		-	3.0	-	ns
ANALOG INPUT					
Input Bandwidth	$V_{IN} = 2V_{P-P}$ (-3dB)	150	-	-	MHz
Analog Input Capacitance, C_{IN}	$V_{IN} = 1V + 0.07V_{RMS}$	-	17	-	pF
Analog Input Resistance, R_{IN}		-	390	-	kΩ
Input Bias Current, I_{IN}	V_{IN} = -1V	-	-	200	µA
REFERENCE INPUTS					
Reference Resistance, R_{REF}		75	110	155	Ω

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, $V_{RT} = 0V$, $V_{RB} = -2V$ (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset Voltage					
E_{OT} V_{RT}		8	18	32	mV
E_{OB} V_{RB}		0	10	24	mV
DIGITAL INPUTS					
Logic H Level, V_{IH}		-1.13	-	-	V
Logic L Level, V_{IL}		-	-	-1.50	V
Logic H Current, I_{IH}	-0.8V is Applied to Input	0	-	50	µA
Logic L Current, I_{IL}	-1.6V is Applied to Input	-50	-	50	µA
Input Capacitance		-	7	-	pF
DIGITAL OUTPUTS					
Logic H Level, V_{OH}	$R_L = 620\Omega$ to DV_{EE}	-1.03	-	-	V
Logic L Level, V_{OL}	$R_L = 620\Omega$ to DV_{EE}	-	-	-1.62	V
TIMING CHARACTERISTICS					
H Pulse Width of Clock, t_{PW1}		6.6	-	-	ns
L Pulse Width of Clock, t_{PW0}		6.6	-	-	ns
Output Rise Time, t_r	$R_L = 620\Omega$ to DV_{EE}, 20% to 80%	-	0.9	-	ns
Output Fall Time, t_f	$R_L = 620\Omega$ to DV_{EE}, 20% to 80%	-	2.1	-	ns
Output Delay, t_{OD}		4.0	6.5	9.0	ns
POWER SUPPLY CHARACTERISTICS					
Supply Current, I_{EE}		-150	-104	-	mA
Power Consumption, P_D	Note 3	-	580	-	mW

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. TPS: Times Per Sample.
3. $P_D = I_{EE} \bullet V_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$
4. T_A specified in still air and without heat sink. To extend temperature range, appropriate heat management techniques must be employed.

Timing Diagram

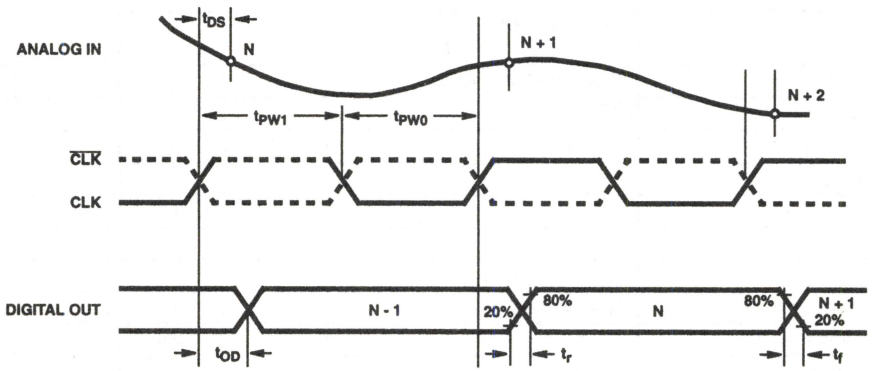


FIGURE 1.

A/D OUTPUT CODE TABLE

V_{IN} (NOTE 1)	STEP	MINV 1 LINV 1		0 1		1 0		0 0	
		D7	D0	D7	D0	D7	D0	D7	D0
0V		000 • • • • • 00		100 • • • • • 00		011 • • • • • 11		111 • • • • • 11	
	0	000 • • • • • 00		100 • • • • • 00		011 • • • • • 11		111 • • • • • 11	
	1	000 • • • • • 01		100 • • • • • 01		011 • • • • • 10		111 • • • • • 10	
		•		•		•		•	
		•		•		•		•	
		•		•		•		•	
-1V	127	011 • • • • • 11		111 • • • • • 11		000 • • • • • 00		100 • • • • • 00	
	128	100 • • • • • 00		000 • • • • • 00		111 • • • • • 11		011 • • • • • 11	
		•		•		•		•	
		•		•		•		•	
		•		•		•		•	
	254	111 • • • • • 10		011 • • • • • 10		100 • • • • • 01		000 • • • • • 01	
	255	111 • • • • • 11		011 • • • • • 11		100 • • • • • 00		000 • • • • • 00	
-2V		111 • • • • • 11		011 • • • • • 11		100 • • • • • 00		000 • • • • • 00	

NOTE:

5. V_{RT} = 0V, V_{RB} = -2V.

Test Circuits

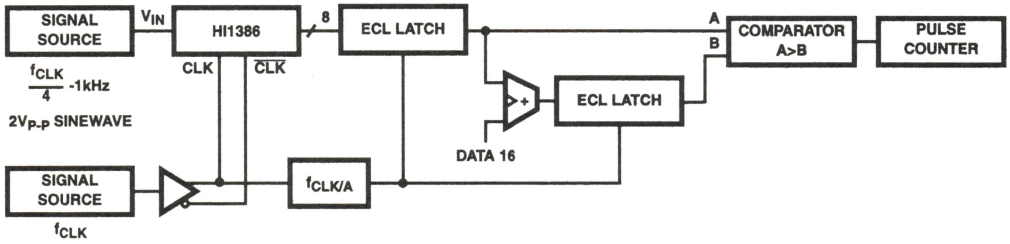


FIGURE 2. MAXIMUM CONVERSION RATE TEST CIRCUIT

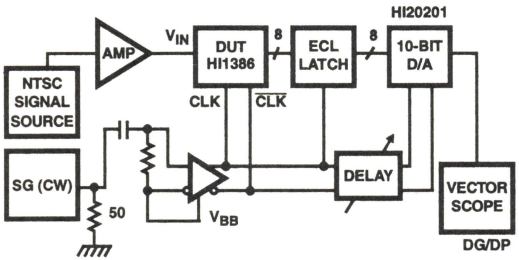


FIGURE 3. DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

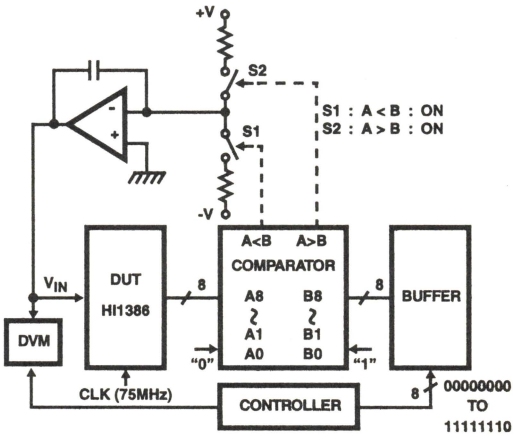


FIGURE 4. INTEGRAL AND DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits (Continued)

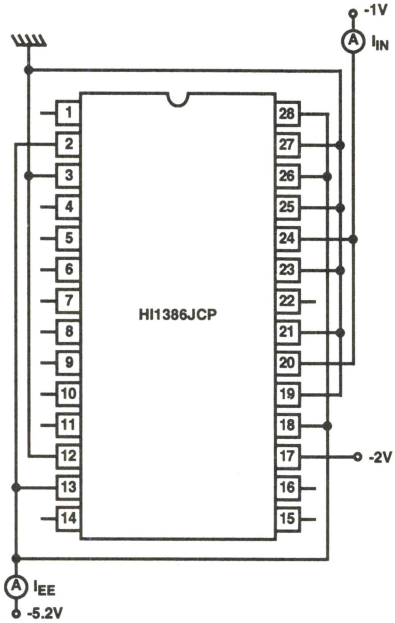


FIGURE 5A.

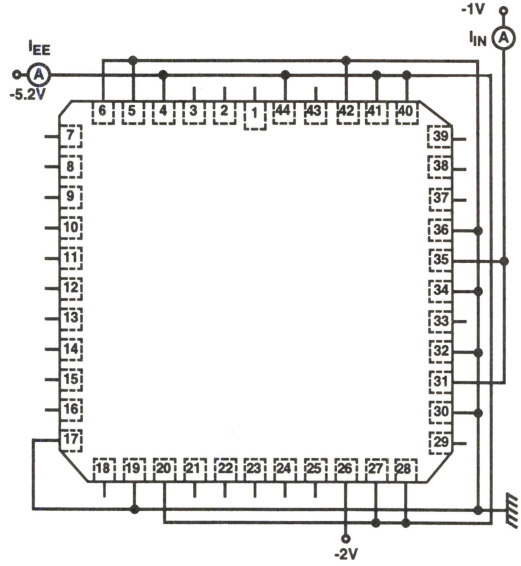


FIGURE 5B.

FIGURE 5. ANALOG INPUT BIAS AND POWER SUPPLY CURRENT TEST CIRCUITS

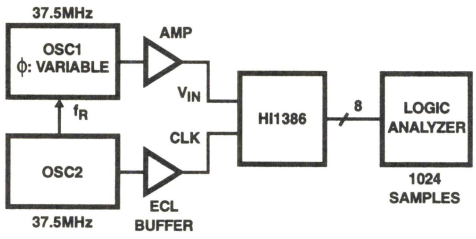
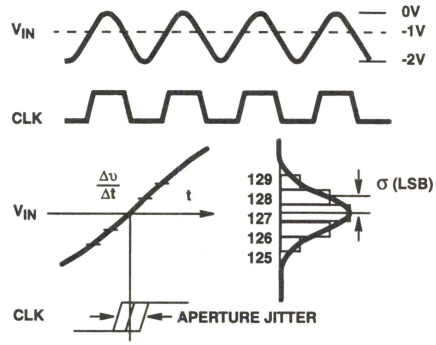


FIGURE 6A.



Aperture jitter is defined as follows:

$$t_{AJ} = \sigma / \frac{\Delta v}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f \right),$$

Where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

FIGURE 6B. APERTURE JITTER TEST METHOD

FIGURE 6. SAMPLING DELAY AND APERTURE JITTER TEST CIRCUIT

8-Bit, 125 MSPS, Flash A/D Converter

Features

- Differential Linearity Error ±0.5 LSB (Typ) or Less
- Integral Linearity Error ±0.5 LSB (Typ) or Less
- Built-In Integral Linearity Compensation Circuit
- Ultra High Speed Operation with Maximum Conversion Rate of 125 MSPS (Min)
- Low Input Capacitance (Typ) 18pF
- Wide Analog Input Bandwidth (Min for Full Scale Input) 200MHz
- Single Power Supply . . . . . -5.2V
- Low Power Consumption (Typ) 870mW
- Low Error Rate
- Operable at 50% Clock Duty Cycle
- Capable of Driving 50Ω Loads
- Direct Replacement for Sony CXA1396

Applications

- Video Digitizing
- HDTV (High Definition TV)
- Direct RF Down-Conversion
- Communication Systems
- Radar Systems
- Digital Oscilloscopes

Description

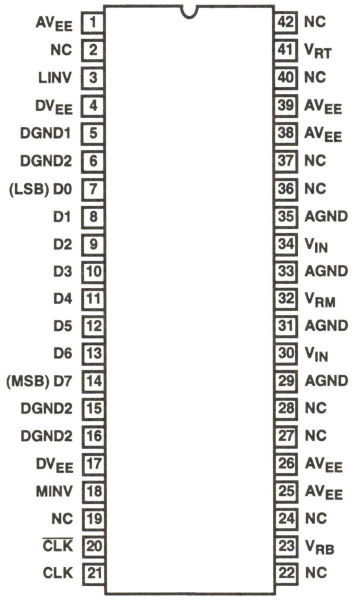
The HI1396 is an 8-bit, ultra high speed flash analog-to-digital converter IC capable of digitizing analog signals at the maximum rate of 125 MSPS. The digital I/O levels of the converter are compatible with ECL 100K/10KH/10K.

Ordering Information

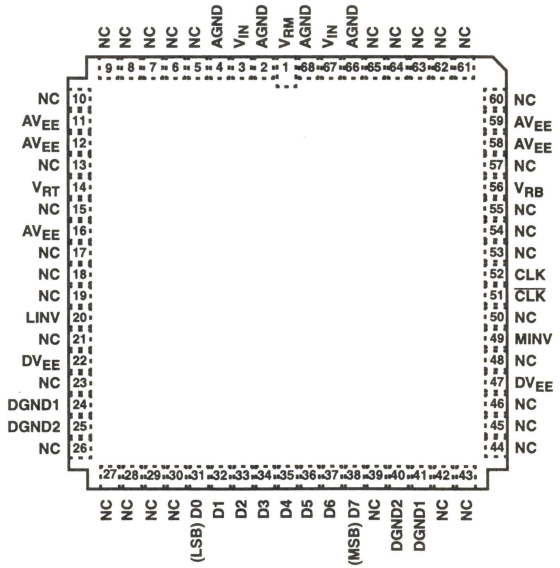
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1396JCJ	-20 to 75	42 Ld SBDIP	D42.6
HI1396AIL	-20 to 100	68 Ld CLCC	J68.A

Pinouts

HI1396 (SBDIP)
TOP VIEW



HI1396 (CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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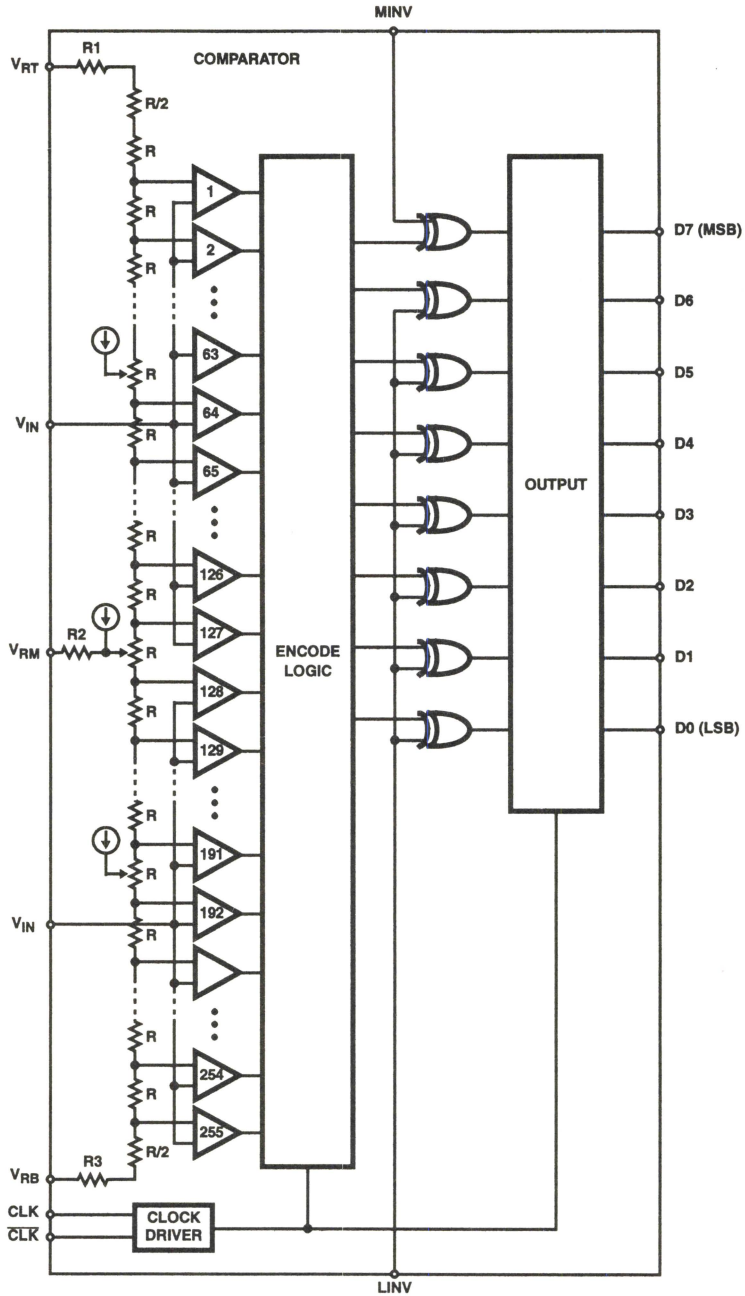
Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{EE}, DV_{EE}) . . . . . -7V
Analog Input Voltage (V_{IN}) . . . . . -2.7V to +0.5V
Reference Input Voltage
  V_{RT}, V_{RB}, V_{RM} . . . . . -2.7V to +0.5V
  $|V_{RT} - V_{RB}|$ 2.5V
Digital Input Voltage
  CLK, $\overline{CLK}$, MINV, LINV . . . . . -4V to +0.5V
  $|CLK-\overline{CLK}|$ 2.7V
V_{RM} Pin Input Current (I_{VRM}) . . . . . -3mA to +3mA
Digital Output Current (ID0 to ID7) . . . . . -30mA to 0mA

Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}{}^oC/W$	$\theta_{JC}{}^oC/W$
SBDIP Package	45	7
CLCC Package	45	8

Maximum Junction Temperature
  Ceramic Packages . . . . . 175°C
Maximum Storage Temperature Range (T_{STG}) . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions (Note 1)

Temperature Ranges (Note 4)
  SBDIP Package, T_A . . . . . -20°C to 75°C
  CLCC Package, T_C . . . . . -20°C to 100°C
Supply Voltage Ranges
  AV_{EE}, DV_{EE} . . . . . -5.5V to -4.95V
  AV_{EE} - DV_{EE} . . . . . -0.05V to 0.05V
  AGND - DGND . . . . . -0.05V to 0.05V
Reference Input Voltage
  V_{RT} . . . . . -0.1V to 0.1V
  V_{RB} . . . . . -2.2V to -1.8V
Analog Input Voltage, V_{IN} . . . . . V_{RB} to V_{RT}
Pulse Width of Clock
  t_{PW1} . . . . . 4.0ns (Min)
  t_{PW0} . . . . . 4.0ns (Min)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, $V_{RT} = 0V$, $V_{RB} = -2V$ (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Resolution		-	8	-	Bits
Integral Linearity Error, INL HI1396JCJ, HI1396AIL	f_C = 125 MSPS	-	±0.3	±0.5	LSB
Differential Linearity Error, DNL HI1396JCJ, HI1396AIL	f_C = 125 MSPS	-	-	±0.5	LSB
ANALOG INPUT					
Input Bandwidth	$V_{IN} = 2V_{P-P}$	200	-	-	MHz
Analog Input Capacitance, C_{IN}	$V_{IN} = 1V + 0.07V_{RMS}$	-	17	-	pF
Analog Input Resistance, R_{IN}		50	190	-	kΩ
Input Bias Current, I_{IN}	V_{IN} = -1V	20	130	400	µA
REFERENCE INPUTS					
Reference Resistance, R_{REF}		75	110	155	Ω
Offset Voltage					
E_{OT} V_{RT}		8	19	32	mV
E_{OB} V_{RB}		0	15	24	mV
DIGITAL INPUTS					
Logic H Level, V_{IH}		-1.13	-	-	V
Logic L Level, V_{IL}		-	-	-1.50	V
Logic H Current, I_{IH}	Input Connected to -0.8V	0	-	50	µA
Logic L Current, I_{IL}	Input Connected to -1.6V	0	-	50	µA
Input Capacitance		-	7	-	pF
DIGITAL OUTPUTS					
Logic H Level, V_{OH}	R_L = 50Ω to -2V	-1.10	-	-	V
Logic L Level, V_{OL}	R_L = 50Ω to -2V	-	-	-1.62	V

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, $V_{RT} = 0V$, $V_{RB} = -2V$ (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING CHARACTERISTICS					
Output Rise Time, t_r	$R_L = 50\Omega$ to -2V, 20% to 80%	0.5	0.9	1.2	ns
Output Fall Time, t_f	$R_L = 50\Omega$ to -2V, 20% to 80%	0.5	1.0	1.3	ns
Output Delay, t_{OD}		3.0	3.6	4.2	ns
H Pulse Width of Clock, t_{PW1}		4.0	-	-	ns
L Pulse Width of Clock, t_{PW0}		4.0	-	-	ns
DYNAMIC CHARACTERISTICS					
Maximum Conversion Rate, f_C	Error Rate 10^{-9} TPS (Note 2)	125	-	-	MSPS
Aperture Jitter, t_{AJ}		-	10	-	ps
Sampling Delay, t_{DS}		-	1.5	-	ns
Signal to Noise Ratio (SINAD) $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	Input = 1MHz, Full Scale f_C = 125 MSPS	-	46	-	dB
	Input = 31.5MHz, Full Scale f_C = 125 MSPS	-	40	-	dB
Error Rate	Input = 31.249MHz, Full Scale Error > 16 LSB, f_C = 125 MSPS	-	-	10^{-9}	TPS (Note 2)
Differential Gain Error, DG	NTSC 40 IRE Mod. Ramp, f_C = 125 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
POWER SUPPLY CHARACTERISTICS					
Supply Current, I_{EE}		-230	-160	-	mA
Power Consumption	Note 3	-	870	-	mW

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. TPS: Times Per Sample.
3. $P_D = I_{EE} \bullet V_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$
4. T_A specified in still air and without heat sink. To extend temperature range, appropriate heat management techniques must be employed.

Timing Diagram

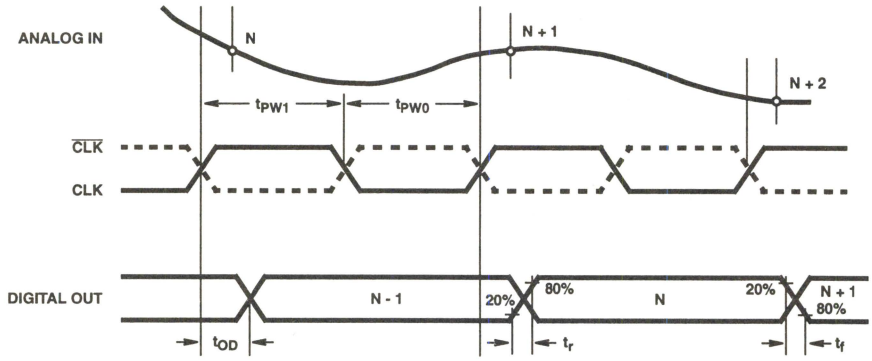
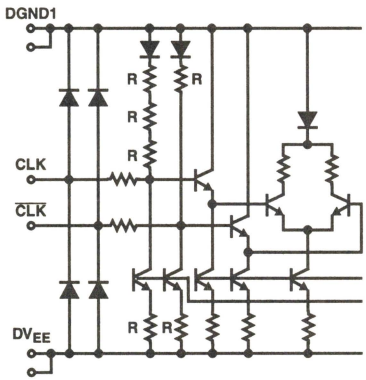
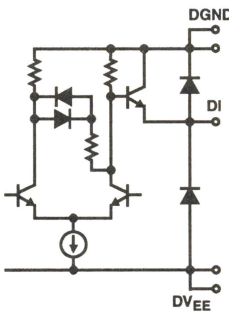
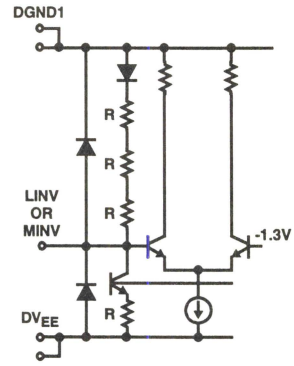
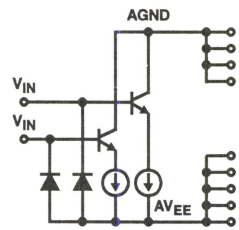
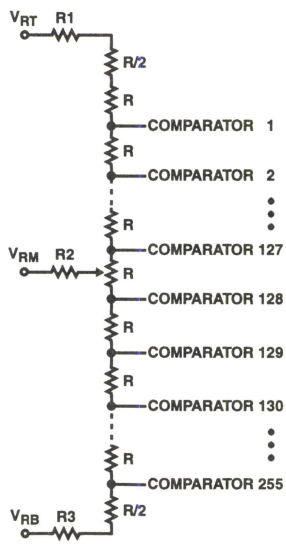


FIGURE 1.

Pin Descriptions and I/O Pin Equivalent Circuits

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
29, 31, 33, 35	49, 51, 53, 55	AGND	-	0V		Analog GND. Used as GND for input buffers and latches of comparators. Isolated from DGND1, DGND2.
1, 25, 26, 38, 39	41, 42, 62, 63, 67	AV_{EE}	-	-5.2V		Analog V_{EE} -5.2V (Typ). Internally connected to DV_{EE} (Resistance: 4Ω to 6Ω). Bypass with 0.1µF to AGND.
21	35	CLK	I	ECL		CLK Input.
20	34	$\overline{CLK}$				Input complementary to CLK. When left open pulled down to -1.3V. Device is operable without $\overline{CLK}$ input, but use of complementary inputs of CLK and $\overline{CLK}$ is recommended to obtain stable high speed operation.
5, 16	7, 24	DGND1	-	0V		Digital GND for internal circuits.
6, 15	8, 23	DGND2	-	0V		Digital GND for output transistors.
4, 17	5, 30	DV_{EE}	-	-5.2V		Digital V_{EE}. Internally connected to AV_{EE} (resistance: 4Ω to 6Ω). Bypass with 0.1µF to DGND
7	14	D0	O	ECL		LSB of data outputs. External pull-down resistor is required.
8	15	D1				Data outputs. External pull-down resistors are required.
9	16	D2				
10	17	D3				
11	18	D4				
12	19	D5				
13	20	D6				
14	21	D7				MSB of data outputs. External pull-down resistor is required.

Pin Descriptions and I/O Pin Equivalent Circuits (Continued)

PIN NUMBER DIP	PIN NUMBER LCC	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
3	3	LINV	I	ECL		Input pin for D0 (LSB) to D6 output polarity inversion (see A/D Output Code Table). Pulled low when left open.
18	32	MINV	I	ECL		Input pin for D7 (MSB) output polarity inversion (see A/D Output Code Table). Pulled low when left open.
30, 34	50, 54	V_{IN}	I	V_{RT} to V_{RB}		Analog input pins. These two pins must be connected externally, since they are not internally connected.
23	39	V_{RB}	I	-2V		Reference voltage (bottom). Typically -2V. Bypass with a 0.1µF and 10µF to AGND.
32	52	V_{RM}	I	$V_{RB}/2$		Reference voltage mid point. Can be used as a pin for integral linearity compensation.
41	65	V_{RT}	I	0V		Reference voltage (top) typically 0V. When a voltage different from AGND is applied to this pin, bypass with a 0.1µF and 10µF to AGND.

Pin Descriptions and I/O Pin Equivalent Circuits (Continued)

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
2, 19, 22, 24, 27, 28, 36, 37, 40, 42	1, 2, 4, 6, 9-13, 25-29, 31, 33, 36-38, 40, 43-48, 56-61, 64, 66, 68	NC	-	-		Unused pins. No internal connections have been made to these pins. Connecting them to AGND or DGND on PC board is recommended.

A/D OUTPUT CODE TABLE

V_{IN} (Note 5)	STEP	MINV 1, LINV 1		0, 1		1, 0		0, 0	
		D7	D0	D7	D0	D7	D0	D7	D0
0V		000 • • • • • 00		100 • • • • • 00		011 • • • • • 11		111 • • • • • 11	
	0	000 • • • • • 00		100 • • • • • 00		011 • • • • • 11		111 • • • • • 11	
	1	000 • • • • • 01		100 • • • • • 01		011 • • • • • 10		111 • • • • • 10	
		•		•		•		•	
		•		•		•		•	
		•		•		•		•	
-1V	127	011 • • • • • 11		111 • • • • • 11		000 • • • • • 00		100 • • • • • 00	
	128	100 • • • • • 00		000 • • • • • 00		111 • • • • • 11		011 • • • • • 11	
		•		•		•		•	
		•		•		•		•	
		•		•		•		•	
	254	111 • • • • • 10		011 • • • • • 10		100 • • • • • 01		000 • • • • • 01	
	255	111 • • • • • 11		011 • • • • • 11		100 • • • • • 00		000 • • • • • 00	
-2V		111 • • • • • 11		011 • • • • • 11		100 • • • • • 00		000 • • • • • 00	

NOTE:

5. V_{RT} = 0V, V_{RB} = -2V.

Test Circuits

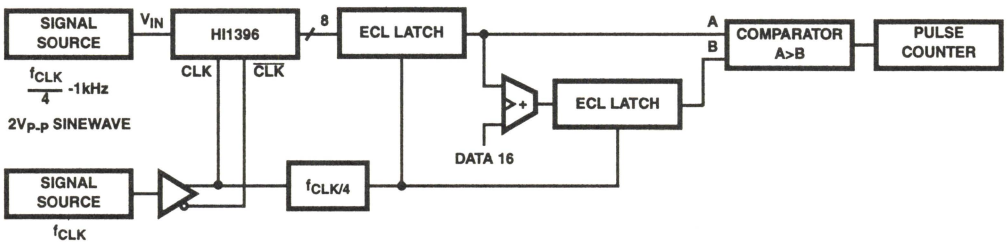


FIGURE 2. MAXIMUM CONVERSION RATE TEST CIRCUIT

Test Circuits (Continued)

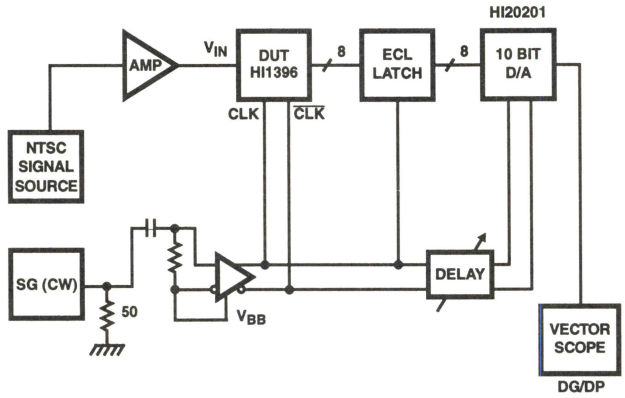


FIGURE 3. DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

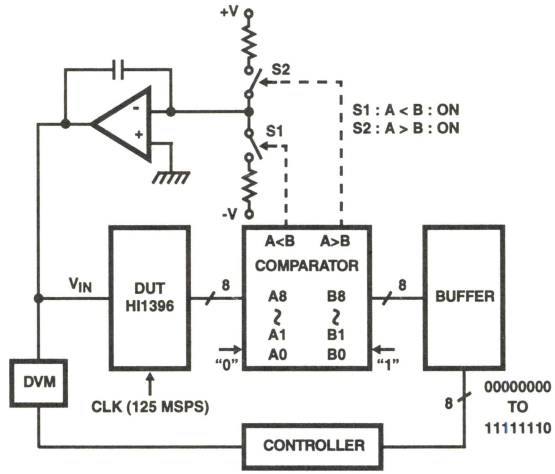


FIGURE 4. INTEGRAL AND DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits (Continued)

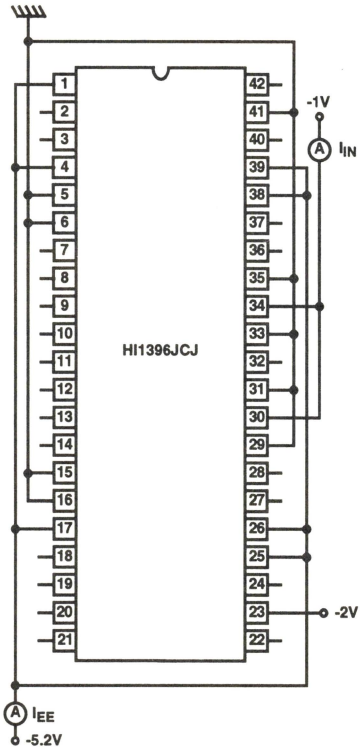


FIGURE 5A.

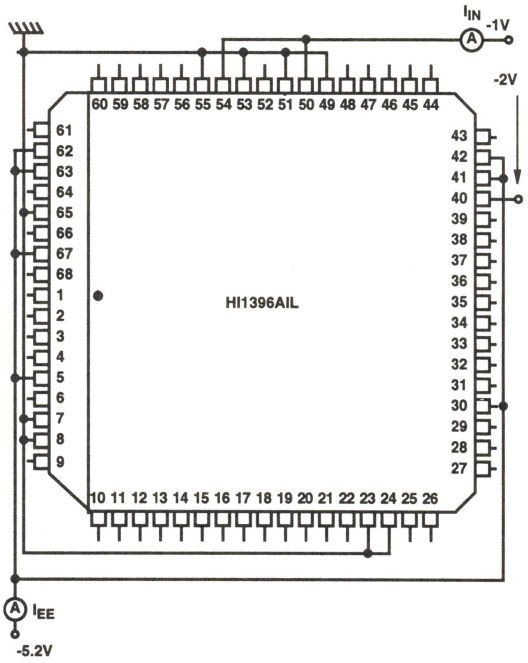


FIGURE 5B.

FIGURE 5. ANALOG INPUT BIAS AND POWER SUPPLY CURRENT TEST CIRCUITS

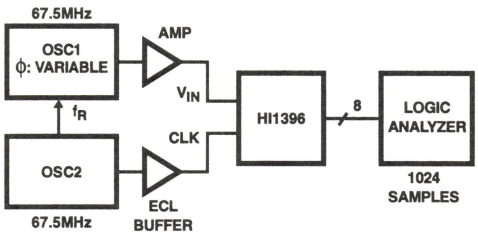
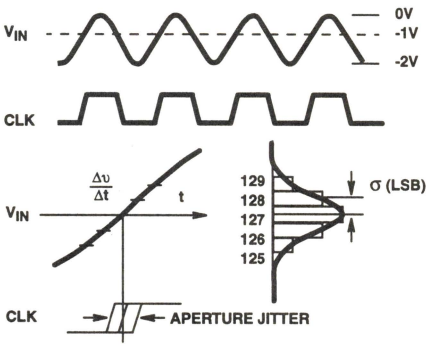


FIGURE 6A.



Aperture jitter is defined as follows:

$$t_{AJ} = \sigma / \frac{\Delta v}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f \right)$$

Where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

FIGURE 6B. APERTURE JITTER TEST METHOD

FIGURE 6. SAMPLING DELAY AND APERTURE JITTER TEST CIRCUIT

HARRIS SEMICONDUCTOR

HI1826

August 1997

6-Bit, 140 MSPS, Flash A/D Converter

Features

- Ultra-High Speed Operation with Maximum Conversion Rate. . . . . 140 MSPS
- Low Input Capacitance 7pF
- Wide Analog Input Bandwidth (Min) 200MHz
- Low Power Consumption 225mW
- Low Error Rate

Applications

- RGB Graphics Processing
- Digital Data Storage Read Channels
- Digital Communications

Description

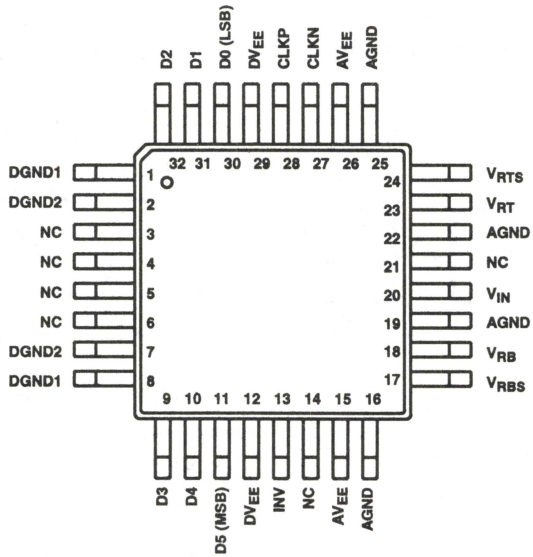
HI1826 is a 6-bit, 140 MSPS, flash A/D converter IC capable of digitizing analog signals at the maximum rate of 140 MSPS. The digital input/output level is compatible with the ECL 100K/10KH/10K.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1826JCQ	-20 to 75	32 Ld MQFP	Q32.7x7-S

Pinout

HI1826
(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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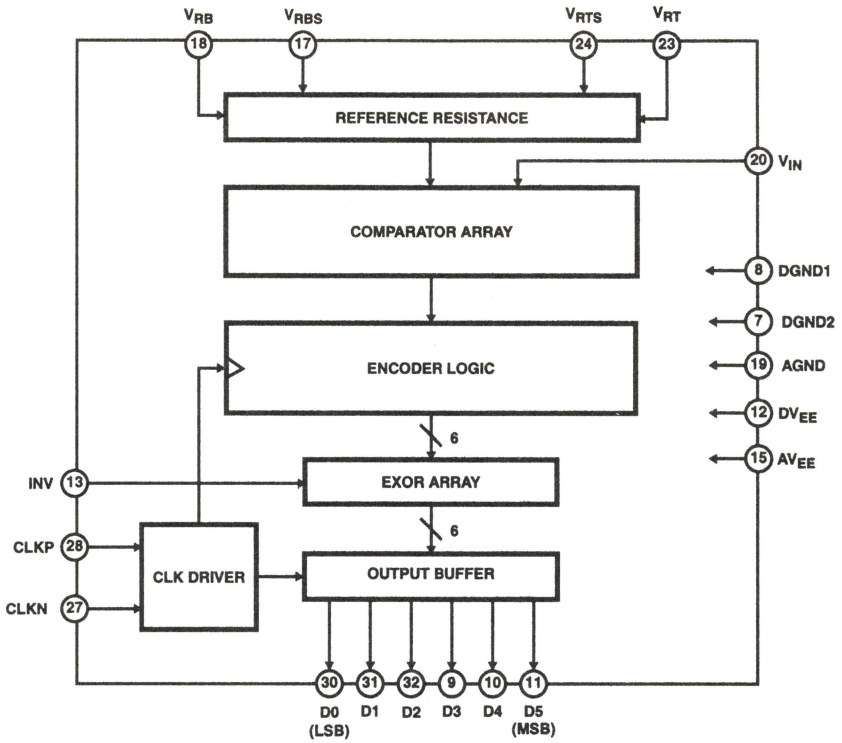
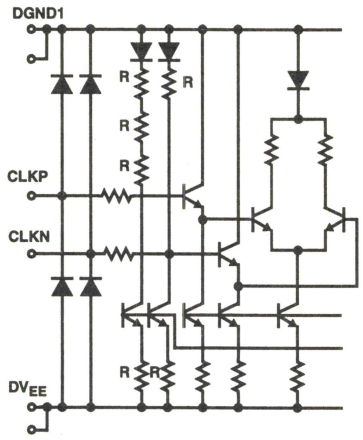
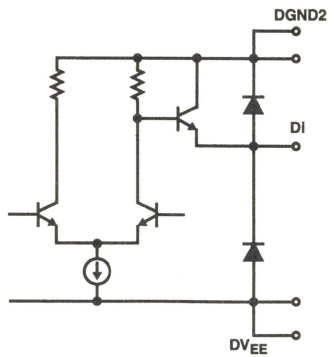
File Number 4107.1

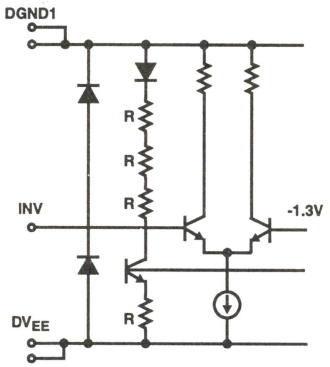
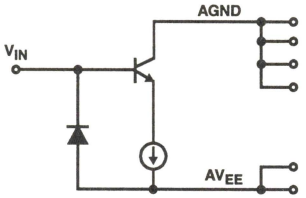
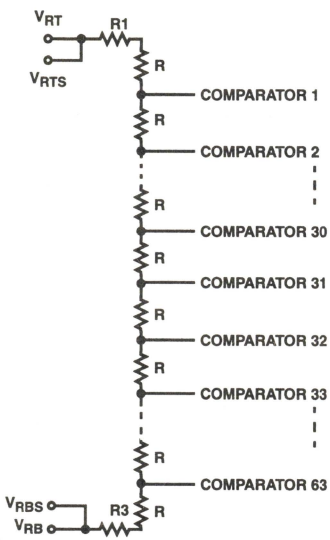
Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
16, 19, 22, 25	AGND	-	0V		Analog GND. Used as GND for input buffers and latches of comparators. Separated from DGND1 and DGND2.
15, 26	AV_{EE}	-	-5.2V		Analog V_{EE}. Typical voltage is -5.2V. Connected internally with DV_{EE}. (Resistance is 4 to 6Ω.) Connect to AGND through a ceramic chip capacitor of 0.1µF or more just near the pin.
28	CLKP	I	ECL		CLK Input.
27	CLKN				CLK Complementary Input. When left open, voltage goes to ECL threshold potential (-1.3V). Although only CLKP input can be used for operation with CLKN input open, complementary input is recommended in order to attain high speed and stable operation.
1, 8	DGND1	-	0V		Digital GND for Internal Circuits.
2, 7	DGND2	-	0V		Digital GND for Output Transistors.
12, 29	DV_{EE}	-	-5.2V		Digital V_{EE}. Connected internally with AV_{EE}. (Resistance is 4 to 6Ω.) Connect to DGND through a ceramic chip capacitor of 0.1µF or more just near the pin.
30	D0	O	ECL		LSB of Data Output. External pull-down resistor is required.
31	D1				Data Output. External pull-down resistors are required.
32	D2				
9	D3				
10	D4				
11	D5				MSB of Data Output. External pull-down resistor is required.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
13	INV	I	ECL		Output polarity inversion input for D0 (LSB) to D5 (MSB). (Refer to the output code table.) When left open, Low levels maintained.
20	V_{IN}	I	V_{RT} to V_{RB}		Analog Input.
18	V_{RB}	I	-2V		Reference Voltage (Bottom) Force; typical voltage is -2V. Connect to AGND through a ceramic chip capacitor of 0.1µF or more and a tantalum capacitor of 10µF or more just near the pin.
17	V_{RBS}				Reference Voltage (Bottom) Sense.
23	V_{RT}	I	0V		Reference Voltage (Top) Force; typical voltage is 0V. When applying a voltage other than AGND to this pin, connect to AGND through a ceramic chip capacitor of 0.1µF for more and a tantalum capacitor of 10µF or more just near the pin.
24	V_{RTS}				Reference Voltage (Top) Sense.
3, 4 5, 6 14, 21	NC	-	-		Not Connected. Although not connected in the IC, it is recommended that these pins should be connected to AGND or DGND on printed circuit board.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{EE}) . . . . . -7V to 0.5V
Reference Voltage (V_{RT}, V_{RB}) . . . . . -1.5V to 0.5V
$|V_{RT} - V_{RB}|$ 2.5V
Analog Input Voltage (V_{IN}) . . . . . -2.7V to 0.5V
Digital Input Voltage (CLKP, CLKN, INV) . . . . . -4V to 0.5V
|CLKP - CLKN| 2.7V
Digital Output Current (I_{D0} to I_{D5}) . . . . . -30mA to 0mA

Operating Conditions

Temperature Range (T_A) . . . . . -20^oC to 75^oC
Supply Voltage
AV_{EE}, DV_{EE} . . . . . -5.5V to -4.95V
AV_{EE}, DV_{EE} . . . . . -0.05V to 0.05V
AGND, DGND . . . . . -0.05V to 0.05V
Reference Voltage
V_{RT} . . . . . -0.1V to 0.1V
V_{RB} . . . . . -2.2V to -1.8V
Analog Input Voltage (V_{IN}) . . . . . V_{RB} to V_{RT}
Clock Pulse Width
t_{PW1} 3.0ns
t_{PW0} 3.0ns

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	122

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{DD} = +5V$, $V_{RB} = 1.0V$, $V_{RT} = 2.0V$, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	n		6	6	6	bits
DC CHARACTERISTICS						
Integral Linearity Error	E_{IL}	$f_C = 140MHz$	-0.25	-	+0.25	LSB
Differential Linearity Error	E_{DL}	$f_C = 140MHz$	-0.25	-	+0.25	LSB
ANALOG INPUT						
Analog Input Capacitance	C_{IN}	$V_{IN} = -1V + 0.07V_{RMS}$	-	7	18	pF
Analog Input Resistance	R_{IN}		300	-	-	kΩ
Input Bias Current	I_{IN}	$V_{IN} = -1V$	-	-	400	µA
REFERENCE INPUT						
Reference Resistance	R_{REF}		-	200	-	Ω
Offset Voltage V_{RT}	E_{OT}		-	-	20	mV
V_{RB}	E_{OB}		-	-	20	mV
DIGITAL INPUT						
Logic High Level	V_{IH}		-1.13	-	-0.65	V
Logic Low Level	V_{IL}		-2.1	-	-1.5	V
Logic High Current	I_{IH}	Apply -0.8V to Input	0	-	50	µA
Logic Low Current	I_{IL}	Apply -1.6V to Input	-50	-	50	µA
Input Capacitance			-	7		pF
SWITCHING CHARACTERISTICS						
Maximum Conversion Frequency	f_C	Error rate 1E-9 TPS (Note 1)	140	-	-	MSPS
Aperture Jitter	t_{AJ}		-	10	-	ps

Electrical Specifications V_{DD} = +5V, V_{RB} = 1.0V, V_{RT} = 2.0V, T_A = 25°C **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sampling Delay	t_{DS}		-	1.5	-	ns
High Pulse Width of Clock	t_{PW1}		3.0	-	-	ns
Low Pulse Width of Clock	t_{PW0}		3.0	-	-	ns
DIGITAL OUTPUT						
Logic High Level	V_{OH}	R_L = 100Ω to -2V	-1.10	-	-0.65	V
Logic Low Level	V_{OL}	R_L = 100Ω to -2V	-2.1	-	-1.6	V
Output Delay	t_{DO}	R_L = 100Ω to -2V	3.0	3.6	4.2	ns
Output Rise Time	t_r	R_L = 100Ω to -2V, 20% to 80%	-	0.8	-	ns
Output Fall Time	t_f	R_L = 100Ω to -2V, 20% to 80%	-	1.0	-	ns
DYNAMIC CHARACTERISTICS						
Analog Input Bandwidth		f_{CLK} = 140MHz, f_{IN} = 69.999MHz	200	-	-	MHz
Error Rate		Error Amplitude ≥ 4 LSB -3dB f_S	-	-	1E-09	TPS (Note 1)
S/N Ratio	SNR	f_{CLK} = 140MHz, f_{IN} = 1MHz	-	36	-	dB
		f_{CLK} = 140MHz, f_{IN} = 35MHz		34		dB
POWER SUPPLY						
Supply Current	I_{EE}	AV_{EE} = DV_{EE} = -5.2V	-60	-40	-25	mA
Power Consumption	P_D		-	225	-	mW

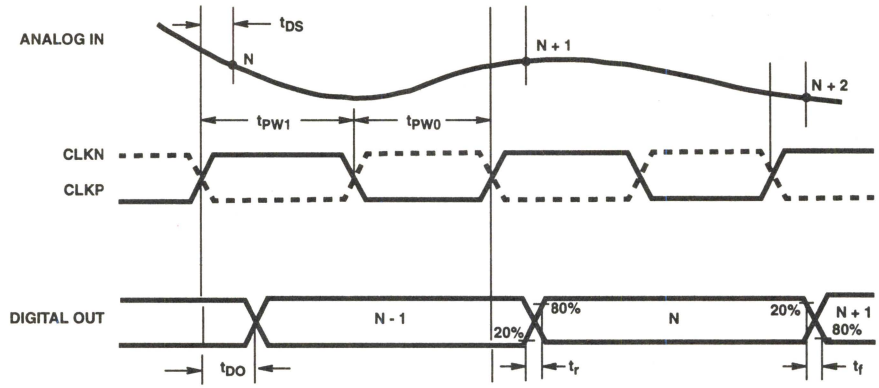
Note 1. TPS: Times Per Sample

Output Code Table

V_{IN} (NOTE)	STEP	INV: 1 D5 D0	INV:0 D5 D0
0V	0	000000	111111
	1	000001	111110
		•	•
		•	•
		•	•
-1.0V	31	011111	100000
	32	100000	011111
		•	•
		•	•
		•	•
	62	111110	000001
-2.0V	63	111111	000000

NOTE: V_{RT} = 0V, V_{RB} = -2V

Timing Diagram



Test Circuits

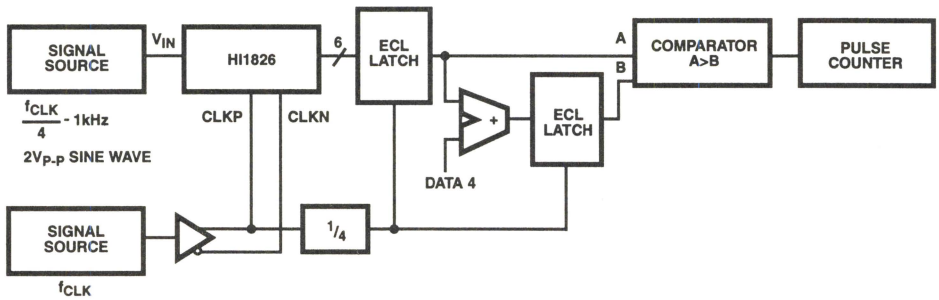


FIGURE 1. MAXIMUM CONVERSION RATE MEASUREMENT CIRCUIT

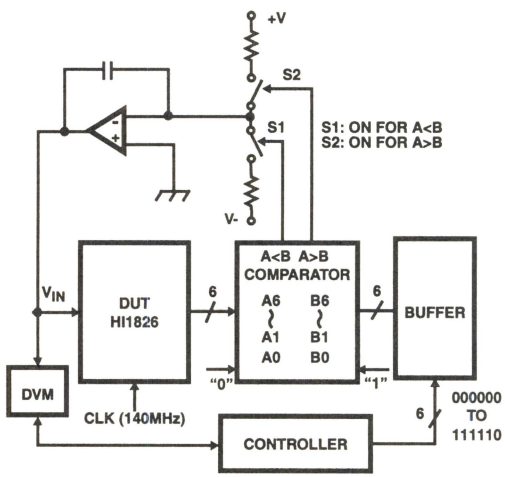


FIGURE 2. INTEGRAL LINEARITY ERROR MEASUREMENT CIRCUIT, DIFFERENTIAL LINEARITY ERROR MEASUREMENT CIRCUIT

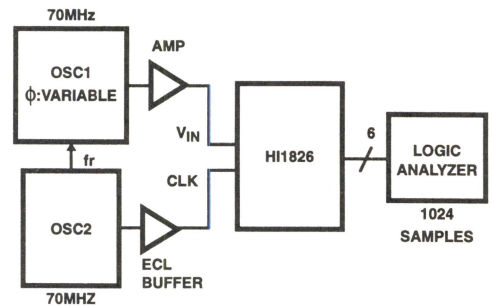


FIGURE 3. SAMPLING DELAY MEASUREMENT CIRCUIT APERTURE JITTER MEASUREMENT CIRCUIT

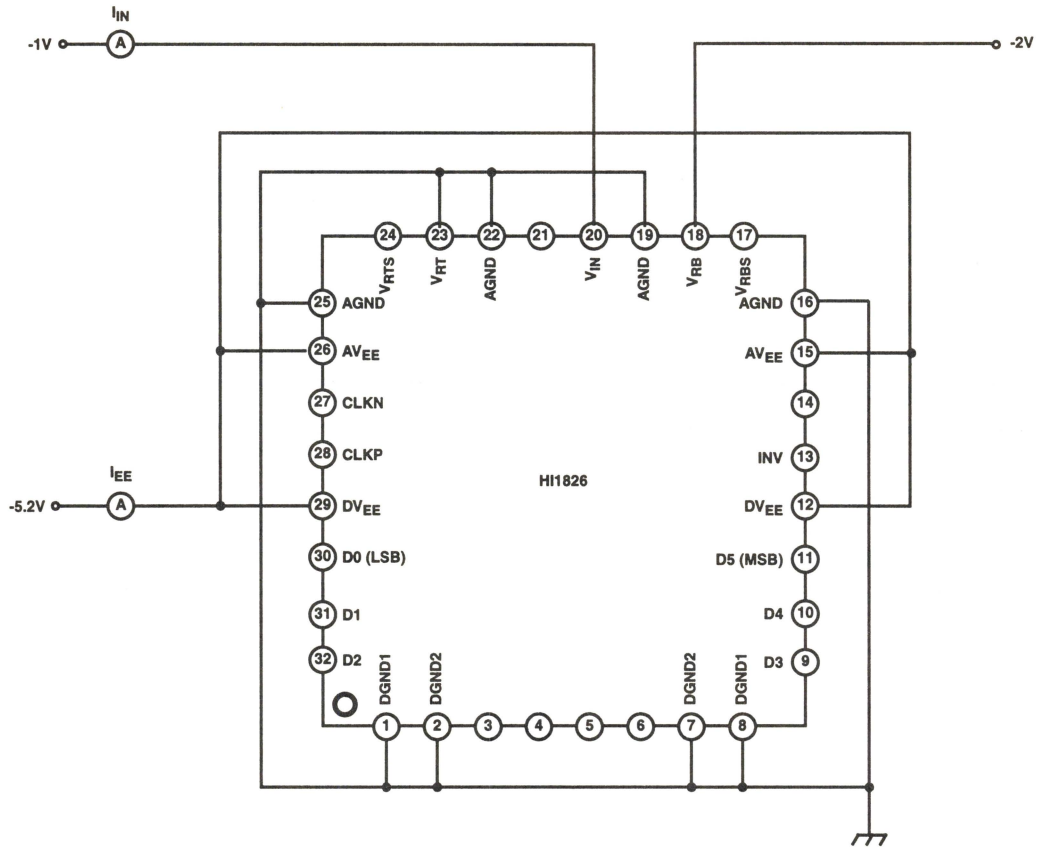


FIGURE 4. SUPPLY CURRENT MEASUREMENT CIRCUIT ANALOG INPUT BIAS CURRENT MEASUREMENT CIRCUIT

HARRIS SEMICONDUCTOR

HI1866

August 1997

6-Bit, 140 MSPS, Flash A/D Converter

Features

- Ultra-High Speed Operation with Maximum Conversion Rate. . . . . 140 MSPS
- Low Input Capacitance 7pF
- Wide Analog Input Bandwidth 210MHz
- Low Power Consumption 325mW
- Low Error Rate
- Excellent Temperature Characteristics
- 1:2 Demultiplexed Output (TTL Level)
- Direct Replacement for Sony CXA1866

Applications

- LCD Panels
- Magnetic Recording (PRML)
- Communications (QPSK, QAM)

Description

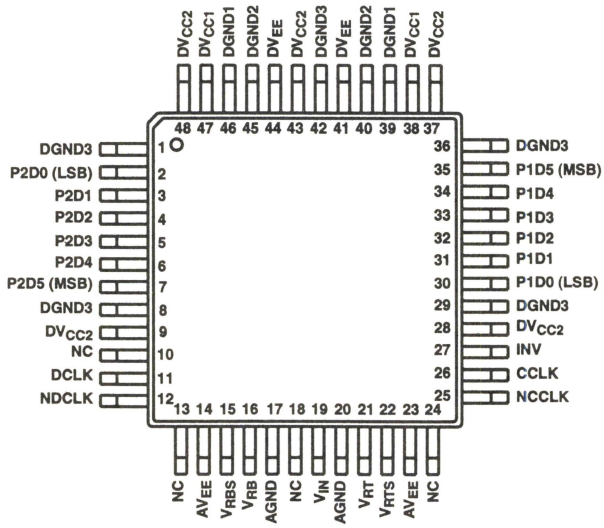
HI1866 is a 6-bit, high-speed, flash A/D converter capable of digitizing analog signals at the maximum rate of 140 MSPS. The digital input level is compatible with the ECL 100K/10KH/10K.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI1866JCQ	-20 to 75	48 Ld MQFP	Q48.12x12-S

Pinout

HI1866
(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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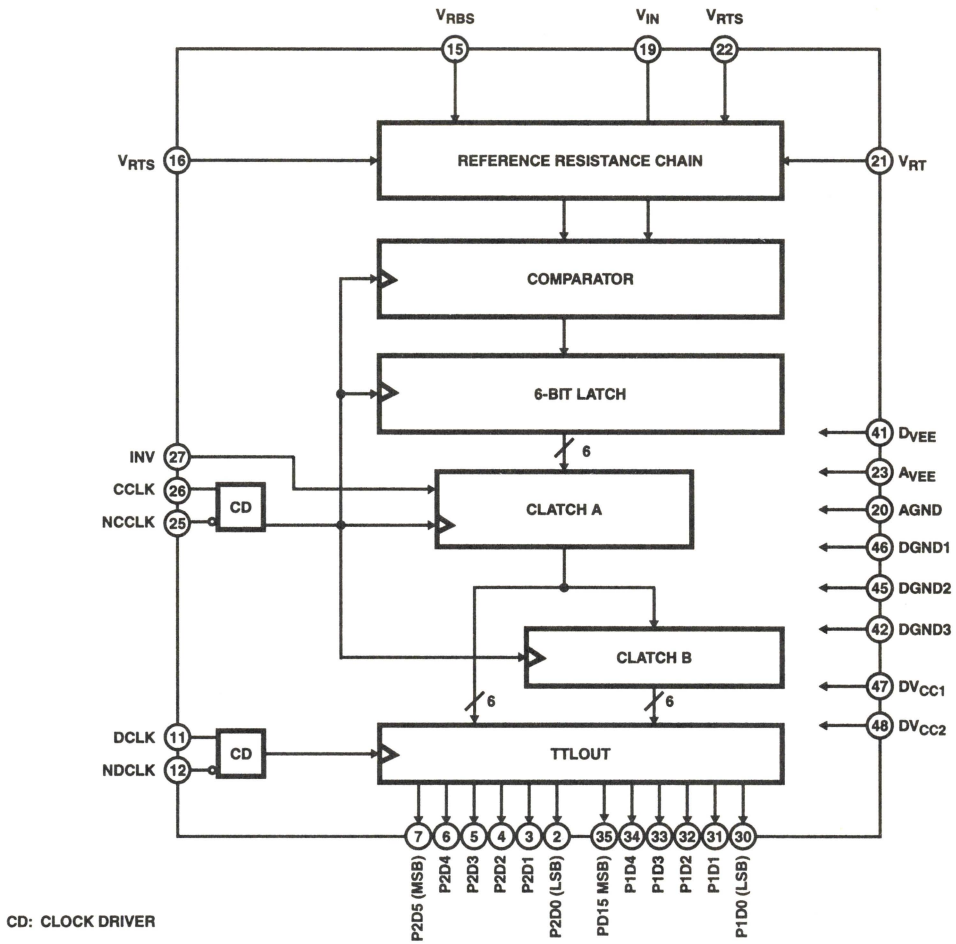
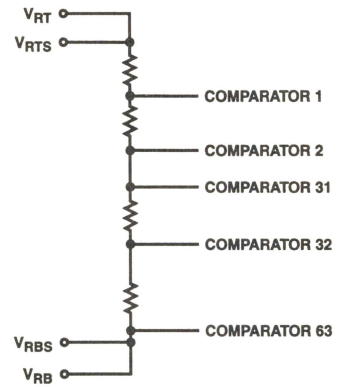
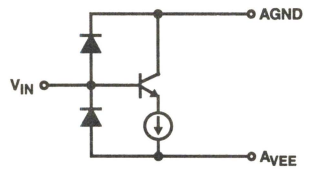
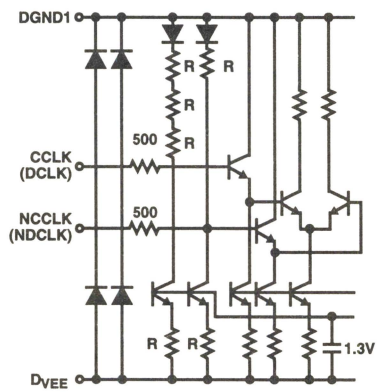
Functional Block Diagram

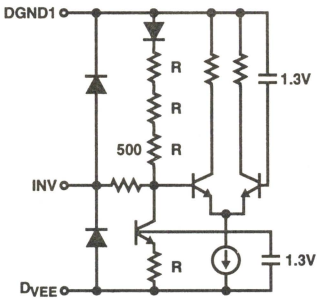
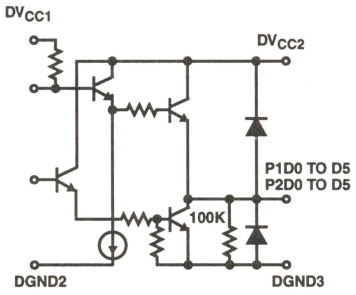


CD: CLOCK DRIVER

Pin Descriptions

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
21	V_{RT}	I	0V		Top reference voltage input (= 0). This is the top reference voltage supplied to the internal resistance chain. The external input can be set in accordance with the peak value on the plus side of the input analog signal amplitude.
22	V_{RTS}	O	0V		V_{RT} sense output. This is the voltage sense pin for V_{RT}.
16	V_{RB}	I	-2V		Bottom reference voltage input (= -2V). This is the bottom reference voltage supplied to the internal resistance chain. The external input can be set in accordance with the peak value on the minus side of the input analog signal amplitude.
15	V_{RBS}	O	-2V		V_{RB} sense output. This is the voltage sense pin for V_{RB}.
19	V_{IN}	I	V_{RTS} to V_{RBS}		Analog input. The input range is $2V_{P-P}$.
26	CCLK	I	ECL		CCLK clock input. This is the conversion clock, and is an ECL level input.
25	NCCLK	I	ECL		CCLK inversion clock input. This is an ECL level input. When left open, this input goes to the ECL threshold potential (-1.3V). Only CCLK input can be used for operation with the NCCLK input left open, but complementary input is recommended to attain fast and stable operation.
11	DCLK	I	ECL		DCLK clock input. This is the 1:2 DMPX latch clock; input a clock of $^1/_2$ frequency of CCLK. Data is output from DMPX port 1 and port 2 synchronously with the rising edge of this signal. This is an ECL level input.
12	NDCLK	I	ECL		DCLK inversion clock input. This is an ECL level input. When left open, this input goes to the ECL threshold potential (-1.3V). Only DCLK input can be used for operation with the NDCLK input left open, but complementary input is recommended to attain fast and stable operation.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
27	INV	I	ECL		Digital output polarity inversion input. This is an ECL level input. This input inverts the polarity of the digital outputs P1D0 to P1D5, and P2D0 to P2D5. (Refer to the Output Code Table.) When left open, this signal is maintained at the low level.
30	P1D0	O	TTL		These pins are for the 6 bits of digital output data for DMPX port 1. P2D5 is the MSB, and P2D0 is the LSB. These are TTL levels outputs.
31	P1D1				
32	P1D2				
33	P1D3				
34	P1D4				
35	P1D5				
2	P2D0				These pins are for the 6 bits of digital output data for DMPX port 2. P2D5 is the MSB, and P2D0 is the LSB. These are TTL level outputs.
3	P2D1				
4	P2D2				
5	P2D3				
6	P2D4				
7	P2D5				
38, 47	DVCC1	-	+5.0V		+5V power supply for TTL level internal circuit.
9, 28, 37, 43, 48	DVCC2	-	+5.0V		+5V power supply for TTL level output buffers (P1D0 to P2D5).
39, 46	DGND1	-	0V		Ground for DV_{EE} digital circuit.
40, 45	DGND2	-	0V		Ground for DV_{CC1} digital circuit.
1, 8, 29, 36, 42	DGND3	-	0V		Ground for DV_{CC2} digital circuit.
17, 20	AGND	-	0V		Ground for AV_{EE} analog circuit. Used as the ground for the comparator input buffers, latches, etc. Separated from DGND.
41, 44	DV_{EE}	-	-5.2V		-5.2V power supply for digital circuit. Connected internally with AV_{EE}. (Resistance is 4Ω to 6Ω.)
14, 23	AV_{EE}	-	-5.2V		-5.2V power supply for analog circuit. Connected internally with DV_{EE}. (Resistance is 4Ω to 6Ω.)

Absolute Maximum Ratings

Supply Voltage (AV_{EE}, DV_{EE}) ..... -7V to 0.5V
(DV_{CC}) (Note 2) ..... 0.5V to 7.0V
Reference Voltage (V_{RT}, V_{RB}) ..... -2.7V to 0.5V
($|V_{RT} - V_{RB}|$) 2.5V
Analog Input Voltage (V_{IN}) ..... -2.7V to 0.5V
Digital Input Voltage (DIN) (Note 3) ..... -4.0V to 0.5V
($|CCLK–NCCLK|$, $|DCLK–NDCLK|$) 2.5V
Digital Output Current (I_{D0} to I_{D6}) ..... -30mA to +30mA
Storage Temperature (T_{STG}) ..... -65^oC to 150^oC
Ambient Operating Temperature (T_A) ..... -20^oC to 75^oC
Allowable Power Dissipation (P_D) 750mW

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	95

Maximum Junction Temperature ..... 150^oC
Maximum Storage Temperature Range (T_{STG}) ... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(Lead Tips Only)

Recommended Operating Conditions

Supply Voltage	MIN	TYP	MAX
AV_{EE}, DV_{EE}	-5.5V	-5.2V	-4.75V
AV_{EE} - DV_{EE}	-0.05V	0V	0.05V
AGND - DGND (Note 4)	-0.05V	0V	0.05V
DV_{CC} (Note 5)	4.75V	5.0V	5.25V
Temperature Range (T_A)	-20^oC	-	75^oC

Reference Input Voltage	MIN	TYP	MAX
V_{RT}	-0.1V	0V	0.1V
V_{RB}	-2.2V	-2.0V	-0.8V
Analog Input Voltage (V_{IN})	V_{RB}	To	V_{RT}
Digital Input Voltage, DIN (H)	-1.1V	-	-
DIN (L)	-	-	-1.5V
CCLK, NCCLK Frequency (f_{CCLK})(MHz)	-	-	140
DCLK, NDCLK Frequency (f_{DCLK})(MHz)	-	-	70
CCLK, NCCLK Duty (D_{CCLK})(%)	40	50	60
DCLK, NDCLK Duty (D_{DCLK})(%)	40	50	60
CCLK-DCLK Time Difference (t_{DCD})(ns)	$-t_{PWL} + 2$	0	$t_{PWH} + 1$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. $DV_{CC} = DV_{CC1}$, DV_{CC2}.
3. D_{IN} = CCLK, NCCLK, DCLK, NDCLK, INV.
4. DGND = DGND1, DGND2, DGND3.
5. Refer to Timing Chart 1 for t_{PWL}, t_{PWH}.

Electrical Specifications

$T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, $DV_{CC} = 5V$, $V_{RT} = 0V$, $V_{RB} = -2V$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution, n	n		-	6	-	bits
DC CHARACTERISTICS						
Integral Linearity Error	E_{IL}	f_C = 140MHz	-	-	±0.2	LSB
Differential Linearity Error	E_{DL}	f_C = 140MHz	-	-	±0.2	LSB
No Missing Code			-	Guaranteed	-	-
ANALOG INPUT						
Analog Input Capacitance	C_{IN}	$V_{IN} = -1V_0.7V_{RMS}$, DC	-	7	-	pF
Analog Input Resistance	R_{IN}	$-2V \leq V_{IN} \leq 0V$	200	-	-	KΩ
Input Bias Current	I_{IN}	$-2V \leq V_{IN} \leq 0V$	-	-	110	µA
REFERENCE INPUT						
Reference Resistance	R_{REF}		-	225	-	Ω
Reference Resistance Current	I_{REF}		-	9	-	mA
Offset Voltage V_{RT}	E_{OT}		0	-	25	mV
V_{RB}	E_{OB}		-	-	25	mV
DIGITAL INPUT						
Logic High Level	V_{IH}		-1.13	-	-	V

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, $DV_{CC} = 5V$, $V_{RT} = 0V$, $V_{RB} = -2V$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Logic Low Level	V_{IL}		-	-	-1.50	V
Logic High Current	I_{IH}	$V_{IH} = -0.8V$	0	-	50	µA
Logic Low Current	I_{IL}	$V_{IL} = -1.6V$	-50	-	50	µA
Input Capacitance			-	3.5	-	pF
SWITCHING CHARACTERISTICS						
Maximum Conversion Frequency	f_C	Error Rate $1E^{-9}$ TPS (Note 1)	140	-	-	MSPS
Aperture Jitter	t_{AJ}		-	5.0	-	ps
Sampling Delay	t_{DS}		-	1.0	-	ns
DIGITAL OUTPUT						
Logic High Level	V_{OH}	$I_{OUT} = -2mA$	2.7	-	-	V
Logic Low Level	V_{OL}	$I_{OUT} = 1mA$	-	-	0.5	V
Output Delay	t_{DO}	$Z_L = 25pF$	2.0	-	8.0	ns
Output Rising Time	t_r	$Z_L = 25pF$, 0.5V to 2.4V	-	1.2	-	ns
Output Falling Time	t_f	$Z_L = 25pF$, 0.5V to 2.4V	-	1.2	-	ns
DYNAMIC CHARACTERISTICS						
Analog Amplitude Input Bandwidth	F_{INB}	$V_{IN} = 2V_{P-P}$, Peak-to-Peak Value = 3dB Down Input Frequency	210	-	-	MHz
S/N Ratio	SNR1 SNR2 SNR3	$f_C = 140MHz$, $f_{IN} = 1MHz$ $f_C = 140MHz$, $f_{IN} = 35MHz$ $f_C = 140MHz$, $f_{IN} = 70MHz$	-	36 34 32	-	dB dB dB
Error Rate		$f_C = 140MHz$, Error > 4 LSB	-	-10^{-9}	-	TPS (Note 1)
POWER SUPPLY						
Supply Current	I_{CC} I_{EE}	$DV_{CC} = +5V$ $AV_{EE} = DV_{EE} = -5.2V$	- -60	20 -40	32 -	mA mA
Power Consumption	P_D		-	325	-	mW

NOTE:

1. TPS: Times Per Sample

Output Code Table

V_{IN}	STEP	DINV: 1 D5 D0	INV:0 D5 D0
0V	0	000000	111111
	1	000001	111110
		•	•
		•	•
		•	•
-1V	31	011111	100000
	32	100000	011111
		•	•
		•	•
		•	•
	62	111110	000001
-2V	63	111111	000000

NOTE: $V_{RT} = 0V$, $V_{RB} = -2V$.

Timing Diagrams

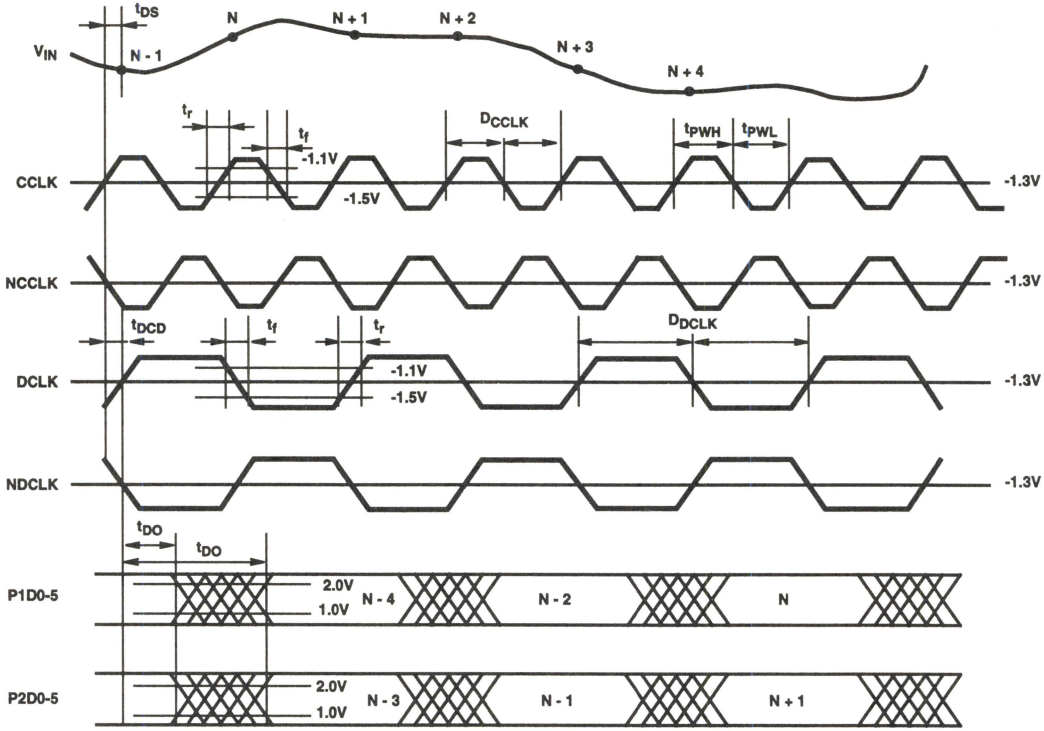


FIGURE 1. TIMING CHART 1

Timing Diagrams (Continued)

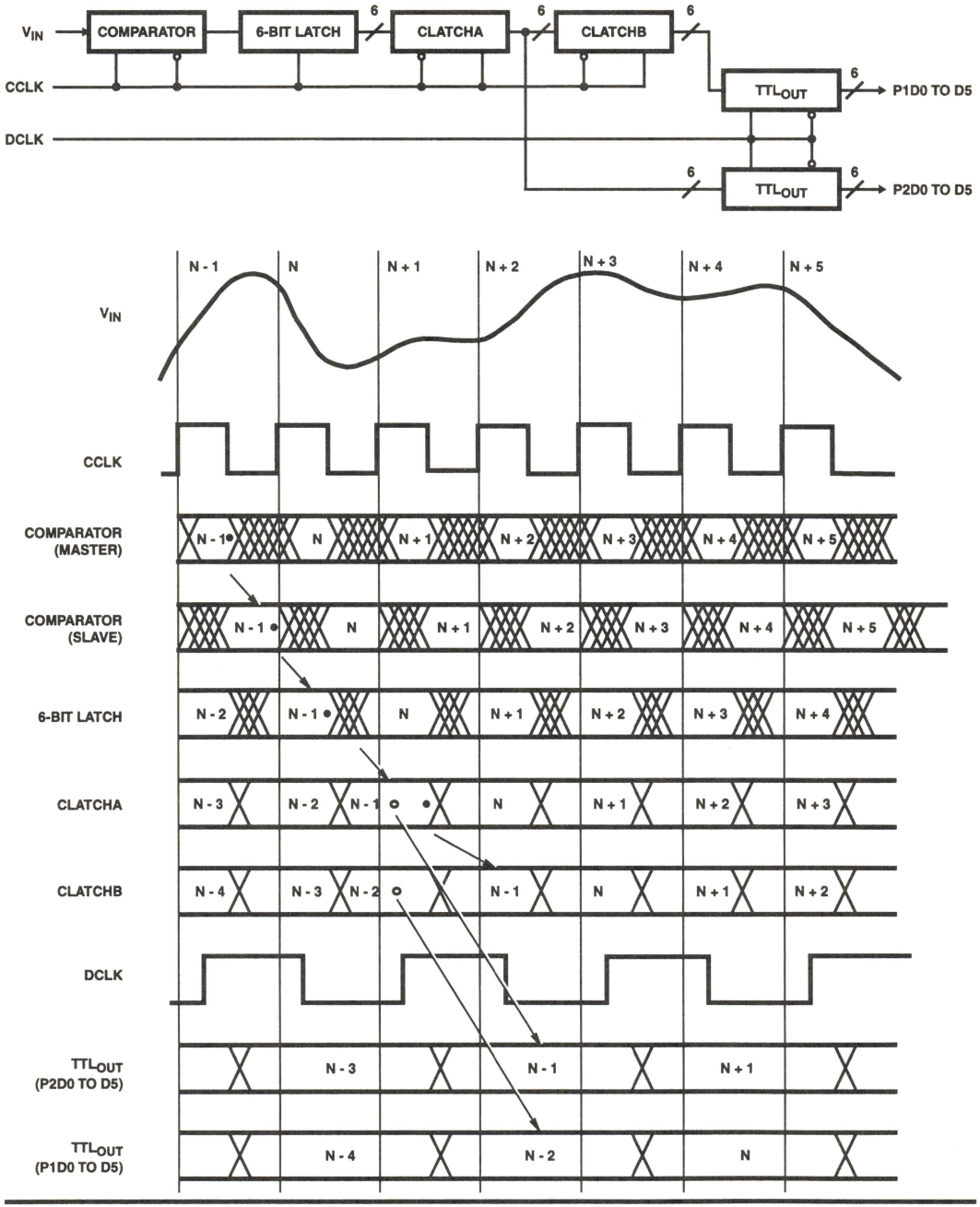


FIGURE 2. TIMING CHART 2

Test Circuits

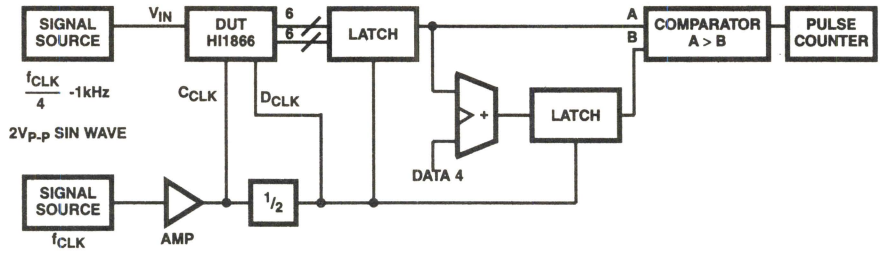


FIGURE 3. MAXIMUM CONVERSION RATE TEST CIRCUIT

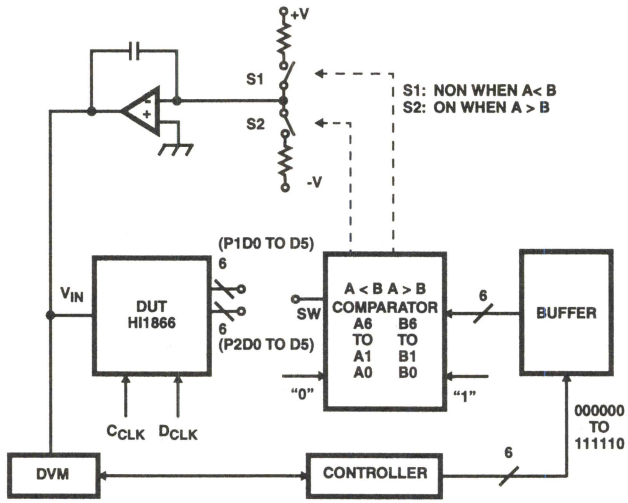


FIGURE 4. INTEGRAL/DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits (Continued)

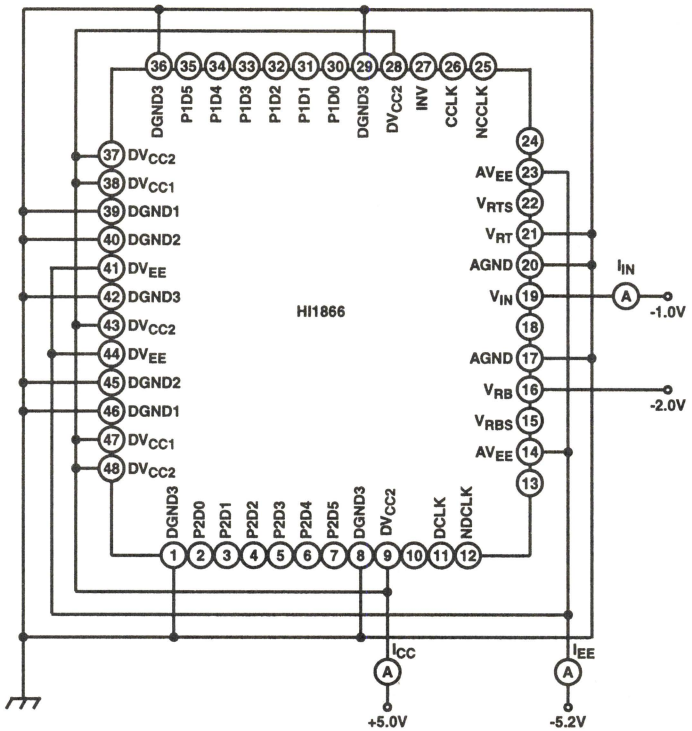


FIGURE 5. CURRENT CONSUMPTION/ANALOG INPUT BIAS TEST CIRCUIT

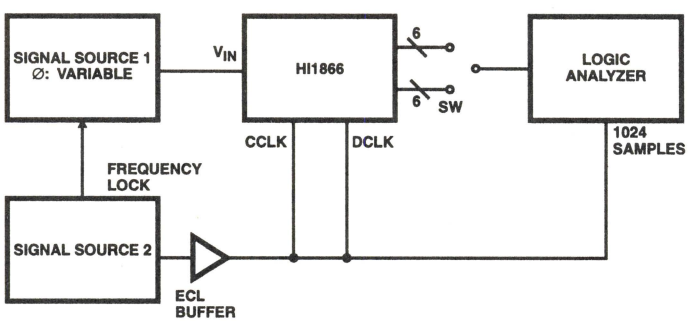


FIGURE 6. SAMPLING DELAY/APERTURE JITTER TEST CIRCUIT

Typical Performance Curves

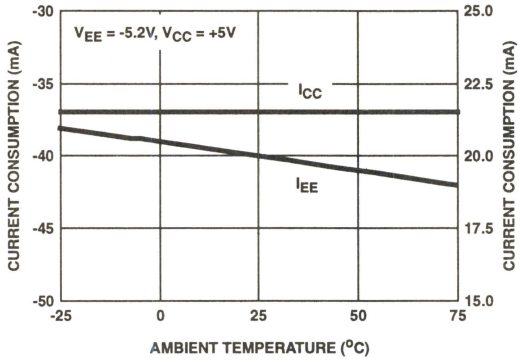


FIGURE 7. CURRENT CONSUMPTION vs AMBIENT TEMPERATURE

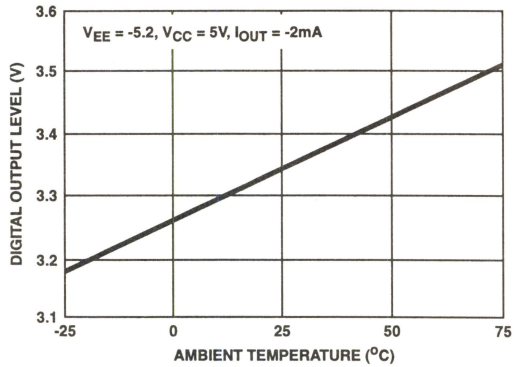


FIGURE 8. V_{OH} vs AMBIENT TEMPERATURE

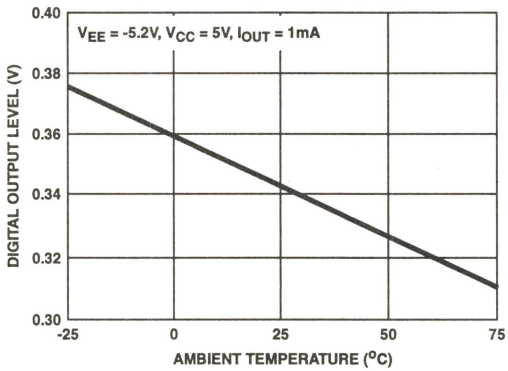


FIGURE 9. V_{OL} vs AMBIENT TEMPERATURE

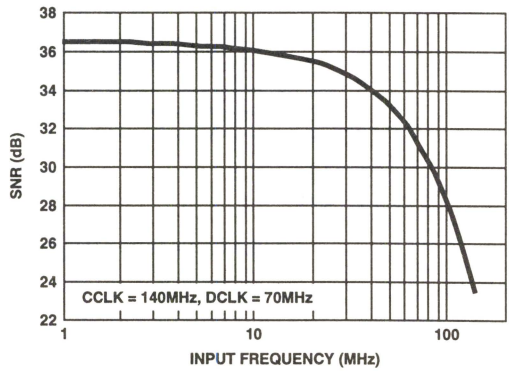


FIGURE 10. SNR vs INPUT FREQUENCY

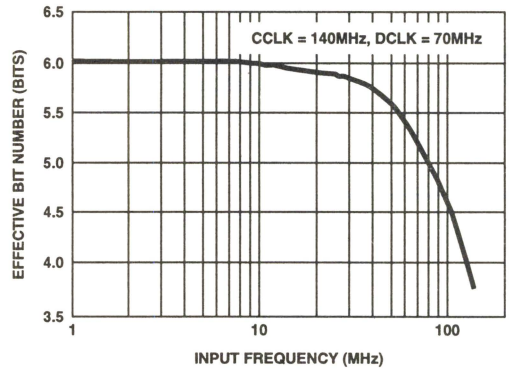


FIGURE 11. EFFECTIVE BIT NUMBER vs INPUT FREQUENCY

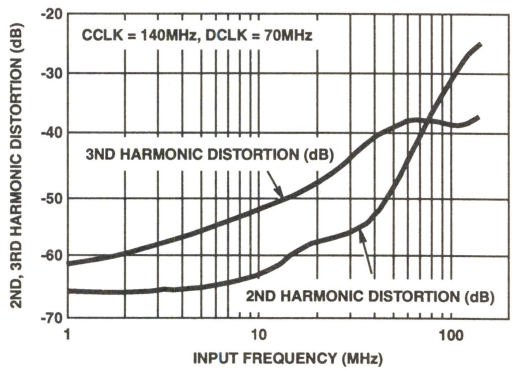


FIGURE 12. 2ND, 3RD HARMONIC DISTORTION vs INPUT FREQUENCY

Notes on Operation

The HI1186 is a high speed A/D converter with ECL level logic input and demultiplexed TT level output. Take notice of the following to ensure optimum performance from this IC.

Power Supply and Grounding

Grounding has a profound influence on converter performance. The higher the frequency is, the more important the way of grounding becomes.

The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using the multi-layer board.

To prevent interference between the AGND and DGND patterns and between the AV_{EE} and DV_{EE} lines, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AV_{EE} and DV_{EE} lines at one point each via a ferrite-bead filter. Shorting analog and digital ground patterns in one place immediately under the A/D converter improves A/D converter performance.

Ground the power supply pins (AV_{EE}, DV_{EE}, DV_{CC}) as close to each pin as possible with a 0.1µF or larger ceramic chip capacitor. (Connect the AV_{EE} pin to the AGND pattern, DV_{EE} to DGND, and DV_{CC} to DGND.)

Analog Input

Make the connection between the V_{IN} pin and the analog input source as short as possible.

There is a slight offset voltage at reference voltage pins V_{RT} and V_{RB}. If it presents no problem in the application, the voltage can be applied directly. However, if the reference voltage is to be set precisely, apply it via a feedback circuit created, using the V_{RTS} and V_{RBS} pins.

Make adequate bypass for high frequency noise at V_{RT} and V_{RB}. The V_{RT} pin is normally connected to AGND on the board. Bypass the V_{RB} pin to the AGND pattern with a 0.1µF or larger ceramic chip capacitor as short as possible. The 10µF tantalum capacitor connected to V_{RB} in the Application Circuit is to stop oscillation in the reference voltage generation circuit.

Digital Input

Noise at the INV pin may cause misoperation of which the cause is extremely hard to identify. If it is okay for the set voltage level to be low only, leave the pin open. If a high level voltage has to be input, bypass the INV pin to DGND with an about 0.1µF ceramic chip capacitor as short as possible. It is recommended that high level input voltage is about -0.5V to -1.0V, and low level input voltage is about -1.6V to -2.5V. When inputting a high level voltage, avoid connecting directly to DGND.

The HI1186 has input pins for two clocks: CCLK and DCLK. For CCLK, which is used for the internal comparator, input an ECL level clock with up to the maximum conversion frequency. For DCLK, which is used for the multiplex output, input an ECL level clock with a rate half that of CCLK. Take notice of the timing between CCLK and DCLK.

It is recommended that differential signals be input to the clock input pins CCLK, NCCLK, DCLK and NDCLK. The A/D converter can be driven only by the clock input pins CCLK and DCLK, but there is a risk of unstable characteristics at maximum speeds.

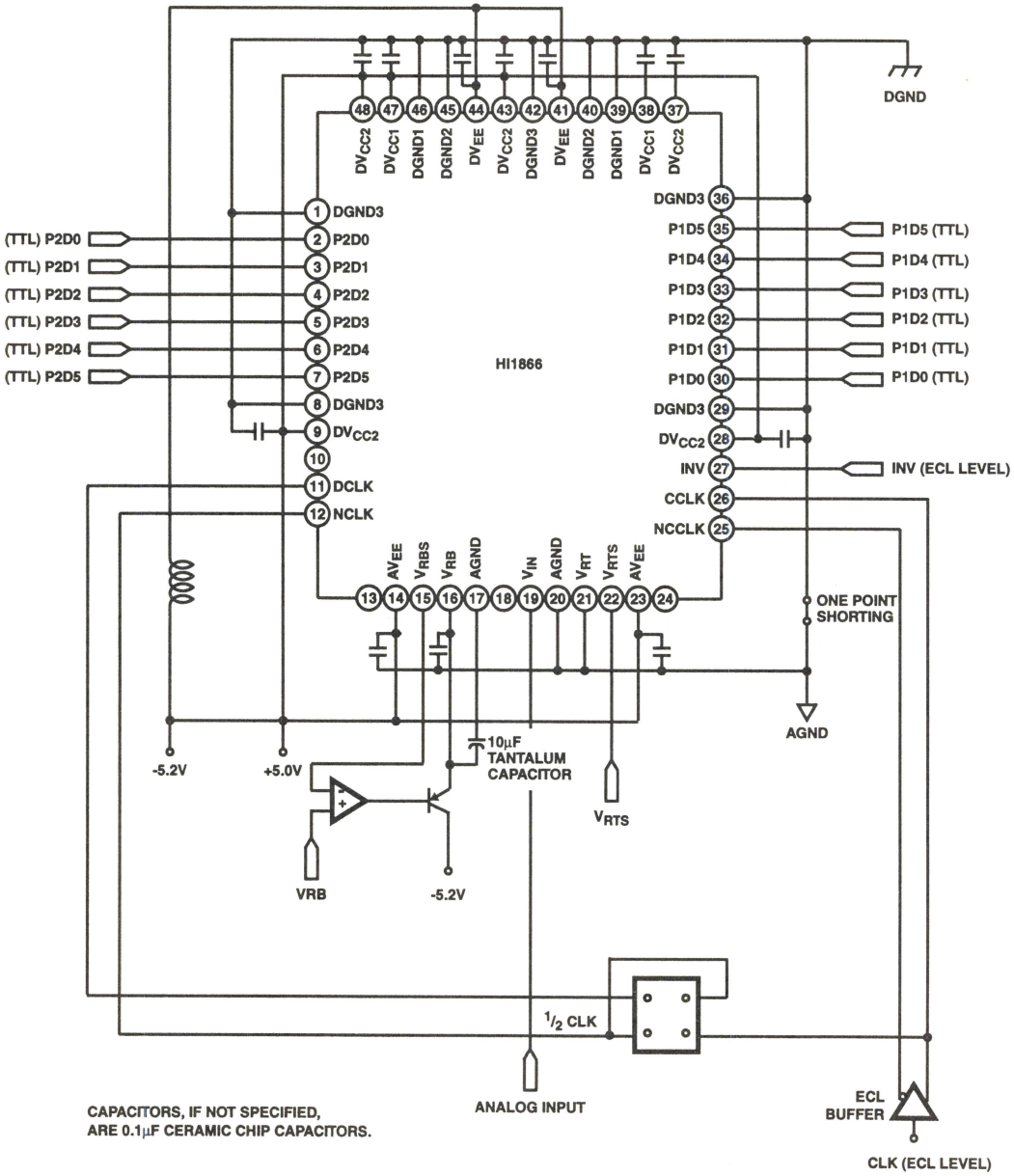
If the NCCLK and NDCLK pins are not used, bypass these pins to DGND with an about 0.1µF capacitor. In this time, about -1.3V voltage is generated at the NCCLK and NDCLK pins. However, this is too weak to be used as threshold voltage V_{BB}; it can not directly drive even one ECL input load.

The clock duty cycle is designed for use at 50%. Any diversion from this percentage will have a slight effect on the maximum performance of the A/D converter, but there is no great need for adjustment.

Digital Output

P1D0 (LSB) to P1D5 (MSB), and P2D0 (LSB) to P2D5 (MSB) are demultiplex digital outputs (2 systems), and are output using the DCLK timing. The polarity of the output data can be inverted using the INV signal.

Typical Application Circuit



HARRIS SEMICONDUCTOR

HI2300

8-Bit, 18 MSPS, Video A/D Converter with 3.3V Power Supply Operation

August 1997

Features

- Resolution ..... 8-Bit $\pm 1/2$ LSB (DL)
- Maximum Sampling Frequency ..... 18 MSPS
- Low Power Consumption at 18 MSPS (Typ) (Reference Current Excluded) 18mW
- Synchronizing Clamp Function
- Clamp ON/OFF Function
- Reference Voltage Self-Bias Circuit
- Input CMOS Compatible
- Three-State TTL Compatible Output
- Power Supply ..... 3.3V Single
- Low Input Capacitance 8pF
- Reference Impedance ..... 330Ω (Typ)
- Direct Replacement for Sony CXD2300

Applications

- Portable Equipment
- Hand-Held Instruments

Description

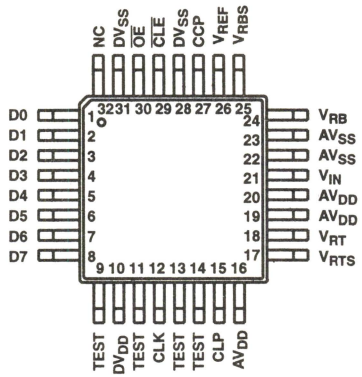
The HI2300 is an 8-bit, CMOS A/D converter for video with synchronizing clamp function and can operate on 3.3V power supply. The adoption of 2 step-parallel method achieves ultra-low power consumption and a maximum conversion speed of 18 MSPS.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI2300JCQ	-40 to 85	32 Ld MQFP	Q32.7x7-S

Pinout

HI2300
(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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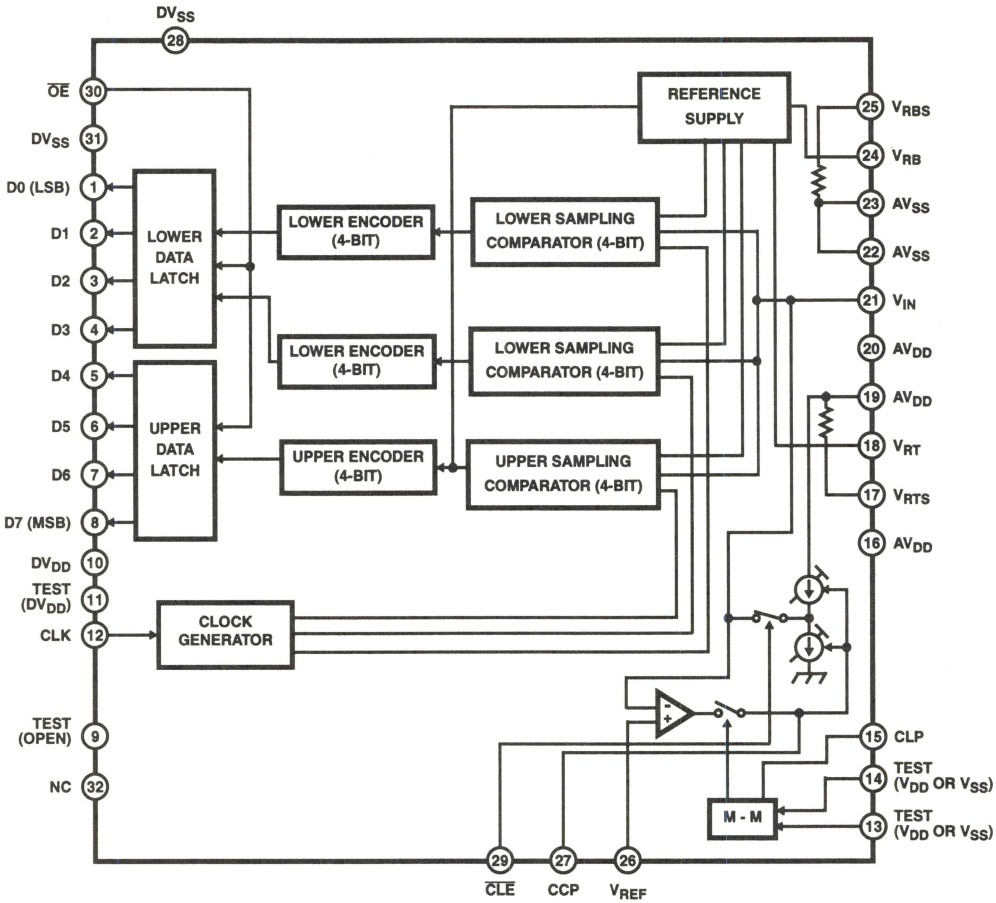
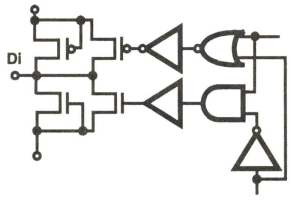
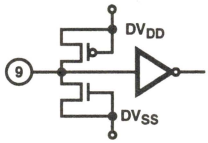
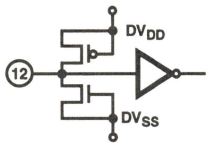
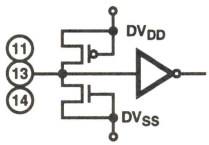
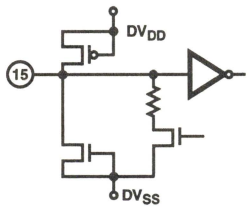
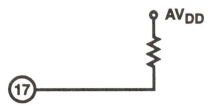
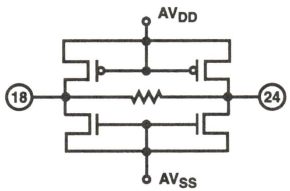
File Number **4103.1**

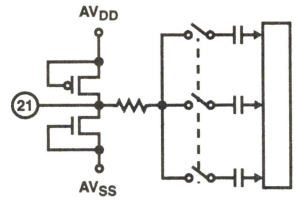
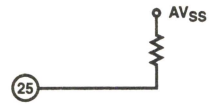
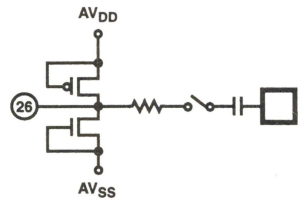
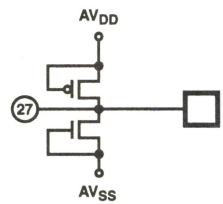
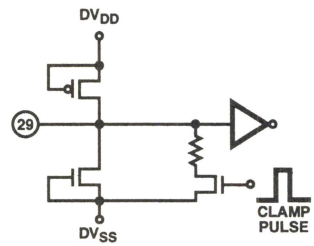
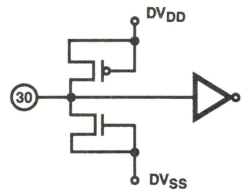
Functional Block Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 8	D0 to D7		D0 (LSB) to D7 (MSB) Output.
9	TEST		Leave open during normal usage.
10	DV_{DD}		Digital +3.3V.
12	CLK		Clock Input.
11, 13, 14	TEST		Fix Pin 11 to V_{DD}, Pins 13 and 14 to V_{DD} or V_{SS} during normal usage.
15	CLP		Inputs Clamp Pulse to Pin 15 (CLP). Clamps the signal voltage during Low interval.
16, 19, 20	AV_{DD}		Analog +3.3V
17	V_{RTS}		Generates approximately +1.8V when shorted with V_{RT}.
18	V_{RT}		Reference Voltage (Top).
24	V_{RB}		Reference Voltage (Bottom).

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
21	V_{IN}		Analog Input.
25	V_{BRS}		Generates approximately +0.4V when shorted with V_{RB}.
26	V_{REF}		Clamp Reference Voltage Input. Clamps so that the reference voltage and the input signal during clamp interval are equal.
27	CCP		Integrates the clamp control voltage. The relationship between the changes in CCP voltage and in V_{IN} voltage is positive phase.
28, 31	DV_{SS}		Digital Ground.
29	$\overline{CLE}$		The clamp function is enabled when $\overline{CLE}$ = Low. The clamp function is set to off and the converter functions as a normal A/D converter when $\overline{CLE}$ = High. The clamp pulse can be measured by connecting $\overline{CLE}$ to DV_{DD} through a several-hundred-ohm resistor.
30	$\overline{OE}$		Data is output when $\overline{OE}$ = Low. Pins D0 to D7 are at high impedance when $\overline{OE}$ = High.
32	NC		No Connect pin.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Reference Voltage (V_{RT}, V_{RB}) ..... V_{DD} +0.5V to V_{SS} - 0.5V
Input Voltage, Analog (V_{IN}) ..... V_{DD} +0.5V to V_{SS} - 0.5V
Input Voltage, Digital (V_{IH}, V_{IL}) ..... V_{DD} +0.5V to V_{SS} - 0.5V
Output Voltage, Digital (V_{OH}, V_{OL}) ..... V_{DD} +0.5V to V_{SS} - 0.5V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP Package 122
Maximum Junction Temperature (Plastic Package) ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(MQFP - Lead Tips Only)

Recommended Operating Conditions

Temperature Range (t_{OPR}) ..... -40^oC to 85^oC
Supply Voltage ($|DV_{SS} - AV_{SS}|$) ..... 0 to 100mV
Power Supply (DV_{DD}, DV_{SS})(AV_{DD}, AV_{SS}) ..... 3.14V to 4.0V
Reference Input Voltage (V_{RB}) 0.4V
(V_{RT}) 1.8V
Analog Input (ADIN) ..... V_{RT} to V_{RB}
Clock Pulse width (t_{PW1}) ..... 27ns (Min)
(t_{PW0}) ..... 27ns (Min)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

When using a single power supply; $f_C = 18$ MSPS, $V_{DD} = 3.3V$, $V_{RB} = 0V$, $V_{RT} = 1.5V$, $T_A = 25^oC$

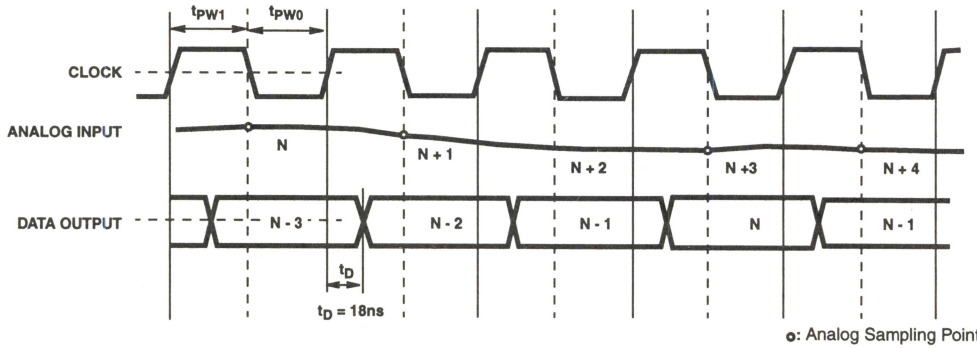
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Conversion Rate	f_C Max	V_{IN} = 0 to 1.5V		18	32	-	MSPS
Minimum Conversion Rate	f_C Min	f_{IN} = 1kHz Ramp		-	32	0.5	MSPS
Supply Current	I_{DD}	f_C = 18 MSPS, NTSC Ramp Wave Input		-	5.5	10	mA
Reference Pin Current	I_{REF}			3.3	4.6	6.6	mA
Analog Input Band Width	BW	$V_{IN} = 1.4V_{P-P}$, 17.9MHz		-	-.9	-	dB
Analog Input Capacitance	C_{IN}	$V_{IN} = 0.75V + 0.07\ V_{RMS}$		-	8	-	pF
Reference Resistance (V_{RT} to V_{RB})	R_{REF}			230	330	440	Ω
Self Bias I	V_{RB1}	Shorts V_{RB} and V_{RBS}		0.33	0.36	0.39	V
	$V_{RT1} - V_{RB1}$	Shorts V_{RT} and V_{RTS}		1.30	1.39	1.48	V
Offset Voltage	E_{OT}			-45	-25	-5	mV
	E_{OB}			40	60	80	mV
Digital Input Voltage	V_{IH}			2.5	-	-	V
	V_{IL}			-	-	0.5	V
Digital Input Current	I_{IH}	V_{DD} = Max	$V_{IH} = V_{DD}$	-	-	5	µA
	I_{IL}		V_{IL} = 0V	-	-	-	µA
Digital Output Current	I_{OH}	$\overline{OE} = V_{SS}$, V_{DD} = Min	$V_{OH} = V_{DD} - 0.5V$	-1.0	-	-	mA
	I_{OL}		V_{OL} = 0.4V	3.3	-	-	mA
Digital Output Current	I_{OZH}	$\overline{OE} = V_{DD}$, V_{DD} = Max	$V_{OH} = V_{DD}$	-	-	16	µA
	I_{OZL}		V_{OL} = 0V	-	-	16	µA
Output Data Delay	t_{DL}	With TTL 1 Gate and 10pF Load		8	18	30	ns
Three-State Output Enable Time	t_{PZH}	$R_L = 1k\Omega$, C_L = 20pF, $\overline{OE}$ = 3V→0V					
	t_{PZL}						
Three-State Output Disable Time	t_{PHZ}	$R_L = 1k\Omega$, C_L = 20pF, $\overline{OE}$ = 0V→3V					
	t_{PLZ}						
Integral Nonlinearity Error	E_L	f_C = 18 MSPS, V_{IN} = 0 to 1.5V		-	+0.5	±1.3	LSB
Differential Nonlinearity Error	E_D	f_C = 18 MSPS, V_{IN} = 0 to 1.5V		-	±0.3	±0.5	LSB
Aperture Jitter	t_{AJ}			-	30	-	ps
Sampling Delay	t_{SD}			-	4	-	ns
Clamp Offset Voltage	E_{OC}	V_{IN} = DC	V_{REF} = 0.5V	-20	0	+20	mV
		PWS = 3µs	V_{REF} = 1.5V	-30	-10	+10	mV
Clamp Pulse Delay	t_{CPD}			-	25	-	ns

Digital Output

The following table shows the relationship between analog input voltage and digital output code.

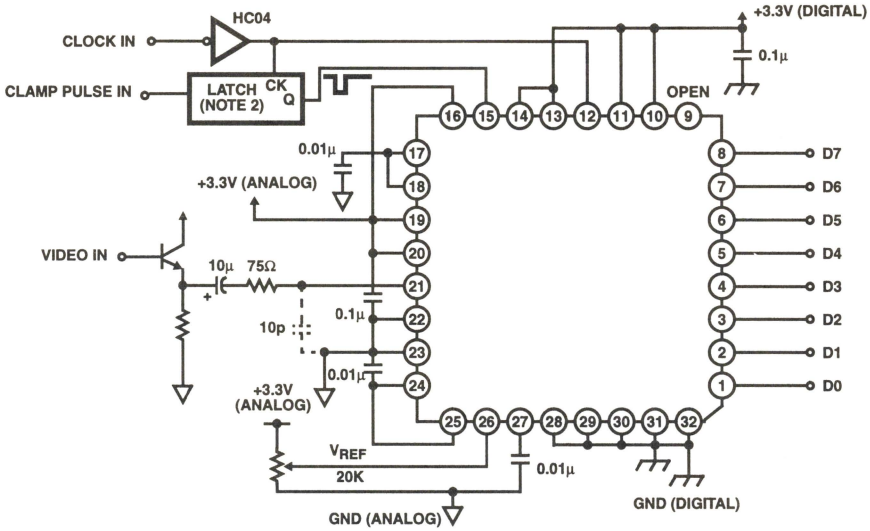
INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB							LSG
V_{RT}	0	1	1	1	1	1	1	1	1
•	•				•				
•	•				•				
•	•				•				
•	127	1	0	0	0	0	0	0	0
•	128	0	1	1	1	1	1	1	1
•	•				•				
•	•				•				
•	•				•				
V_{RB}	255	0	0	0	0	0	0	0	0

Timing Chart



o: Analog Sampling Point

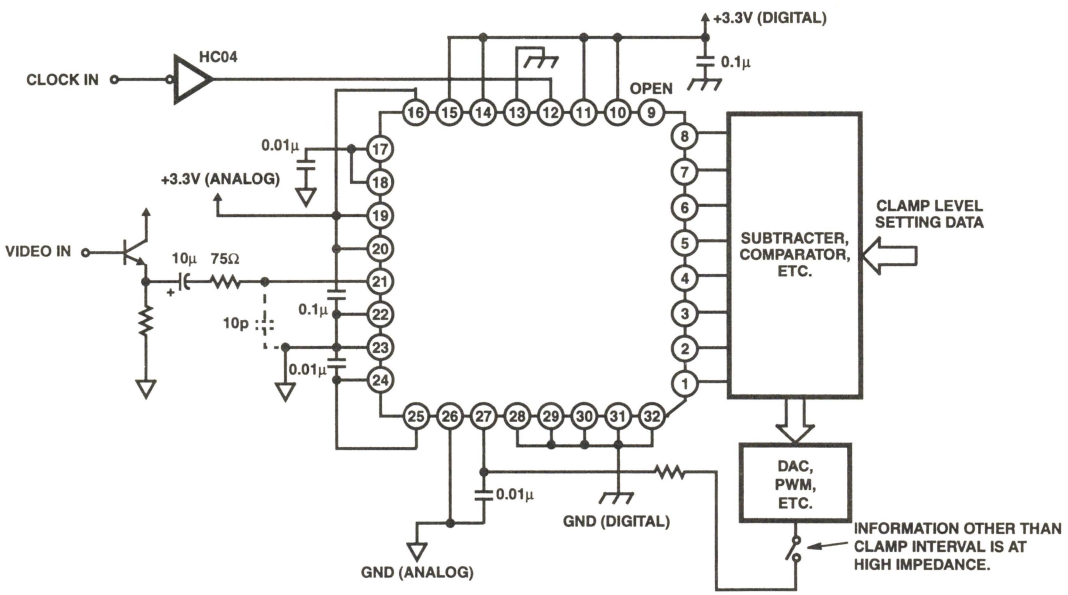
Typical Application Circuits



NOTE:

1. The clamp pulse is latched by the sampling clock of ADC, but that is not necessary for basic clamp operaiotn. However, slight small beat may be generated as Vertical sag according to the relationship between the sampling frequency and the clamp pulse frequency. At such time, the latch circuit is efective in this case.

FIGURE 1. WHEN CLAMP IS USED (SELF BIAS)



NOTES:

2. The relationship between the changes in CCP voltage (Pin 27) and in V_{IN} voltage is positive phase.
3. $\Delta V_{IN}/\Delta V_{CCP} = 3.0$ ($f_S = 20$ MSPS).

FIGURE 2. DIGITAL CLAMP (SELF BIAS)

Typical Application Circuits (Continued)

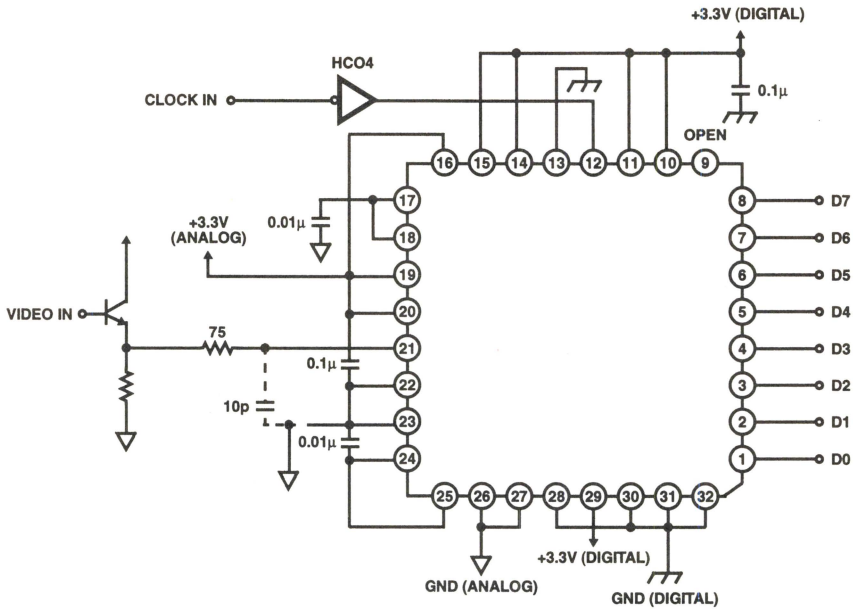


FIGURE 3. WHEN CLAMP IS NOT USED (SELF BIAS)

HARRIS SEMICONDUCTOR

HI2301

8-Bit, 30 MSPS, Video A/D Converter with Amplifier/Clamp

August 1997

Features

- Resolution ..... 8-Bit ±0.5 LSB (DNL)
- Maximum Sampling Frequency ..... 30 MSPS
- Low Power Consumption, 120mW (Including Reference Current)
- Standby Function
- Amplifier Functions
  - Built-In 3x Amplifier (15MHz Band)
  - 2-Input Selector Function Provided
- Built-In Input Clamp Function (DC Restore)
- Clamp ON/OFF Function
- Internal Voltage Reference
- Three-State TTL Compatible Output
- Power Supply .....+5V Single or +4.75/3.3V Dual
- Direct Replacement for Sony CXD2301

Applications

- Desktop Video
- Multimedia
- Video Digitizing
- Image Scanners

Description

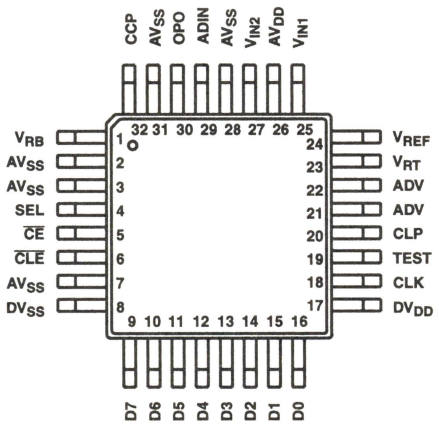
The HI2301 is an 8-bit CMOS analog-to-digital converter for video use that features a sync clamp function and on-chip amplifier. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 30 MSPS.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI2301JCQ	-20 to 75	32 Ld MQFP	Q32.7x7-S

Pinout

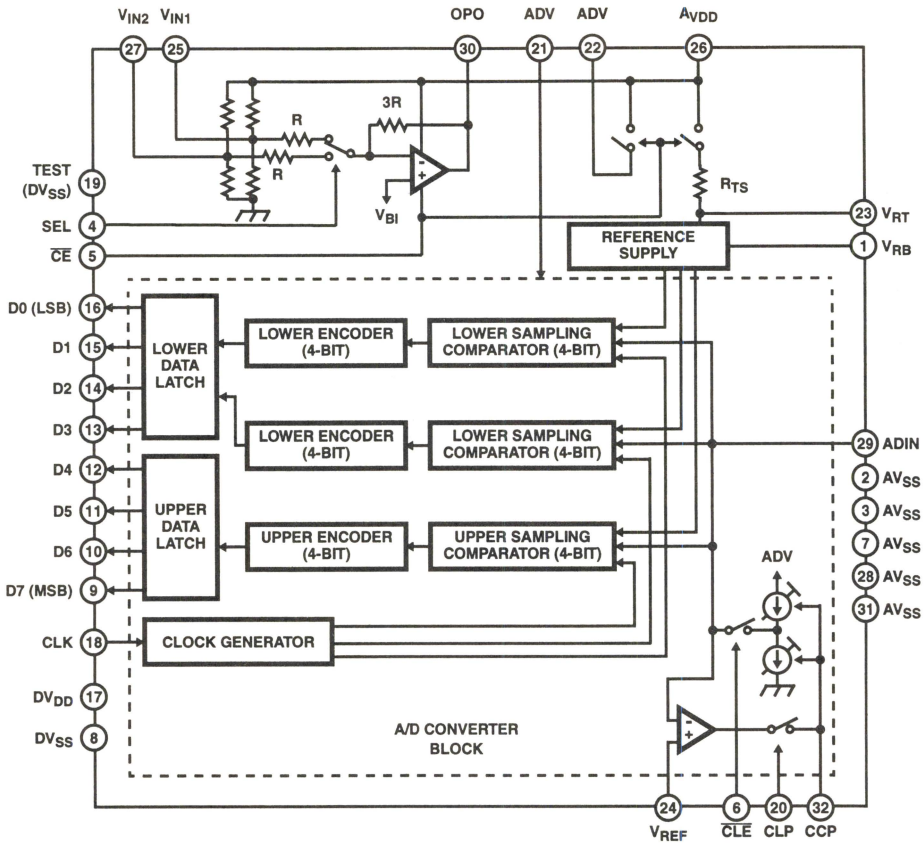
HI2301
(MQFP)
TOP VIEW



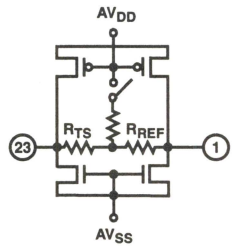
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

File Number 4104.1

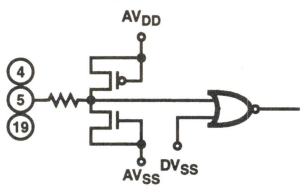
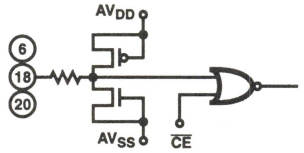
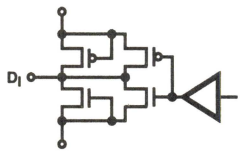
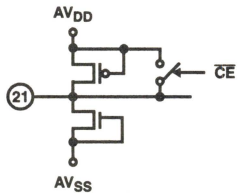
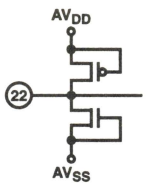
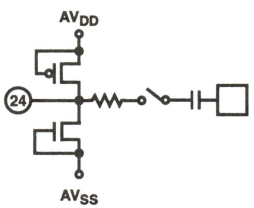
Functional Block Diagram



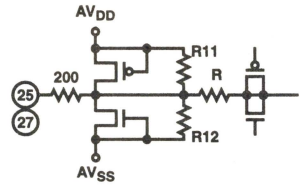
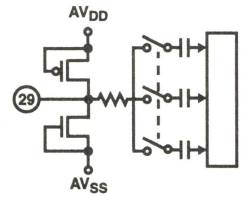
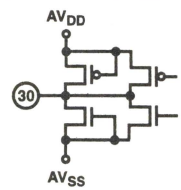
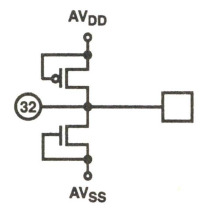
Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1	V_{RB}		Reference voltage (bottom) connect to AV_{SS} for normal use. When another external voltage is input, connect an external 0.1µF capacitor and retain a 1.5V differential compared to the top reference voltage.
23	V_{RT}		Reference voltage (top) by setting V_{RB} to AV_{SS}, outputs approximately 1.5V. Connect only a 0.1µF external by-pass capacitor for normal use. When another external voltage is input, it must be 2.2V or lower.
2, 3, 7, 28, 31	AV_{SS}		Analog GND.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
4	SEL		Switches the input of the 3x amplifier. When SEL is at Low level, V_{IN1} is selected. When SEL is at High level, V_{IN2} is selected.
5	$\overline{CE}$		Standby function ON/OFF selector. In standby state when High.
19	TEST		Fix to V_{SS} for normal use.
6	$\overline{CLE}$		When $\overline{CLE}$ = Low: Clamp function is enabled. When $\overline{CLE}$ = High: Clamp function is disabled, and only the normal A/D converter function is enabled.
18	CLK		Clock Input.
20	CLP		Inputs the clamp pulse to Pin 20 (CLP). Clamps the High interval signal voltage.
8	DV_{SS}		Digital GND.
9 to 16	D_7 to D_0		D_7 (MSB) to D_0 (LSB) output. Outputs Low level in standby. In operation, the phase of D_7 to D_0 output is inverted against the phase of ADIN.
17	D_{VDD}		5V or 3.3V
21	ADV		Short Pins 21 and 22, and connect 0.1µF external capacitor.
22	ADV		
24	V_{REF}		Clamp reference voltage input. Clamps so that the reference voltage and the clamp interval ADIN input signal are equal. The reference voltage is more than 0.5V.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
25	V_{IN1}		Amplifier input pin. Biased internal at 1.9V (when AV_{DD} = 5V) or at 1.8V (when AV_{DD} = 4.75V). When standby as well. When SEL is at Low level, V_{IN1} is selected for input; when SEL is at High level, V_{IN2} is selected for input.
27	V_{IN2}		
26	AV_{DD}		5V or 4.75V
29	ADIN		A/D converter block analog input.
30	OPO		Amplifier Output. The phase of this output is inverted against the phase of $V_{IN1, 2}$. In standby mode, it becomes high-impedance output condition.
32	CCP		Integrates the clamp control voltage. The relationship between the CCP voltage variation and the ADIN voltage is positive phase.

The following table shows the status of the digital output pins when the TEST pin is used with the $\overline{CE}$ and SEL pins.

TEST	CE	SEL	D1	D2	D3	D4	D5	D6	D7	D8
L	L	X	D1	D2	D3	D4	D5	D6	D7	D8
L	H	X	L	L	L	L	L	L	L	L
H	L	X	TEST MODE							
H	H	L	H	L	H	L	H	L	H	L
H	H	H	L	H	L	H	L	H	L	H

Digital Output

The following table shows the correlation between the ADIN input voltage and the digital output code. Take notice that the phase of ADIN input signal voltage is inverted against the phase of the digital output.

ADIN INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB							LSB
V_{RT}	0	0	0	0	0	0	0	0	0
•	•				•				
•	•				•				
•	•				•				
•	127	0	1	1	1	1	1	1	1
•	128	1	0	0	0	0	0	0	0
•	•				•				
•	•				•				
•	•				•				
V_{RB}	255	1	1	1	1	1	1	1	1

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Reference Voltage (V_{RT}, V_{RB}) . . . . . V_{DD} 0.5 to V_{SS} -0.5V
Input Voltage, Analog (V_{IN}) . . . . . V_{DD} 0.5 to V_{SS} -0.5V
Input Voltage, Digital (V_{IH}, V_{IL}) . . . . . V_{DD} 0.5 to V_{SS} -0.5V
Output Voltage, Digital (V_{OH}, V_{OL}) . . . . . V_{DD} 0.5 to V_{SS} -0.5V

Operating Conditions

Supply Voltage (IDV_{SS} - $AV_{SS}I$) . . . . . 0 to 100mV
Single Power Supply (AV_{DD}, DV_{DD}) . . . . . 5.0 ±0.25V
Dual Power Supply (AV_{DD}) . . . . . 4.75 ±0.25V
(DV_{DD}) . . . . . 3.3 ±0.3V
Reference Input Voltage (V_{RB}) . . . . . 0V to 2.2V
(V_{RT}) . . . . . 0V to 2.2V
Analog Input (ADIN) . . . . . More than $1.2V_{P-P}$
Clock Pulse width, t_{PW1} . . . . . 16ns (Min)
t_{PW0} . . . . . 16ns (Min)
Temperature Range (T_{OPR}) . . . . . -20 to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
MQFP Package	122

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Electrical Specifications; When using a single power supply (f_C = 30 MSPS, AV_{DD} = DV_{DD} = +5V, V_{RB} = 0V, V_{RT} = 1.5V, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	$I_{AD} + I_{DD}$	f_C = 35 MSPS, NTSC Ramp Wave Input		-	27	35	mA
Standby Supply Current	I_{STB}	$\overline{CE}$ = DV_{DD}		-	130	200	µA
Max Conversion Rate	f_C Max	V_{IN} = 0V to 1.5V, f_{IN} = 1kHz Ramp		30	-	-	MSPS
Min Conversion Rate	f_C Min			-	-	0.5	MSPS
ADIN Input Band (At -1dB)	BW			-	20	-	MHz
ADIN Input Capacitance	C_{ADIN}	V_{IN} = 0.75V + $0.07V_{RMS}$		-	8	-	pF
Reference Resistance (V_{RT} to V_{RB})	R_{REF}			230	330	440	Ω
Self Bias	V_{RT}	V_{RB} = AV_{SS}		1.38	1.52	1.66	V
Offset Voltage	EOT			-40	-20	0	mV
	EOB			+25	+45	+65	mV
Digital Input Voltage	V_{IH}			3.5	-	-	V
	V_{IL}			-	-	0.5	V
Digital Input Current	I_{IH}	DV_{DD} = Max	V_{IH} = V_{DD}	-	-	5	µA
	I_{IL}		V_{IL} = 0V	-	-	5	µA
Digital Output Current	I_{OH}	DV_{DD} = Min	V_{OH} = V_{DD} - 0.5V	-1.1	-2.5	-	mA
	I_{OL}		V_{OL} = 0.4V	3.7	6.5	-	mA
Output Data Delay	t_{DL}	With TTL 1 Gate and 10pF Load		7	13	25	ns
Integral Nonlinearity Error	E_L	f_C = 30 MSPS, V_{IN} = 0V To 1.5V		-	+0.5	+1.3	LSB
Differential Gain Error	DG	NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS		-	1	-	%
Differential Phase Error	DP			-	0.5	-	Degrees
Aperture Jitter	t_{AJ}			-	30	-	ps
Sampling Delay	t_{SD}			-	2	-	ns
Clamp Offset Voltage	E_{OC}	V_{ADIN} = DC PWS = 3µ	V_{REF} = 0.5V	0	+20	+40	mV
			V_{REF} = 1.5V	-40	-20	0	mV

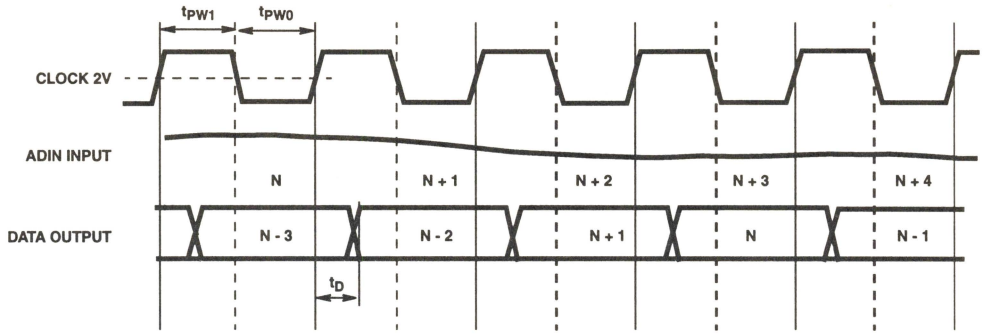
Electrical Specifications Electrical Specifications; When using a single power supply (f_C = 30 MSPS, AV_{DD} = DV_{DD} = +5V, V_{RB} = 0V, V_{RT} = 1.5V, T_A = 25°C **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Clamp Pulse Delay	t_{CPD}		-	25	-	ns
Amplifier Gain		DC To 15MHz	8.5	9.5	10.5	dB
V_{IN1} and V_{IN2} Bias Voltage	$V_{BI1, 2}$	When Open	-	1.9	-	V
V_{IN1} and V_{IN2} Input Resistance	$R_{I1, 2}$		19	27	35	kW
V_{IN1} and V_{IN2} Input Capacitance	$C_{I1, 2}$		-	15	-	pF

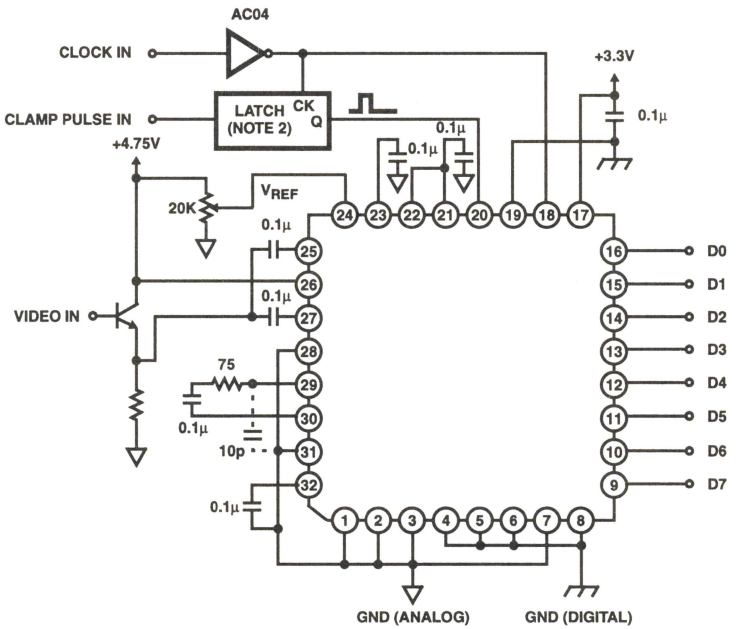
Electrical Specifications When Using a Dual Power Supply (f_C = 30 MSPS, AV_{DD} = DV_{DD} = +5V, V_{RT} = 1.5V, V_{RT} = 1.5V, T_A = 25°C

(2) When Using A Dual Power Supply	f_C = 30 MSPS, AV_{DD} = 4.75V, DV_{DD} = 0V, V_{RT} = 1.5V, T_A = 25°C					
Analog Supply Current	I_{AD}	f_C = 30 MSPS, NTSC Ramp Wave Input	-	24	32	mA
Digital Supply Current	I_{DD}	f_C = 30 MSPS, NTSC Ramp Wave Input	-	1	2	mA
Standby Supply Current	I_{STB}	$\overline{CE}$ = DV_{DD}	-	130	200	µA
Maximum Conversion Rate	f_C Max	V_{IN} = 0 to 1.5V, f_{IN} = 1kHz Ramp	30	-	-	MSPS
Minimum Conversion Rate	f_C Min		-	-	0.5	MSPS
ADIN Input Band (at -1dB)	BW		-	20	-	MHz
ADIN Input Capacitance	C_{ADIN}	V_{IN} = 0.75V + 0.07V_{RMS}	-	8	-	pF
Referenced Resistance (V_{RT} to V_{RB})	R_{REF}		230	330	440	Ω
Self Bias	V_{RT}	V_{RB} = AV_{SS}	1.44	1.52	1.6	V
Offset Voltage	E_{OT}		-40	-20	0	mV
	E_{OB}		+25	+45	+65	mV
Digital Input Voltage	V_{IH}		2.5	-	-	V
	V_{IL}		-	-	0.5	V
Digital Input Current	I_{IH}	DV_{DD} = Max, V_{IH} = DV_{DD}	-	-	5	µA
	I_{IL}	V_{IL} = 0V	-	-	5	µA
Digital Output Current	I_{OH}	DV_{DD} = Min, V_{OH} = V_{DD} -0.5V	-1.1	-2.5	-	mA
	I_{OL}	V_{OL} = 0.4V	3.7	6.5	-	mA
Output Data Delay	t_{DL}	With TTL 1 Gate and 10pF Load	7	13	25	ns
Integral Nonlinearity Error	E_L	f_C = 30 MSPS, V_{IN} = 0 to 1.5V	-	+0.5	+1.3	LSB
Differential Nonlinearity Error	E_D	f_C = 30 MSPS, V_{IN} = 0 to 1.5V	-	0.3	0.5	LSB
Differential Gain Error	DG	NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS	-	1	-	%
Differential Phase Error	DP		-	0.5	-	deg
Aperture Jitter	t_{AJ}		-	30	-	ps
Sampling delay	t_{SD}		-	2	-	ns
Clamp Offset Voltage	E_{OC}	V_{IN} = DC, PWS = 3µs, V_{REF} = 0.5V	0	+20	+40	mV
		V_{REF} = 1.5V	-40	-20	0	mV
Clamp Pulse Delay	t_{CPD}		-	25	-	ns
3x Amplifier Gain		DC to 15MHz	8.5	9.5	10.5	dB
V_{IN1} and V_{IN2} Bias Voltage	$V_{BI1, 2}$	When Open	-	1.8	-	V
V_{IN1} and V_{IN2} Input Resistance	$R_{I1, 2}$		19	27	35	kΩ
V_{IN1} and V_{IN2} Input Capacitance	$C_{I1, 2}$		-	15	-	pF

Timing Chart



Application Circuits

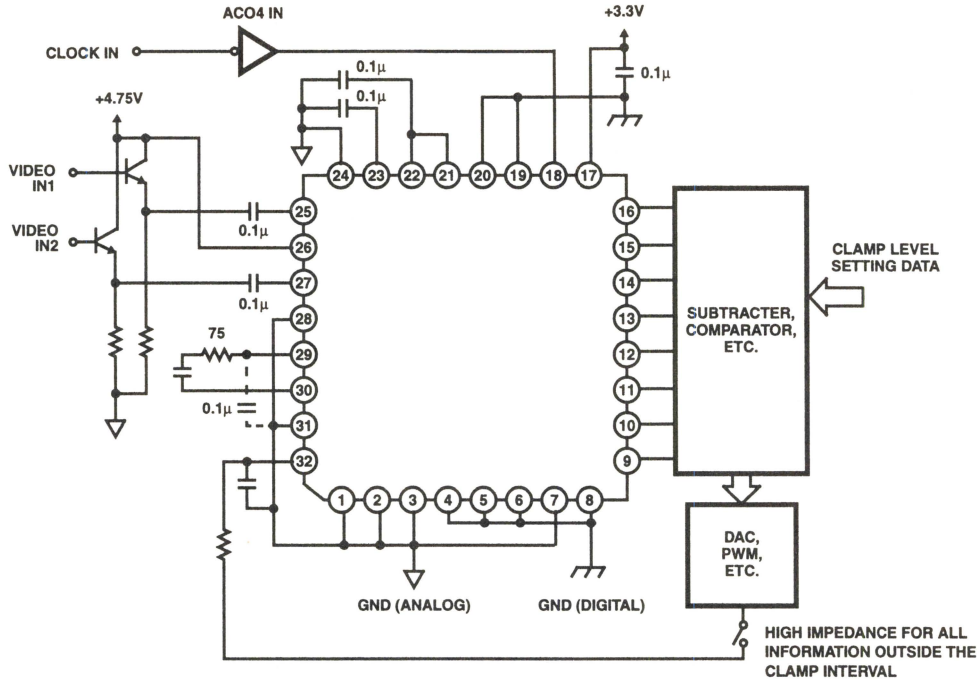


NOTE:

2. Although the ADC sampling clock latches the clamp pule, it is not needed for basic clamp operation. However, depending on the relationship between the sampling frequency and the clamp pulse frequency, a small beat might be generated as V_{SAG}. The latch circuit is valid at this time.

FIGURE 1. CLAMP USAGE EXAMPLE (USING SELF BIAS, CIRCUIT WHEN USING THE INTERNAL AMPLIFIER)

Application Circuits (Continued)



NOTES:

3. The relationship between the CCP voltage (Pin 32) variation and the ADIN voltage variation is position phase.
4. $\Delta ADIN/\Delta V_{CCP} = 3.0$ ($f_S = 30$ MSPS).

FIGURE 2. DIGITAL CLAMP USAGE EXAMPLE (USING SELF BIAS), CIRCUIT WHEN USING THE INTERNAL AMPLIFIER

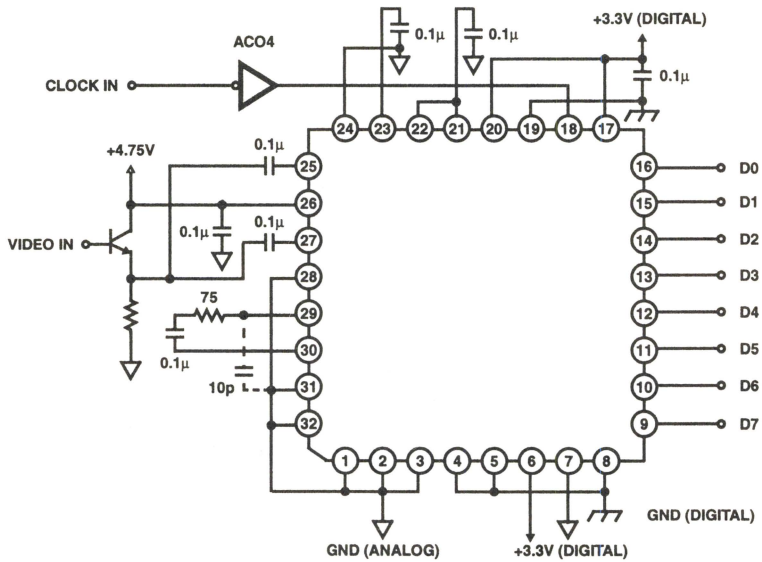
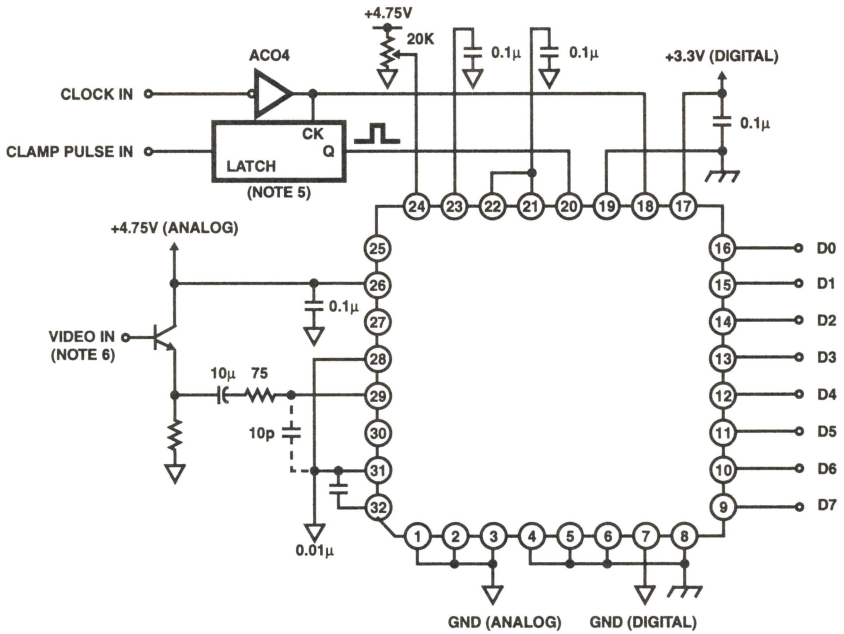


FIGURE 3. WHEN NOT USING THE CLAMP, CIRCUIT WHEN USING THE INTERNAL AMPLIFIER

Application Circuits (Continued)

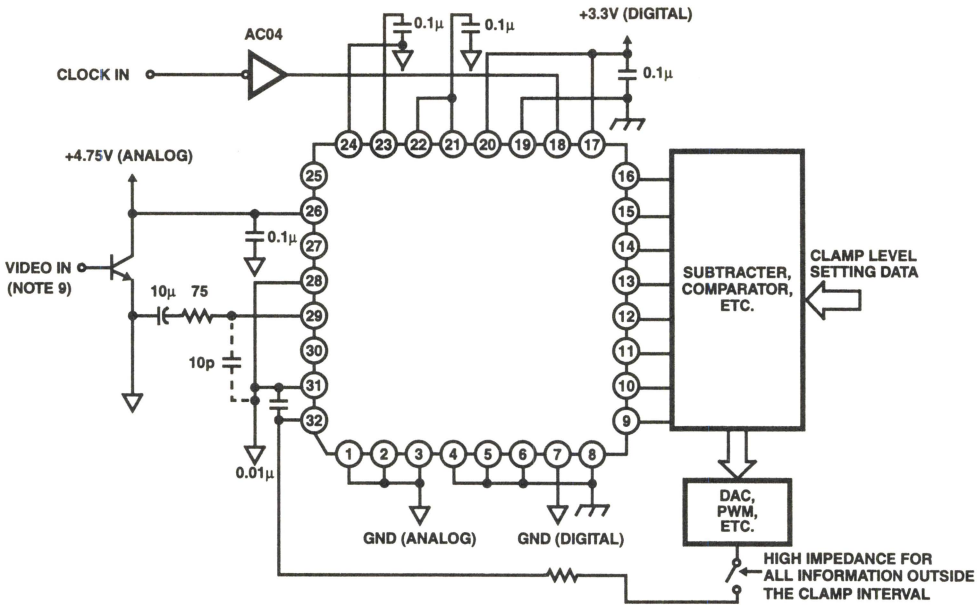


NOTES:

5. Although the ADC sampling clock latches the clamp pulse, it is not needed for basic clamp operation. However, depending on the relationship between the sampling frequency and the clamp pulse frequency, a small abeat might be generated as V_{SAG}. The latch circuit is valid at this time.
6. Take care that the phase of ADIN input is inverted against the phase of the digital output, because the use of the built-in inverting amplifier is standard. (Refer to "Digital Output".)

FIGURE 4. CLAMP USAGE EXAMPLE WHEN NOT USING THE INTERNAL AMPLIFIER

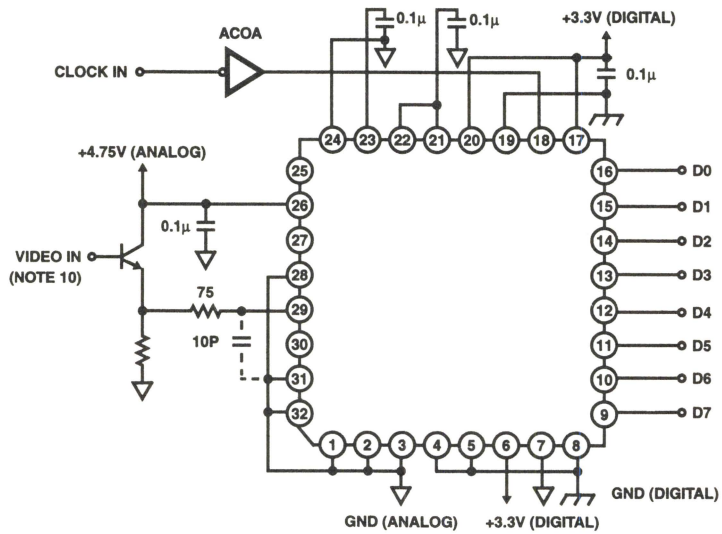
Application Circuits (Continued)



NOTES:

7. The relationship between the CCP voltage (Pin 32) variation and the ADIN voltage variation is positive phase.
8. $\Delta V_{ADIN}/\Delta V_{CCP} = 3.0$ ($f_S = 20$ MSPS).
9. Take care that the phase of ADIN input is inverted against the phase of the digital output, because the use of the built-in inverting amplifier is standard. (Refer to "Digital Output.")

FIGURE 5. DIGITAL CLAMP USAGE EXAMPLE



NOTE:

10. Take care that the phase of ADIN input is inverted against the phase of the digital output, because the use of the built-in inverting amplifier is standard. (Refer to "Digital Output".)

FIGURE 6. WHEN NOT USING THE CLAMP

Typical Performance Curves

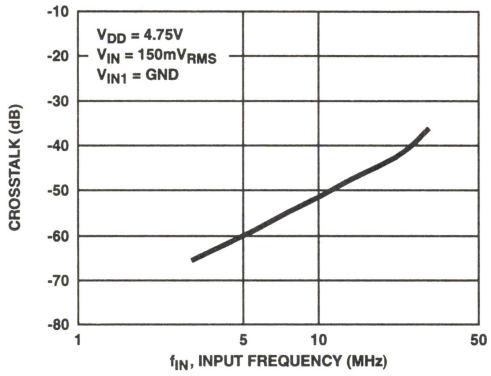


FIGURE 7. INPUT FREQUENCY OF V_{IN2} vs CROSSTALK $V_{IN2} \rightarrow V_{IN1}$

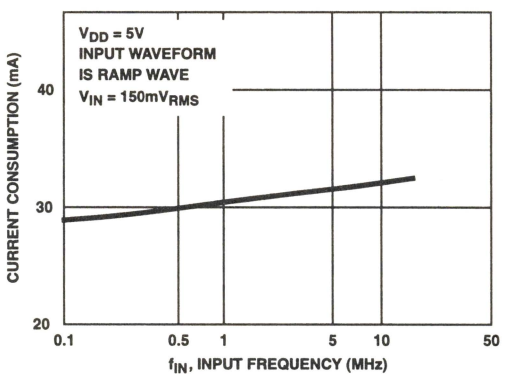


FIGURE 8. INPUT FREQUENCY vs CURRENT CONSUMPTION

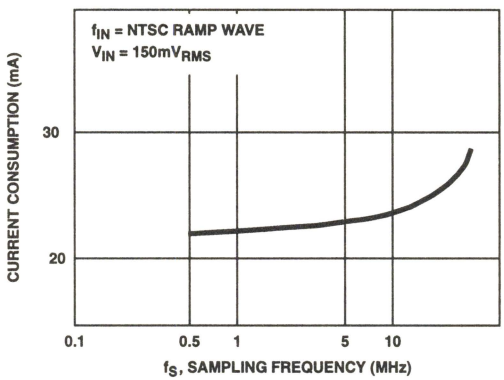


FIGURE 9. SAMPLING FREQUENCY vs CURRENT CONSUMPTION

HARRIS SEMICONDUCTOR

HI2302

8-Bit, 50 MSPS, Video A/D Converter with Clamp Function

August 1997

Features

- Resolution ..... 8-Bit ±0.5 LSB (DNL)
- Maximum Sampling Frequency ..... 50 MSPS
- Low Power Consumption .....125mW (Reference Current Excluded)
- Built-In Input Clamp Function (DC Restore)
- Clamp ON/OFF Function
- Internal Voltage Reference
- Input CMOS/TTL Compatible
- Three-State TTL Compatible Output
- Power Supply .....+5V Single or +5V/3.3V Dual
- Direct Replacement for Sony CXD2302Q

Applications

- Video Digitizing
- Wireless Receivers
- LCD Projectors/Panels
- Cable Modems
- RGB Graphics Processing
- Camcorders
- Instrumentation

Description

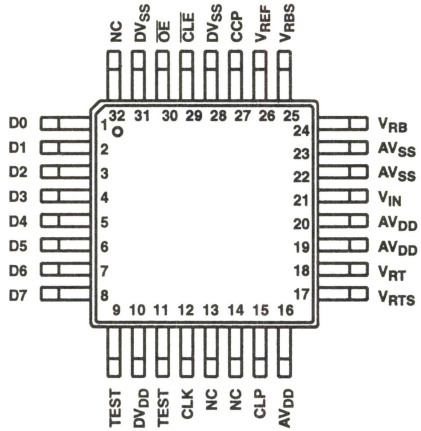
The HI2302 is an 8-bit CMOS A/D Converter for video with synchronizing clamp function. The adoption of two-step parallel method achieves low power consumption and a maximum conversion rate of 50 MSPS. For pin compatible lower sample rate converters refer to HI1179 (35 MSPS) or HI1176 (20 MSPS) data sheets.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI2302JCQ	-40 to 85	32 Ld MQFP	Q32.7x7-S

Pinout

HI2302 (MQFP)
TOP VIEW

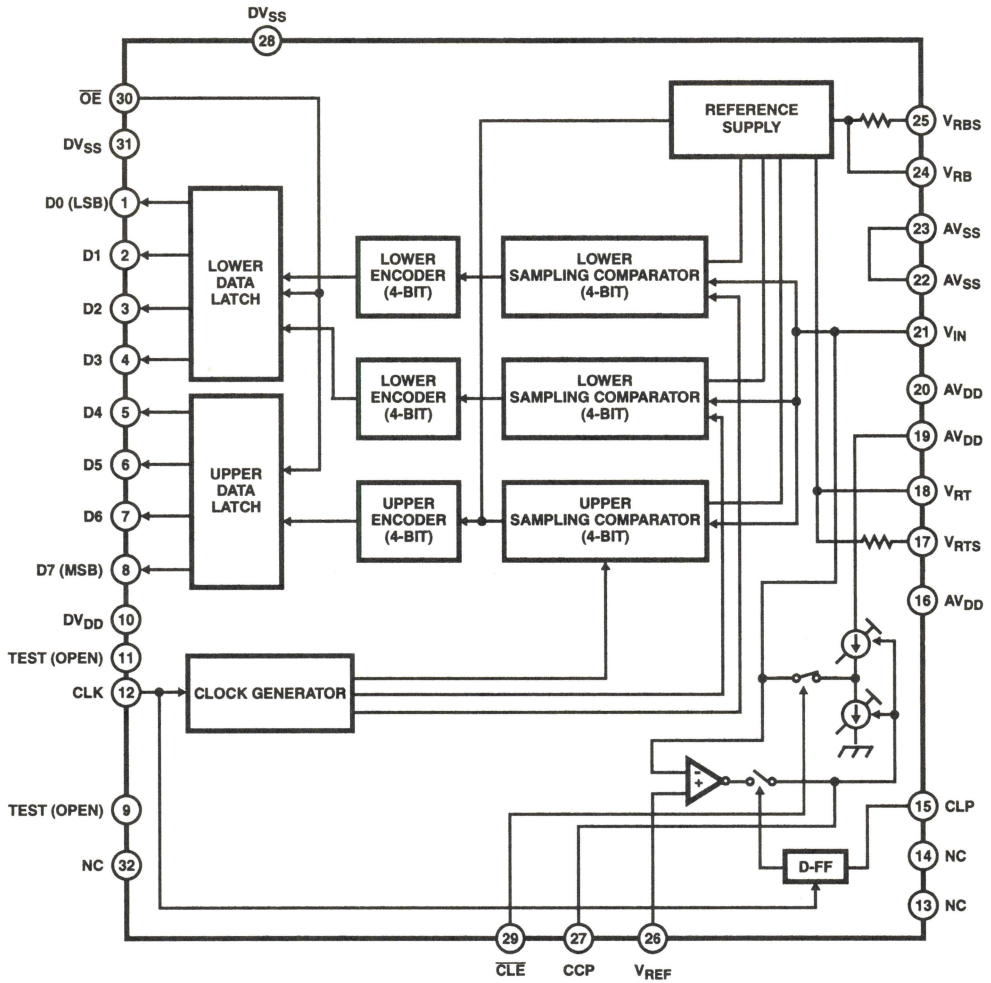


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1997

File Number **4105.1**

Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Reference Voltage (V_{RT}, V_{RB}) . . . . . V_{DD} +0.5 to V_{SS} -0.5V
Input Voltage (Analog) (V_{IN}) . . . . . V_{DD} +0.5 to V_{SS} -0.5V
Input Voltage (Digital) (V_I) . . . . . V_{DD} +0.5 to V_{SS} -0.5V
Output Voltage (Digital) (V_O) . . . . . V_{DD} +0.5 to V_{SS} -0.5V

Operating Conditions

Supply Voltage (AV_{DD}, AV_{SS}) . . . . . 4.75 to 5.25V
(DV_{DD}, DV_{SS}) . . . . . 3.0 to 5.5V
($|DV_{SS}$-$AV_{SS}|$) . . . . . 0 to 100mV
Reference Input Voltage
(V_{RB}) . . . . . 0 and Above V
(V_{RT}) . . . . . 2.7 and Below V
Analog Input (V_{IN}) . . . . . $1.7V_{P-P}$ Above
Clock Pulse Width (t_{PW1}, t_{PW0}) . . . . . 10ns (Min)
Ambient Temperature (T_{OPR}) . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP Package 122
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -55^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications f_C = 50 MSPS, AV_{DD} = 5V, DV_{DD} = 3 to 5.5V, V_{RB} = 0.5V, V_{RT} = 2.5V, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS		NOTES	MIN	TYP	MAX	UNITS
ANALOG CHARACTERISTICS								
Maximum Conversion Rate	f_C Max	AV_{DD} = 4.75 to 5.25V, T_A = 20 to 75^oC, V_{IN} = 0.5 to 2.5V, f_{IN} = 1kHz Triangular Wave			50	65	-	MSPS
Minimum Conversion Rate	f_C Min				-	-	0.5	MSPS
Input Bandwidth Full Scale	BW	Envelope R_{IN} = 33Ω	-1dB		-	60	-	MHz
			-3dB		-	100	-	MHz
Differential Nonlinearity Error	E_D	End Point			-	±0.3	0.5	LSB
Integral Nonlinearity Error	E_L				-	+0.7	1.5	LSB
Offset Voltage	E_{OT}	Potential Difference to V_{RT}		Note 2	-70	-50	-30	mV
	E_{OB}	Potential Difference to V_{RB}			20	40	60	mV
Differential Gain Error	DG	NTSC 40 IRE Mod Ramp f_C = 14.3 MSPS			-	3	-	%
Differential Phase Error	DP				-	1.5	-	Degrees
Sampling Delay	t_{SD}				-	0	-	ns
Clamp Offset Voltage	E_{OC}	V_{IN} = DC, C_{IN} = 10µF t_{PCW} = 2.75µs, f_C = 14.3 MSPS, f_{CLP} = 15.75kHz	V_{REF} = 0.5V		0	20	40	mV
			V_{REF} = 2.5V		0	20	40	mV
Signal-To-Noise Ratio	SNR	f_{IN} = 100kHz			-	45	-	dB
		f_{IN} = 500kHz			-	44	-	dB
		f_{IN} = 1MHz			-	44	-	dB
		f_{IN} = 3MHz			-	43	-	dB
		f_{IN} = 10MHz			-	38	-	dB
		f_{IN} = 25MHz			-	32	-	dB
Spurious Free Dynamic	SFDR	f_{IN} = 100kHz			-	51	-	dB
		f_{IN} = 500kHz			-	46	-	dB
		f_{IN} = 1MHz			-	49	-	dB
		f_{IN} = 3MHz			-	46	-	dB
		f_{IN} = 10MHz			-	45	-	dB
		f_{IN} = 25MHz			-	45	-	dB

Electrical Specifications f_C = 50 MSPS, AV_{DD} = 5V, DV_{DD} = 3 to 5.5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		NOTES	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS f_C = 50 MSPS, AV_{DD} = 5V, DV_{DD} = 5V or 3.3V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C								
Supply Current	$I_{AD} + I_{DD}$	NTSC Ramp, Wave Input, $\overline{CLE}$ = 0V	DV_{DD} = 5V		-	25	36	mA
Analog	I_{AD}		DV_{DD} = 3.3V		-	23	33	mA
Digital	I_{DD}				-	2	3	mA
Reference Current	I_{REF}				4.1	5.4	7.7	mA
Reference Resistance (V_{RT} - V_{RB})	R_{REF}				260	370	480	Ω
Self-Bias Voltage	V_{RB}	Shorts V_{RTS} and A_{VDD} Shorts V_{RBS} and A_{VSS}			0.52	0.56	0.60	V
	V_{RT} - V_{RB}				1.80	1.92	2.04	V
Input Capacitance	C_{AI1}	V_{IN}, V_{IN} = 1.5V + 0.07V_{RMS}			-	15	-	pF
	C_{AI2}	V_{RTS}, V_{RT}, V_{RB}, V_{RBS}, V_{REF}			-	-	11	pF
	C_{DIN}	TEST, CLK, CLP, $\overline{CLE}$, $\overline{OE}$			-	-	11	pF
Output Capacitance	C_{AO}	CCP			-	-	11	pF
	C_{DO}	D0 to D7, TEST			-	-	11	pF
Digital Input Voltage	V_{IH}	AV_{DD} = 4.75 to 5.25V, DV_{DD} = 3 to 5.5V, T_A = -20°C to 75°C			2.2	-	-	V
	V_{IL}				-	-	0.8	V
Digital Input Current	I_{IH} I_{IL}	V_I = 0V to AV_{DD}, T_A = 20°C to 75°C	CLK		-240	-	240	µA
			TEST, CLP, $\overline{CLE}$		-240	-	40	µA
			$\overline{OE}$		-40	-	240	µA
Digital Output Current	I_{OH}	$\overline{OE}$ = 0V, DV_{DD} = 5V T_A = 20°C to 75°C	V_{OH} = DV_{DD} - 0.8V		-	-	-2	mA
	I_{OL}		V_{OL} = 0.4V		4	-	-	mA
	I_{OH}	$\overline{OE}$ = 0V DV_{DD} = 3.3V T_A = -20°C to 75°C	V_{OH} = DV_{DD} - 0.8V		-	-	-1.2	mA
	I_{OL}		V_{OL} = 0.4V		2.4	-	-	mA
	I_{OZH}	$\overline{OE}$ = 3V DV_{DD} = 3 to 5.5V T_A = -20°C to 75°C	V_{OH} = DV_{DD}		-40	-	40	µA
	I_{OZL}		V_{OL} = 0V		-40	-	40	µA
TIMING f_C = 50 MSPS, AV_{DD} = 5V, DV_{DD} = 5V or 3.3V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C								
Output Data Delay	t_{PZH}	CL = 15pF $\overline{OE}$ = 0V	DV_{DD} = 5V		5.5	9.5	12.0	ns
	t_{PHL}					8.5		ns
	t_{PLH}		DV_{DD} = 3.3V		4.3	11.8	16.3	ns
	t_{PHL}					7.6		ns
Three-State Output Enable Time	t_{PZH}	R_L = 1kΩ C_L = 15pF $\overline{OE}$ = 3V→0V	DV_{DD} = 5V		2.5	4.5	8.0	ns
	t_{PZL}					6.0		ns
	t_{PZH}		DV_{DD} = 3.3V		3.0	7.0	9.0	ns
	t_{PZL}					5.0		ns
Three-State Output Enable Time	t_{PHZ}, t_{PLZ}	R_L = 1kΩ, C_L = 15pF $\overline{OE}$ = 3V→0V	DV_{DD} = 5V		3.5	5.5	7.5	ns
	t_{PZH}, t_{PZL}		DV_{DD} = 3.3V		2.5	5.5	8.0	ns
Clamp Pulse Width	t_{CPW}	f_C = 14.3MHz, C_{IN} = 10µF for NTSC Wave		Note 4	1.75	2.75	3.75	µs

NOTES:

2. The offset voltage E_{OB} is a potential difference between V_{RB} and a point of position where the voltage drops equivalent to $^1/_2$ LSB of the voltage when the output data changes from "00000000" to "00000001". E_{OT} is a potential difference between V_{RT} and a potential point where the voltage rises equivalent to $^1/_2$ LSB of the voltage when the output data changes from "11111111" to "11111110".
3. The voltage of up to (AV_{DD} + 0.5V) can be input when DV_{DD} = 3.3V. But the output pin voltage is less than the DV_{DD} voltage. When the digital output is in the high impedance mode, the IC may be damaged by applying the voltage which is more than the (DV_{DD} + 0.5V) voltage to the digital output.
4. The clamp pulse width is for NTSC as an example. Adjust the rate to the clamp pulse cycle (1/15.75kHz for NTSC) for other processing systems to equal the values for NTSC.

Timing Diagrams

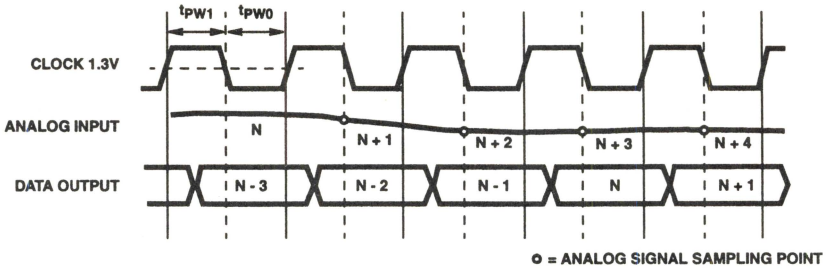


FIGURE 1A. TIMING CHART

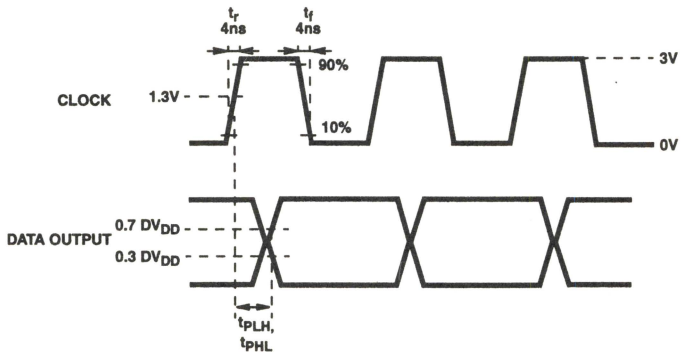


FIGURE 1B. TIMING CHART

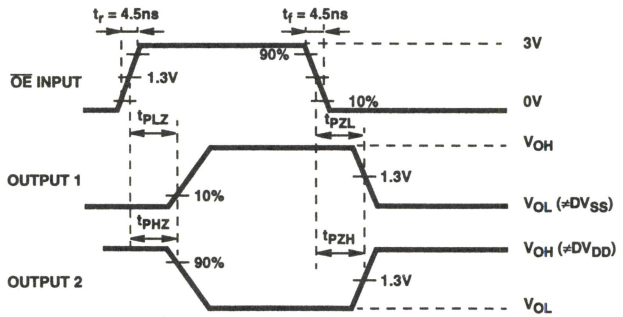


FIGURE 1C. TIMING CHART

Timing Diagrams (Continued)

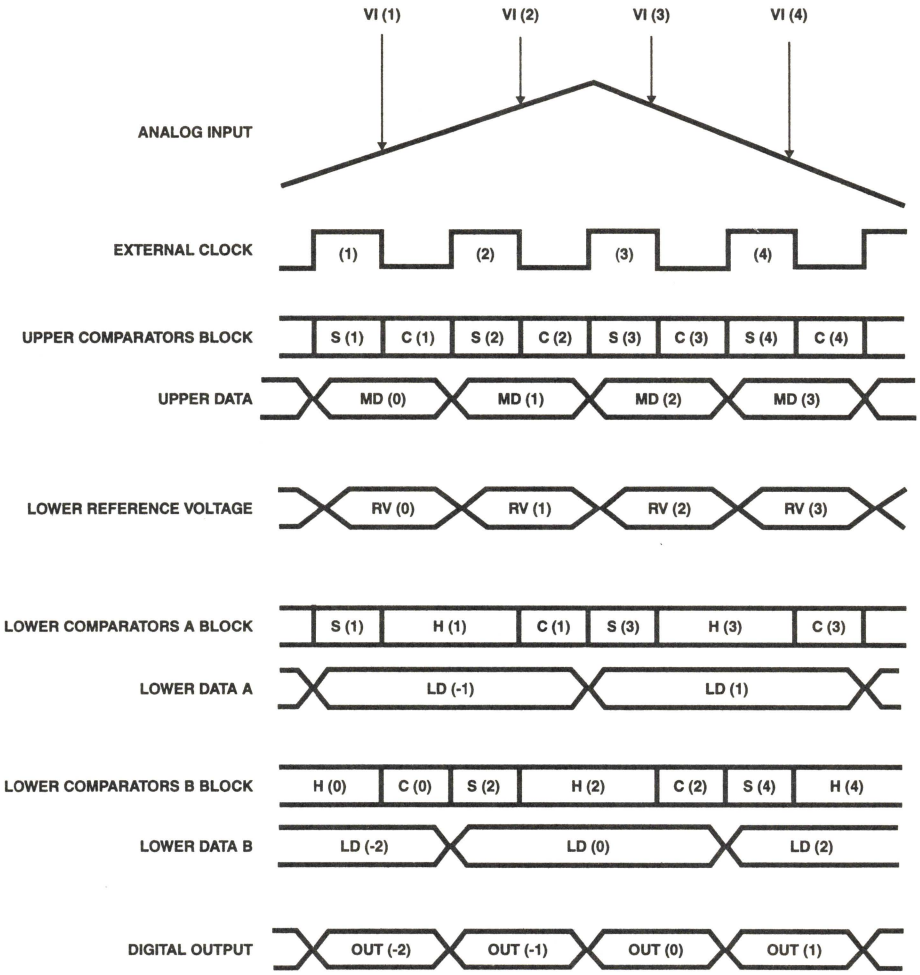
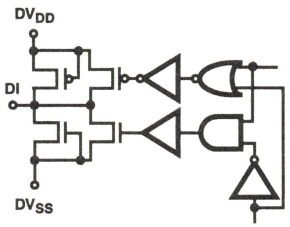
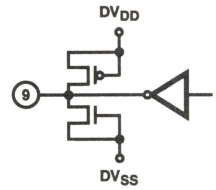
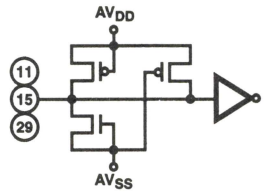
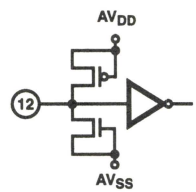
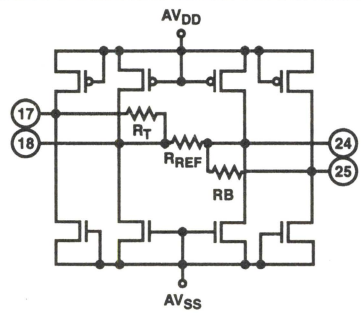
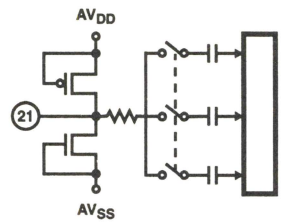


FIGURE 1D. TIMING CHART II

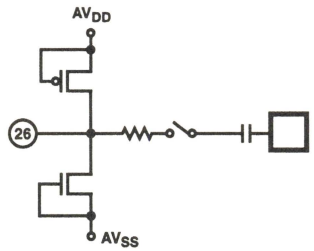
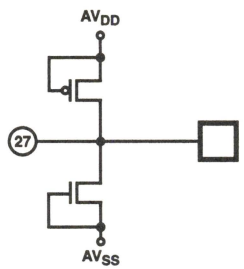
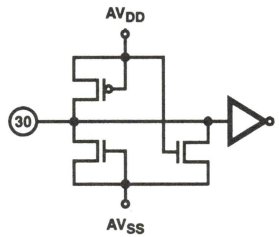
Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 8	D0 to D7		D0 (LSB) to D7 (MSB) Output.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
9	TEST		Leave open for normal use.
10	DV_{DD}		Digital Power Supply +5V or +3.3V.
11	TEST		Leave open for normal use. Pull-up resistor is built in.
15	CLP		Input for the clamp pulse. Clamps the signal voltage during low interval. Pull-up resistor is built in.
29	$\overline{CLE}$		The clamp function is enabled when $\overline{CLE}$ = Low. The clamp function is off and the device functions as a normal A/D converter when $\overline{CLE}$ = High. Pull-up resistor is built in.
12	CLK		Clock Input. Set to Low level when no clock is input.
13, 14, 32	NC		
16, 19, 20	AV_{DD}		Analog Power Supply +5V.
17	V_{RTS}		Generates approximately +2.5V when shorted with AV_{DD}.
18	V_{RT}		Reference Voltage (Top).
24	V_{RB}		Reference Voltage (Bottom).
25	V_{RBS}		Generates approximately +0.6V when shorted with AV_{SS}.
21	V_{IN}		Analog Input.

Pin Descriptions (Continued)

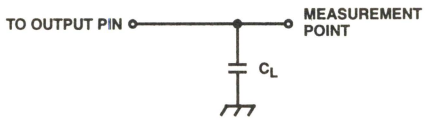
PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
22, 23	AV_{SS}		Analog Ground.
26	V_{REF}		Clamp Reference Voltage Input. Clamps so that the reference voltage and the input signal during clamp interval are equal.
27	CCP		Integrates the clamp control voltage. The relationship between the changes in CCP voltage and in V_{IN} voltage is positive phase.
28, 31	DV_{SS}		Digital Ground.
30	$\overline{OE}$		Data is output when $\overline{OE}$ = Low. Pins D0 to D7 are at high impedance when $\overline{OE}$ = High. Pull-down resistor is built in.

Digital Output

The following table shows the relationship between analog input voltage and digital output code.

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB							LSB
V_{RT}	0	1	1	1	1	1	1	1	1
•	•				•				
•	•				•				
•	•				•				
•	127	1	0	0	0	0	0	0	0
•	128	0	1	1	1	1	1	1	1
•	•				•				
•	•				•				
•	•				•				
V_{RB}	255	0	0	0	0	0	0	0	0

Electrical Specifications Measurement Circuits



NOTE: C_L includes capacitance of probes.

FIGURE 2. OUTPUT DATA DELAY MEASUREMENT CIRCUIT

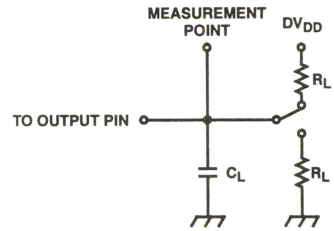


FIGURE 3. THREE-STATE OUTPUT MEASUREMENT CIRCUIT

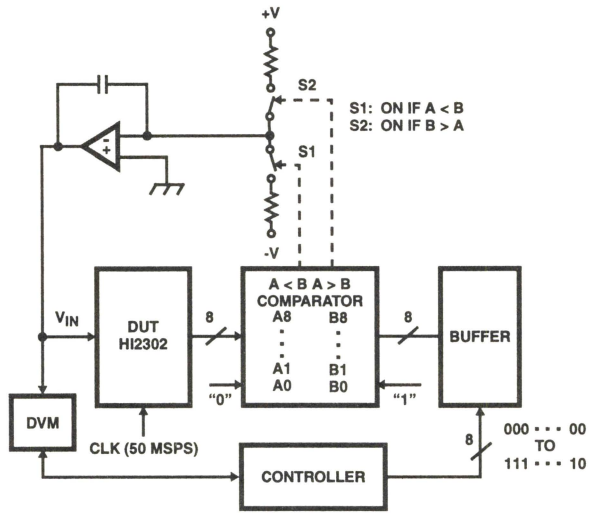


FIGURE 4. INTEGRAL NONLINEARITY ERROR/DIFFERENTIAL NONLINEARITY ERROR/OFFSET VOLTAGE TEST CIRCUIT

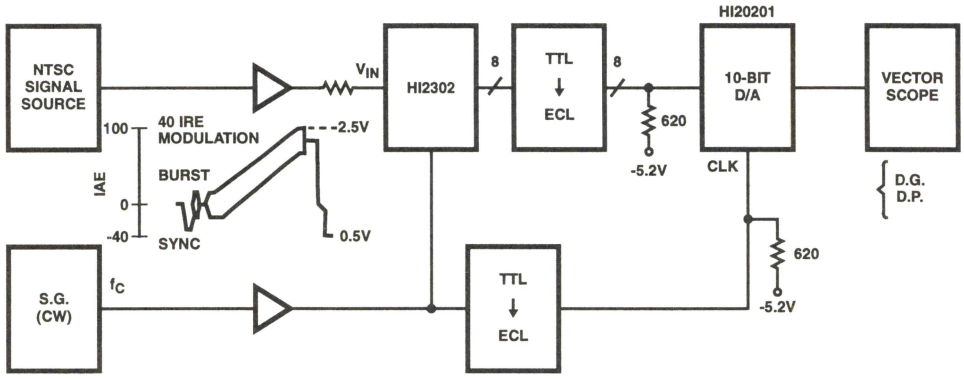


FIGURE 5. DIFFERENTIAL GAIN ERROR, DIFFERENTIAL PHASE ERROR TEST CIRCUIT

Electrical Specifications Measurement Circuits (Continued)

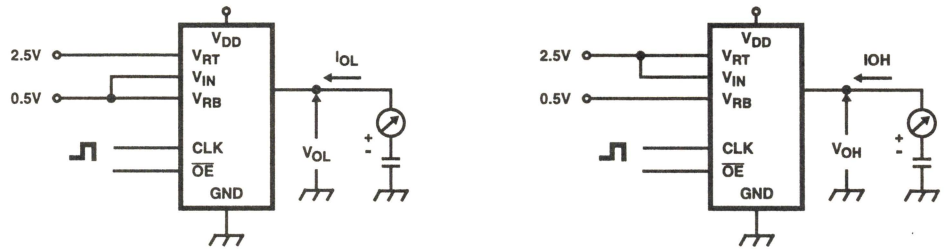


FIGURE 6. DIGITAL OUTPUT CURRENT TEST CIRCUIT

Operation (See Block diagram and Timing Chart II)

- The HI2302 is a two-step parallel system A/D converter featuring a 4-bit upper comparator block and two lower comparator blocks of 4-bit each. The reference voltage that is equal to the voltage between V_{RT} - V_{RB}/16 is constantly applied to the upper 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower 4-bit comparator block. V_{RTS} and V_{RBS} pins serve for the self generation of V_{RT} (reference voltage top) and V_{RB} (reference voltage bottom), and they are also used as the sense pins as shown in the Application Circuit examples Figures 10 and 11.
- This IC uses an offset cancel type comparator which operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the Timing Chart II with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.
- The operation of respective parts is as indicated in the Timing Chart II. For instance, input voltage VI (1) is sampled with the falling edge of the external clock (1) by means of the upper comparator block and the lower comparator A block.
  The upper comparator block finalizes comparison data MD (1) with the rising edge of the external clock (2). Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator A Block finalizes comparison data LD (1) with the rising edge of the external clock (3). MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the external clock (4). Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Notes On Operation

- V_{DD}, V_{SS}
  To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1µF set as close as possible to the pin to bypass to the respective GNDs.
- Analog Input
  Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However, it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasitic oscillation may occur. That may be prevented by insetting a resistance of about 33Ω in series between the amplifier output and A/D input. When the V_{IN} signal of pin No. 21 is monitored, the kickback noise of clock is. However, this has no effect on the characteristics of A/D conversion.
- Clock Input
  The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.
- Reference Input
  Voltage V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing V_{RT} and V_{RB} pins to GND, by means of a capacitor about 0.1µF, stable characteristics are obtained. By shorting V_{DD} and V_{RTS}, V_{SS} and V_{RBS} respectively, the self-bias function that generates V_{RT} = about 2.5V and V_{RB} = about 0.6V, is activated.
- Timing
  Analog input is sampled with the falling edge of CLK and output as digital data synchronized with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 9ns (DV_{DD} = 5V).
- $\overline{OE}$ Pin
  Pins 1 to 8 (D_0 to D_7) are in the output mode by leaving $\overline{OE}$ open or connecting it to DV_{SS}, and they are in the high impedance mode by connecting it to DV_{DD}.

Application Circuits

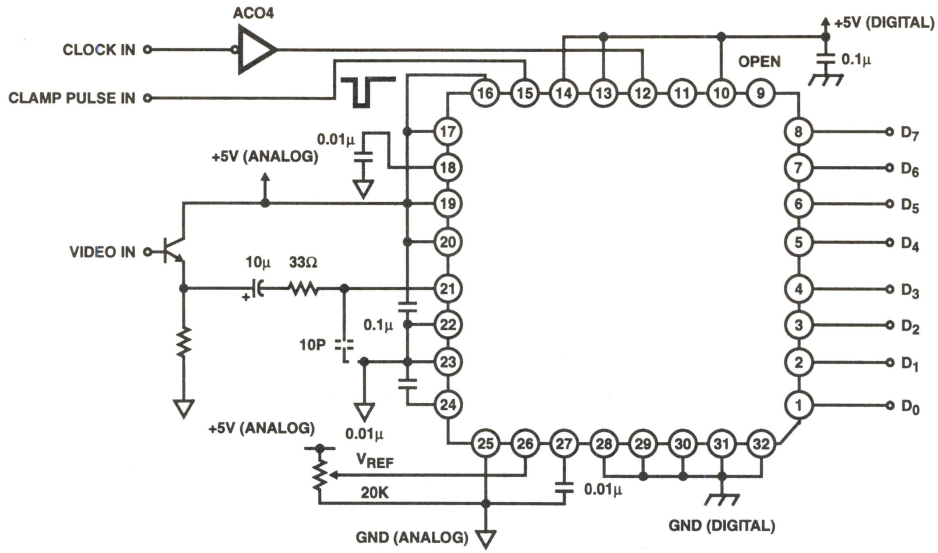
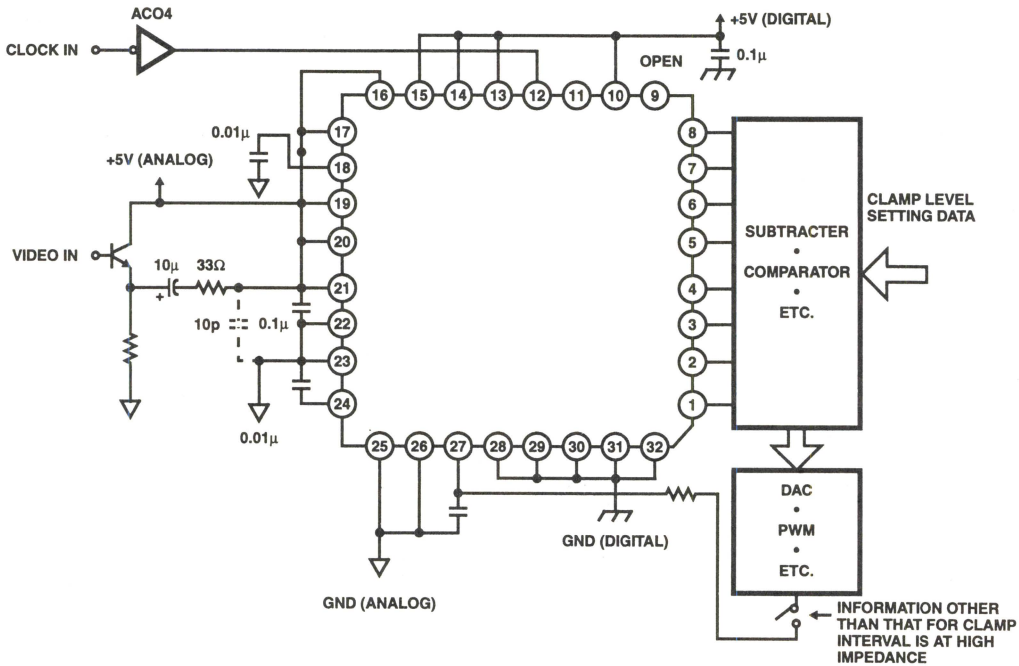


FIGURE 7. SINGLE +5V POWER SUPPLY WHEN CLAMP IS USED (SELF-BIAS USED)



NOTES:

5. The relationship between the changes in CCP voltage (Pin 27) and in V_{IN} voltage is positive phase.
6. $\Delta V_{IN} / \Delta V_{CCP} = 3.0$ ($f_S = 20$ MSPS).

FIGURE 8. SINGLE +5V POWER SUPPLY DIGITAL CLAMP (SELF-BIAS USED)

Application Circuits (Continued)

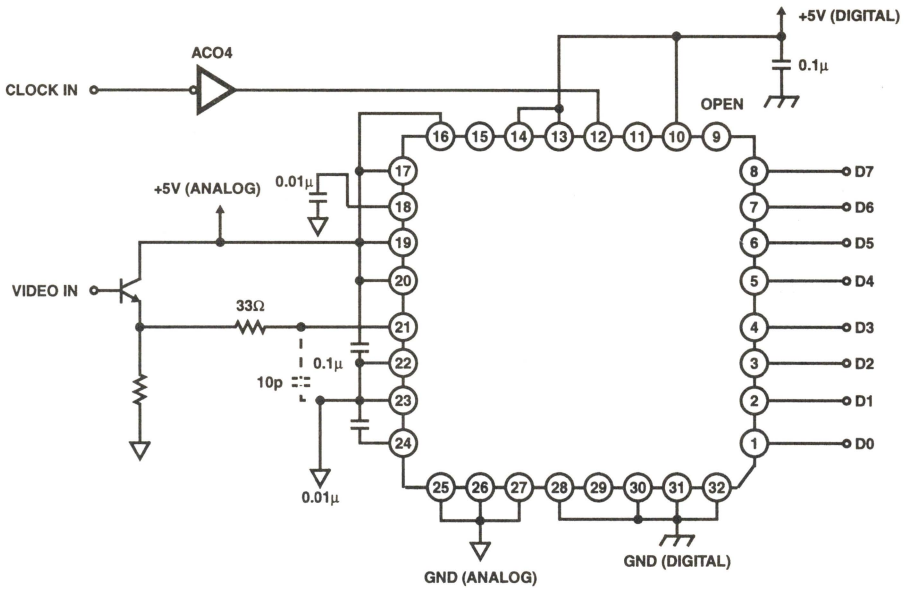


FIGURE 9. SINGLE +5V POWER SUPPLY WHEN CLAMP IS NOT USED (SELF-BIAS USED)

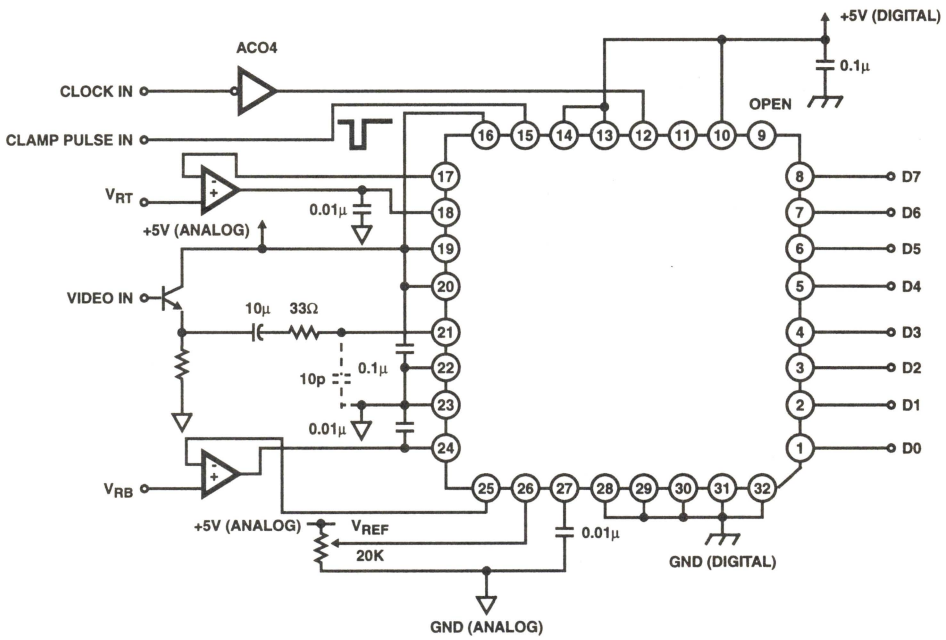


FIGURE 10. WHEN CLAMP IS USED (SELF-BIAS NOT USED)

Application Circuits (Continued)

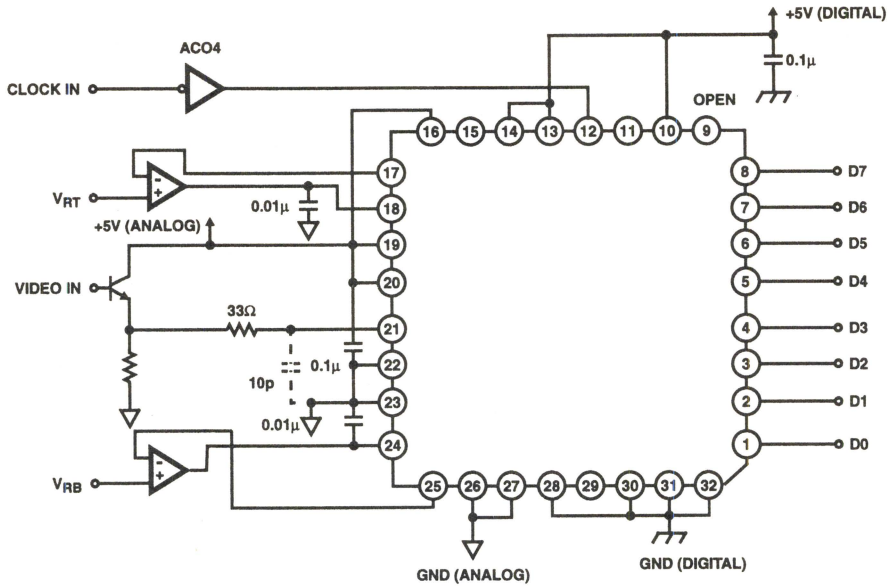


FIGURE 11. SINGLE +5V POWER SUPPLY WHEN CLAMP IS NOT USED (SELF-BIAS NOT USED)

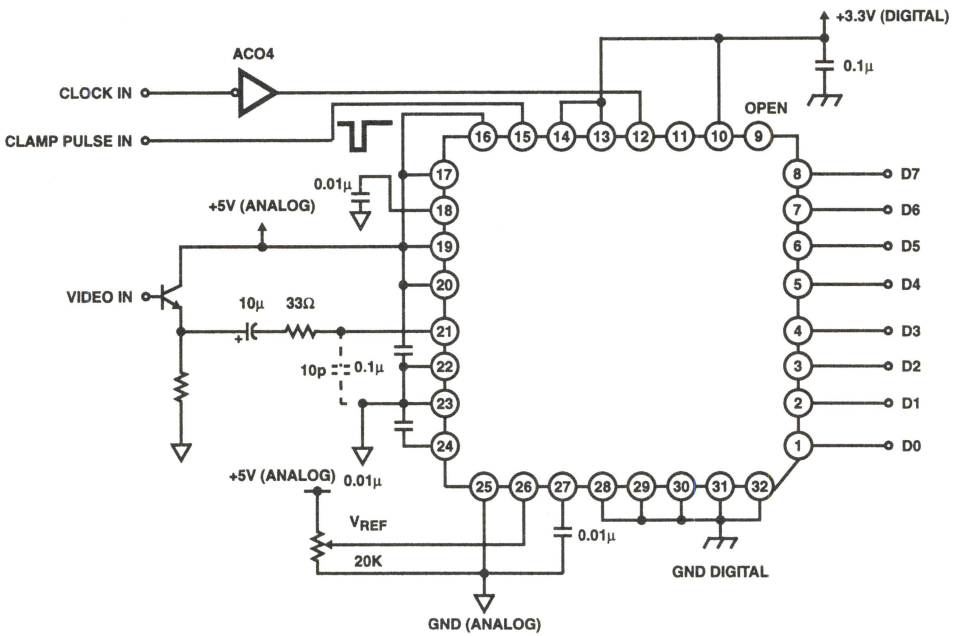


FIGURE 12. DUAL +5V/+3.3V POWER SUPPLY WHEN CLAMP IS USED (SELF-BIAS USED)

Typical Performance Curves

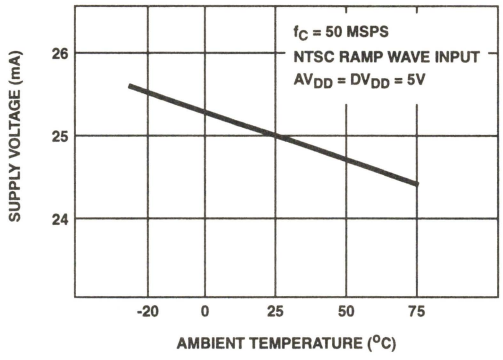


FIGURE 13. AMBIENT TEMPERATURE vs SUPPLY CURRENT

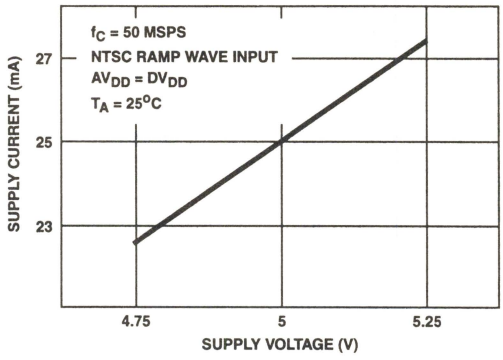


FIGURE 14. SUPPLY VOLTAGE vs SUPPLY CURRENT

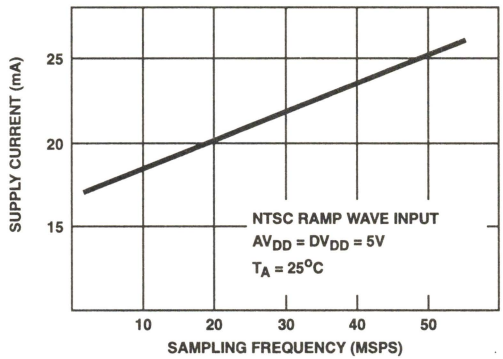


FIGURE 15. SAMPLING FREQUENCY vs SUPPLY CURRENT

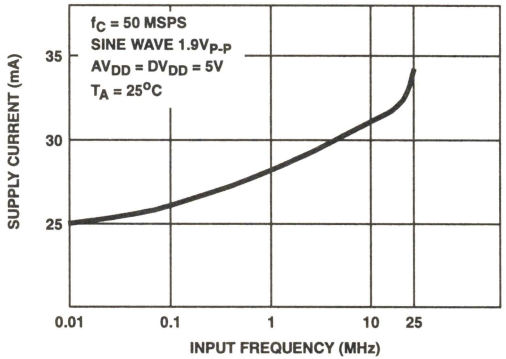


FIGURE 16. INPUT FREQUENCY vs SUPPLY CURRENT

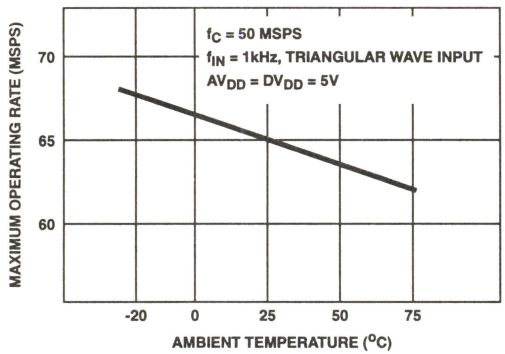


FIGURE 17. AMBIENT TEMPERATURE vs MAXIMUM OPERATING FREQUENCY

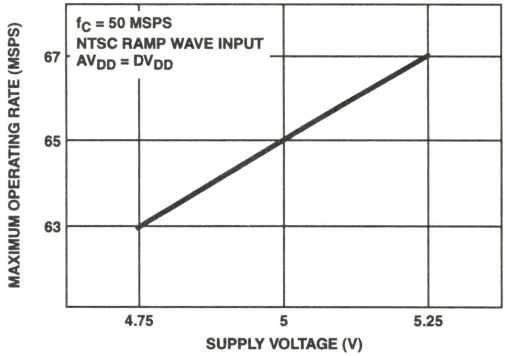


FIGURE 18. SUPPLY VOLTAGE vs MAXIMUM OPERATING FREQUENCY

Typical Performance Curves (Continued)

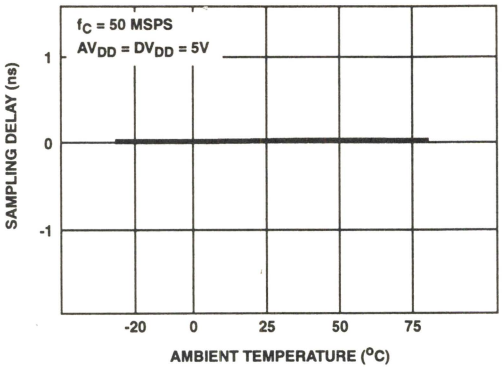


FIGURE 19. AMBIENT TEMPERATURE vs SAMPLING DELAY

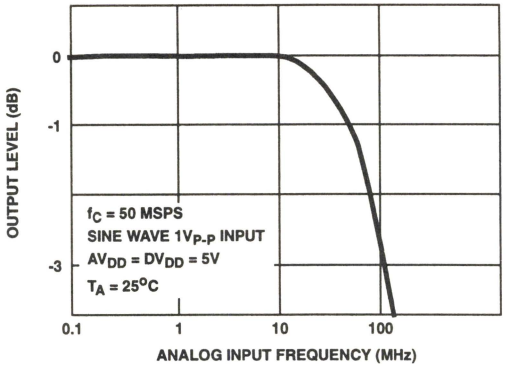


FIGURE 20. FULL SCALE INPUT BANDWIDTH

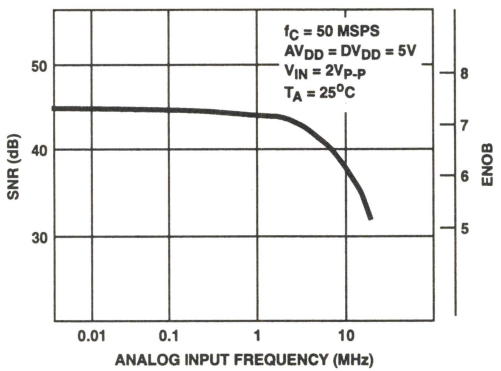


FIGURE 21. ANALOG INPUT FREQUENCY vs SNR, EFFECTIVE NUMBER OF BITS (ENOB)

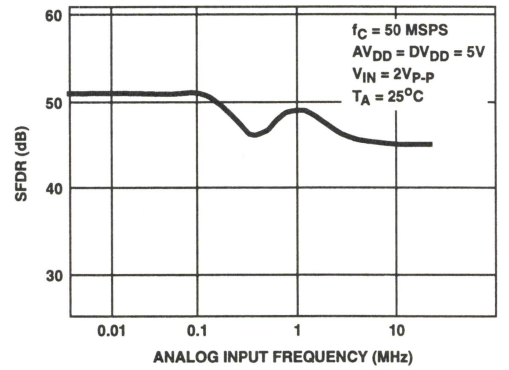


FIGURE 22. ANALOG INPUT FREQUENCY vs SFDR

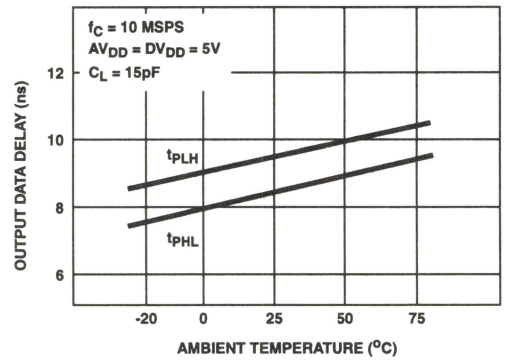


FIGURE 23. AMBIENT TEMPERATURE vs OUTPUT DATA DELAY

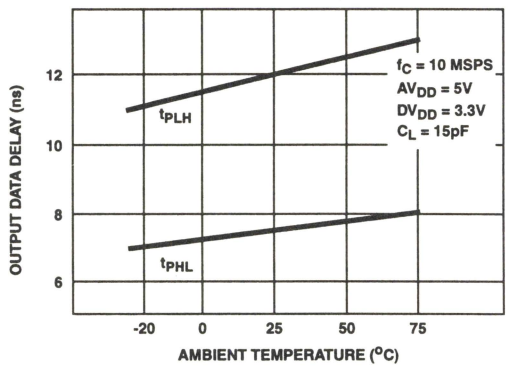


FIGURE 24. AMBIENT TEMPERATURE vs OUTPUT DATA DELAY

Typical Performance Curves (Continued)

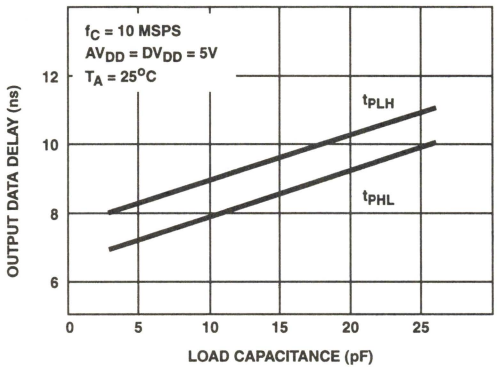


FIGURE 25. LOAD CAPACITANCE vs OUTPUT DATA DELAY

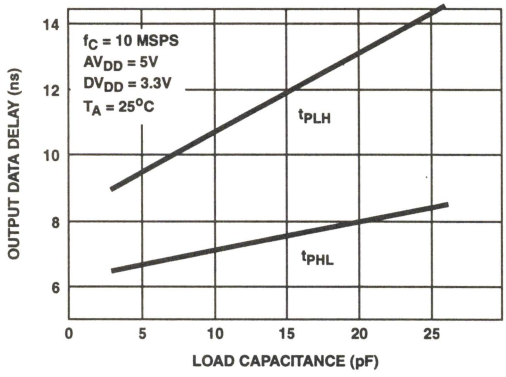


FIGURE 26. LOAD CAPACITANCE vs OUTPUT DATA DELAY

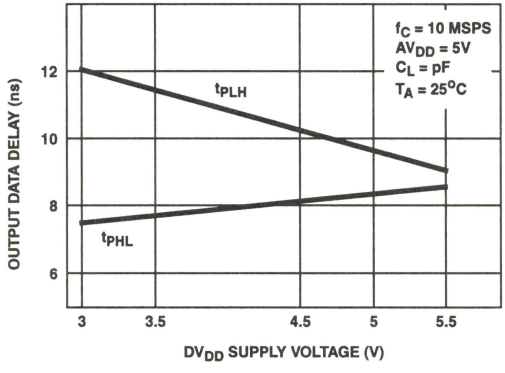


FIGURE 27. DV_{DD} SUPPLY VOLTAGE vs OUTPUT DATA DELAY

HARRIS SEMICONDUCTOR

HI2303

PRELIMINARY

August 1997

Triple 8-Bit, 50 MSPS, Video A/D Converter With Clamp Function

Features

- Resolution 8-Bit $\pm^1/_2$ LSB (DL)
- Low Power Consumption (at 50 MSPS Typ) (Reference Current Excluded) 500mW
- Synchronizing Digital Clamp Function
- Clamp ON/OFF Function
- Reference Voltage Self-Bias Circuit
- Input CMOS/TTL Compatible
- Three-State TTL Compatible Output
- Single 5V Power Supply or Dual 5V or 3.3V Power Supplies
- Low Input Capacitance .....TBD pF
- Different Digital Output Multiplex Format
  - 4:4:4 Format
  - 4:2:2 Format
  - 4:1:1 Format
- Direct Replacement for Sony CXD2303

Description

The HI2303 is an 8-bit, 3-Channel CMOS A/D converter for video with synchronizing digital clamp function. The adoption of two-step parallel method achieves low power consumption and a maximum conversion rate of 50 MSPS.

Applications

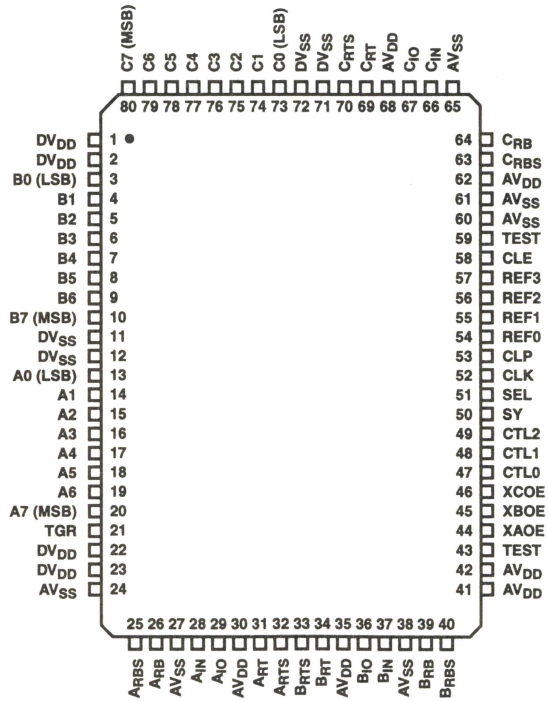
- Video Digitizing (Composite and Y-C)
- LCD Projectors
- LCD Panels
- RGB Graphics Processing

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI2303JCQ	-40 to 85	80 Ld MQFP	Q80.14x20-S

Pinout

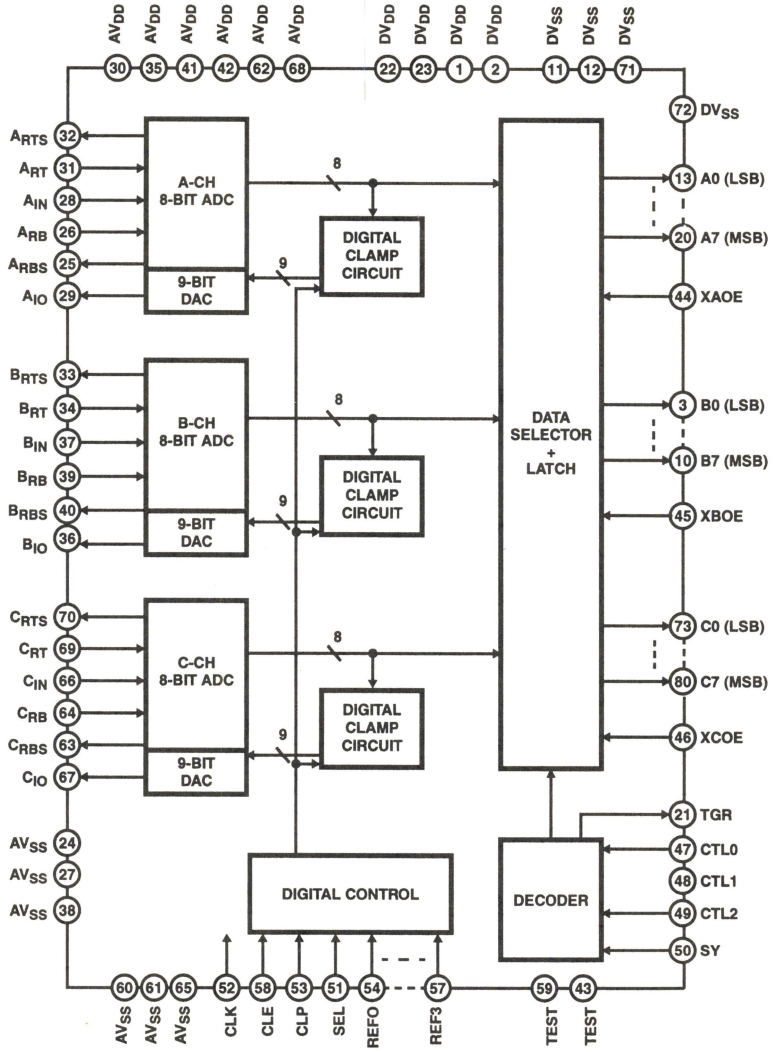
HI2303 (MQFP)
TOP VIEW



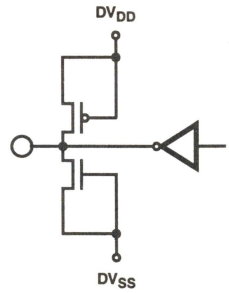
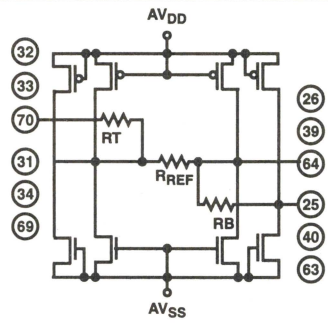
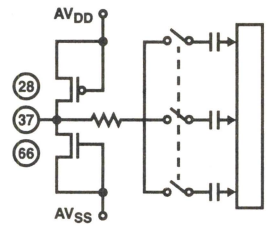
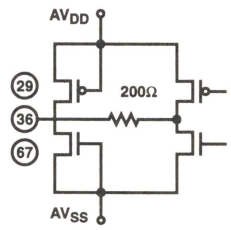
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

File Number **4106**

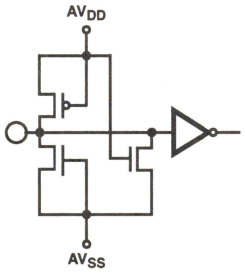
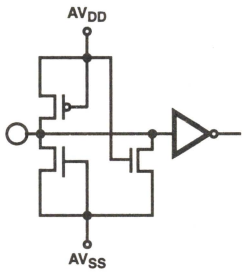
Functional Block Diagram



Pin Description

PIN NO.	SYMBOL		EQUIVALENT CIRCUIT	DESCRIPTION
1, 2, 22, 23	DV_{DD}	-		Digital Power Supply. +5V or +3.3V.
13, to 20 3 to 10 73 to 80	A0 to A7 B0 to B7 C0 to C7	O		Digital output. A0 (LSB) to A7 (MSB) B0 (LSB) to B7 (MSB) C0 (LSB) to C7 (MSB).
21	TGR	O		See the Timing Pulse Output Timing Chart.
11, 12, 71, 72	DV_{SS}	-		Digital Ground.
24, 27, 38, 60, 61, 65	AV_{SS}	-		Analog Ground.
25 40 63	ARBS BRBS CRBS	-		Shorting these pins to AVSS generates voltage of approximately 0.6V at the ARB, BRB and CRB pins.
26 39 64	ARB BRB CRB	-		Reference Voltage (Bottom).
31 34 69	ART BRT CRT	-		Reference Voltage (Top).
32 33 70	ARTS BRTS CRTS	-		Shorting these pins to AV_{DD} generates voltage of about 2.5V at the ART, BRT and CRT pins.
28 37 66	AIN BIN CIN	I		Analog Input.
29 36 67	AIO BIO CIO	O		Analog Output. These pins are the D/A converter outputs which comprise the digital clamp circuit.

Pin Description (Continued)

PIN NO.	SYMBOL		EQUIVALENT CIRCUIT	DESCRIPTION
30, 35, 41, 42, 62, 68	AV_{DD}			Analog +5V Power Supply.
43 59	TEST	I		Normally open. Pull-down resistors are incorporated.
44 45 46	XAOE XBOE XCOE	I		Output Enable Input. When these pins are Low, data is output from the digital output pins. When these pins are High, the digital output pins are High impedance. The A, B and C Channels can be controlled separately. Also, these pins are not synchronized with the clock signal. Pull-down resistors are incorporated.
47 48 49	CTL0 CTL1 CLT2	I		Determines the digital output mode. See the Mode tables and Timing Charts. Pull-down resistors are incorporated.
50	SY	I		Controls the digital output mode switching timing. The mode is switched by detecting the transition point where this pin changes from Low to High. See the Mode Tables and Timing Charts for details. A pull-down resister is incorporated.
51	SEL	I		Controls the CLP signal polarity. When this pin is Low, CLP is High active. When this pin is High, CLP is Low active. This pin has a built-in pull-down resistor.
52	CLK	I		Clock Input. A pull-down resistor is incorporated.
53	CLP	I		Clamp Pulse Input. The polarity can be set to either High or Low by setting SEL. This pin has a built-in pull-down resistor.
54 55 56 57	REF0 REF1 REF2 REF3	I		Determines the clamp circuit reference data. See the mode tables for the set data. These pins are not synchronized with the clock input signal. Pull-down resistors are incorporated.
58	CLE	I		Clamp Enable. When this pin is Low the clamp circuit does not operate. When this pin is High, the clamp circuit operates. A pull-down resistor is incorporated.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{DD}, DV_{DD}) 7V
Input Voltage (V_{IN}, All Pins) . . . . . V_{DD} +0.5V to V_{SS} -0.5V
Output Voltage (V_D, Digital) . . . . . V_{DD} +0.5V to V_{SS} -0.5V

Operating Conditions

Supply Voltage:
AV_{DD}, AV_{SS} . . . . . .4.75V to 5.25V
DV_{DD}, DV_{SS} . . . . . .3.0V to 5.5V
$|DV_{SS}, AV_{SS}|$ . . . . . .0mV to 100mV
Reference Input Voltage:
V_{ARB}, V_{BRB}, V_{CRB} . . . . . .0V or More
V_{ART}, V_{BRT}, V_{CRT} . . . . . 2.7V or Less
Analog Input:
A_{IN}, B_{IN}, C_{IN} . . . . . 1.7V_{P-P} or More
Clock Pulse Width:
t_{PW1}, t_{PW0} . . . . . 9ns (Min) to 1.1ms (Max)
Ambient Temperature (TOPR) . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
MQFP Package 88
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range (T_{STG}) . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications f_C = 50 MSPS, AV_{DD} = 5V, V_{RB} = 0.5V, V_{RT} = 2.5V, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG CHARACTERISTICS DV_{DD} = 3V to 5.5V							
Conversion Rate	f_C	AV_{DD} = 4.75V to 5.25V, T_A = -20°C to 75°C, V_{IN} = 0.5V to 2.5V, f_{IN} = 1kHz Triangular Wave		0.5	-	50	MSPS
Analog Input Band (-1dB)	BW	Envelope	-1dB	-	60	-	MHz
		R_{IN} = 33Ω	-3dB	-	100	-	MHz
Differential Non-Linearity Error	E_D	End Point		-	±0.3	-	LSB
Integral Non-Linearity Error	E_L			-	±0.7	-	LSB
Offset Voltage (Note 2)	E_{OT}	Potential Difference to A_{RT}, B_{RT}, C_{RT}		-	-	-	mV
	E_{OB}	Potential Difference to A_{RB}, B_{RB}, C_{RB}		-	-	-	mV
Differential Gain Error	DG	NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS		-	3	-	%
Differential Phase Error	DP			-	1.5	-	Deg
Sampling Delay	t_{SD}			-	-	-	ns
Clamp Offset Voltage	E_{OC}	V_{IN} = DC	Ref. Data = "00010000"	-	-	±1	LSB
		C_{IN} = 10µF		-	-	±1	LSB
		t_{PCW} = 2.75µs		-	-	±1	LSB
		f_{CLK} = 14.3MHz	Ref. Data = "10000000"	-	-	±1	LSB
		f_{CLP} = 15.75kHZ		-	-	±1	LSB
Full Scale Input Ratio (Note 3)				-	-	-	%

Electrical Specifications f_C = 50 MSPS, AV_{DD} = 5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Signal To Noise Ratio		SNR	f_{IN} = 100kHz		-	TBD	-	dB
			f_{IN} = 500kHz		-	TBD	-	dB
			f_{IN} = 1MHz		-	TBD	-	dB
			f_{IN} = 3MHz		-	TBD	-	dB
			f_{IN} = 10MHz		-	TBD	-	dB
			f_{IN} = 25MHz		-	TBD	-	dB
Spurious Free Dynamic Range		FSDR	f_{IN} = 100KHz		-	TBD	-	dB
			f_{IN} = 500kHz		-	TBD	-	dB
			f_{IN} = 1MHz		-	TBD	-	dB
			f_{IN} = 3MHz		-	TBD	-	dB
			f_{IN} = 10MHz		-	TBD	-	dB
			f_{IN} = 25MHz		-	TBD	-	dB
DC CHARACTERISTICS DV_{DD} = 5V or 3.3V								
Supply Current	Both	$I_{AD} + I_{DD}$	NTSC Ramp Wave Input CLE = High f_{CLP} = 15.75kHz	DV_{DD} = 5V	-	TBD	-	mA
	Analog	I_{AD}		D_{VDD} = 3.3V	-	TBD	-	mA
	Digital	I_{DD}			-	TBD	-	mA
	Both	$I_{AD} + I_{DD}$	NTSC Ramp Wave Input CLE = Low	D_{VDD} = 5V	-	TBD	-	mA
	Analog	I_{AD}		D_{VDD} = 3.3V	-	TBD	-	mA
	Digital	I_{DD}			-	TBD	-	mA
Reference Current		I_{REF}	For Every Channel		-	5.4	-	mA
Reference Resistance (V_{RT} to V_{RB})		R_{REF}	For Every Channel		-	370	-	Ω
Self Bias		V_{RT}	Shorts AV_{SS} and A_{RBS}, B_{RBS}, C_{RBS}		-	TBD	-	V
		V_{RT} - V_{RB}	Shorts AV_{DD} and A_{RTS}, B_{RTS}, C_{RTS}		-	TBD	-	V
Analog Input Resistance		R_{IN}	V_{IN}	f_{CLK} = 50MHz	-	13	-	kΩ
				f_{CLK} = 35MHz	-	16	-	kΩ
				f_{CLK} = 20MHz	-	30	-	kΩ
Input Capacitance		C_{A11}	A_{IN}, B_{IN}, C_{IN}, V_{IN} = 1.5V + 0.07V_{RMS}		-	TBD	-	pF
		C_{A12}	A_{RTS}, A_{RT}, A_{RB}, A_{BFS}, B_{RTS}, B_{RT}, B_{RB}, B_{RBS}, C_{RTS}, C_{RT}, C_{RB}, C_{RBS}		-	TBD	9	pF
		C_{DIN}	Digital Input Pin		-	TBD	9	pF
Output Capacitance		C_{AO}	A_{IO}, B_{IO}, C_{IO}		-	TBD	-	pF
		C_{DO}	Digital Output Pin		-	TBD	11	pF
Digital Input Voltage		V_{IH}	AV_{DD} = 4.75V to 5.25V, DV_{DD} = 3V to 5.5V T_A = 20°C to 75°C		2.2	-	-	V
		V_{IL}			-	-	0.8	V

Electrical Specifications f_C = 50 MSPS, AV_{DD} = 5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Digital Input Current	I_{IH}	V_I = 0V to AV_{DD}		-40	-	240	µA
	I_{IL}	T_A = 20°C to 75°C		-40	-	240	µA
Digital Output Current	I_{OH}	X_{OE} = 0V DV_{DD} = 5V T_A = -20°C to 75°C	V_{OH} = DV_{DD} - 0.8V	-	-	-2	mA
	I_{OL}		V_{OL} = 0.4V	4	-	-	mA
	I_{OH}	X_{OE} = 0V DV_{DD} = 3.3V T_A = -20°C to 75°C	V_{OH} = DV_{DD} - 0.8V	-	-	-1.2	mA
	I_{OL}		V_{OL} = 0.4V	2.4	-	-	mA
	I_{OZH}	X_{OE} = 3V DV_{DD} = 3V to 5.5V T_A = 20°C to 75°C	V_{OH} = DV_{DD}	-40	-	40	mA
	I_{OZL}		V_{OL} = 0V	-40	-	40	mA
Digital Output Voltage	V_{OH}	X_{OE} = 0V DV_{DD} = 5V T_A = 20°C to 75°C	I_{OH} = -2mA	DV_{DD} -0.8	-	-	V
	V_{OL}		I_{OL} = 4mA	-	-	0.4	V
	V_{OH}	X_{OE} = 0V DV_{DD} = 3.3V T_A = -20°C to 75°C	I_{OH} = -1.2mA	DV_{DD} -0.8	-	-	V
	V_{OL}		I_{OL} = -2.4mA	-	-	0.4	V

NOTES:

2. The offset voltage E_{OB} is a potential difference between A_{RB}, B_{RB}, C_{RB} and a point of position where the voltage drops equivalent to $^1/_2$ LSB of the voltage when the output data changes from "00000000" to "00000001". E_{OR} is a potential difference between A_{RT}, B_{RT}, C_{RT} and a potential of point where the voltage rises equivalent to $^1/_2$ LSB of the voltage when the output data changes from "11111111" to "11111110".

3. Full scale input ratio = $\left| \frac{(2V + E_{OT} - E_{OB}) \text{ of each channel}}{\text{Average of } (2V + E_{OT} - E_{OB}) \text{ of each channel}} - 1 \right| \times 100(\%)$.

Timing f_C = 50 MSPS, AV_{DD} = 5.V, DV_{DD} = 5V or 3.3V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output Data Delay	t_{PLH}	C_L = 15pF XOE = 0V	DV_{DD} = 5V	-	TBD	-	ns
	t_{PHL}			-	TBD	-	ns
	t_{PLM}		DV_{DD} = 3.3V	-	TBD	-	ns
	t_{PHL}			-	TBD	-	ns
Three-State Output Enable Time	t_{PZH}	R_L = 1kΩ CL = 15pF XOE = OV → 3V	DV_{DD} = 5V	-	TBD	-	ns
	t_{PZL}			-	TBD	-	ns
	t_{PZH}		DV_{DD} = 3.3V	-	TBD	-	ns
	t_{PZL}			-	TBD	-	ns
Three-State Output Disable Time	t_{PHZ}	R_L = 1kΩ C_L = 15pF XOE = 0V → 3V	DV_{DD} = 5V	-	TBD	-	ns
	t_{PLZ}			-	TBD	-	ns
	t_{PHZ}		DV_{DD} = 3.3V	-	TBD	-	ns
	t_{PLZ}			-	TBD	-	ns
Set-up Time	t_S			-	TBD	-	ns
Hold Time	t_H			-	TBD	-	ns
Clamp Pulse Width	t_H	CLK Conversion		2	-	-	Cycle

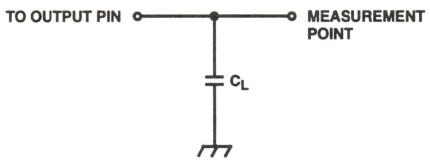
Digital Output

The following table shows the relationship between analog input voltage and digital output code.

TABLE 1. I/O CORRESPONDENCE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB	DIGITAL OUTPUT CODE LSB
V_{RTS}, V_{BRT}, V_{CRT}	0	1 1 1 1	1 1 1 1
	•	•	•
	•	•	•
	•		
	127	1 0 0 0	0 0 0 0
	128	0 1 1 1	1 1 1 1
	•	•	•
	•	•	•
V_{ARB}, V_{BRB}, V_{CRB}	255	0 0 0 0	0 0 0 0

Test Circuits



NOTE: C_L includes capacitance of probes.

FIGURE 1. OUTPUT DATA DELAY MEASUREMENT CIRCUIT

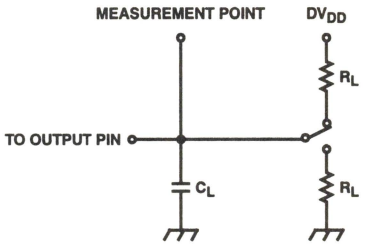


FIGURE 2. THREE-STATE MEASUREMENT CIRCUIT

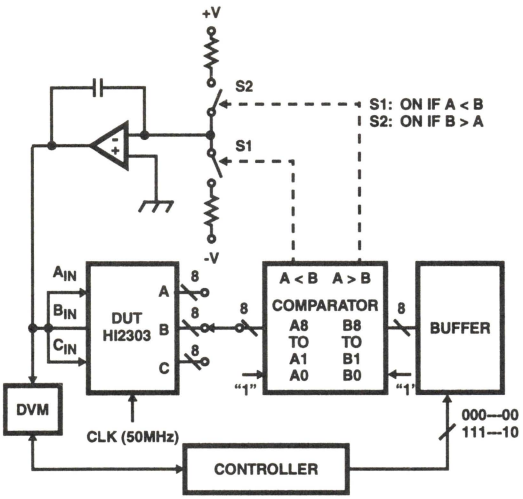


FIGURE 3. INTEGRAL NON-LINEARITY ERROR, DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

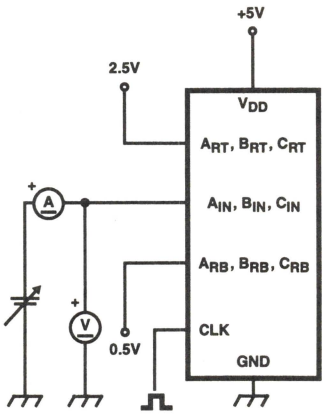


FIGURE 4. ANALOG INPUT RESISTANCE TEST CIRCUIT

Test Circuits (Continued)

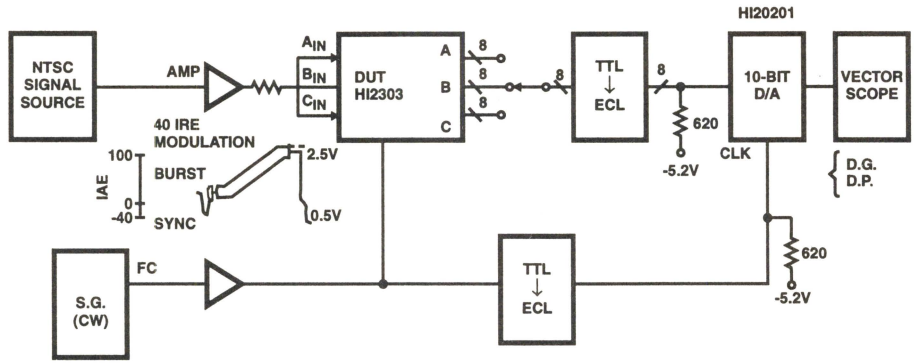


FIGURE 5. DIFFERENTIAL GAIN AND PHASE ERROR vs TEST CIRCUIT

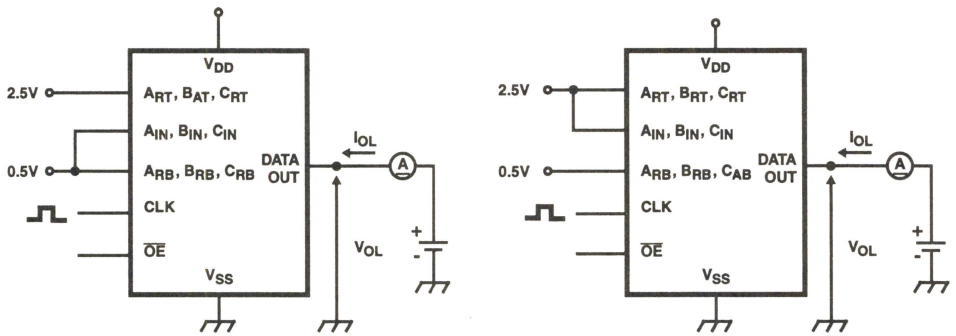


FIGURE 6. DIGITAL OUTPUT TEST CIRCUIT

Description of Operation

Output Format

The HI2303 can select six different types to output formats through a combination of the CTL0, CTL1 and CTL2 inputs as shown in the table below. Output is synchronized to the SY input signal transition from Low to High.

TABLE 2. SETTING VALUES AND OUTPUT FORMATS

SETTING			OUTPUT	
CTL2	CTL1	CTLO	MODE	FORMAT
L	L	L	0	4:4:4
L	L	H	1	4:2:2 ($8F_S$)
L	H	L	2	4:2:2 (D2)
L	H	H	3	4:2:2 (Special)
H	L	L	4	4:1:1
H	L	H	5	4:1:1 (Special)
H	H	L	6	Simple Boundary, Scan 1
H	H	H	7	Simple Boundary, Scan 2

Note that when the SY input is open or Low level, the output format is mode #0 (4:4:4). However, when the SY input signal temporarily goes to Low level for the mode switching, the mode changes as shown in Timing Chart II. When digital data is being output in the mode N output format, if the SY input signal changes from High level to Low level, the digital data continues to be output in the mode N output format for the following two clocks, The output format for the digital data output from the third to fifth clocks is not established, so its use is prohibited. If the SY input signal remains Low level, the digital data is output in the mode #0 output format from the sixth clock. After the SY input signal changes from Low level to High level, the digital data is output in the mode M output format from the sixth clock At this time, the data Output at the sixth clock is the data A/D converted from the analog input signal that was sampled at the falling edge of the clock input signal immediately after the SY input signal changes from Low level to High level.

The output format control input signals CTL2, CTL1 and CTL0 are fetched only in sync with the rising edge of the clock input signal after the SY input signal has risen.

Timing Diagrams

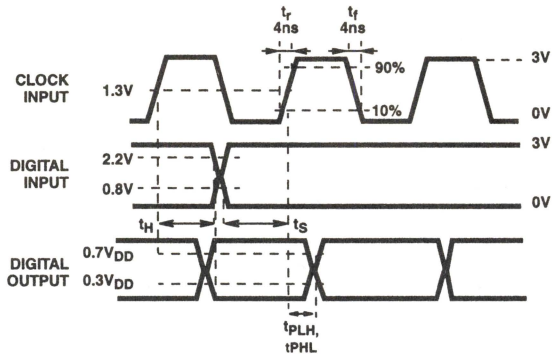


FIGURE 7.

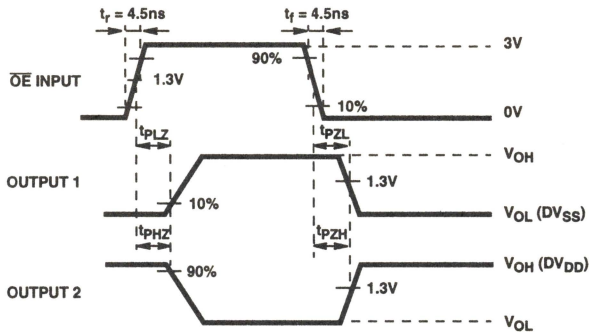


FIGURE 8. TIMING CHART I-2

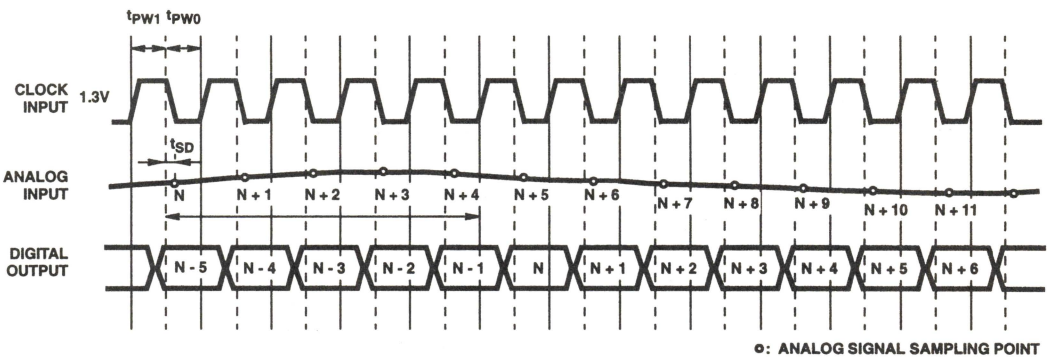


FIGURE 9.

Timing Diagrams (Continued)

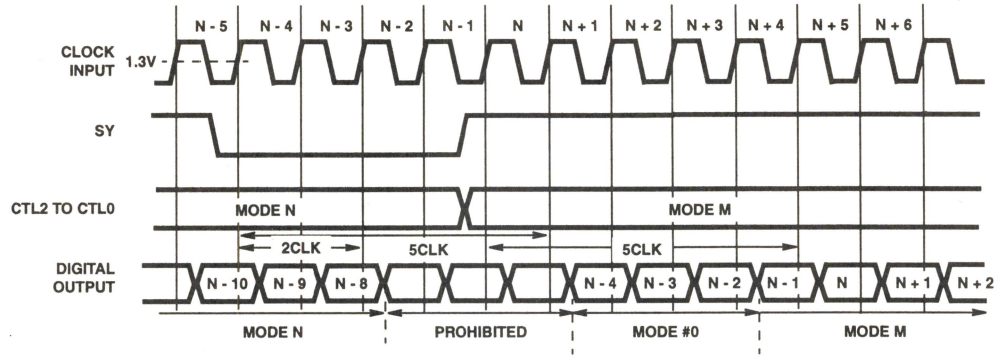


FIGURE 10.

Mode #0 4:4:4

ADC CHANNEL	OUTPUT	DATA							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B70	B71	B72	B73	B74	B75	B76	B77
	B6	B60	B61	B62	B63	B64	B65	B66	B67
	B5	B50	B51	B52	B53	B54	B55	B56	B57
	B4	B40	B41	B42	B43	B44	B45	B46	B47
	B3	B30	B31	B32	B33	B34	B35	B36	B37
	B2	B20	B21	B22	B23	B24	B25	B26	B27
	B1	B10	B11	B12	B13	B14	B15	B16	B17
	B0	B00	B01	B02	B03	B04	B05	B06	B07
C	C7	C70	C71	C72	C73	C74	C75	C76	C77
	C6	C60	C61	C62	C63	C64	C65	C66	C67
	C5	C50	C51	C52	C53	C54	C55	C56	C57
	C4	C40	C41	C42	C43	C44	C45	C46	C47
	C3	C30	C31	C32	C33	C34	C35	C36	C37
	C2	C20	C21	C22	C23	C24	C25	C26	C27
	C1	C10	C11	C12	C13	C14	C15	C16	C17
	C0	C00	C01	C02	C03	C04	C05	C06	C07
TGR		Low →							

NOTE: See Figure 9.

Mode #2 4:2:2(D2)

A73 → BIT
A73 → SAMPLING TIMING (NOTE)
A73 → ADC CHANNEL

ADC CHANNEL	OUTPUT	DATA							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B70	C70	B72	C72	B74	C74	B76	C76
	B6	B60	C60	B62	C62	B64	C64	B66	C66
	B5	B50	C50	B52	C52	B54	C54	B56	C56
	B4	B40	C40	B42	C42	B44	C44	B46	C46
	B3	B30	C30	B32	C32	B34	C34	B36	C36
	B2	B20	C20	B22	C22	B24	C24	B26	C26
	B1	B10	C10	B12	C12	B14	C14	B16	C16
	B0	B00	C00	B02	C02	B04	C05	B06	SC06
C	C7	HiZ	→						
	C6	HiZ	→						
	C5	HiZ	→						
	C4	HiZ	→						
	C3	HiZ	→						
	C2	HiZ	→						
	C1	HiZ	→						
	C0	HiZ	→						
TGR		HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW

HiZ: High Impedance

NOTE: See Figure 9.

Mode #3 4:2:2 (Special)

ADC CHANNEL	OUTPUT	DATA							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B70	C71	B72	C73	B74	C75	B76	C77
	B6	B60	C61	B62	C63	B64	C65	B66	C67
	B5	B50	C51	B52	C53	B54	C55	B56	C57
	B4	B40	C41	B42	C43	B44	C45	B46	C47
	B3	B30	C31	B32	C33	B34	C35	B36	C37
	B2	B20	C21	B22	C23	B24	C25	B26	C27
	B1	B10	C11	B12	C13	B14	C15	B16	C17
	B0	B00	C01	B02	C03	B04	C05	B06	C07
C	C7	HiZ	→						
	C6	HiZ	→						
	C5	HiZ	→						
	C4	HiZ	→						
	C3	HiZ	→						
	C2	HiZ	→						
	C1	HiZ	→						
	C0	HiZ	→						
TGR		HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW

HiZ: High Impedance

NOTE: See Figure 9.

Mode #1 4:2:2 ($8F_S$)

ADC CHANNEL	OUTPUT	DATA							
A	A7	A70	A70	A72	A72	A74	A74	A76	A76
	A6	A60	A60	A62	A62	A64	A64	A66	A66
	A5	A50	A50	A52	A52	A54	A54	A56	A56
	A4	A40	A40	A42	A42	A44	A44	A46	A46
	A3	A30	A30	A32	A32	A34	A34	A36	A36
	A2	A20	A20	A22	A22	A24	A24	A26	A26
	A1	A10	A10	A12	A12	A14	A14	A16	A16
	A0	A00	A00	A02	A02	A04	A04	A06	A06
B	B7	B70	B70	C70	C70	B74	B74	C74	C74
	B6	B60	B60	C60	C60	B64	B64	C64	C64
	B5	B50	B50	C50	C50	B54	B54	C54	C54
	B4	B40	B40	C40	C40	B44	B44	C44	C44
	B3	B30	B30	C30	C30	B34	B34	C34	C34
	B2	B20	B20	C20	C20	B24	B24	C24	C24
	B1	B10	B10	C10	C10	B14	B14	C14	C14
	B0	B00	B00	C00	C00	B04	B04	C04	C04
C	C7	B70	A70	C70	A72	B74	A74	C74	A76
	C6	B60	A60	C60	A62	B64	A64	C64	A66
	C5	B50	A50	C50	A52	B54	A54	C54	A56
	C4	B40	A40	C40	A42	B44	A44	C44	A46
	C3	B30	A30	C30	A32	B34	A34	C34	A36
	C2	B20	A20	C20	A22	B24	A24	C24	A26
	C1	C10	A10	C10	A12	B14	A14	C14	A16
	C0	B00	A00	C00	A02	B04	A04	C04	A06
TGR		HIGH	LOW	→		HIGH	LOW	→	

NOTE: See Figure 9.

Mode #4 4:1:1

ADC CHANNEL	OUTPUT	DATA							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B70	B60	B30	B10	B74	B54	B34	B14
	B6	B60	B40	B20	B00	B64	B44	B24	B04
	B5	C10	C50	C30	C10	C74	C54	C34	C14
	B4	C60	C40	C20	C00	C64	C44	C24	C04
	B3	HiZ	→						
	B2	HiZ	→						
	B1	HiZ	→						
	B0	HiZ	→						
C	C7	HiZ	→						
	C6	HiZ	→						
	C5	HiZ	→						
	C4	HiZ	→						
	C3	HiZ	→						
	C2	HiZ	→						
	C1	HiZ	→						
	C0	HiZ	→						
TGR		HIGH	LOW	→		HIGH	LOW	→	

HiZ: High Impedance

NOTE: See Figure 9.

Mode #5 4:1:1 (Special)

ADC CHANNEL	OUTPUT	DATA							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B30	B70	C32	C72	B34	B74	C36	C76
	B6	B20	B60	C22	C62	B24	B64	C26	C66
	B5	B10	B50	C12	C52	B14	B54	C16	C56
	B4	B00	B40	C02	C42	B04	B44	C06	C46
	B3	HiZ	→						
	B2	HiZ	→						
	B1	HiZ	→						
	B0	HiZ	→						
C	C7	HiZ	→						
	C6	HiZ	→						
	C5	HiZ	→						
	C4	HiZ	→						
	C3	HiZ	→						
	C2	HiZ	→						
	C1	HiZ	→						
	C0	HiZ	→						
TGR		HIGH	LOW	→		HIGH	LOW	→	

HiZ: High Impedance

NOTE: See Figure 9.

Mode #6, #7 - Simple Boundary Scan 1 and Scan 2

The HI2303 has a simple boundary scan function.

TABLE 3. SIMPLE BOUNDARY SCAN

BITS			OUTPUT DATA	
			MODE #6	MODE #7
A7	B7	C7	H	L
A6	B6	C6	L	H
A5	B5	C5	H	L
A4	B4	C4	L	H
A3	B3	C3	H	L
A2	B2	C2	L	H
A1	B1	C1	H	L
A0	B0	C0	L	H

NOTE: CLK and SY must be set.

2. Clamp Function

The following two points should be noted when using the digital clamp circuit.

- The clamp pulse must be supplied externally.
- The clamp circuit is not designed for V cycle clamping.

16 different reference levels can be selected for the digital clamp circuit through a combination of the REFO, REF1, REF2 and REF3 inputs as shown in the table below. Note that the REFO, REF1, REF2 and REF3 input signals are fetched asynchronously with the clock input signal.

TABLE 4. SETTING VALUES AND REFERENCE LEVEL

SETTING				REFERENCE LEVEL				
					CHANNEL A		CHANNELS B AND C	
REF3	REF2	REF1	REFO	MODE	DECIMAL	BINARY	DECIMAL	BINARY
L	L	L	L	0	16	00010000	128	10000000
L	L	L	H	1	32	00100000	128	10000000
L	L	H	L	2	48	00110000	128	10000000
L	L	H	H	3	64	01000000	128	10000000
L	H	L	L	4	1	00000001	1	00000001
L	H	L	H	5	16	00010000	16	00010000
L	H	H	L	6	32	00100000	32	00100000
L	H	H	H	7	48	00110000	8	00110000
H	L	L	L	8	239	11101111	127	01111111
H	L	L	H	9	223	11011111	127	01111111
H	L	H	L	A	207	11001111	127	01111111
H	L	H	H	B	191	10111111	127	01111111
H	H	L	L	C	254	11111110	254	11111110
H	H	L	H	D	239	11101111	239	11101111
H	H	H	L	E	223	11011111	223	1101111
H	H	H	H	F	207	11001111	207	11001111

August 1997

8-Bit, 120 MSPS, Flash A/D Converter

Features

- Differential Linearity Error ..... ±0.5 LSB
- Integral Linearity Error ..... ±0.5 LSB
- Integral Linearity Compensation Circuit
- Low Input Capacitance 21pF
- Wide Analog Input Bandwidth 150MHz
- Low Power Consumption 760mW
- Internal $^1/_2$ Frequency Divider Circuit (w/Reset Function)
- CLK/2 Clock Output
- Compatible with ECL, PECL and TTL Digital Input Levels
- 1:2 Demultiplexed Output Pin
- Surface Mounting Package
- Direct Replacement for Sony CXA3026Q

Applications

- RGB Graphics Processing (LCD, PDP)
- Digital Oscilloscopes
- Digital Communications (QPSK, QAM)
- Magnetic Recording (PRML)

Description

The HI3026 is an 8-bit, high-speed, flash analog-to-digital converter optimized for high speed, low power, and ease of use. With a 120 MSPS encode rate capability and full-power analog bandwidth of 150MHz, this component is ideal for applications requiring the highest possible dynamic performance.

To minimize system cost and power dissipation, only a +5V power supply is required. The HI3026's clock input interfaces directly to TTL, ECL, or PECL logic and will operate with single-ended inputs. The user may select 16-bit demultiplexed output or 8-bit single channel digital outputs. The demultiplexed mode interleaves the data through two 8-bit channels at $^1/_2$ the clock rate. Operation in demultiplexed mode reduces the speed and cost of external digital interfaces, while allowing the A/D converter to be clocked to the full 120 MSPS conversion rate.

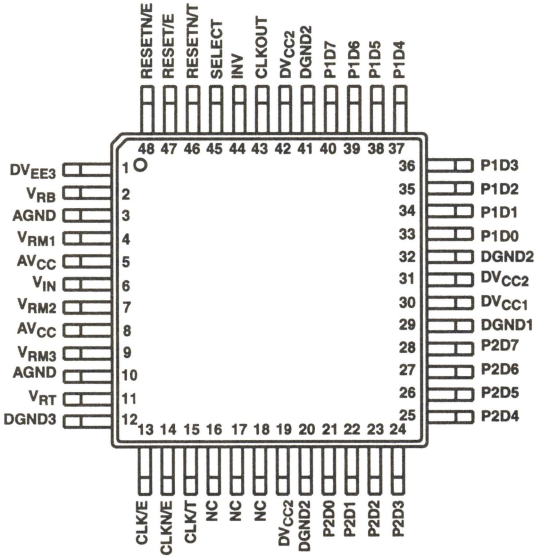
Fabricated with an advanced Bipolar process, the HI3026 is provided in a space-saving 48-lead MQFP surface mount plastic package and is specified over the -20°C to 75°C temperature range. For a faster clock rate, please refer to the HI3026A (140 MSPS), AnswerFAX Document number 4246.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3026JCQ	-20 to 75	48 Ld MQFP	Q48.12x12-S
HI3026EVAL	25	Evaluation Board	

Pinout

HI3026 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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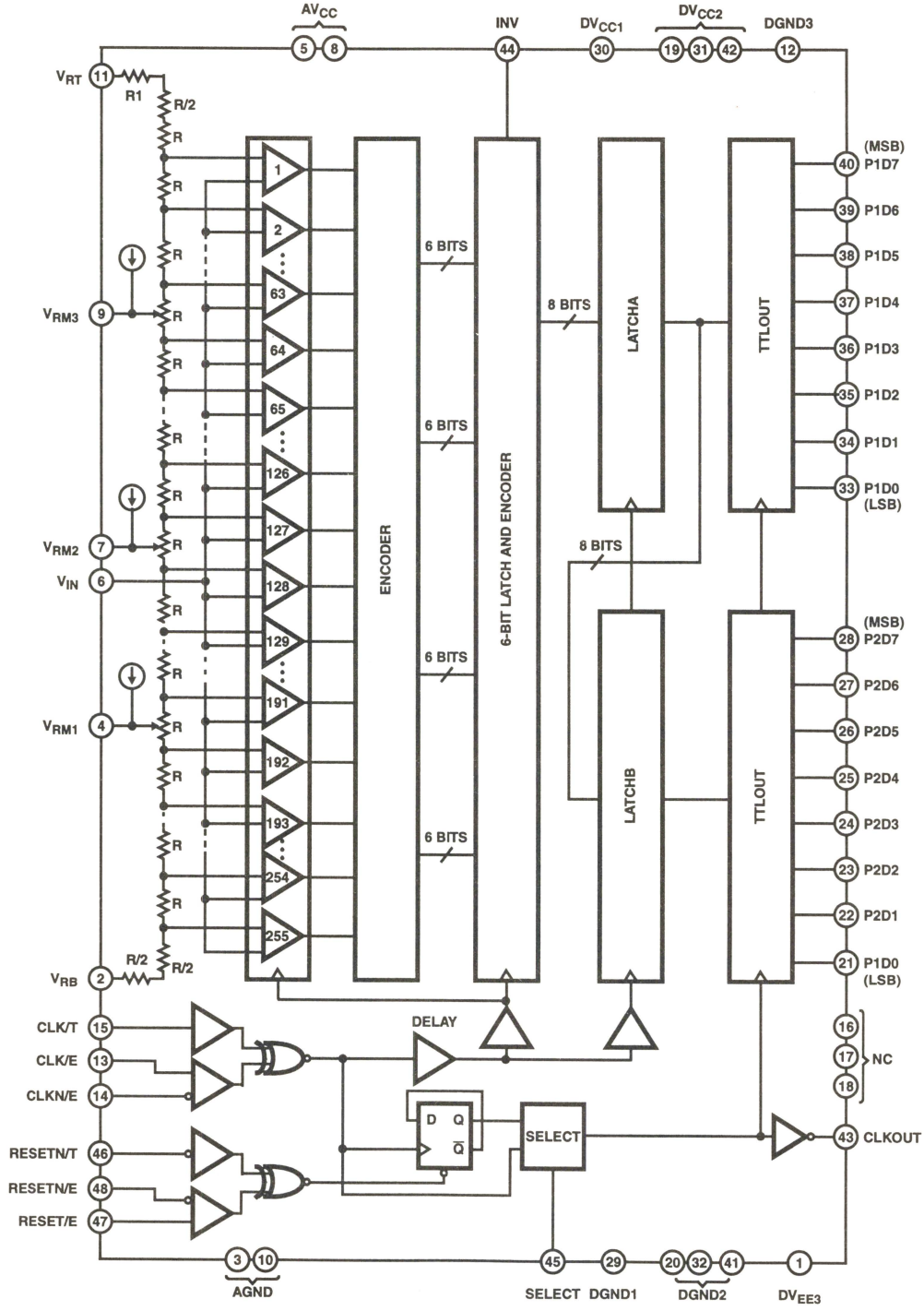
File Number **4109.3**

Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{CC}, DV_{CC1}, DV_{CC2}) ..... -0.5V to 7.0V
($DGND3$) ..... -0.5V to 7.0V
(DV_{EE3}) ..... -7.0V to 0.5V
($DGND3 - DV_{EE3}$) ..... -0.5V to 7.0V
Analog Input Voltage (V_{IN}) ..... V_{RT} - 2.7V to AV_{CC}
Reference Input Voltage (V_{RT}) ..... 2.7V to AV_{CC}
(V_{RB}) ..... V_{IN} - 2.7V to AV_{CC}
($|V_{RT} - V_{RB}|$) 2.5V
Digital Input Voltage
ECL (***/E (Note 2)) ..... DV_{EE3} to 0.5V
PECL (***/E) ..... -0.5V to DGND3
TTL (***/T, INV) ..... -0.5V to DV_{CC1}
Other (SELECT) ..... -0.5V to DV_{CC1}
V_{ID} (|***/E - ***N/E|) (Note 3)) 2.7V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	63

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

Recommended Operating Conditions

WITH A SINGLE POWER SUPPLY	MIN	TYP	MAX
Supply Voltage			
DV_{CC1}, DV_{CC2}, AV_{CC}	+4.75	+5.0	+5.25V
DGND1, DGND2, AGND	-0.05	0	+0.05V
DGND3	+4.75	+5.0	+5.25V
DV_{EE3}	-0.05	0	+0.05V
Analog Input Voltage (V_{IN})	V_{RB}	-	V_{RT}
Reference Input Voltage			
V_{RT}	+2.9	-	+4.1V
V_{RB}	1.4	-	+2.6V
$\|V_{RT} - V_{RB}\|$	1.5	-	2.1V
Digital Input Voltage			
PECL (***/E) V_{IH}	DGND3 - 1.05		DGND3 - 1.4V
PECL (***/E) V_{IL}	DGND3 - 3.2		DGND3 - 1.4V
TTL (***/T, INV) V_{IH}	2.0V	-	-
TTL (***/T, INV) V_{IL}	-	-	0.8V
Other (SELECT) V_{IH}	-	DV_{CC1}	-
Other (SELECT) V_{IL}	-	DGND1	-
VID (Note 3) (|***/E- ***N/E|)	0.4	0.8	-
Max Conversion Rate (f_C, Straight Mode)	100 MSPS	-	-
Max Conversion Rate (f_C, DMUX Mode)	120 MSPS	-	-
Ambient Temperature (T_A)	-20°C to 75°C		

WITH DUAL POWER SUPPLIES	MIN	TYP	MAX
Supply Voltage			
DV_{CC1}, DV_{CC2}, AV_{CC}	+4.75	+5.0	+5.25V
DGND1, DGND2, AGND	-0.05	0	+0.05V
DGND3	-0.05	0	+0.05V
DV_{EE3}	-5.5	-5.0	-4.75V
Analog Input Voltage (V_{IN})	V_{RB}	-	V_{RT}
Reference Input Voltage			
V_{RT}	+2.9	-	+4.1V
V_{RB}	1.4	-	+2.6V
$\|V_{RT} - V_{RB}\|$	1.5	-	2.1V
Digital Input Voltage			
ECL (***/E) V_{IH}	DGND3 - 1.05		DGND3 - 0.5V
ECL (***/E) V_{IL}	DGND3 - 3.2		DGND3 - 1.4V
TTL (***/T, INV) V_{IH}	2.0V	-	-
TTL (***/T, INV) V_{IL}	-	-	0.8V
Other (SELECT) V_{IH}	-	DV_{CC1}	-
Other (SELECT) V_{IL}	-	DGND1	-
V_{ID} (Note 3) (|***/E- ***N/E|)	0.4	0.8	-
Max Conversion Rate (f_C, Straight Mode)	100 MSPS	-	-
Max Conversion Rate (f_C, DMUX Mode)	120 MSPS	-	-
Ambient Temperature (T_A)	-20°C to 75°C		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. ***/E and ***T indicate CLK/E and CLK/T, etc., for the pin name.
3. V_{ID}: Input Voltage Differential.

Electrical Specifications

$DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, $T_A = 25^oC$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		-	8	-	Bits
DC CHARACTERISTICS					
Integral Linearity Error, E_{IL}	$V_{IN} = 2V_{P-P}$, f_C = 5 MSPS	-	-	±0.5	LSB
Differential Linearity Error, E_{DL}		-	-	±0.5	LSB
ANALOG INPUT					
Analog Input Capacitance, C_{IN}	V_{IN} = +3.0V +0.07V_{RMS}	-	21	-	pF
Analog Input Resistance, R_{IN}		4	-	50	kΩ
Analog Input Current, I_{IN}		0	-	500	µA

Electrical Specifications $DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, $T_A = 25^oC$ **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUT					
Reference Resistance (Note 4), R_{REF}		75	115	155	Ω
Reference Current (Note 5), I_{REF}		9.7	17.4	28	mA
Offset Voltage V_{RT} Side, EOT		2	-	15	mV
Offset Voltage V_{RB} Side, EOB		2	-	10	mV
DIGITAL INPUT (ECL, PECL)					
Digital Input Voltage: High, V_{IH}		DGND3 - 1.05	-	DGND3 - 0.5	V
Digital Input Voltage: Low, V_{IL}		DGND3 - 3.2	-	DGND3 -1.4	V
Threshold Voltage, V_{TH}		-	DGND3 - 1.2	-	V
Digital Input Current: High, I_{IH}	V_{IH} = DGND3 - 0.8V	-50	-	+50	µA
Digital Input Current: Low, I_{IL}	V_{IL} = DGND3 - 1.6V	-75	-	0	µA
Digital Input Capacitance		-	-	5	pF
DIGITAL INPUT (TTL)					
Digital Input Voltage: High, V_{IH}		2.0	-	-	V
Digital Input Voltage: Low, V_{IL}		-	-	0.8	V
Threshold Voltage, V_{TH}		-	1.5	-	V
Digital Input Current: High, I_{IH}	V_{IH} = 3.5V	-50	-	0	µA
Digital Input Current: Low, I_{IL}	V_{IL} = 0.2V	-500	-	0	µA
Digital Input Capacitance		-	-	5	pF
DIGITAL OUTPUT (TTL)					
Digital Output Voltage: High, V_{OH}	I_{OH} = -2mA	2.4	-	-	V
Digital Output Voltage: Low, V_{OL}	I_{OL} = 1mA	-	-	0.5	V
SWITCHING CHARACTERISTICS					
Maximum Conversion Rate, f_C	DMUX Mode	120	-	-	MSPS
Aperture Jitter, t_{AJ}		-	10	-	ps
Sampling Delay, t_{DS}		3	4.5	6	ns
Clock High Pulse Width, t_{PW1}	CLK	3.2	-	-	ns
Clock Low Pulse Width, t_{PW0}	CLK	3.2	-	-	ns
Reset Pulse Width, t_{PWR} (Note 6)	RESETN	t x 2	-	-	ns
RESET Signal Setup Time, t_{RS}	RESETN-CLK	3.5	-	-	ns
RESET Signal Hold Time, t_{RH}	RESETN-CLK	0	-	-	ns
CLKOUT Output Delay, t_{DCLK}	(C_L = 5pF)	3.5	7	9	ns
Data Output Delay (Note 6), t_{DO1} t_{DO2}	DEMUX Mode (C_L = 5pF)	t	t + 1	t + 2	ns
	(C_L = 5pF)	4.5	8	10	ns
Output Rise Time, t_r	0.8 to 2.0V (C_L = 5pF)	-	2	-	ns
Output Fall Time, t_f	0.8 to 2.0V (C_L = 5pF)	-	2	-	ns
DYNAMIC CHARACTERISTICS					
Input Bandwidth	V_{IN} = $2V_{P-P}$, -3dB	150	-	-	MHz
S/N Ratio	f_C = 120 MSPS, f_{IN} = 1kHz Full Scale, DMUX Mode	-	46	-	dB
	f_C = 120 MSPS, f_{IN} = 29.999MHz Full Scale, DMUX Mode	-	40	-	dB

Electrical Specifications $DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Rate (Note 7)	f_C = 120 MSPS, f_{IN} = 1kHz Full Scale, DMUX Mode, Error > 16 LSB	-	-	10^{-12}	TPS
	f_C = 120 MSPS, f_{IN} = 29.999MHz Full Scale, DMUX Mode, Error > 16 LSB	-	-	10^{-9}	TPS
	f_C = 100 MSPS, f_{IN} = 24.999MHz Full Scale, Straight Mode, Error > 16 LSB	-	-	10^{-9}	TPS
POWER SUPPLY					
Supply Current, I_{CC}		125	145	185	mA
Supply Current, I_{EE}		0.4	0.6	0.8	mA
Power Consumption (Note 8), P_D		660	760	960	mW

NOTES:

4. R_{REF}: Resistance value between V_{RT} and V_{RB}.
5. $I_{REF} = \frac{V_{RT} - V_{RB}}{R_{REF}}$.
6. $T = \frac{1}{f_C}$.
7. The unit of measure TPS: Times Per Sample.
8. $P_D = (I_{CC} + I_{EE}) \bullet V_{CC} + \frac{(V_{RT} - V_{RB})^2}{V_{REF}}$.

Timing Diagrams

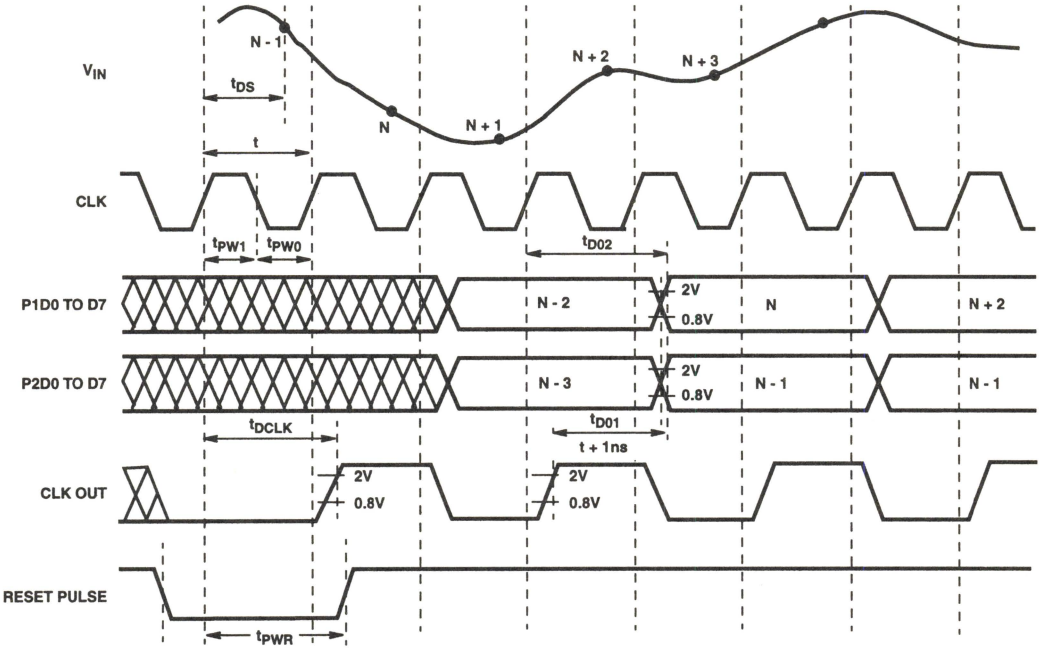


FIGURE 1. DEMUX MODE TIMING CHART (SELECT = V_{CC})

Timing Diagrams

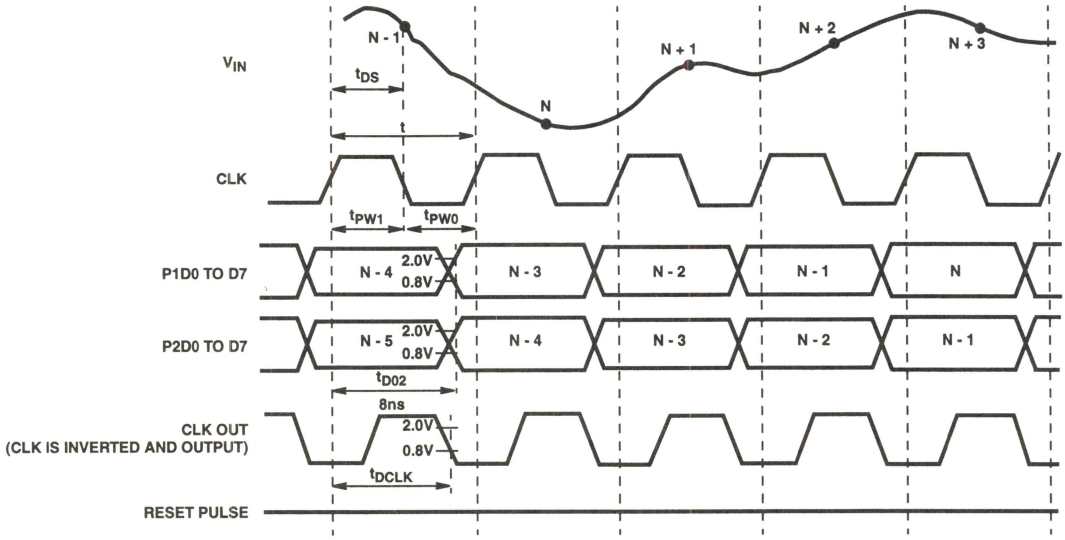


FIGURE 2. STRAIGHT MODE TIMING CHART (SELECT = GND)

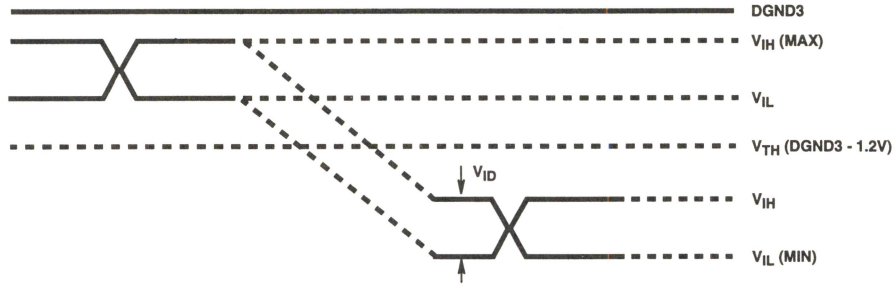
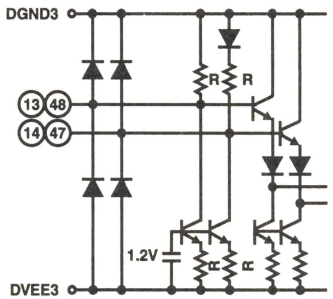
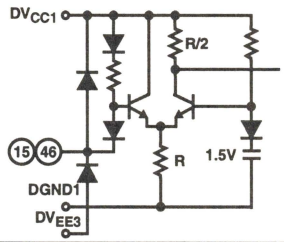
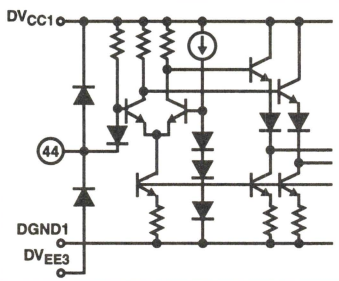
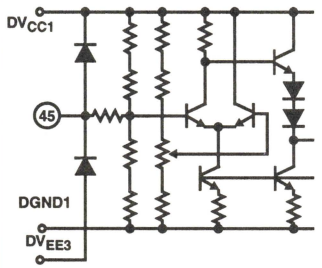


FIGURE 3. ECL AND PECL SWITCHING LEVEL

Pin Descriptions

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
3, 10	AGND		GND		Analog Ground. Separated from the digital ground.
5, 8	AV_{CC}		+5V (Typ)		Analog Power Supply. Separated from the digital power supply.
20, 29 32, 41	DGND1 DGND2		GND		Digital Ground.
19, 30 31, 42	DV_{CC1} DV_{CC2}		+5V (Typ)		Digital Power Supply.
12	DGND3		+5V (Typ) (With a Single Power Supply) GND (With Dual Power Supplies)		Digital Power Supply. Ground for ECL input. -5V for PECL and TTL input.

Pin Descriptions (Continued)

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
1	DV_{EE3}		GND (With a Single Power Supply) +5V (Typ) (With Dual Power Supplies)		Digital Power Supply. Ground for ECL input. -5V for PECL and TTL input.
16, 17, 18	NC				No Connect pin. Not connected with the internal circuits.
13	CLK/E	I	ECL/PECL		Clock Input.
14	CLK/NE	I			CLK/E Complementary Input. When left open, this pin goes to the threshold potential. Only CLK/E can be used for operation, but complementary input is recommended to attain fast and stable operation.
48	RE-SETN/E	I			Reset Input. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
47	RESET/E	I			RESETN/E Complementary Input. When left open, this pin goes to the threshold voltage. Only RESETN/E can be used for operation.
15	CLK/T	I	TTL		Clock input.
46	RESETN/T	I			Reset Input. When left open, this input goes to high level. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
44	INV	I	TTL		Data Output Polarity Inversion Input. When left open, this input goes to high level. (See Table 1; I/O Correspondence Table).
45	SELECT		V_{CC} or Ground		Data Output Mode Selection. (See Table 2; Operating Mode Table).

Pin Descriptions (Continued)

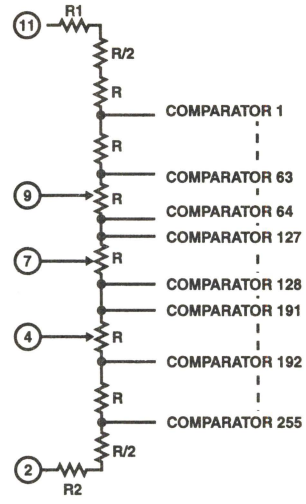
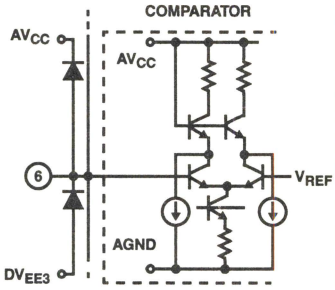
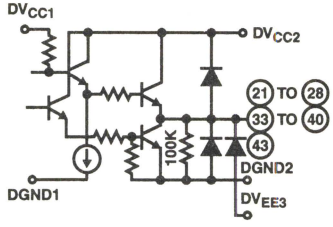
PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
11	V_{RT}	I	4.0V (Typ)		Top Reference Voltage. Bypass to AGND with a 1µF tantal capacitor and a 0.1µF chip capacitor.
9	V_{RM3}		$V_{RB} + \frac{3}{4}(V_{RT} - V_{RB})$		Reference Voltage Mid Point. Bypass to AGND with a 0.1µF chip capacitor.
7	V_{RM2}		$V_{RB} + \frac{2}{4}(V_{RT} - V_{RB})$		Reference Voltage Mid Point. Bypass to AGND with a 0.1µF chip capacitor.
4	V_{RM1}		$V_{RB} + \frac{1}{4}(V_{RT} - V_{RB})$		Reference Voltage Mid Point. Bypass to AGND with a 0.1µF chip capacitor.
2	V_{RB}	I	2.0V (Typ)		Bottom Reference Voltage. Bypass to AGND with a 1µF tantal capacitor and a 0.1µF chip capacitor.
6	V_{IN}	I	V_{RT} to V_{RB}		Analog Input.
33 to 40	P1D0 to P1D7	O	TTL		Port 1 Side Data Output.
21 to 28	P2D0 to P2D7	O			Port 2 Side Data Output.
43	CLKOUT	O			Clock Output. (See Table 2; Operating Mode Table).

TABLE 1. A/D CODE TABLE

V_{IN}	STEP	INV 1 D7							D0	INV 0 D7							D0
V_{RT}	255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	254	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
	•				•								•				
	•				•								•				
	•				•								•				
V_{RM2}	128	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	127	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	•				•								•				
	•				•								•				
	•				•								•				
	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
V_{RB}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Notes on Operation

- The HI3026 is a high-speed A/D converter which is capable of TTL, ECL and PECL level clock input. Characteristic impedance should be properly matched to ensure optimum performance during high-speed operation.
- The power supply and grounding have a profound influence on converter performance. The power supply and grounding method are particularly important during high-speed operation. General points for caution are as follows:
  - The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using a multi-layer board.
  - To prevent interference between AGND and DGND and between AV_{CC} and DV_{CC}, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AV_{CC} and DV_{CC} lines at one point each, via a ferrite-bead filter. Shorting the AGND and DGND patterns in one place immediately under the A/D converter improves A/D converter performance.
  - Ground the power supply pins (AV_{CC}, DV_{CC1}, DV_{CC2}, DV_{EE3}) as close to each pin as possible with a 0.1µF or larger ceramic chip capacitor. (Connect the AV_{CC} pin to the AGND pattern and the DV_{CC1}, DV_{CC2}, DV_{EE3} pins to the DGND pattern).
  - The digital output wiring should be as short as possible. If the digital output wiring is long, the wiring capacitance will increase, deteriorating the output slew rate and resulting in reflection to the output waveform since the original output slew rate is quite fast.
- The analog input pin V_{IN} has an input capacitance of approximately 21pF. To drive the A/D converter with proper frequency response, it is necessary to prevent performance deterioration due to parasitic capacitance or parasitic inductance by using a large capacity drive circuit; keeping wiring as short as possible, and using chip parts for resistors and capacitors, etc.
- The V_{RT} and V_{RB} pins must have adequate bypass to protect them from high-frequency noise. Bypass them to AGND with approximately 1µF tantal capacitor and, 0.1µF capacitor. At this time, approximately DGND3 - 1.2V voltage is generated. However, this is not recommended for use as threshold voltage V_{BB} as it is too weak.

When the digital input level is ECL or PECL level, ***/E pins should be used and ***/T pins left open. When the digital input level is TTL, ***/T pins should be used and III/E pins left open.

Test Circuits

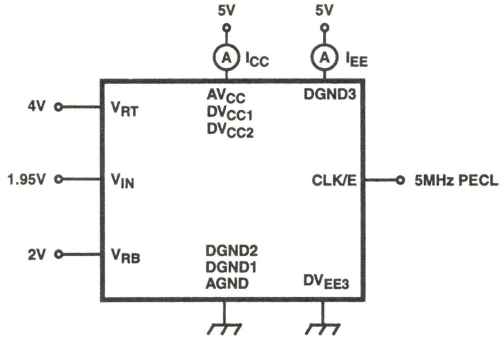


FIGURE 4. CURRENT CONSUMPTION MEASUREMENT CIRCUIT

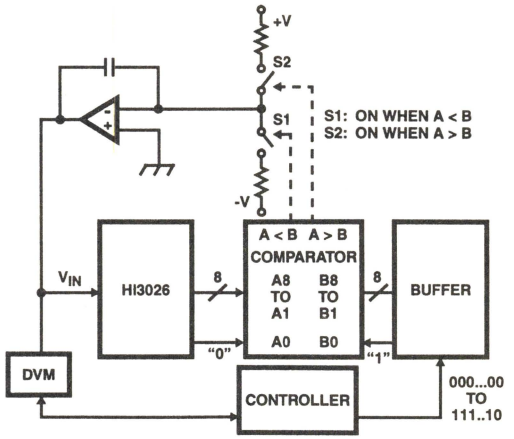


FIGURE 5. INTEGRAL LINEARITY ERROR/DIFFERENTIAL LINEARITY ERROR MEASUREMENT CIRCUIT

Test Circuits (Continued)

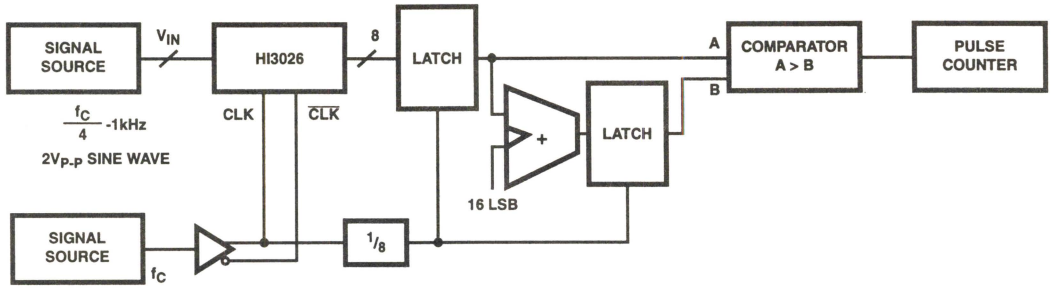


FIGURE 6. ERROR RATE MEASUREMENT CIRCUIT

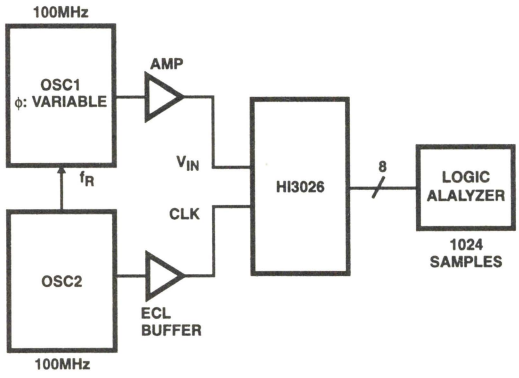
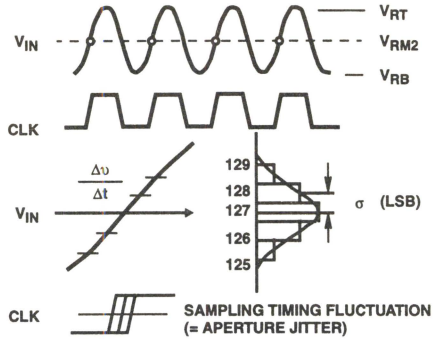


FIGURE 7. SAMPLING DELAY/APERTURE JITTER MEASUREMENT CIRCUIT



NOTE: Where σ (LSB) is the deviation of the output codes when the largest slew rate point is sampled at the clock which has exactly the same frequency as the analog input signal, the aperture jitter t_{AJ} is:

$$t_{AJ} = \left(\sigma / \frac{\Delta v}{\Delta t}\right) = \sigma / \left(\frac{256}{2} \times 2\pi f\right).$$

FIGURE 8. APERTURE JITTER MEASUREMENT METHOD

Operating Modes

The HI3026 has two types of operating modes which are selected with Pin 45 (SELECT).

TABLE 2. OPERATING MODE TABLE

OPERATING MODE	SELECT	MAXIMUM CONVERSION RATE	DATA OUTPUT	CLOCK OUTPUT
DMUX Mode	V_{CC}	120 MSPS	Demultiplexed Output 60 MBPS	The input clock is $^1/_2$ frequency divided and output at 60MHz.
Straight Mode	GND	100 MSPS	Straight Output 100 MBPS	The input clock is inverted and output at 100MHz.

DMUX Mode (See Application Circuits, Figures 18, 19, 20)

Set the SELECT pin to V_{CC} for this mode. In this mode, the clock frequency is divided by 2 in the IC, and the data is output after being demultiplexed by this $^1/_2$ frequency divided clock. The $^1/_2$ frequency divided clock, which has adequate setup time and hold time for the output data, is output from the CLKOUT pin.

When using multiple HI3026 units in parallel in this mode, differences in the start timing of the $^1/_2$ frequency divided clock may cause operation as shown in the figure below. As a countermeasure, the HI3026 is equipped with a function which resets the $^1/_2$ frequency divided clock. When resetting this clock, the RESET pulse must be input to the RESET pin. See the Timing Charts for the RESET pulse input timing. The A/D converter can operate at f_C (Min) = 120 MSPS in this mode.

Straight Mode (See Application Circuits, Figures 21, 22, 23)

Set the SELECT pin to GND for this mode. In this mode, data output can be obtained in accordance with the clock frequency applied to the A/D converter for applications which use the clock applied to the A/D converter as the system clock.

The A/D converter can operate at f_C (Min) = 100 MSPS in this mode.

Digital Input Level and Supply Voltage Settings

The logic input level for the HI3026 supports ECL, PECL and TTL levels.

The power supplies (DV_{EE3}, DGND3) for the logic input block must be set to match the logic input (CLK and RESET signals) level.

TABLE 3. LOGIC INPUT LEVEL AND POWER SUPPLY SETTINGS

DIGITAL INPUT LEVEL	DV_{EE3}	DGND3	SUPPLY VOLTAGE	APPLICATION CIRCUITS
ECL	-5V	0V	5V	Figures 18, 21
PECL	0V	+5V	+5V	Figures 19, 22
TTL	0V	+5V	+5V	Figures 20, 23

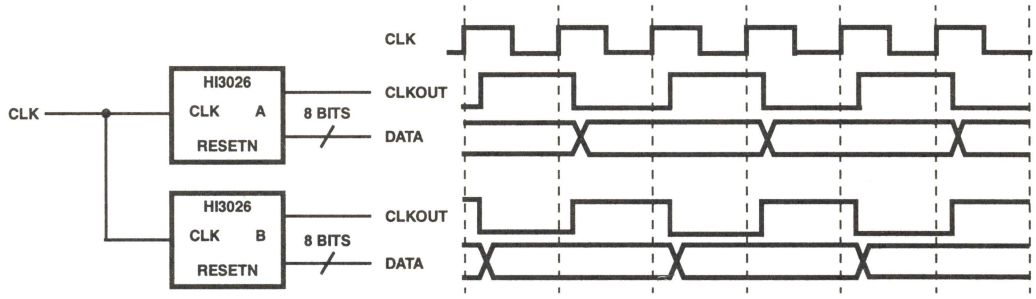


FIGURE 9. WHEN THE RESET PULSE IS NOT USED

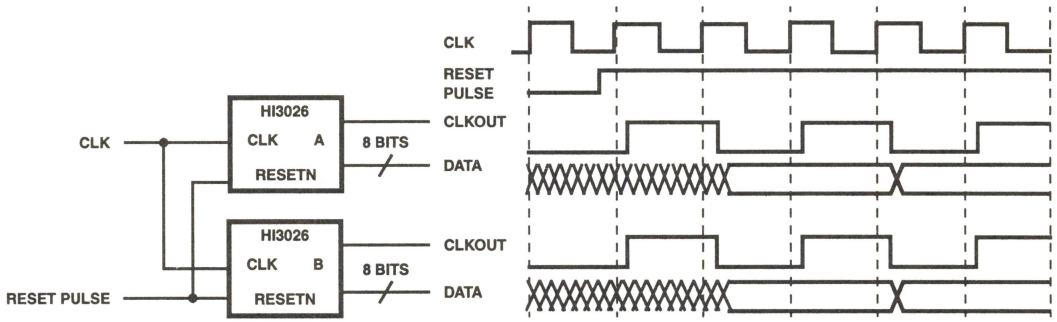


FIGURE 10. WHEN THE RESET PULSE IS USED

Typical Performance Curves

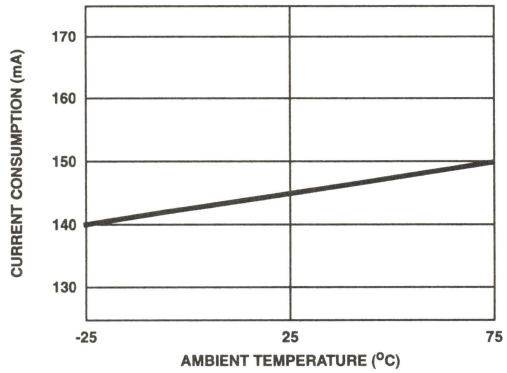


FIGURE 11. CURRENT CONSUMPTION vs AMBIENT TEMPERATURE CHARACTERISTICS

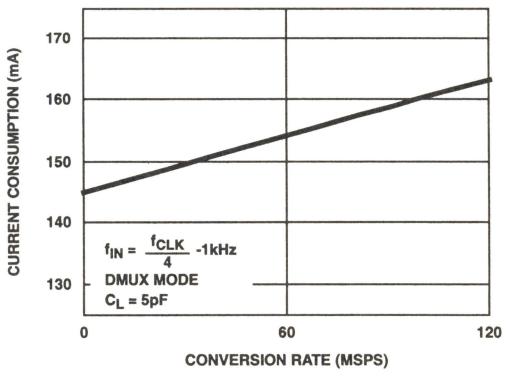


FIGURE 12. CURRENT CONSUMPTION vs CONVERSION RATE CHARACTERISTICS RESPONSE

Typical Performance Curves (Continued)

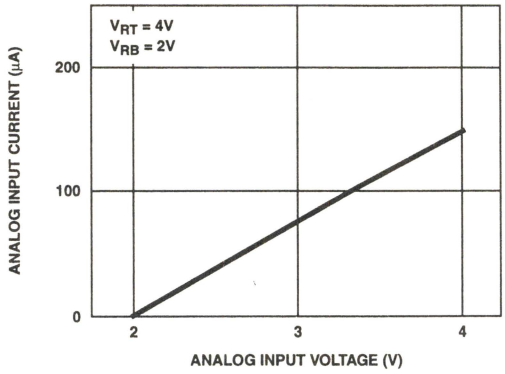


FIGURE 13. ANALOG INPUT CURRENT vs ANALOG INPUT VOLTAGE CHARACTERISTICS

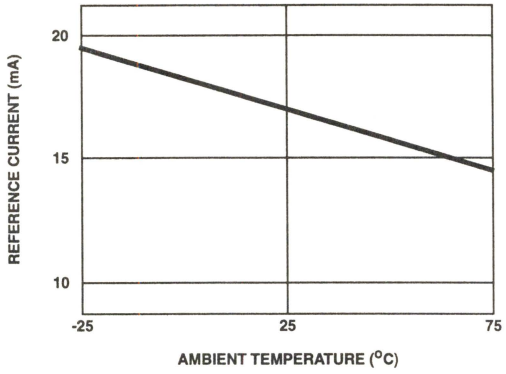


FIGURE 14. REFERENCE CURRENT vs AMBIENT TEMPERATURE CHARACTERISTICS

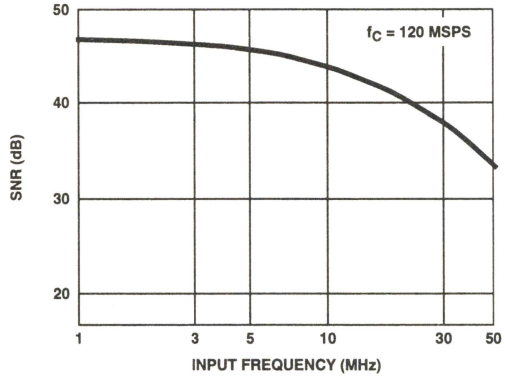


FIGURE 15. SNR vs INPUT FREQUENCY RESPONSE

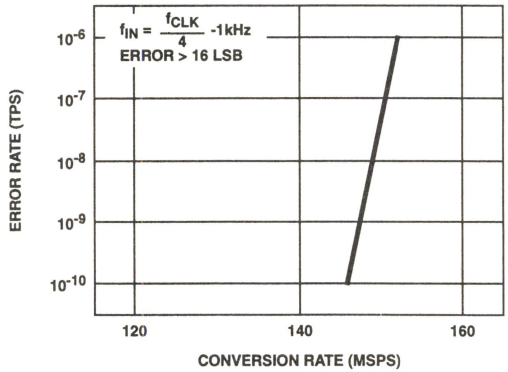


FIGURE 16. ERROR RATE vs CONVERSION RATE CHARACTERISTICS

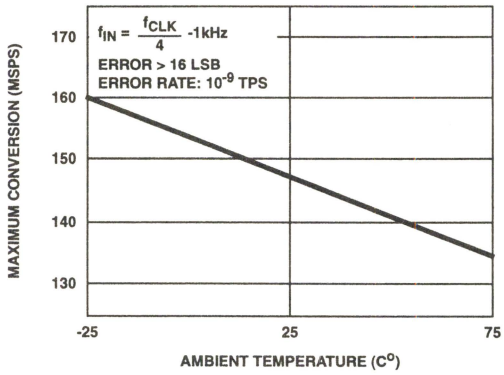


FIGURE 17. MAXIMUM CONVERSION RATE vs AMBIENT TEMPERATURE CHARACTERISTICS

Application Circuits

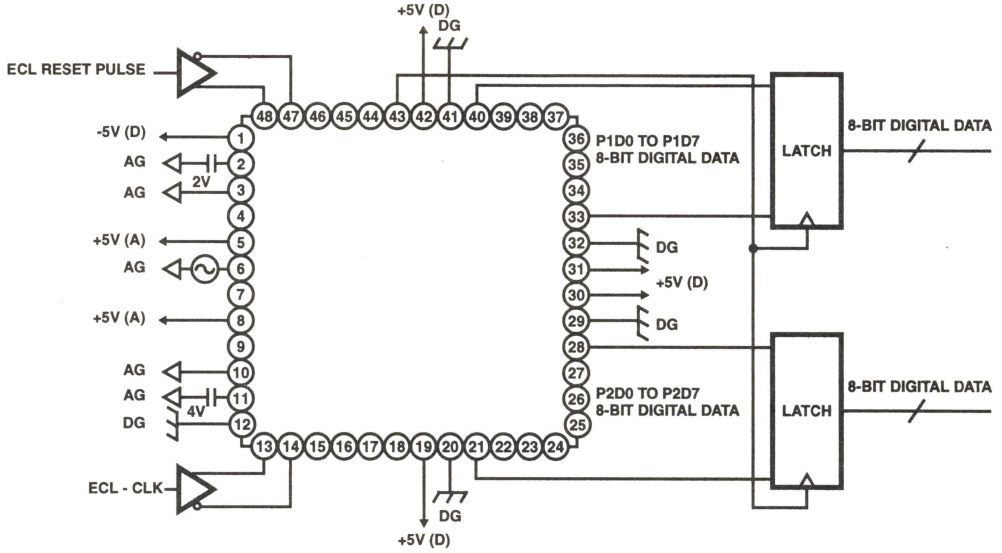


FIGURE 18. DMUX ECL INPUT

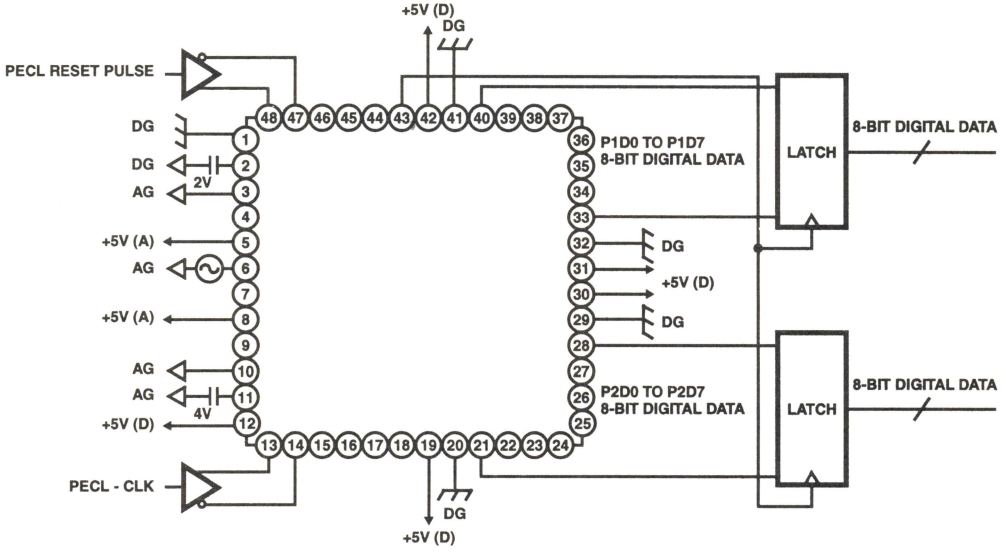


FIGURE 19. DMUX PECL INPUT

Application Circuits (Continued)

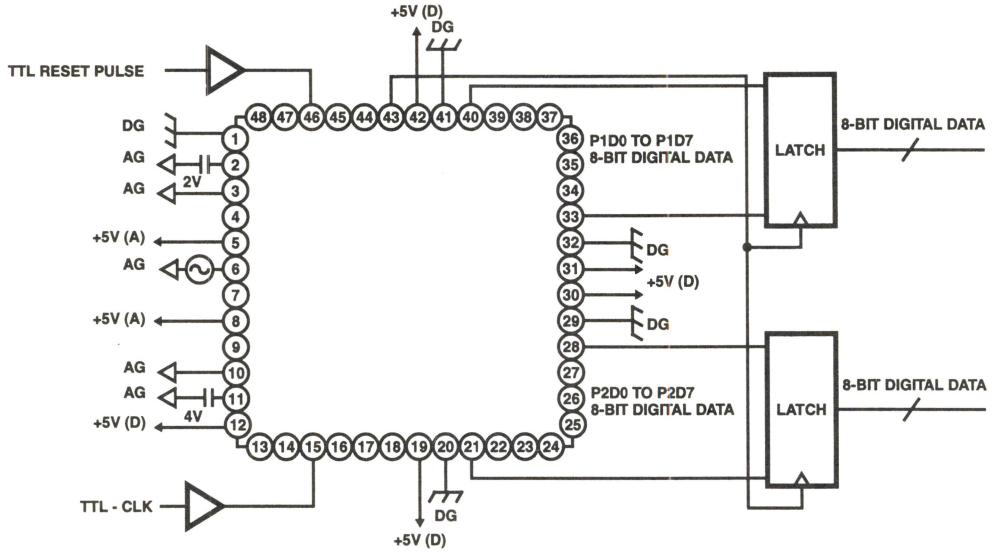


FIGURE 20. DMUX TTL INPUT

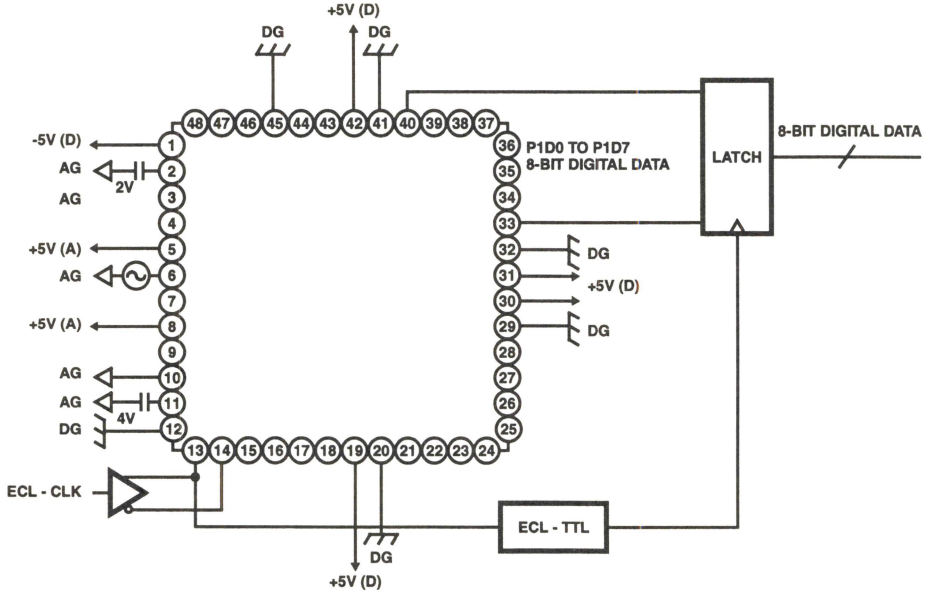


FIGURE 21. STRAIGHT ECL INPUT

Application Circuits (Continued)

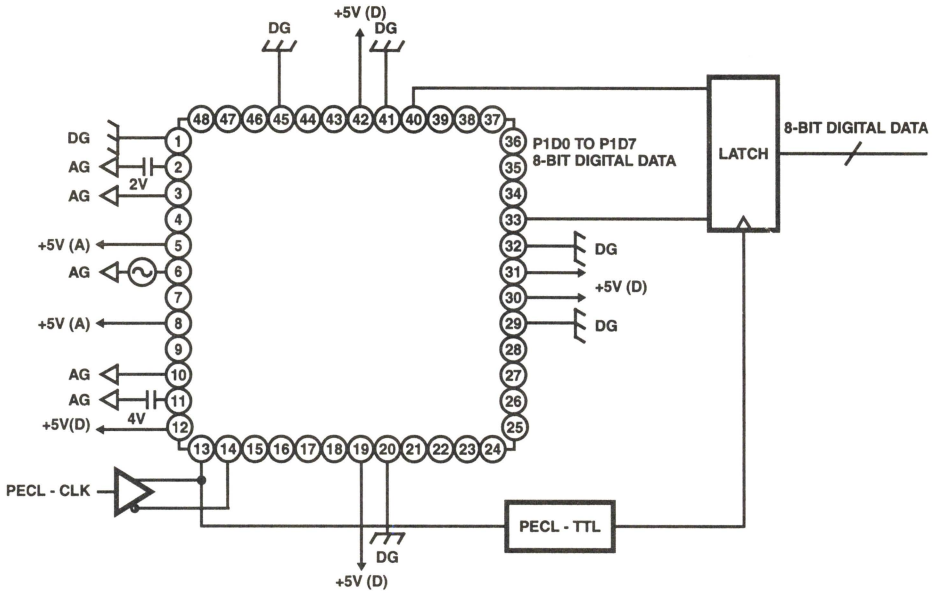


FIGURE 22. STRAIGHT PECL INPUT

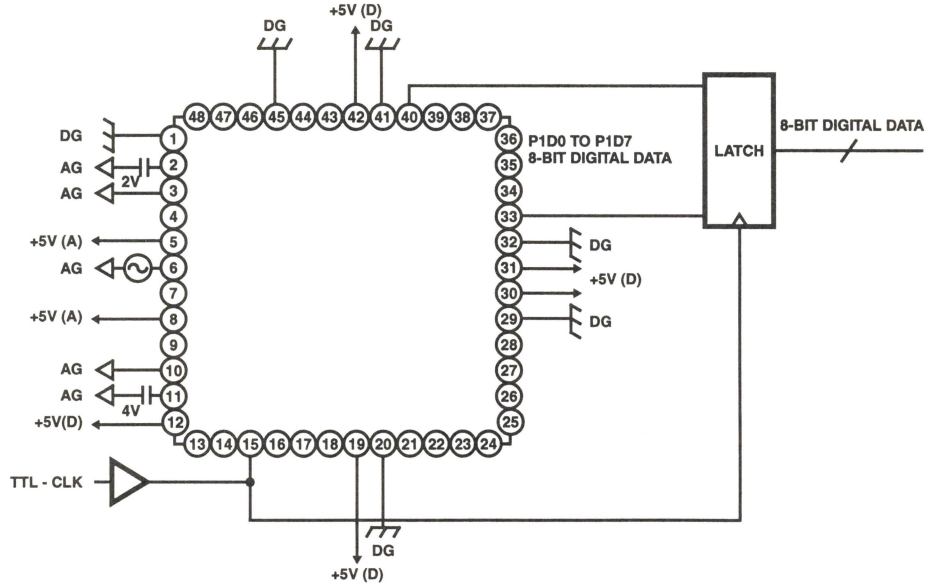


FIGURE 23. STRAIGHT TTL INPUT

Application Circuits (Continued)

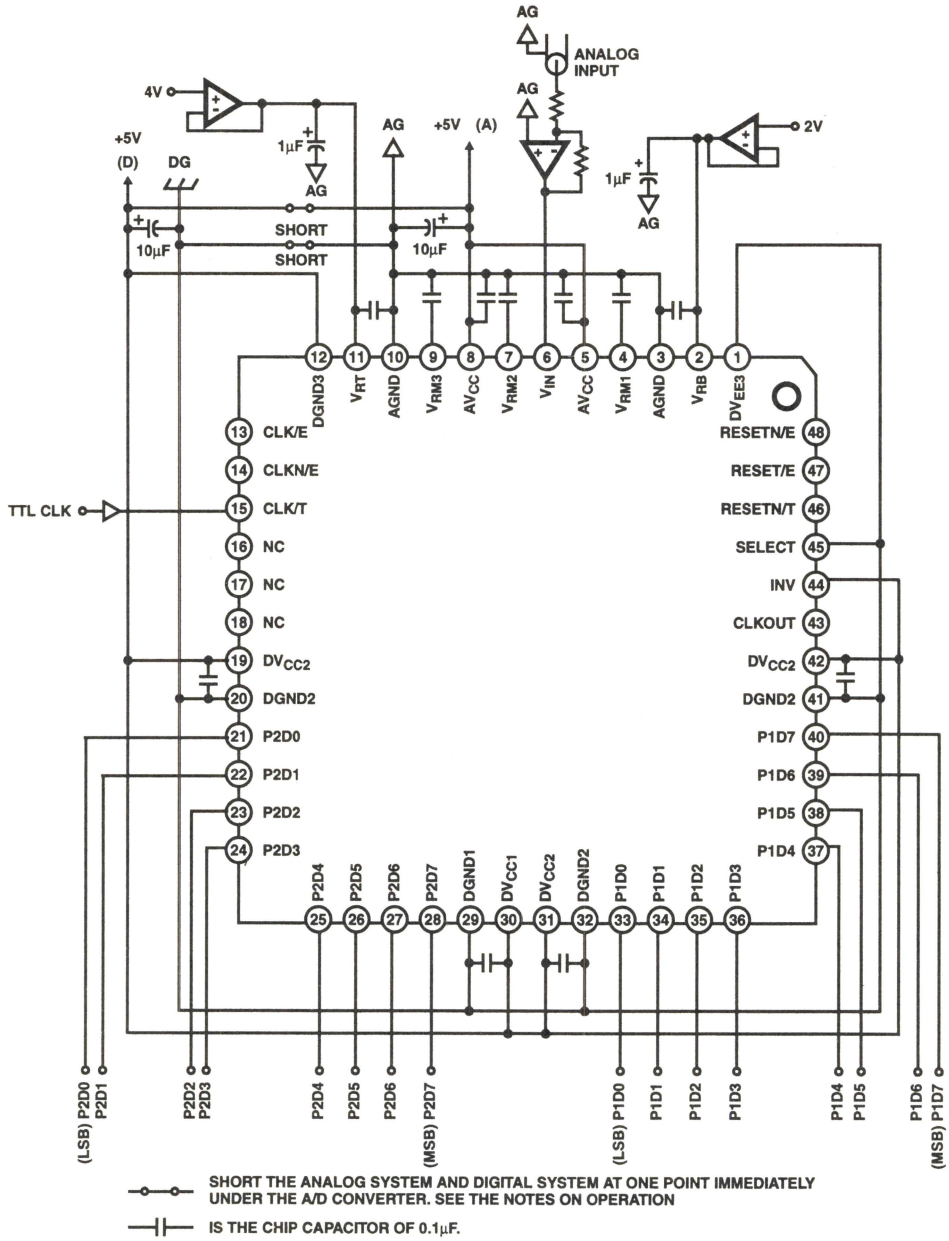


FIGURE 24. STRAIGHT MODE TTL I/O (WHEN A SINGLE POWER SUPPLY IS USED)

HI3026A

August 1997

8-Bit, 140 MSPS, Flash A/D Converter

Features

- Differential Linearity Error . . . . . ±0.5 LSB
- Integral Linearity Error . . . . . ±0.5 LSB
- Integral Linearity Compensation Circuit
- Low Input Capacitance 21pF
- Wide Analog Input Bandwidth 150MHz
- Low Power Consumption 790mW
- Internal $^1/_2$ Frequency Divider Circuit (With Reset Function)
- CLK/2 Clock Output Pin
- Compatible with ECL, PECL and TTL Digital Input Levels
- 1:2 Demultiplexed Output
- Direct Replacement for Sony CXA3026A

Applications

- RGB Graphics Processing (LCD, PDP)
- Digital Oscilloscopes
- Digital Communications (QPSK, QAM)
- Magnetic Recording (PRML)

Description

The HI3026A is an 8-bit, high-speed, flash analog-to-digital converter optimized for high speed, low power, and ease of use. With a 140 MSPS encode rate capability and full-power analog bandwidth of 150MHz, this component is ideal for applications requiring the highest possible dynamic performance.

To minimize system cost and power dissipation, only a +5V power supply is required. The HI3026A's clock input interfaces directly to TTL, ECL, or PECL logic and will operate with single-ended inputs. The user may select 16-bit demultiplexed output or 8-bit single-channel digital outputs. The demultiplexed mode interleaves the data through two 8-bit channels at $^1/_2$ the clock rate. Operation in demultiplexed mode reduces the speed and cost of external digital interfaces, while allowing the A/D converter to be clocked to the full 140 MSPS conversion rate.

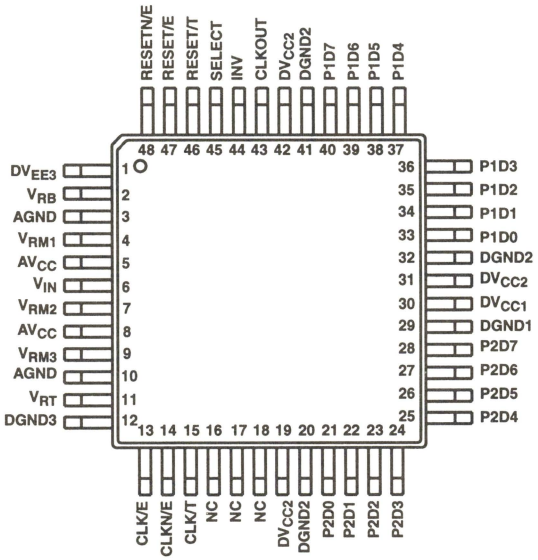
Fabricated with an advanced bipolar process, the HI3026A is provided in a space-saving 48-lead MQFP surface mount plastic package and is specified over the -20°C to 75°C temperature range.

Ordering Information

PART NUMBER	TEMPT. RANGE (°C)	PACKAGE	PKG. NO.
HI3026AJCQ	-20 to 75	48 Ld MQFP	Q48.12x12-S
HI3026AEVAL	25	Evaluation Board	

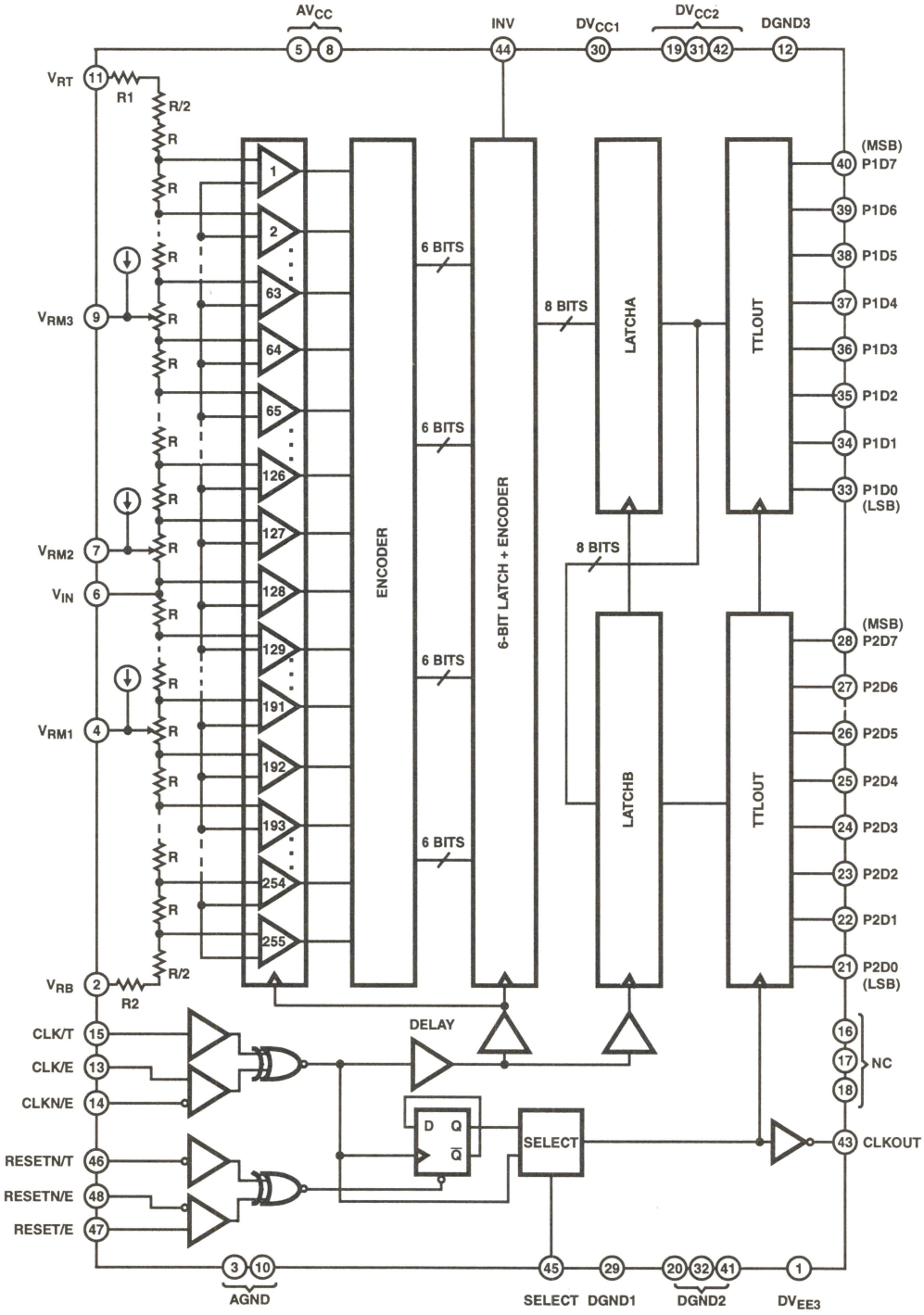
Pinout

HI3026A (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage
- AV_{CC}, DV_{CC1}, DV_{CC2} ..... -0.5V to 7.0V
- DGND3 ..... -0.5V to 7.0V
- DV_{EE3} ..... -7.0V to 0.5V
- DGND3 - DV_{EE3} ..... -0.5V to 7.0V

Analog Input Voltage (V_{IN}) ..... V_{RT} - 2.7V to AV_{CC}

Reference Input Voltage
- V_{RT} ..... 2.7V to AV_{CC}
- V_{RB} ..... V_{IN} - 2.7V to AV_{CC}
- $|V_{RT} - V_{RB}|$ 2.5V

Digital Input Voltage
- ECL (***/E (Note 2)) ..... DV_{EE3} to 0.5V
- PECL (***/E) ..... -0.5V to DGND3
- TTL (***/T, INV) ..... -0.5V to DV_{CC1}
- Other (SELECT) ..... -0.5V to DV_{CC1}
- V_{ID} (I***/E - ***N/EI (Note 3)) 2.7V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	63

Maximum Junction Temperature ..... 150°C

Maximum Storage Temperature Range ..... -65°C to 150°C

Maximum Lead Temperature (Soldering 10s) ..... 300°C
(MQFP - Lead Tips Only)

Recommended Operating Conditions

WITH A SINGLE POWER SUPPLY	MIN	TYP	MAX
Supply Voltage			
DV_{CC1}, DV_{CC2}, AV_{CC}	+4.75	+5.0	+5.25V
DGND1, DGND2, AGND	-0.05	0	+0.05V
DGND3	+4.75	+5.0	+5.25V
DV_{EE3}	-0.05	0	+0.05V
Analog Input Voltage (V_{IN})	V_{RB}	-	V_{RT}
Reference Input Voltage			
V_{RT}	+2.9	-	+4.1V
V_{RB}	1.4	-	+2.6V
$\|V_{RT} - V_{RB}\|$	1.5	-	2.1V
Digital Input Voltage			
PECL (***/E) V_{IH}	DGND3 - 1.05		DGND3 - 1.4V
PECL (***/E) V_{IL}	DGND3 - 3.2		DGND3 - 1.4V
TTL (***/T, INV) V_{IH}	2.0V	-	-
TTL (***/T, INV) V_{IL}	-	-	0.8V
Other (SELECT) V_{IH}	-	DV_{CC1}	-
Other (SELECT) V_{IL}	-	DGND1	-
V_{ID} (Note 3) (I***/E- ***N/EI)	0.4	0.8	-
Max Conversion Rate (f_C, Straight Mode)	100 MSPS	-	-
Max Conversion Rate (f_C, DMUX Mode)	140 MSPS	-	-
Ambient Temperature (T_A)	-20°C to 75°C		

WITH DUAL POWER SUPPLIES	MIN	TYP	MAX
Supply Voltage			
DV_{CC1}, DV_{CC2}, AV_{CC}	+4.75	+5.0	+5.25V
DGND1, DGND2, AGND	-0.05	0	+0.05V
DGND3	-0.05	0	+0.05V
DV_{EE3}	-5.5	-5.0	-4.75V
Analog Input Voltage (V_{IN})	V_{RB}	-	V_{RT}
Reference Input Voltage			
V_{RT}	+2.9	-	+4.1V
V_{RB}	1.4	-	+2.6V
$\|V_{RT} - V_{RB}\|$	1.5	-	2.1V
Digital Input Voltage			
ECL (***/E) V_{IH} DGND3	DGND3 - 1.05		DGND3 - 0.5V
ECL (***/E) V_{IL} DGND3	DGND3 - 3.2		DGND3 - 1.4V
TTL (***/T, INV) V_{IH}	2.0V	-	-
TTL (***/T, INV) V_{IL}	-	-	0.8V
Other (SELECT) V_{IH}	-	DV_{CC1}	-
Other (SELECT) V_{IL}	-	DGND1	-
V_{ID} (Note 3) (I***/E- ***N/EI)	0.4	0.8	-
Max Conversion Rate (f_C, Straight Mode)	100 MSPS	-	-
Max Conversion Rate (f_C, DMUX Mode)	140 MSPS	-	-
Ambient Temperature (T_A)	-20°C to 75°C		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. ***/E and ***T indicate CLK/E and CLK/T, etc. for the pin name.
3. V_{ID}: Input Voltage Differential.

Electrical Specifications

$DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution			-	8	-	Bits
DC CHARACTERISTICS						
Integral Linearity Error	E_{IL}	V_{IN} = $2V_{P-P}$, f_C = 5 MSPS	-	-	±0.5	LSB
Differential Linearity Error	E_{DL}		-	-	±0.5	LSB

Electrical Specifications $DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, T_A = 25°C **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Analog Input Capacitance	C_{IN}	V_{IN} = +3.0V + 0.07V_{RMS}	-	21	-	pF
Analog Input Resistance	R_{IN}		4	-	50	kΩ
Analog Input Current	I_{IN}		0	-	500	µA
REFERENCE INPUT						
Reference Resistance (Note 4)	R_{REF}		75	115	155	Ω
Reference Current (Note 5)	I_{REF}		9.7	17.4	28	mA
Offset Voltage, V_{RT} Side	EOT		2	-	15	mV
Offset Voltage, V_{RB} Side	EOB		2	-	10	mV
DIGITAL INPUT (ECL, PECL)						
Digital Input Voltage: High	V_{IH}		DGND3 - 1.05	-	DGND3 - 0.5	V
Digital Input Voltage: Low	V_{IL}		DGND3 - 3.2	-	DGND3 - 1.4	V
Threshold Voltage	V_{TH}		-	DGND3 - 1.2	-	V
Digital Input Current: High	I_{IH}	V_{IH} = DGND3 - 0.8V	-50	-	+50	µA
Digital Input Current: Low	I_{IL}	V_{IL} = DGND3 - 1.6V	-75	-	0	µA
Digital Input Capacitance			-	-	5	pF
DIGITAL INPUT (TTL)						
Digital Input Voltage: High	V_{IH}		2.0	-	-	V
Digital Input Voltage: Low	V_{IL}		-	-	0.8	V
Threshold Voltage	V_{TH}		-	1.5	-	V
Digital Input Current: High	I_{IH}	V_{IH} = 3.5V	-50	-	0	µA
Digital Input Current: Low	I_{IL}	V_{IL} = 0.2V	-500	-	0	µA
Digital Input Capacitance			-	-	5	pF
DIGITAL OUTPUT (TTL)						
Digital Output Voltage: High	V_{OH}	I_{OH} = -2mA	2.4	-	-	V
Digital Output Voltage: Low	V_{OL}	I_{OL} = 1mA	-	-	0.5	V
SWITCHING CHARACTERISTICS						
Maximum Conversion Rate	f_C	DMUX Mode	140	-	-	MSPS
Aperture Jitter	t_{AJ}		-	10	-	ps
Sampling Delay	t_{DS}		3	4.5	6	ns
Clock High Pulse Width	t_{PW1}	CLK	2.8	-	-	ns
Clock Low Pulse Width	t_{PW0}	CLK	2.8	-	-	ns
Reset Pulse Width (Note 6)	t_{PWR}	RESETN	t x 2	-	-	ns
RESETN_CLK Setup	$t_{_RST}$	RESETN-CLK	3.5	-	-	ns
CLKOUT Output Delay	t_{DCLK}	(CL = 5pF)	3.5	7	9	ns
Data Output Delay (Note 6)	t_{DO1}	DMUX Mode (C_L = 5pF)	t	t + 1	t + 2	ns
	t_{DO2}	(C_L = 5pF)	4.5	8	10	ns
Output Rise Time	t_r	0.8V to 2.0V (C_L = 5pF)	-	2	-	ns
Output Fall Time	t_f	0.8V to 2.0V (C_L = 5pF)	-	2	-	ns
DYNAMIC CHARACTERISTICS						
Input Bandwidth		V_{IN} = 2V_{P-P}, -3dB	150	-	-	MHz
S/N Ratio		f_C = 140 MSPS, f_{IN} = 1kHz Full Scale, DMUX Mode	-	46	-	dB
		f_C = 140 MSPS, f_{IN} = 34.999MHz Full Scale, DMUX Mode	-	40	-	dB

Electrical Specifications $DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, T_A = 25°C **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Rate		f_C = 140 MSPS, f_{IN} = 1kHz Full Scale, DMUX Mode, Error > 16 LSB	-	-	10^{-12}	TPS
		f_C = 140 MSPS, f_{IN} = 34.999MHz Full Scale, DMUX Mode, Error > 16 LSB	-	-	10^{-9}	TPS
		f_C = 100 MSPS, f_{IN} = 24.999MHz Full Scale, Straight Mode, Error > 16 LSB	-	-	10^{-9}	TPS (Note 7)
POWER SUPPLY						
Supply Current	I_{CC}		130	150	190	mA
Supply Current	I_{EE}		0.4	0.6	0.8	mA
Power Consumption (Note 8)	P_D		690	790	990	mW

NOTES:

4. R_{REF}: Resistance value between V_{RT} and V_{RB}.
5. $I_{REF} = \dfrac{V_{RT} - V_{RB}}{R_{REF}}$.
6. $t = \dfrac{1}{f_C}$.
7. TPS = Times Per Sample.
8. $P_D = (I_{CC} + I_{EE}) \bullet V_{CC} + \dfrac{(V_{RT} - V_{RB})^2}{V_{REF}}$.

Timing Waveforms

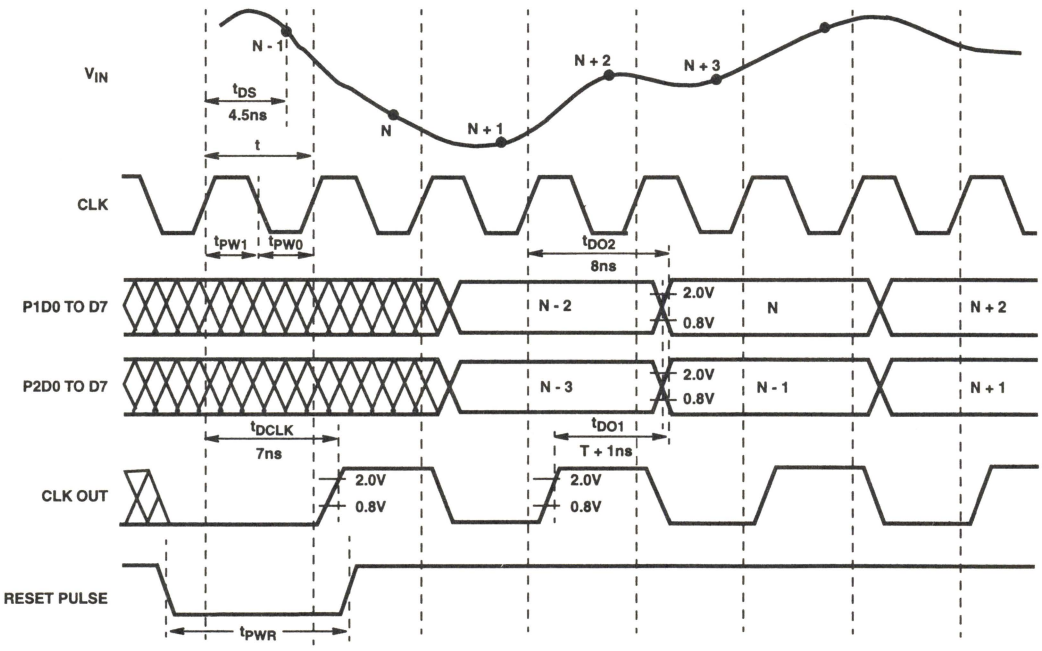


FIGURE 1. DEMUX MODE TIMING CHART (SELECT = V_{CC})

Timing Waveforms (Continued)

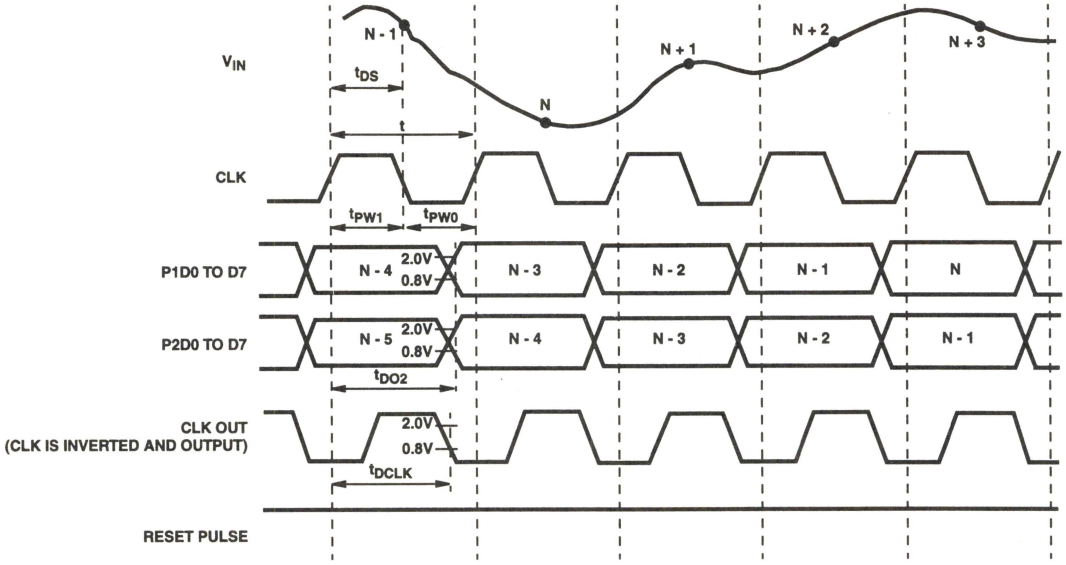


FIGURE 2. STRAIGHT MODE TIMING CHART (SELECT = GND)

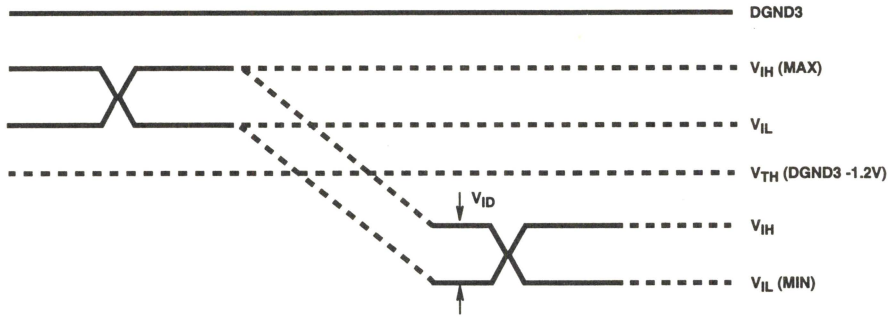
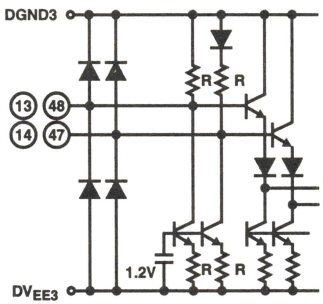
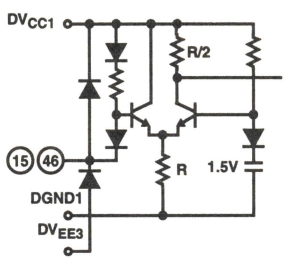
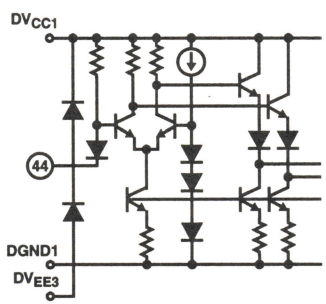


FIGURE 3. ECL AND PECL SWITCHING LEVEL

Pin Descriptions

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
3, 10	AGND		GND		Analog Ground. Separated from the digital ground.
5, 8	AV_{CC}		+5V (Typ)		Analog Power Supply. Separated from the digital power supply.
20, 29 32, 41	DGND1 DGND2		GND		Digital Ground.
19, 30 31, 42	DV_{CC1} DV_{CC2}		+5V (Typ)		Digital Power Supply.

Pin Descriptions (Continued)

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
12	DGND3		+5V (Typ) (With a Single Power Supply) GND (With Dual Power Supplies)		Digital Power Supply. Ground for ECL input. +5V for PECL and TTL input.
1	DV_{EE3}		GND (With a Single Power Supply) -5V (Typ) (With Dual Power Supplies)		Digital Power Supply. -5V for ECL input. Ground for PECL and TTL Input
16, 17, 18	NC				No Connect pin. Not connected with the internal circuits.
13	CLK/E	I	ECL/PECL		Clock Input.
14	CLKN/E	I			CLK/E Complementary Input. When left open, this pin goes to the threshold potential. Only CLK/E can be used for operation, but complementary input is recommended to attain fast and stable operation.
48	RESETN/E	I			Reset Input. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
47	RESET/E	I			RESETN/E Complementary Input. When left open, this pin goes to the threshold voltage. Only RESETN/E can be used for operation.
15	CLK/T	I	TTL		Clock Input.
46	RESETN/T	I			Reset Input. When left open, this input goes to high level. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
44	INV	I	TTL		Data Output Polarity Inversion Input. When left open, this input goes to high level. (See Table 1, I/O Correspondence Table.)

Pin Descriptions (Continued)

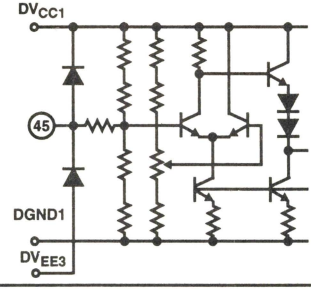
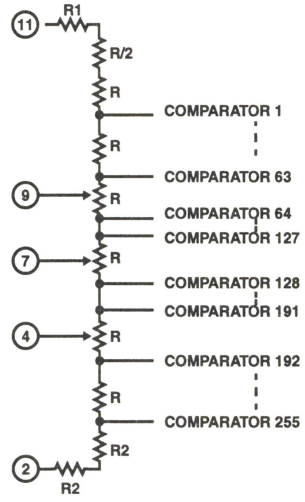
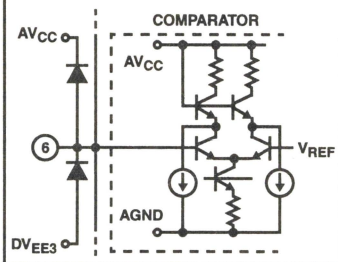
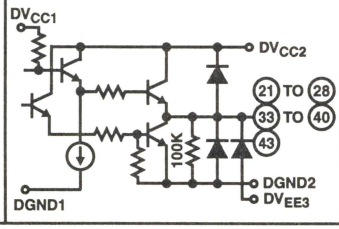
PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
45	SELECT		V_{CC} or GND		Data Output Mode Selection. (See Table 2, Operating Mode Table.)
11	V_{RT}	I	4.0V (Typ)		Top Reference Voltage. By-pass to AGND with a 1µF tantal capacitor and a 0.1µF chip capacitor.
9	V_{RM3}		$V_{RB} + \frac{3}{4}(V_{RT} - V_{RB})$		Reference Voltage Mid Point. Bypass to AGND with a 0.1µF chip capacitor.
7	V_{RM2}		$V_{RB} + \frac{2}{4}(V_{RT} - V_{RB})$		Reference Voltage Mid Point. Bypass to AGND with a 0.1µF chip capacitor.
4	V_{RM1}		$V_{RB} + \frac{1}{4}(V_{RT} - V_{RB})$		Reference Voltage Mid Point. Bypass to AGND with a 0.1µF chip capacitor.
2	V_{RB}	I	2.0V (Typ)		Bottom Reference Voltage. Bypass to AGND with a 1µF tantal capacitor and a 0.1µF chip capacitor.
6	V_{IN}	I	V_{RT} to V_{RB}		Analog Input.
33 to 40	P1D0 to P1D7	O	TTL		Port 1 Side Data Output.
21 to 28	P2D0 to P2D7	O			Port 2 Side Data Output.
43	CLKOUT	O			Clock Output. (See Table 2, Operating Mode Table.)

TABLE 1. A/D CODE TABLE

V_{IN}	STEP	INV 1 D7							D0	INV 0 D7							D0
V_{RT}	255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	254	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
	•				•								•				
	•				•								•				
	•				•								•				
V_{RM2}	128	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	127	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	•				•								•				
	•				•								•				
	•				•								•				
	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
V_{RB}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Notes On Operation

- The HI3026A is a high-speed A/D converter which is capable of TTL, ECL and PECL level clock input. Characteristic impedance should be properly matched to ensure optimum performance during high-speed operation.
- The power supply and grounding have a profound influence on converter performance. The power supply and grounding method are particularly important during high-speed operation. General points for caution are as follows:
  - The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using a multi-layer board.
  - To prevent interference between AGND and DGND and between AV_{CC} and DV_{CC}, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AV_{CC} and DV_{CC} lines at one point each via a ferrite-bead filter. Shorting the AGND and DGND patterns in one place immediately under the A/D converter improves A/D converter performance.
  - Ground the power supply pins (AV_{CC}, DV_{CC1}, DV_{CC2}, DV_{EE3}) as close to each pin as possible with a 0.1µF or larger ceramic chip capacitor. (Connect the AV_{CC} pin to the AGND pattern and the DV_{CC1}, DV_{CC2}, DV_{EE3} pins to the DGND pattern.)
  - The digital output wiring should be as short as possible. If the digital output wiring is long, the wiring capacitance will increase, deteriorating the output slew rate and resulting in reflection to the output waveform since the original output slew rate is quite fast.
- The analog input pin V_{IN} has an input capacitance of approximately 21pF. To drive the A/D converter with proper frequency response, it is necessary to prevent performance deterioration due to parasitic capacitance or parasitic inductance by using a large capacity drive circuit, keeping wiring as short as possible, and using chip parts for resistors and capacitors, etc.
- The V_{RT} and V_{RB} pins must have adequate bypass to protect them from high-frequency noise. Bypass them to AGND with approximately 1µF tantal capacitor and, 0.1µF capacitor as short as possible.
- When the digital input level is ECL or PECL level, ***/E pins should be used and ***/T pins left open. When the digital input level is TTL, ***/T pins should be used and III/E pins left open.

Test Circuits

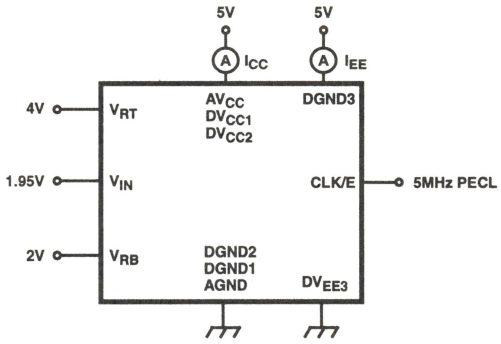


FIGURE 4. CURRENT CONSUMPTION MEASUREMENT CIRCUIT

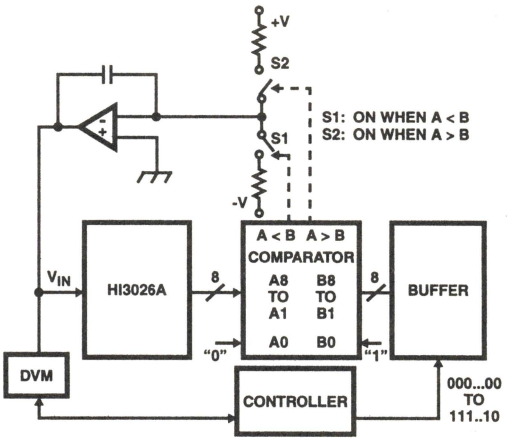


FIGURE 5. INTEGRAL LINEARITY ERROR/DIFFERENTIAL LINEARITY ERROR MEASUREMENT CIRCUIT

Test Circuits (Continued)

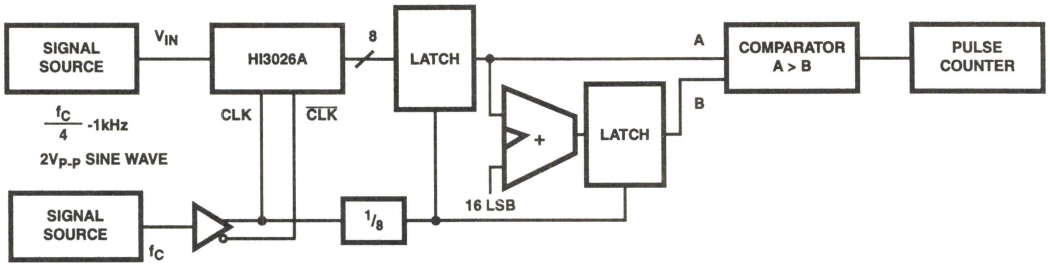


FIGURE 6. ERROR RATE MEASUREMENT CIRCUIT

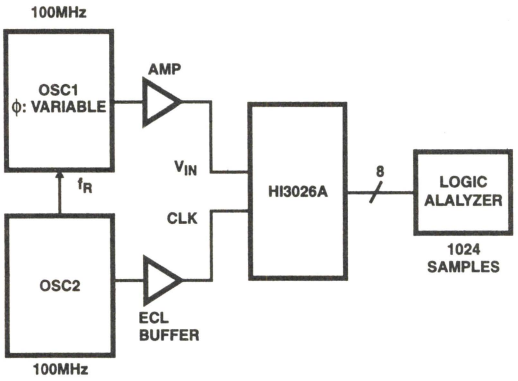
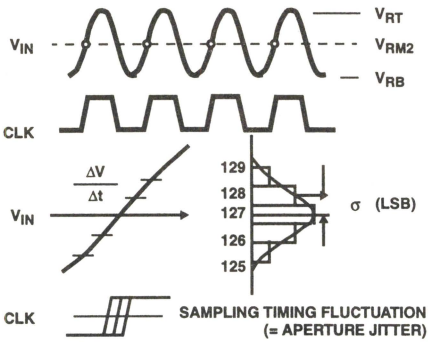


FIGURE 7. SAMPLING DELAY/APERTURE JITTER MEASUREMENT CIRCUIT



NOTE: Where σ (LSB) is the deviation of the output codes when the largest slew rate point is sampled at the clock which has exactly the same frequency as the analog input signal, the aperture jitter, t_{AJ} is:

$$t_{AJ} = \left(\frac{\sigma/\Delta V}{\Delta t}\right) = \sigma/\left(\frac{256}{2} \times 2\pi f\right).$$

FIGURE 8. APERTURE JITTER MEASUREMENT METHOD

Operating Modes

The HI3026A has two types of operating modes which are selected with Pin 45 (SELECT).

TABLE 2. OPERATING MODE TABLE

OPERATING MODE	SELECT	MAXIMUM CONVERSION RATE	DATA OUTPUT	CLOCK OUTPUT
DMUX Mode	V_{CC}	140 MSPS	Demultiplexed Output 70 Mbps	The input clock is $^1/_2$ frequency divided and output at 70MHz.
Straight Mode	GND	100 MSPS	Straight Output 100 Mbps	The input clock is inverted and output at 100MHz.

DMUX Mode (See Application Circuits, Figures 18, 19, 20)

Set the SELECT pin to V_{CC} for this mode. In this mode, the clock frequency is divided by 2 in the IC, and the data is output after being demultiplexed by this $^1/_2$ frequency divided clock. The $^1/_2$ frequency divided clock, which has adequate setup time and hold time for the output data, is output from the CLKOUT pin.

When using multiple HI3026A units in parallel in this mode, differences in the start timing of the $^1/_2$ frequency divided clock may cause operation as shown in the figure below. As a countermeasure, the HI3026A is equipped with a function which resets the $^1/_2$ frequency divided clock. When resetting this clock, the RESET pulse must be input to the RESET pin. See the Timing Charts for the RESET pulse input timing. The A/D converter can operate at f_C (Min) = 140 MSPS in this mode.

Straight Mode (See Application Circuits, Figures 21, 22, 23)

Set the SELECT pin to GND for this mode. In this mode, data output can be obtained in accordance with the clock frequency applied to the A/D converter for applications which use the clock applied to the A/D converter as the system clock.

The A/D converter can operate at f_C (Min) = 100 MSPS in this mode.

Digital Input Level and Supply Voltage Settings

The logic input level for the HI3026A supports ECL, PECL and TTL levels.

The power supplies (DV_{EE3}, DGND3) for the logic input block must be set to match the logic input (CLK and RESET signals) level.

TABLE 3. LOGIC INPUT LEVEL AND POWER SUPPLY SETTINGS

DIGITAL INPUT LEVEL	DV_{EE3}	DGND3	SUPPLY VOLTAGE	APPLICATION CIRCUITS (FIGURE)	
ECL	-5V	0V	±5V	(18)	(21)
PECL	0V	+5V	+5V	(19)	(22)
TTL	0V	+5V	+5V	(20)	(23)

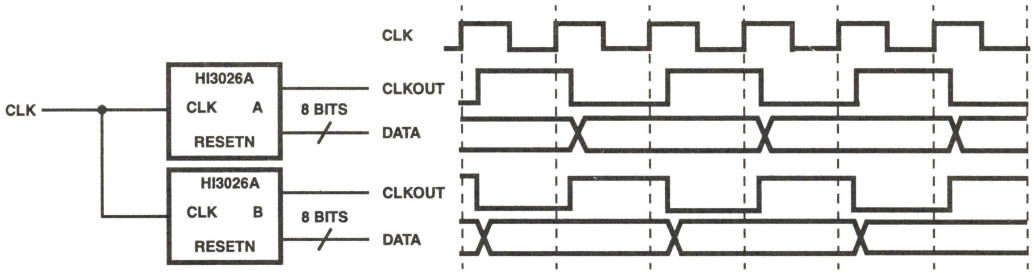


FIGURE 9. WHEN THE RESET PULSE IS NOT USED

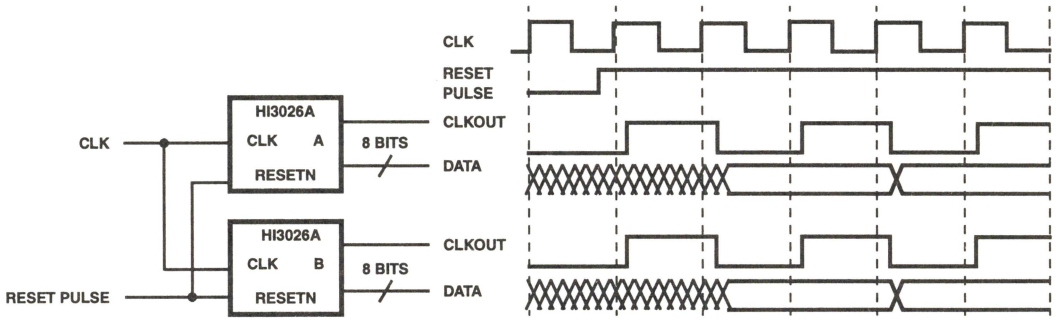


FIGURE 10. WHEN THE RESET PULSE IS USED

Typical Performance Curves

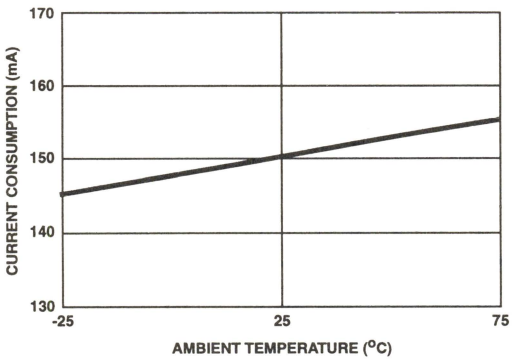


FIGURE 11. CURRENT CONSUMPTION vs AMBIENT TEMPERATURE CHARACTERISTICS

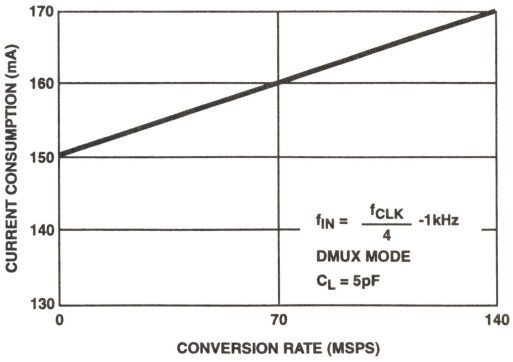


FIGURE 12. CURRENT CONSUMPTION vs CONVERSION RATE CHARACTERISTICS RESPONSE

Typical Performance Curves (Continued)

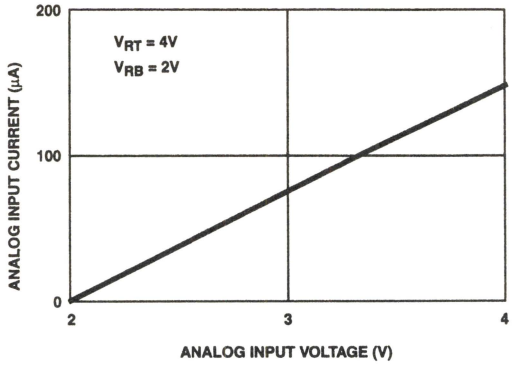


FIGURE 13. ANALOG INPUT CURRENT vs ANALOG INPUT VOLTAGE CHARACTERISTICS

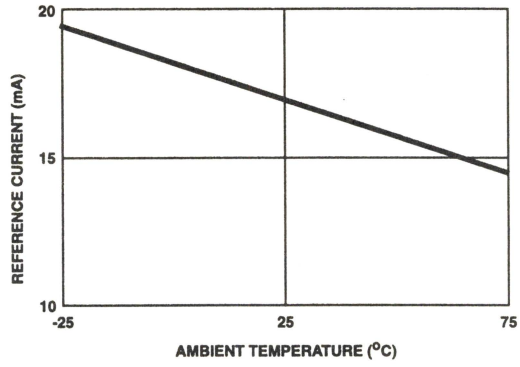


FIGURE 14. REFERENCE CURRENT vs AMBIENT TEMPERATURE CHARACTERISTICS

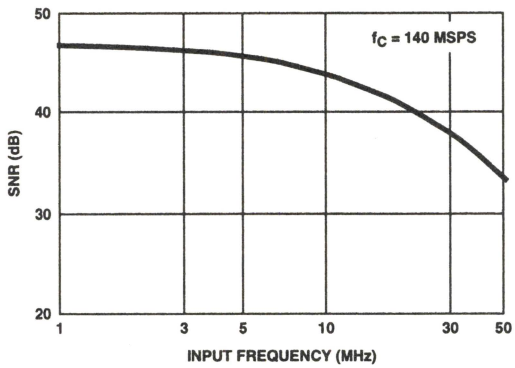


FIGURE 15. SNR vs INPUT FREQUENCY RESPONSE

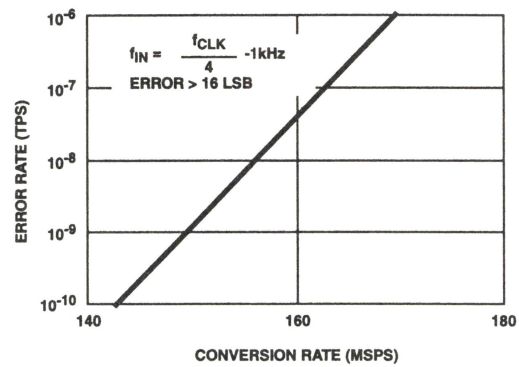


FIGURE 16. ERROR RATE vs CONVERSION RATE CHARACTERISTICS

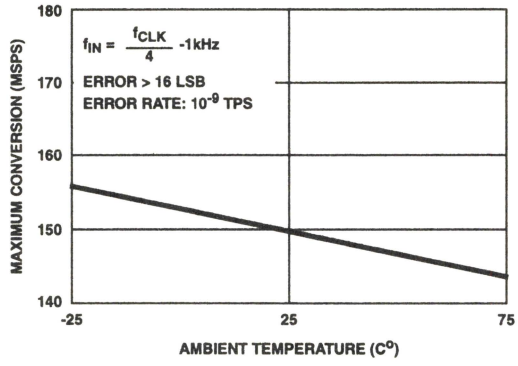


FIGURE 17. MAXIMUM CONVERSION RATE vs AMBIENT TEMPERATURE CHARACTERISTICS

Typical Application Circuits

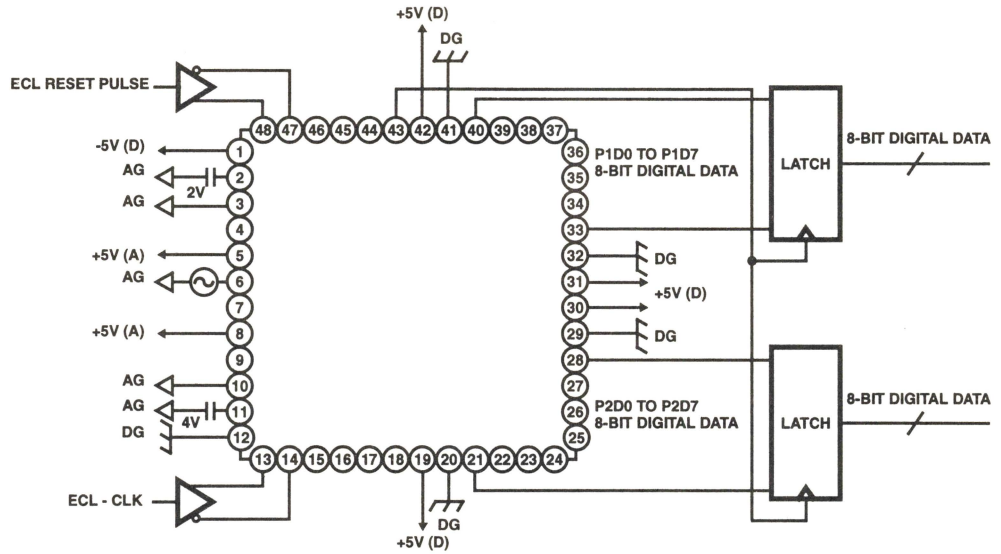


FIGURE 18. DMUX ECL INPUT

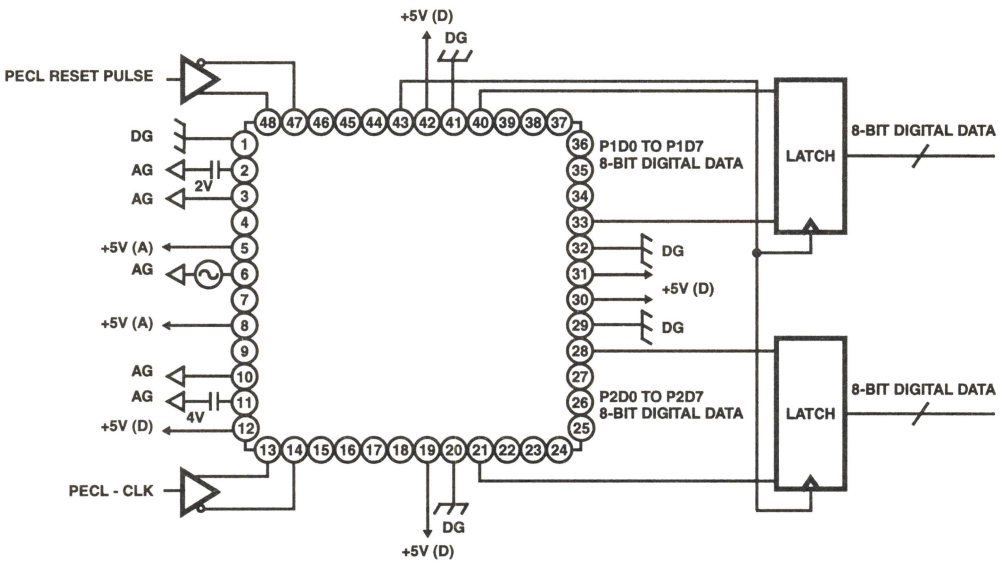


FIGURE 19. DMUX PECL INPUT

Typical Application Circuits (Continued)

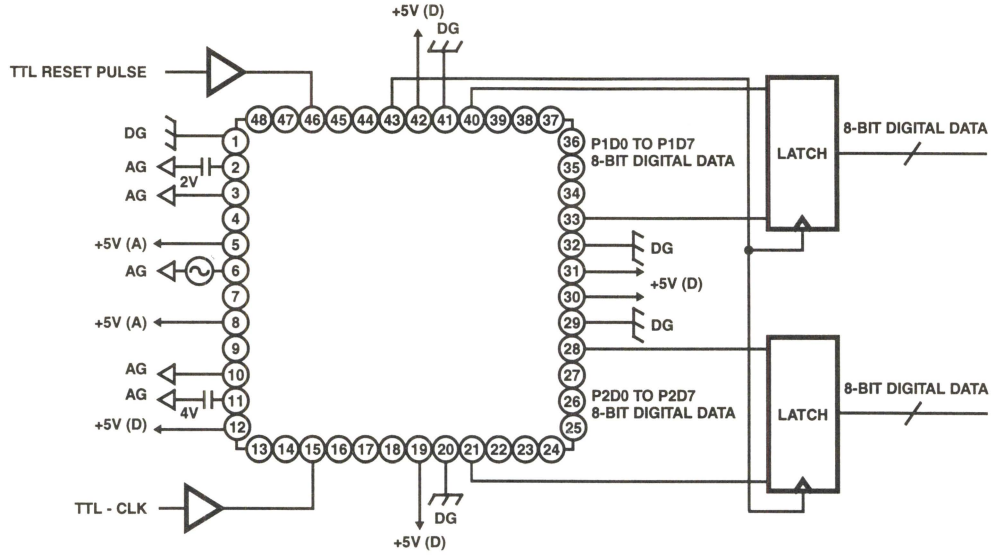


FIGURE 20. DMUX TTL INPUT

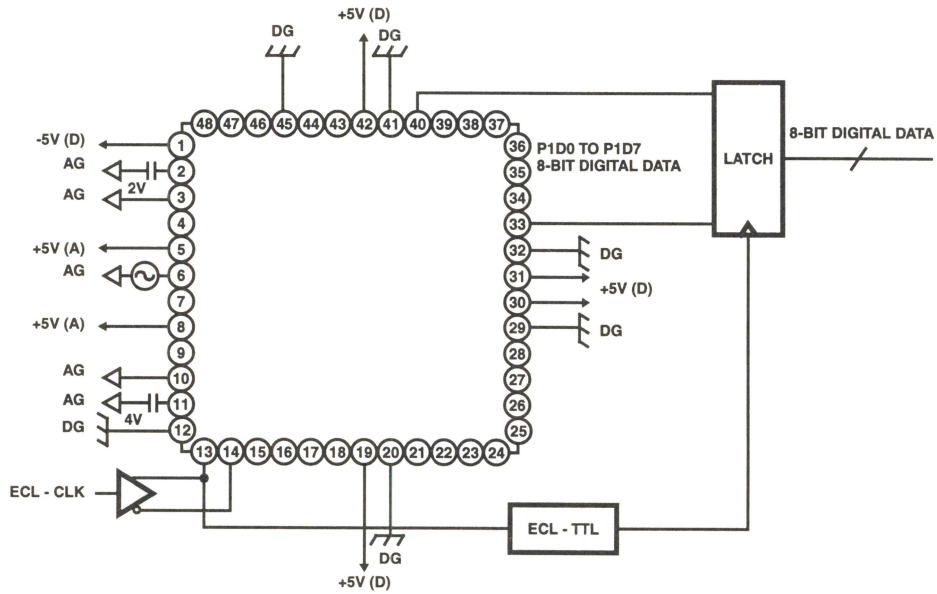


FIGURE 21. STRAIGHT ECL INPUT

Typical Application Circuits (Continued)

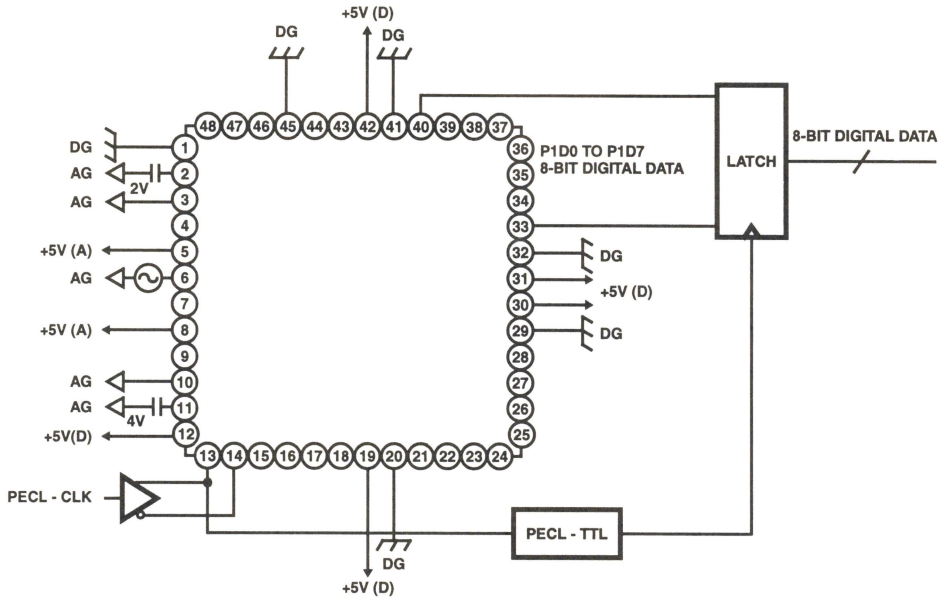


FIGURE 22. STRAIGHT PECL INPUT

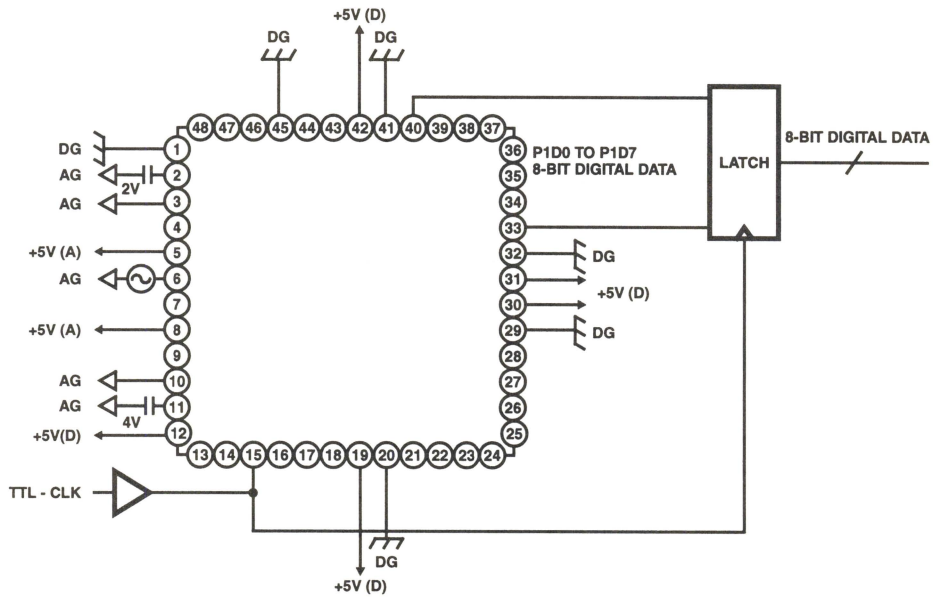


FIGURE 23. STRAIGHT TTL INPUT

Typical Application Circuits (Continued)

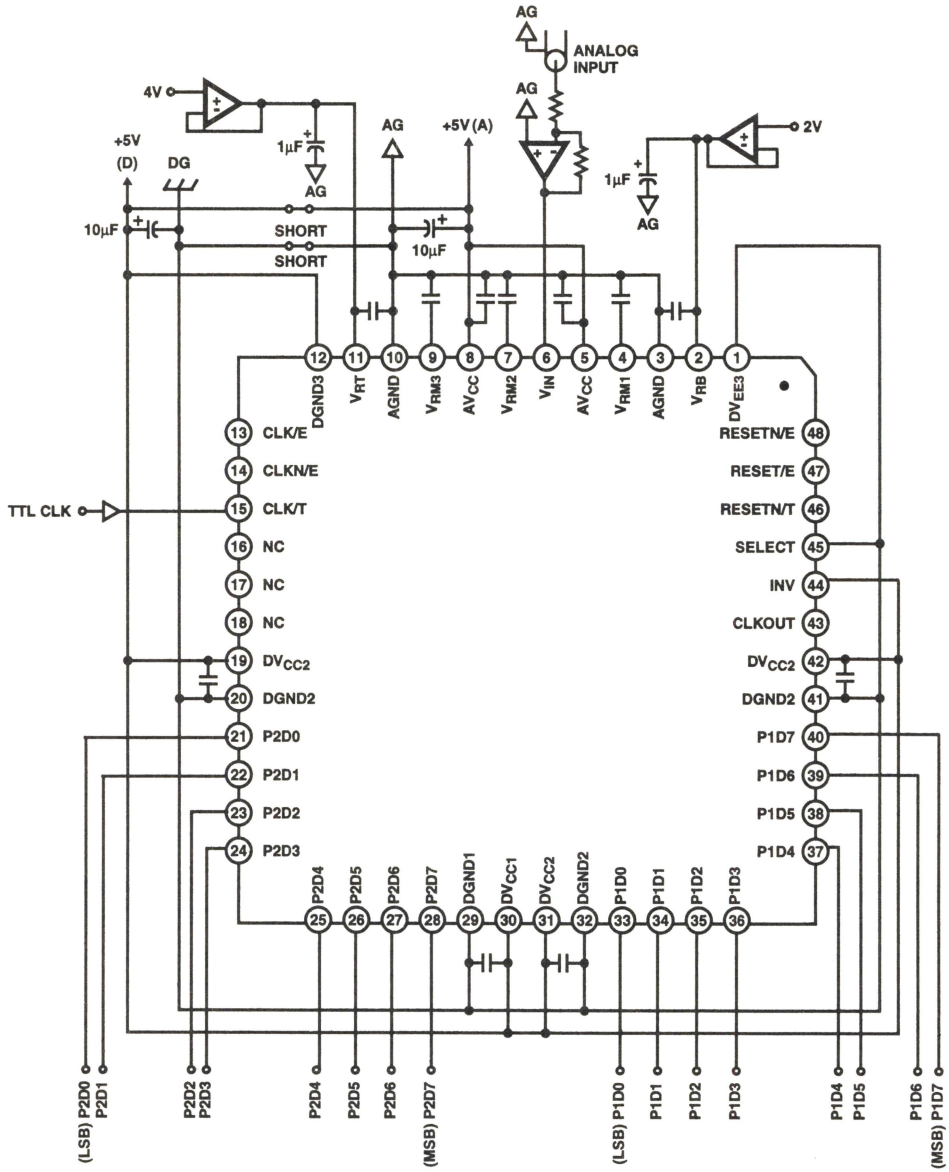


FIGURE 24. STRAIGHT MODE TTL I/O (WHEN A SINGLE POWER SUPPLY IS USED)

August 1997

6-Bit, 140 MSPS, Flash A/D Converter

Features

- Differential Linearity Error..... ±0.2 LSB
- Integral Linearity Error ..... ±0.2 LSB
- Single +5V Power Supply Operation Available
- Low Input Capacitance 7pF
- Wide Analog Input Bandwidth 200MHz
- Low Power Consumption 360mW
- CLK/2 Clock Output Pin
- Excellent Temperature Characteristics
- 1:2 Demultiplexed Output
- Internal $^1/_2$ Frequency Divider Circuit (With Reset Function)
- Compatible with ECL, PECL and TTL Digital Input Levels
- Direct Replacement for Sony CXA3086

Applications

- RGB Graphics Processing (LCD, PDP)
- Digital Communications (QPSK, QAM)
- Magnetic Recording (PRML)

Description

The HI3086 is a 6-bit, high-speed, flash analog-to-digital converter optimized for high speed, low power, and ease of use. With a 140 MSPS encode rate capability and full-power analog bandwidth of 200MHz, this component is ideal for applications requiring the highest possible dynamic performance.

To minimize system cost and power dissipation, only a +5V power supply is required. The HI3086's clock input interfaces directly to TTL, ECL, or PECL logic and will operate with single-ended inputs. The user may select 16-bit demultiplexed output or 8-bit single-channel digital outputs. The demultiplexed mode interleaves the data through two 8-bit channels at $^1/_2$ the clock rate. Operation in demultiplexed mode reduces the speed and cost of external digital interfaces, while allowing the A/D converter to be clocked to the full 140 MSPS conversion rate.

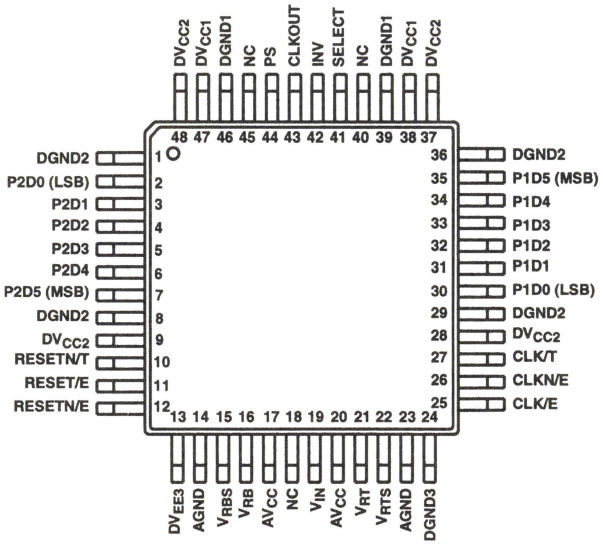
Fabricated with an advanced bipolar process, the HI3086 is provided in a space-saving 48-lead MQFP surface mount plastic package and is specified over the -20°C to 75°C temperature range.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3086JCQ	-20 to 75	48 Ld MQFP	Q48.12x12-S
HI3086EVAL	25	Evaluation Board	

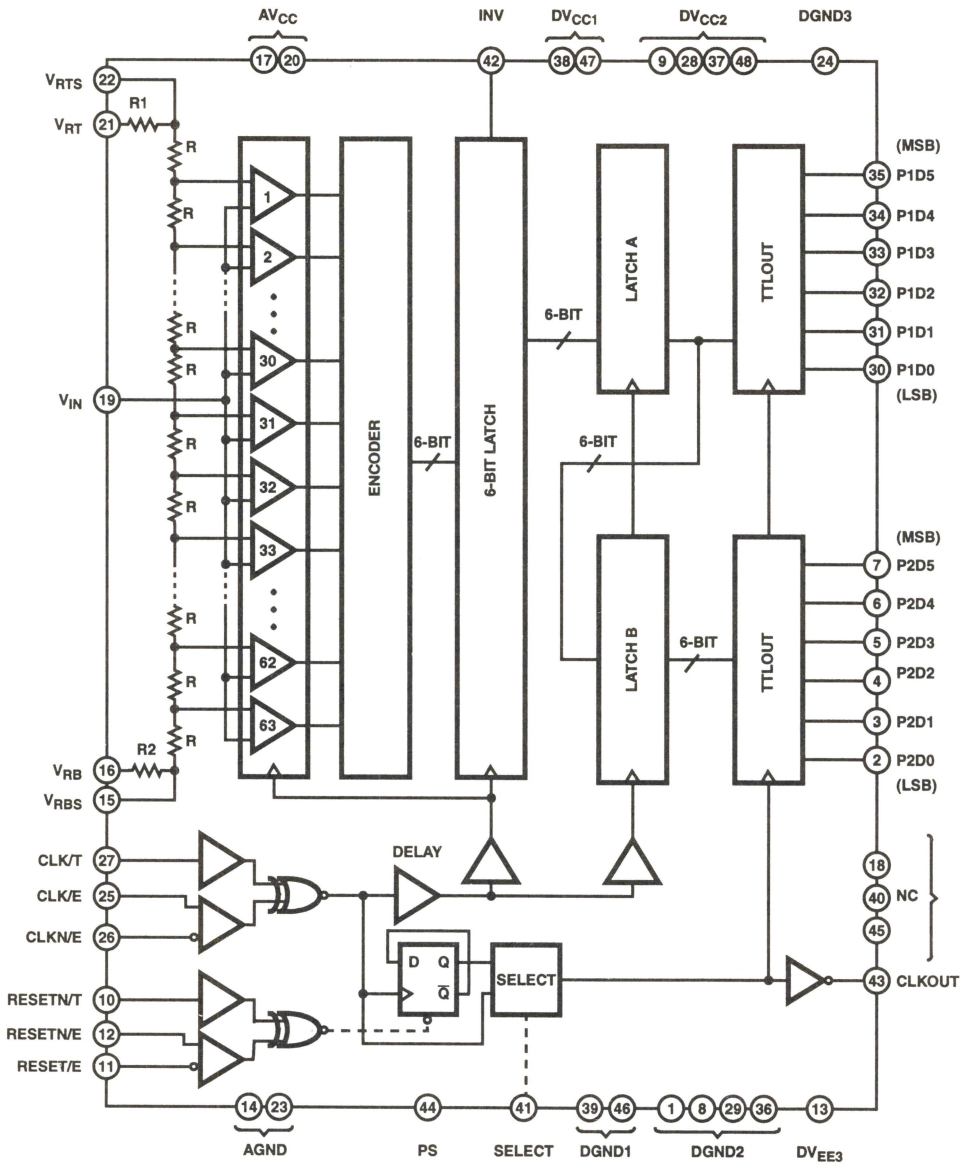
Pinout

HI3086 (MQFP)
TOP VIEW

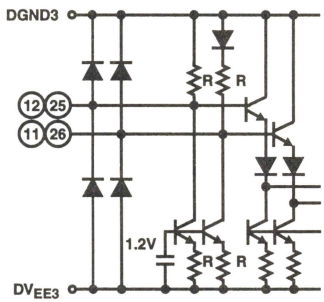


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

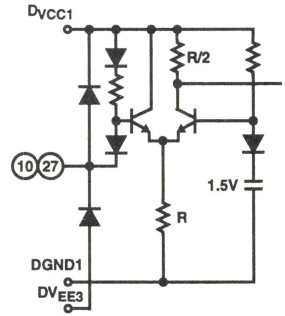
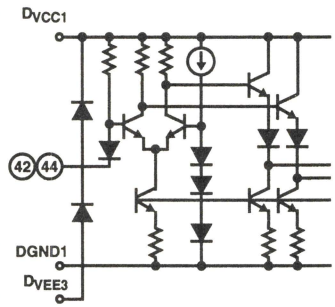
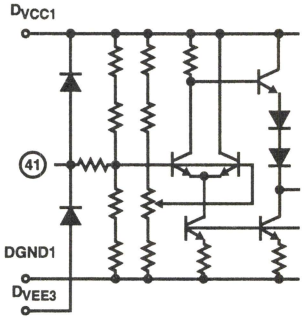
Functional Block Diagram



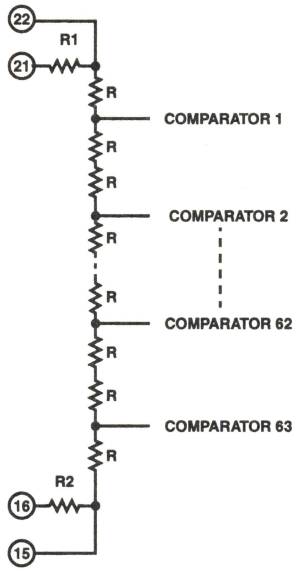
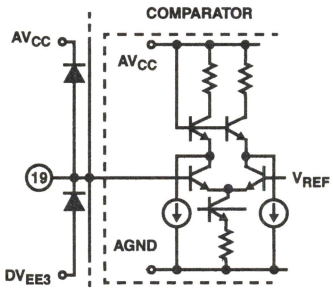
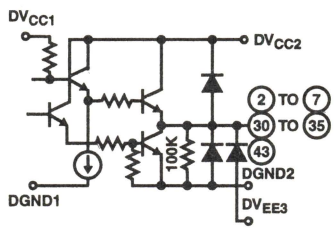
Pin Descriptions

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
14, 23	AGND		GND		Analog Ground. Separated from the digital ground.
17, 20	AV_{CC}		+5V (Typ)		Analog Power Supply. Separated from the digital power supply.
1, 8, 29, 36, 39, 46	DGND1 DGND2		GND		Digital Ground.
9, 28, 37, 38, 47, 48	DV_{CC1} DV_{CC2}		+5V (Typ)		Digital Power Supply.
24	DGND3		+5V (Typ) (With a Single Power Supply) GND (With Dual Power Supplies)		Digital Power Supply. Ground for ECL input. +5V for PECL and TTL input.
13	D_{VEE3}		GND (With a Single Power Supply) -5V (Typ) (With Dual Power Supplies)		Digital Power Supply. Ground for ECL input. -5V for PECL and TTL input.
18, 40, 45	NC				No Connect pin. Not connected with the internal circuits.
25	CLK/E	I	ECL/PECL		Clock input.
26	CLKN/E	I			CLK/E Complementary Input. When left open, this pin goes to the threshold potential. Only CLK/E can be used for operation, but complementary input is recommended to attain fast and stable operation.
12	RESETN/E	I			Reset Input. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
11	RESET/E	I			RESETN/E Complementary Input. When left open, this pin goes to the threshold voltage. Only RESETN/E can be used for operation.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
27	CLK/T	I	TTL		Clock Input.
10	RESETN/T	I			Reset Input. When left open, this input goes to high level. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
42	INV	I	TTL		Data Output Polarity Inversion Input. When left open, this input goes to high level. (See Table 1; I/O Correspondence Table).
44	PS	I	TTL		Power Saving Input. When the input is set to low level, the power saving mode is set. In this time the all TTL ouputs go into the high impedance state. Normally, set to high level or left open.
41	SELECT		V_{CC} or GND		Data Output Mode Selection. (See Table 2, Operating Mode Table).

Pin Descriptions (Continued)

PIN NO.	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
22	V_{RTS}	O	+4.0V (Typ)		Reference Voltage Sense. Bypass to AGND with a 0.1µF chip capacitor.
21	V_{RT}	I	V_{RTS} + R1 x I_{REF}		Top Reference Voltage. Bypass to AGND with a 1µF tantal capacitor and 0.1µF chip capacitor.
16	V_{RB}	I	V_{RBS} -R2 x I_{REF}		Bottom Reference Voltage. Bypass to AGND with a 1µF tantal capacitor and a 0.1µF chip capacitor.
15	V_{RBS}	O	+2.0V (Typ)		Reference Voltage Sense. Bypass to AGND with a 0.1µF chip capacitor.
19	V_{IN}	I	V_{RT} to V_{RB}		Analog Input.
30 to 35	P1D0 to P1D5	O	TTL		Port 1 Side Data Output.
2 to 7	P2D0 to P2D5	O			Port 2 Side Data Output.
43	CLKOUT	O			Clock Output. (See Table 2. Operating Mode Table.)

Absolute Maximum Ratings ($T_A = 25^oC$)

Supply Voltage ..... (AV_{CC}, DV_{CC1}, DV_{CC2}) -0.5V to 7.0V
($DGND3$) ..... -0.5V to 7.0V
(DV_{EE3}) ..... -7.0V to 0.5V
($DGND3 - DV_{EE3}$) ..... -0.5V to 7.0V
Analog Input Voltage (V_{IN}) ..... V_{RT} - 2.7V to AV_{CC}
Reference Input Voltage (V_{RT}) ..... 2.7V to AV_{CC}
(V_{RB}) ..... V_{IN} - 2.7V to AV_{CC}
($|V_{RT} - V_{RB}|$) 2.5V
Digital Input Voltage
ECL (***/E (Note 2)) ..... DV_{EE3} to 0.5V
PECL (***/E) ..... -0.5V to DGND3
TTL (***/T, INV P_S) ..... -0.5V to DV_{CC1}
Other (SELECT) ..... -0.5V to DV_{CC1}
V_{ID} (I***/E - ***N/EI (Note 3)) 2.7V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	63

Maximum Junction Temperature (Plastic Package) ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(MQFP - Lead Tips Only)

Recommended Operating Conditions

WITH A SINGLE POWER SUPPLY	MIN	TYP	MAX
Supply Voltage			
DV_{CC1}, DV_{CC2}, AV_{CC}	+4.75	+5.0	+5.25V
DGND1, DGND2, AGND	-0.05	0	+0.05V
DGND3	+4.75	+5.0	+5.25V
DV_{EE3}	-0.05	0	+0.05V
Analog Input Voltage (V_{IN})	V_{RB}	-	V_{RT}
Reference Input Voltage			
V_{RT}	+2.9	-	+4.1V
V_{RB}	1.4	-	+2.6V
$\|V_{RT} - V_{RB}\|$	1.5	-	2.1V
Digital Input Voltage			
ECL (***/E) V_{IH}	DGND3 - 1.05		DGND3 - 0.5V
PECL (***/E) V_{IL} DGND3	DGND3 - 3.2		DGND3 - 1.4V
TTL (***/T, INV, PS) V_{IH}	2.0V	-	-
TTL (***/T, INV) V_{IL}	-	-	0.8V
Other (SELECT) V_{IH}	-	DV_{CC1}	-
Other (SELECT) V_{IL}	-	DGND1	-
V_{ID} (Note 3) (I***/E- ***N/EI)	0.4	0.8	-
Max Conversion Rate (f_C, Straight Mode)	100 Units = MSPS	-	-
Max Conversion Rate (f_C, DMUX Mode)	140 Units = MSPS	-	-
Ambient Temperature (T_A)	-20^oC		75^oC

WITH DUAL POWER SUPPLIES	MIN	TYP	MAX
Supply Voltage			
DV_{CC1}, DV_{CC2}, AV_{CC}	+4.75	+5.0	+5.25V
DGND1, DGND2, AGND	-0.05	0	+0.05V
DGND3	-0.05	0	+0.05V
DV_{EE3}	-5.5	-5.0	-4.75V
Analog Input Voltage (V_{IN})	V_{RB}	-	V_{RT}
Reference Input Voltage			
V_{RT}	+2.9	-	+4.1V
V_{RB}	1.4	-	+2.6V
$\|V_{RT} - V_{RB}\|$	1.5	-	2.1V
Digital Input Voltage			
ECL (***/E) V_{IH} DGND3	DGND3 - 1.05		DGND3 - 0.5V
ECL (***/E) V_{IL} DGND3	DGND3 - 3.2		DGND3 - 1.4V
TTL (***/T, INV) V_{IH}	2.0V	-	-
TTL (***/T, INV) V_{IL}	-	-	0.8V
Other (SELECT) V_{IH}	-	DV_{CC1}	-
Other (SELECT) V_{IL}	-	DGND1	-
V_{ID} (Note 3) (I***/E- ***N/EI)	0.4	0.8	-
Max Conversion Rate (f_C, Straight Mode)	100 Units = MSPS	-	-
Max Conversion Rate (f_C, DMUX Mode)	140 Units = MSPS	-	-
Ambient Temperature (T_A)	-20^oC		75^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. ***/E and ***T indicate CLK/E and CLK/T, etc. for the pin name.
3. V_{ID}: Input Voltage Differential.

Electrical Specifications

$DV_{CC1, 2}$, AV_{CC}, DGND1, 2, AGND, $DV_{EE3} = 0V$, $V_{RT} = 4V$, $V_{RB} = 2V$, $T_A = 25^oC$, PECL Input

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution			-	6	-	Bits
DC CHARACTERISTICS						
Integral Linearity Error	E_{IL}	$V_{IN} = 2V_{P-P}$, $f_C = 5$ MSPS	-	-	±0.2	LSB
Differential Linearity Error	E_{DL}		-	-	±0.2	LSB

Electrical Specifications $DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, $T_A = 25^oC$, PECL Input **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Analog Input Capacitance	C_{IN}	V_{IN} = +3.0V + 0.07V_{RMS}	-	7	-	pF
Analog Input Resistance	R_{IN}		16	-	150	kΩ
Analog Input Current	I_{IN}		0	-	125	µA
REFERENCE INPUT						
Reference Resistance (Note 5)	R_{REF}		160	225	308	Ω
Reference Current (Note 6)	I_{REF}		6.5	9.0	12.5	mA
Residual Resistance	R1		3.0	4.2	5.7	Ω
	R2		3.0	4.2	5.7	Ω
DIGITAL INPUT (ECL, PECL)						
Digital Input Voltage: High	V_{IH}		DGND3 -1.05	-	DGND3 -0.5	V
Digital Input Voltage: Low	V_{IL}		DGND3 -3.2	-	DGND3-1.4	V
Threshold Voltage	V_{TH}		-	DGND3 -1.2	-	V
Digital Input Current: High	I_{IH}	V_{IH} = DGND3 -0.8V	-50	-	+50	µA
Digital Input Current: Low	I_{IL}	V_{IL} = DGND3 -1.6V	-75	-	0	µA
Digital Input Capacitance			-	-	5	pF
DIGITAL INPUT (TTL)						
Digital Input Voltage: High	V_{IH}		2.0	-	-	V
Digital Input Voltage: Low	V_{IL}		-	-	0.8	V
Threshold Voltage	V_{TH}		-	1.5	-	V
Digital Input Current: High	I_{IH}	V_{IH} = 3.5V	-50	-	0	µA
Digital Input Current: Low	I_{IL}	V_{IL} = 0.2V	-500	-	0	µA
Digital Input Capacitance			-	-	5	pF
DIGITAL OUTPUT (TTL)						
Digital Output Voltage: High	V_{OH}	I_{OH} = -2mA	2.4	-	-	V
Digital Output Voltage: Low	V_{OL}	I_{OL} = 1mA	-	-	0.5	V
Leakage Current	I_{OZ}	Power Saving Mode	-15	-	70	µA
SWITCHING CHARACTERISTICS						
Maximum Conversion Rate	f_C	DMUX Mode	140	-	-	MSPS
Aperture Jitter	t_{AJ}		-	10	-	ps
Sampling Delay	t_{DS}		3	4.5	6	ns
Clock High Pulse Width	t_{PW1}	CLK	2.9	-	-	ns
Clock Low Pulse Width	t_{PW0}	CLK	2.9	-	-	ns
Reset Signal Setup	t_{RS}	RESETN - CLK	3.5	-	-	ns
RESET Signal Hold	t_{RH}	RESETN - CLK	0	-	-	ns
CLKOUT Output Delay	t_{DCLK}	(C_L = 5pF)	3.5	7	9	ns
Data Output Delay (Note 7)	t_{DO1}	DMUX Mode (C_L = 5pF)	t (Note 6)	t + 1	t + 2	ns
	t_{DO2}	(C_L = 5pF)	4.5	8	10	ns
Output Rise Time	t_r	0.8V to 2.0V (C_L = 5pF)	-	2	-	ns
Output Fall Time	t_f	0.8V to 2.0V (C_L = 5pF)	-	2	-	ns

Electrical Specifications $DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, $T_A = 25^oC$, PECL Input **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Input Bandwidth		$V_{IN} = 2V_{P-P}$, -3dB	200	-	-	MHz
S/N Ratio		f_C = 140 MSPS, f_{IN} = 1kHz Full Scale, DMUX Mode	-	37.0	-	dB
		f_C = 140 MSPS, f_{IN} = 34.999MHz Full Scale, DMUX Mode	-	34.5	-	dB
Error Rate		f_C = 140 MSPS, f_{IN} = 1kHz Full Scale, DMUX Mode Error > 4 LSB	-	-	10^{-12}	TPS (Note 8)
		f_C = 140 MSPS, f_{IN} = 34.999MHz Full Scale, DMUX Mode Error > 4 LSB	-	-	10^{-9}	TPS
		f_C = 100 MSPS, f_{IN} = 24.999MHz Full Scale, Straight Mode Error > 4 LSB	-	-	10^{-9}	TSP
POWER SUPPLY						
Supply Current	I_{CC}		54.0	67.5	90.0	mA
Supply Current	I_{EE}		0.4	0.6	0.8	mA
Power Consumption (Note 9)	P_D		290	360	470	mW
Supply Current	$I_{CC} + I_{EE}$	Power Saving Mode	2.0	-	8.0	mA
Power Consumption	P_D	Power Saving Mode	28.0	-	58.0	mW

NOTES:

4. R_{REF}: Resistance value between V_{RT} and V_{RB}.

5. $I_{REF} = \frac{V_{RT} - V_{RB}}{R_{REF}}$.

6. $t = \frac{1}{f_C}$.

7. TPS: Times Per Sample.

8. $P_D = (I_{CC} + I_{EE}) \bullet V_{CC} + \frac{(V_{RT} - V_{RB})^2}{V_{REF}}$.

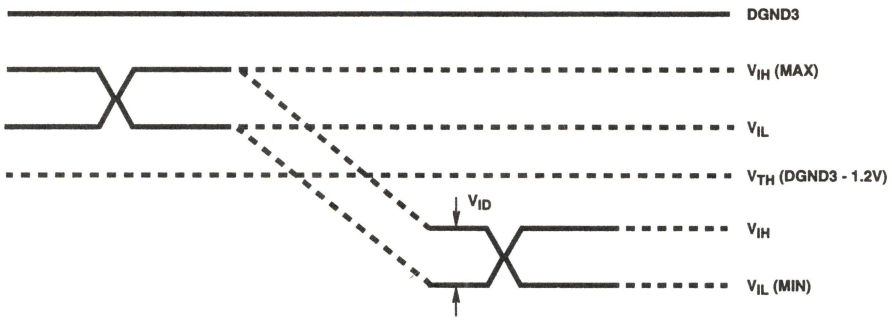


FIGURE 1. ECL AND PECL SWITCHING LEVEL

TABLE 1. I/O CORRESPONDENCE

V_{IN}	STEP	INV = 1 D5	INV = 1 D0	INV = 0 D5	INV = 0 D0
V_{RTS}	63	1 1 1 1 1 1		0 0 0 0 0 0	
	62	1 1 1 1 1 0		0 0 0 0 0 1	
	•		•		•
	•		•		•
	•		•		•
	32	1 0 0 0 0 0		0 1 1 1 1 1	
	31	0 1 1 1 1 1		1 0 0 0 0 0	
	•		•		•
	•		•		•
	•		•		•
	1	0 0 0 0 0 1		1 1 1 1 1 0	
V_{RBS}	0	0 0 0 0 0 0		1 1 1 1 1 1	

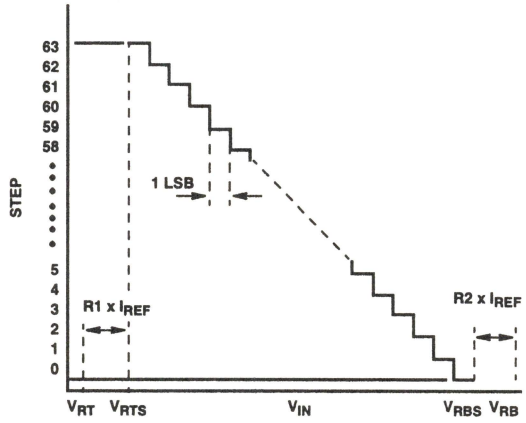


FIGURE 2.

Test Circuits

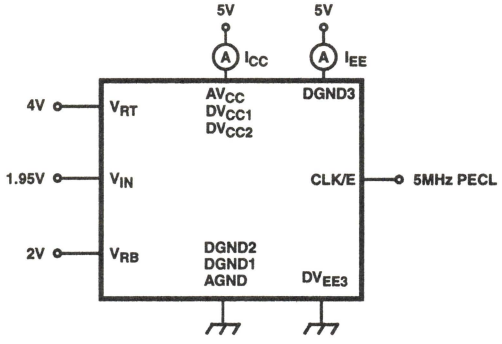


FIGURE 3. CURRENT CONSUMPTION MEASUREMENT CIRCUIT

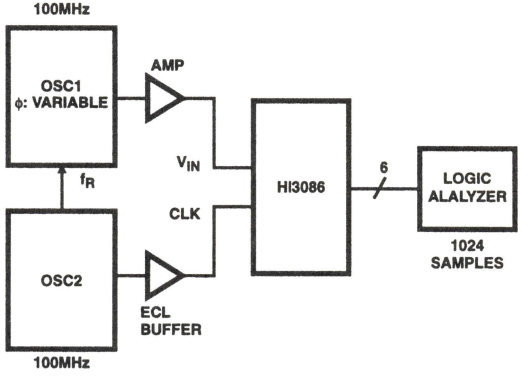


FIGURE 4. SAMPLING DELAY MEASUREMENT CIRCUIT APERTURE JITTER MEASUREMENT CIRCUIT

Test Circuits (Continued)

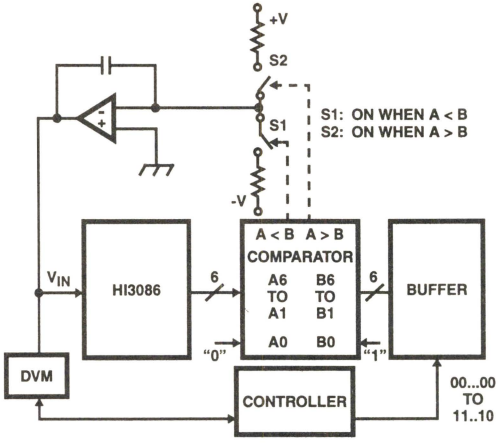
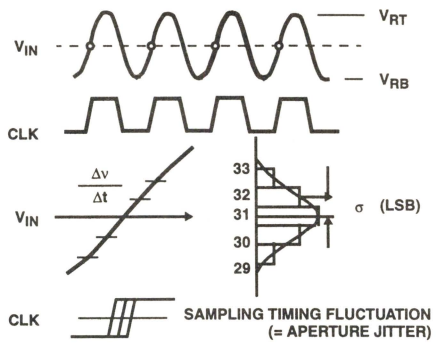


FIGURE 5. INTEGRAL LINEARITY ERROR MEASUREMENT CIRCUIT DIFFERENTIAL LINEARITY ERROR MEASUREMENT CIRCUIT



NOTE: Where σ (LSB) is the deviation of the output codes when the largest slew rate point is sampled at the clock which has exactly the same frequency as the analog input signal, the aperture jitter Tai is:

$$t_{AJ} = \sigma / \frac{\Delta v}{\Delta T} = \sigma / \left(\frac{64}{2} \times 2\pi f\right).$$

FIGURE 6. APERTURE JITTER MEASUREMENT METHOD

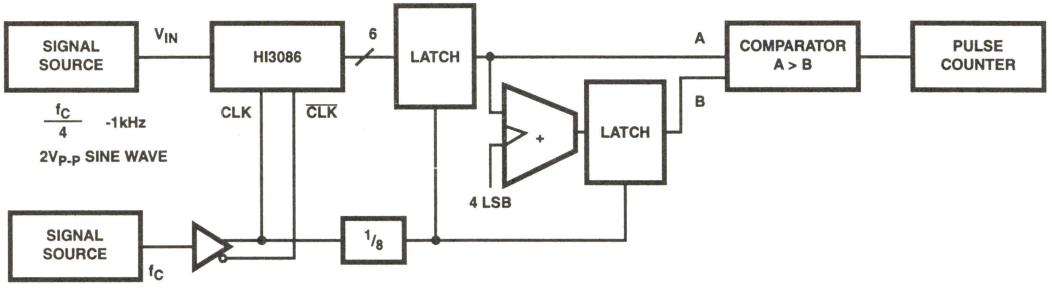


FIGURE 7. ERROR RATE MEASUREMENT CIRCUIT

Operating Modes

The HI3086 has two types of operating modes which are selected with Pin 41 (SELECT).

TABLE 2. OPERATING MODE

OPERATING MODE	SELECT	MAXIMUM CONVERSION RATE	DATA OUTPUT	CLOCK OUTPUT
DMUX Mode	V_{CC}	140 Mbps	Demultiplexed Output 70 Mbps	The input clock is $^1/_2$ frequency divided and output at 70MHz.
Straight Mode	GND	100 Mbps	Straight Output 100 Mbps	The input clock is inverted and output at 100MHz.

Demux Mode (See Figures 19, 20, 21).

Set the SELECT pin to V_{CC} for this mode. In this mode, the clock frequency is divided by 2 in the IC, and the data is output after being demultiplexed by this $^1/_2$ frequency divided clock. The $^1/_2$ frequency divided clock, which has adequate setup time and hold time for the output data, is output from the CLKOUT pin.

When using multiple HI3086 units in parallel in this mode, differences in the start timing of the $^1/_2$ frequency divided clock may cause operation as shown in Figures 8 and 9. As a countermeasure, the HI3086 is equipped with a function which resets the $^1/_2$ frequency divided clock. When resetting this clock, the RESET pulse must be input to the RESET pin. See the Timing Charts for the RESET pulse input timing. The A/D converter can operate at f_C (Min) = 140 MSPS in this mode.

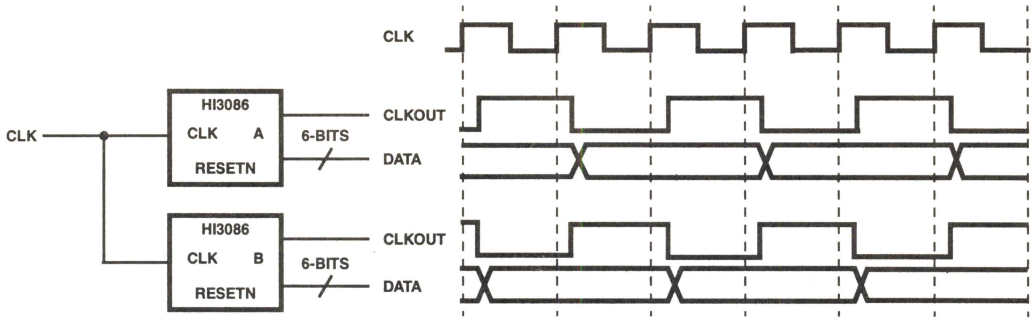


FIGURE 8. WHEN THE RESET PULSE IS NOT USED

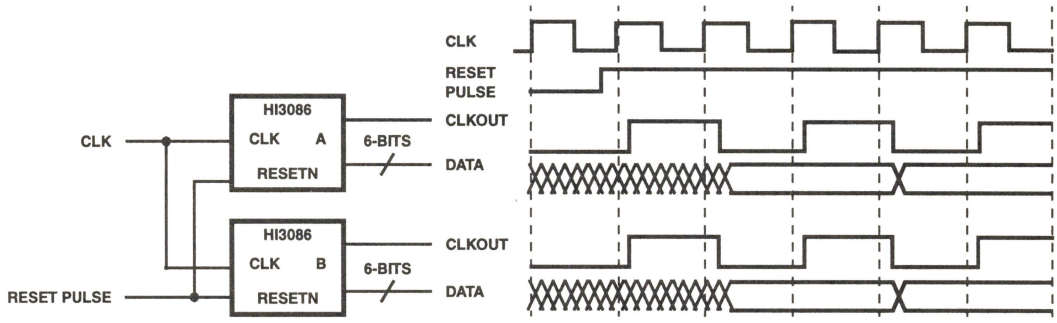


FIGURE 9. WHEN THE RESET PULSE IS USED

Straight Mode (See Figures 22, 23, 24 and 25).

Set the SELECT pin to GND for this mode. In this mode, data output can be obtained in accordance with the clock frequency applied to the A/D converter for applications which use the clock applied to the A/D converter as the system clock.

The A/D converter can operate at f_C (Min) = 100 MSPS in this mode.

Digital Input Level and Supply Voltage Settings

The logic input level for the HI3086 supports ECL, PECL and TTL levels. The power supplies (D_{VEE3}, DGND3) for the logic input block must be set to match the logic input (CLK and RESET signals) level.

TABLE 3. LOGIC INPUT LEVEL AND POWER SUPPLY SETTINGS

DIGITAL INPUT LEVEL	D_{VEE3}	DGND3	SUPPLY VOLTAGE	APPLICATION CIRCUITS
ECL	-5V	0V	±5V	Figures 19, 22
PECL	0V	+5V	+5V	Figures 20, 23
TTL	0V	+5V	+5V	Figures 21, 24, 25

Timing Waveforms

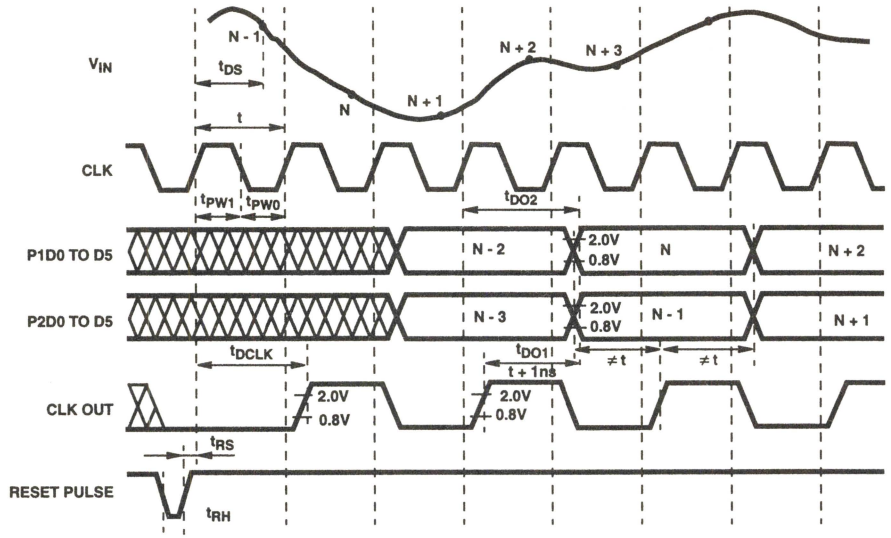


FIGURE 10. DEMUX MODE TIMING CHART (SELECT = V_{CC})

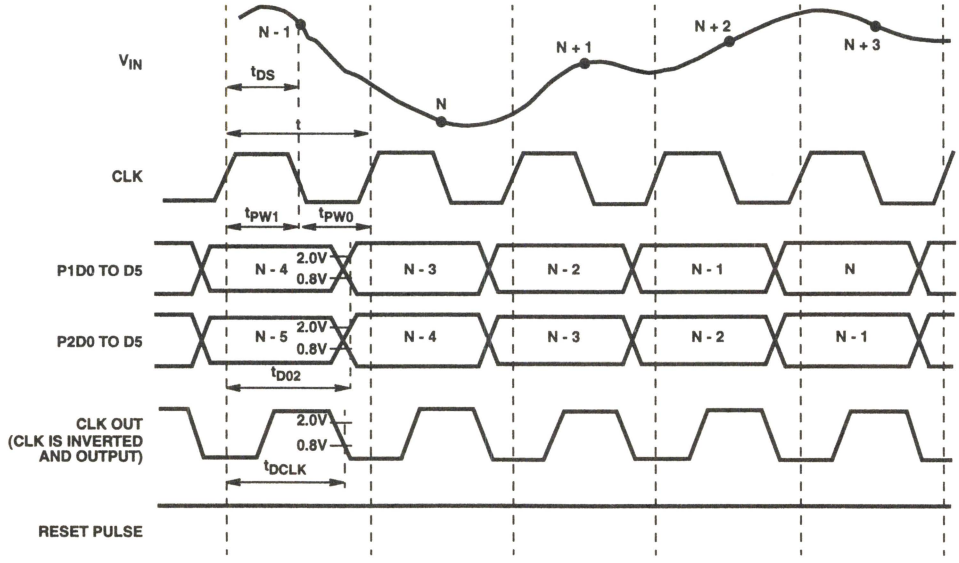


FIGURE 11. STRAIGHT MODE TIMING CHART (SELECT = GND)

Notes on Operation

- The HI3086 is a high-speed A/D converter which is capable of TTL, ECL and PECL level clock input. Characteristic impedance should be properly matched to ensure optimum performance during high-speed operation.
- The power supply and grounding have a profound influence on converter performance. The power supply and grounding method are particularly important during high-speed operation. General points for caution are as follows:
  - The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using a multi-layer board.
  - To prevent interference between AGND and DGND and between AV_{CC} and DV_{CC}, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AV_{CC} and DV_{CC} lines at one point each via a ferrite-bead filter. Shorting the AGND and DGND patterns in one place immediately under the A/D converter improves A/D converter performance.
  - Ground the power supply pins (AV_{CC}, DV_{CC1}, DV_{CC2}, DVEE3) as close to each pin as possible with a 0.1µF or larger ceramic chip capacitor. (Connect the AVCC pin to the AGND pattern and the DV_{CC1}, DV_{CC2}, DV_{EE3} pins to the DGND pattern.)
  - The digital output wiring should be as short as possible. If the digital output wiring is long, the wiring capacitance will increase, deteriorating the output slew rate and resulting in reflection to the output waveform since the original output slew rate is quite fast.
- The analog input pin V_{IN} has an input capacitance of approximately 7pF. To drive the A/D converter with proper frequency response, it is necessary to prevent performance deterioration due to parasitic capacitance or parasitic inductance by using a large capacity drive circuit; keeping wiring as short as possible, and using chip parts for resistors and capacitors, etc.
- The V_{RT} and V_{RB} pins must have adequate bypass to protect them from high-frequency noise. Bypass them to AGND with approximately 1µF tantal capacitor and, 0.1µF chip capacitor as short as possible.
- The offset for residual is generated each for the reference voltage pins V_{RT} and V_{RB}. When the offset voltage has no influence on the IC operation, the voltage should be applied to the V_{RT} and V_{RB} pins directly, keeping the V_{RBS} pin open. When the reference voltage is to be supplied to these pins precisely, form the feedback loop circuit with V_{RT} and V_{RB} as a force pin and adjust the offset voltage to be 0V. See Figure 25 for details.
- If the CLKN/E pin is not used, bypass this pin to DGND with an approximately 0.1µF capacitor. At this time, approximately DGND3 -1.2V voltage is generated. However, this is not recommended for use as threshold voltage V_{BB} as it is too weak.
- When the digital input level is ECL or PECL level, ***/E pins should be used and ***/T pins left open. When the digital input level is TTL, ***/T pins should be used and ***/E pins left open.

Typical Performance Curves

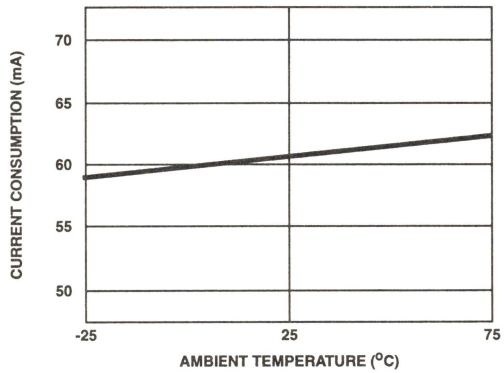


FIGURE 12. CURRENT CONSUMPTION vs AMBIENT TEMPERATURE CHARACTERISTICS

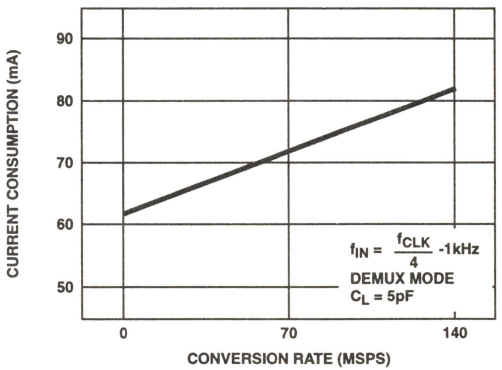


FIGURE 13. CURRENT CONSUMPTION vs CONVERSION RATE CHARACTERISTICS

Typical Performance Curves (Continued)

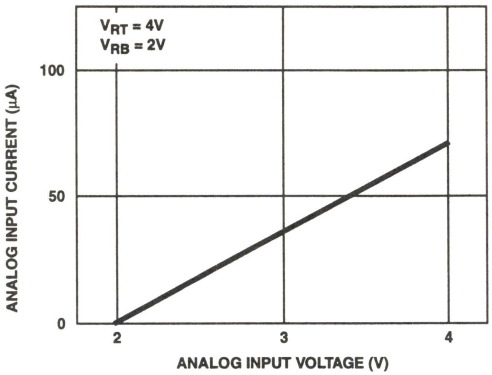


FIGURE 14. ANALOG INPUT CURRENT vs ANALOG INPUT VOLTAGE CHARACTERISTICS

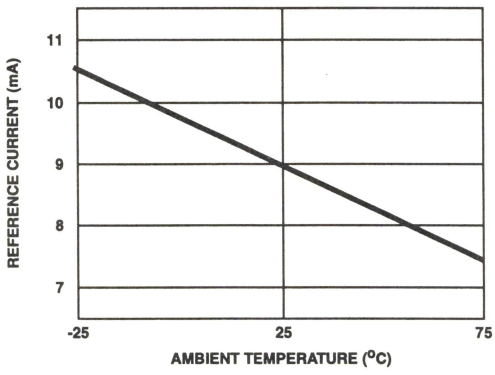


FIGURE 15. REFERENCE CURRENT vs AMBIENT TEMPERATURE CHARACTERISTICS

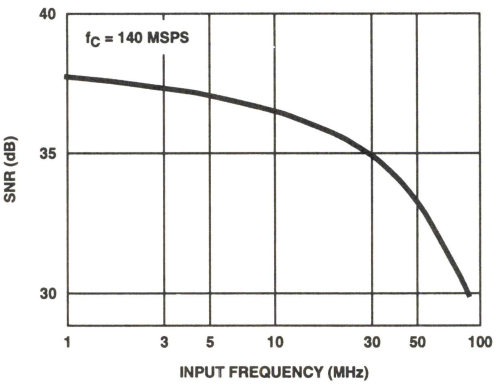


FIGURE 16. SNR vs INPUT FREQUENCY RESPONSE

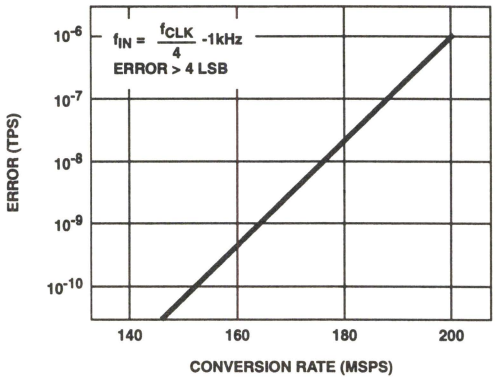


FIGURE 17. ERROR RATE vs CONVERSION RATE CHARACTERISTICS

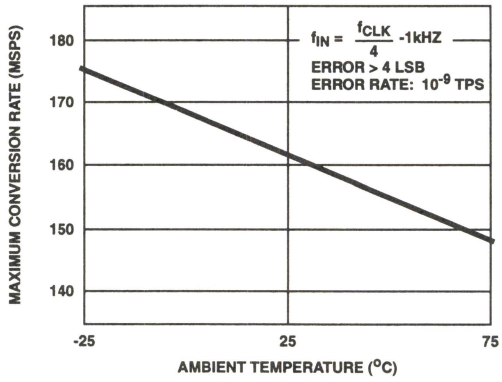


FIGURE 18. MAXIMUM CONVERSION RATE vs AMBIENT TEMPERATURE CHARACTERISTICS

Application Circuits

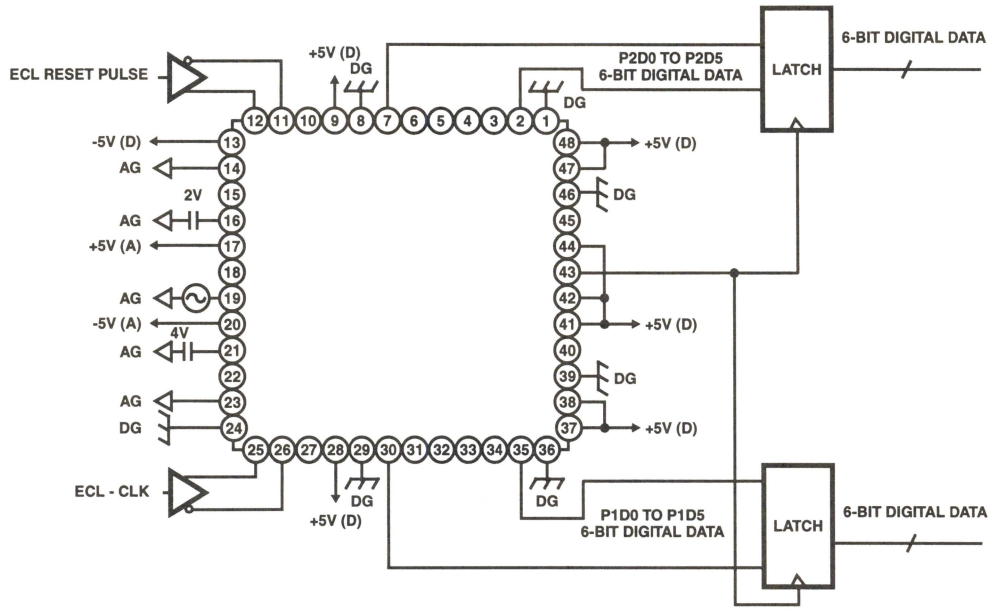


FIGURE 19. DEMUX ECL INPUT

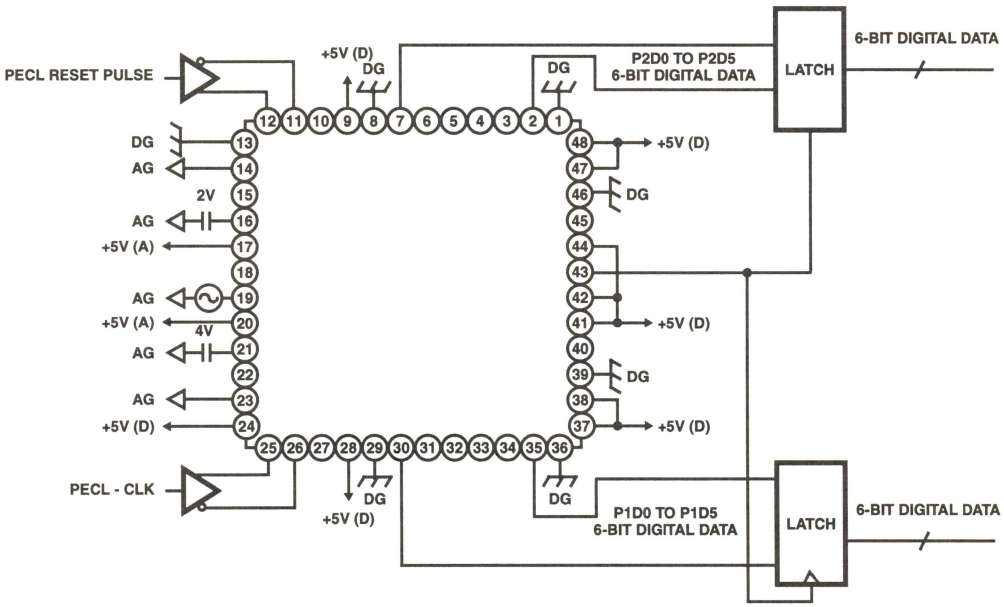


FIGURE 20. DEMUX PECL INPUT

Application Circuits (Continued)

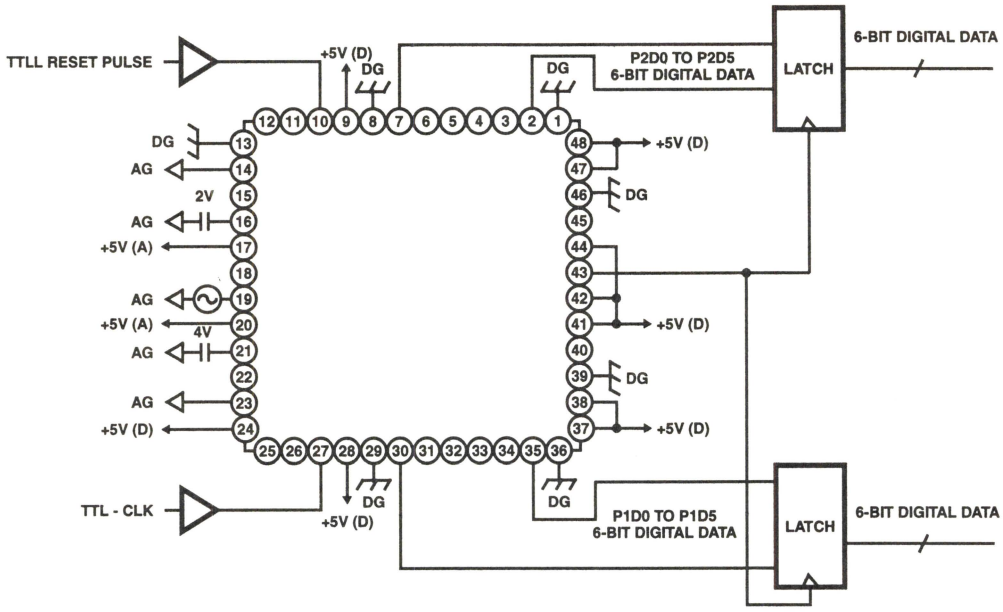


FIGURE 21. DMUX TTL INPUT

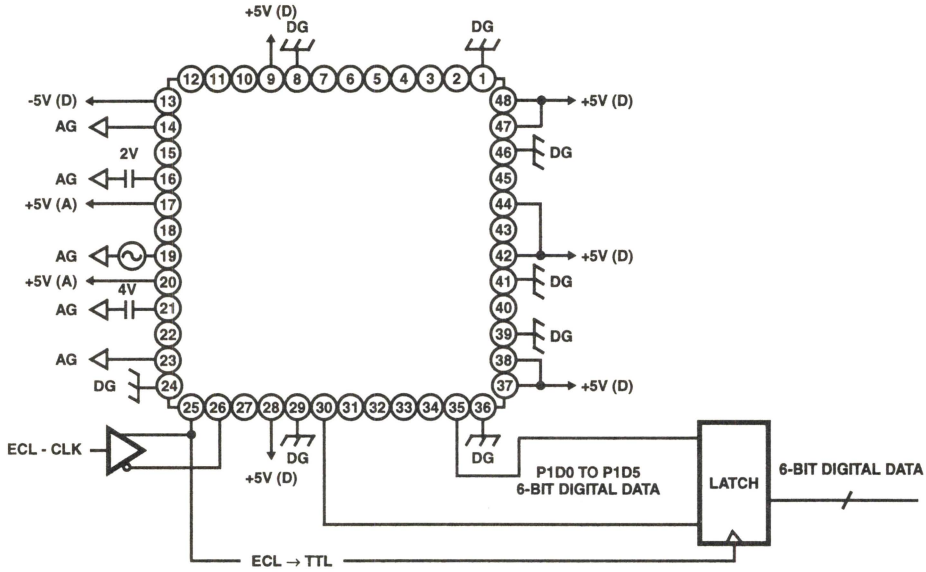


FIGURE 22. STRAIGHT ECL INPUT

Application Circuits (Continued)

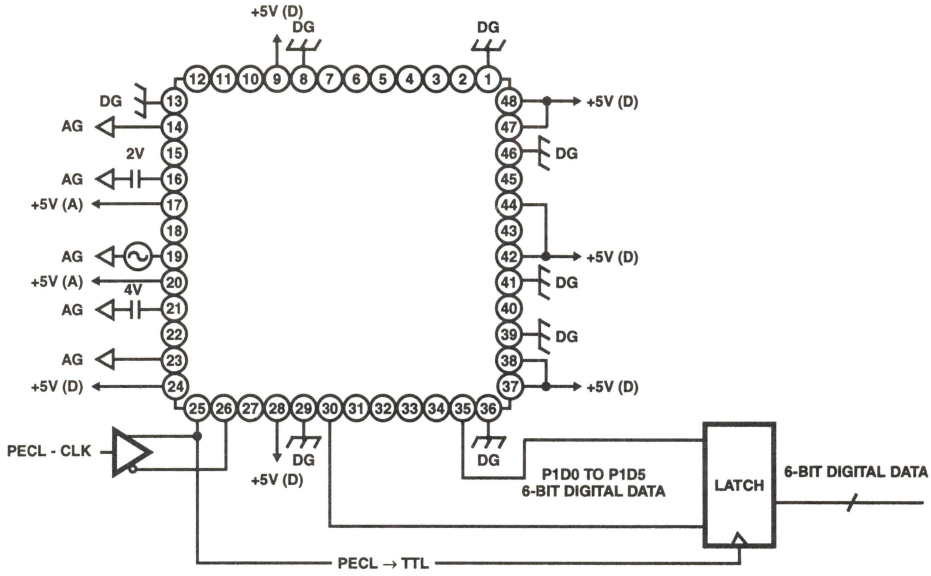


FIGURE 23. STRAIGHT PECL INPUT

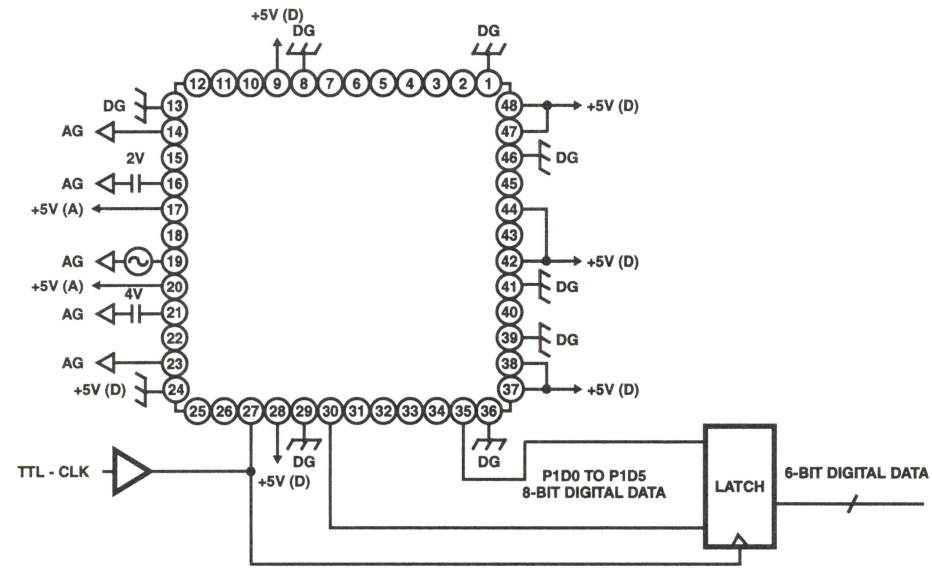


FIGURE 24. STRAIGHT TTL INPUT

Application Circuits (Continued)

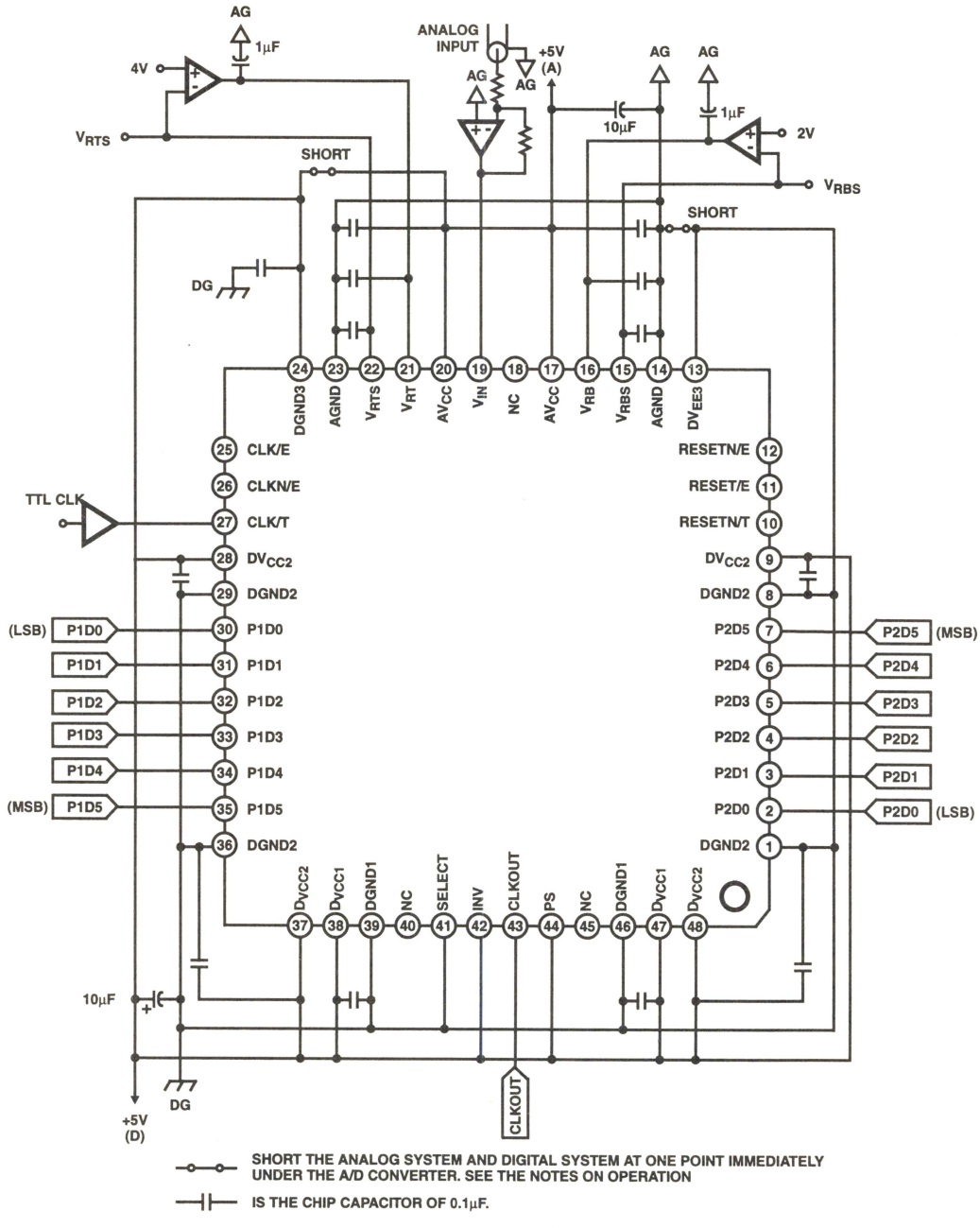


FIGURE 25. STRAIGHT MODE TTL I/O (WHEN A SINGLE POWER SUPPLY IS USED)

HI3304

August 1997

4-Bit, 25 MSPS, Flash A/D Converter

Features

- CMOS Low Power (Typ) 35mW
- Parallel Conversion Technique
- Single Power Supply Voltage . . . . . 3V to 7.5V
- Sampling Rate at 5V Supply 25MHz
- 4-Bit Latched Three-State Output with Overflow and Data Change Outputs
- Maximum Nonlinearity . . . . . $^1/_8$ LSB
- Inherent Resistance to Latch-Up
- Bipolar Input Range with Optional Second Supply
- Input Bandwidth (Typ) 40MHz
- Linearity (INL, DNL):
  - HI3304JIP . . . . . ±0.25 LSB
  - HI3304JIB . . . . . ±0.25 LSB
- Sampling Rate:
  - HI3304JIP 25MHz (40ns)
  - HI3304JIB 25MHz (40ns)

Applications

- Video Digitizing
- High Speed Data Acquisition
- Digital Communication Systems
- Radar Signal Processing

Description

The Harris HI3304 is a CMOS parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high speed digitization. Digitizing at 25MHz, for example, requires only about 35mW.

The HI3304 operates over a wide, full-scale signal input voltage range of 0.5V up to the supply voltage. Power consumption is as low as 10mW, depending upon the clock frequency selected.

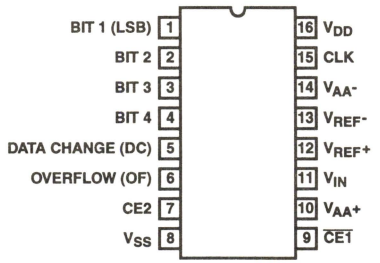
Sixteen paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the HI3304. Fifteen comparators are required to quantize all input voltage levels in this 4-bit converter, and the additional comparator is required for the overflow bit. A data change pin indicates when the present output differs from the previous, thus allowing compaction of data storage.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3304JIP	-40 to 85	16 Ld PDIP	E16.3
HI3304JIB	-40 to 85	16 Ld SOIC	M16.3

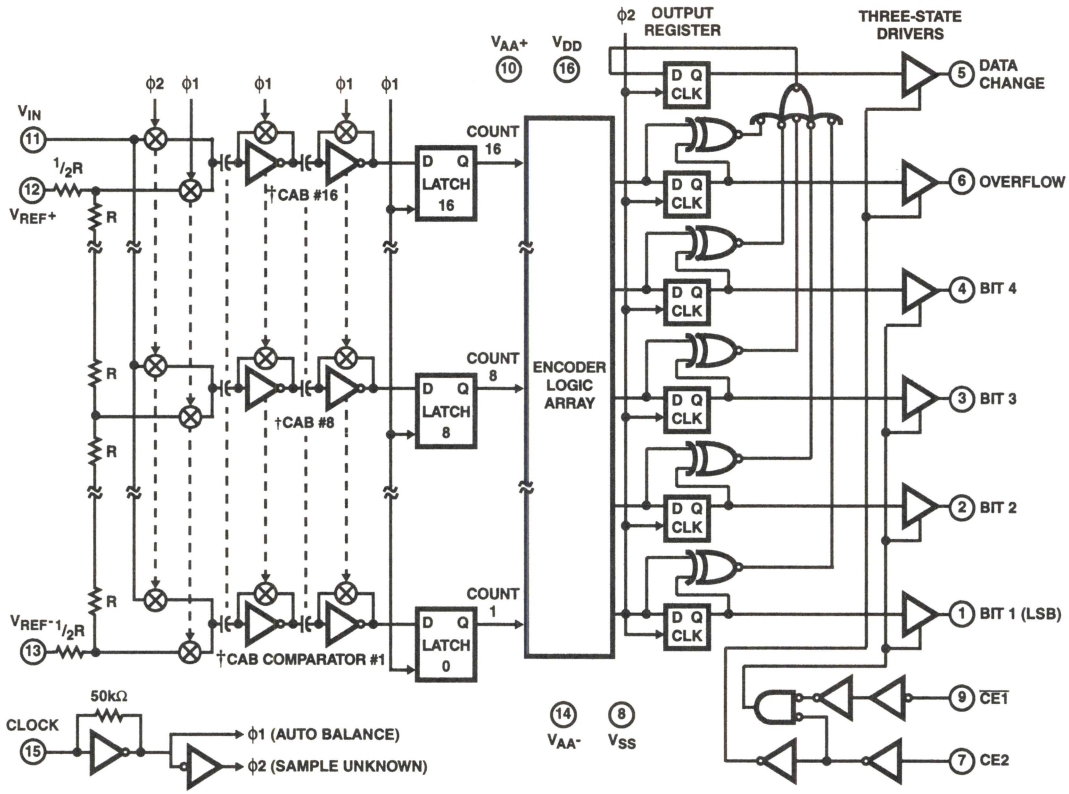
Pinout

HI3304
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

Functional Block Diagram



†Cascaded Auto Balance (CAB)

NOTE: $\overline{CE1}$ and CE2 inputs and data outputs have standard CMOS protection networks to V_{DD} and V_{SS}. Analog inputs and clock have standard CMOS protection networks to $V_{AA}+$ and $V_{AA}-$.

Absolute Maximum Ratings

DC Supply Voltage Range (V_{DD} or V_{AA}+)
(Voltage Referenced to V_{SS} or V_{AA}- Terminal, Whichever is More Negative) ..... -0.5V to +8V
Input Voltage Range
CE1, CE2 Inputs ..... V_{SS} -0.5V to V_{DD} +0.5V
Clock, V_{REF}+, V_{REF}-, V_{IN} Inputs ..... V_{AA} -0.5V to V_{AA} +0.5V
DC Input Current, Any Input ..... ±20mA

Operating Conditions

Supply Voltage Range (V_{DD} or V_{AA}+) ..... 3V to 7.5V
V_{AA}+ Voltage Range ..... V_{DD} -1V to V_{DD} +2.5V
V_{AA}- Voltage Range ..... V_{SS} -2.5V to V_{SS} +1V
Operating Temperature Range ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package	100

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range (T_{STG}) ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = 25°C, V_{REF}+ = 2V, V_{DD} = V_{AA}+ = 5V, V_{AA}- = V_{REF}- = V_{SS} = GND, f_{CLK} = 25MHz Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE						
Resolution			4	-	-	Bits
Input Errors	Integral Linearity Error		-	±0.125	±0.25	LSB
	Differential Linearity Error		-	±0.125	±0.25	LSB
	Offset Error (Unadjusted)		-	-	±1.0	LSB
	Gain Error (Unadjusted)		-	-	±1.0	LSB
DYNAMIC CHARACTERISTICS Input Signal Level 0.5dB Below Full Scale						
Conversion Timing	Aperture Delay		-	3	-	ns
Signal to Noise Ratio (SNR) = $\frac{\text{RMS Signal}}{\text{RMS Noise}}$		f_S = 25MHz, f_{IN} = 100kHz	-	23.7	-	dB
		f_S = 25MHz, f_{IN} = 5MHz	-	23.6	-	dB
Signal to Noise Ratio (SINAD) = $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$		f_S = 25MHz, f_{IN} = 100kHz	-	23.4	-	dB
		f_S = 25MHz, f_{IN} = 5MHz	-	22.8	-	dB
Total Harmonic Distortion, THD		f_S = 25MHz, f_{IN} = 100kHz	-	-34.5	-	dBc
		f_S = 25MHz, f_{IN} = 5MHz	-	-31.0	-	dBc
Effective Number of Bits, ENOB		f_S = 25MHz, f_{IN} = 100kHz	-	3.67	-	Bits
		f_S = 25MHz, f_{IN} = 5MHz	-	3.57	-	Bits
ANALOG INPUTS						
Input Range	Full Scale Input Range	(Notes 1, 4)	0.5	-	V_{AA}	V
Input Loading	Input Capacitance		-	10	-	pF
	Input Current	V_{IN} = 2V (Note 2)	-	150	200	µA
-3dB Input Bandwidth			-	40	-	MHz

Electrical Specifications $T_A = 25^oC$, $V_{REF}+ = 2V$, $V_{DD} = V_{AA}+ = 5V$, $V_{AA}- = V_{REF}- = V_{SS} = GND$, $f_{CLK} = 25MHz$ Unless Otherwise Specified **(Continued)**

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUTS							
Input Range	$V_{REF}+$ Range		(Note 4)	$V_{AA}- +0.5$	-	$V_{AA}+$	V
	$V_{REF}-$ Range		(Note 4)	$V_{AA}-$	-	$V_{AA}+ -0.5$	V
Input Loading	Resistor Ladder Impedance		$V_{IN} = 5V$, CLK = Low	640	-	960	Ω
DIGITAL INPUTS							
Digital Input	Maximum V_{IN}, Low	CLOCK	(Notes 3, 4)	-	-	$0.3 \times V_{AA}$	V
		$\overline{CE1}$, CE2	(Note 4)	-	-	$0.3 \times V_{DD}$	V
	Minimum V_{IN}, High	CLOCK	(Notes 3, 4)	$0.7 \times V_{AA}$	-	-	V
		$\overline{CE1}$, CE2	(Note 4)	$0.7 \times V_{DD}$	-	-	V
	Input Leakage, Except CLK		V = 0V, 5V	-	-	±1	µA
	Input Leakage, CLK		(Note 3)	-	±100	±150	µA
DIGITAL OUTPUTS							
Digital Outputs	Output Low (Sink) Current		$V_O = 0.4V$	6	-	-	mA
	Output High (Source) Current		$V_O = 4.6V$	-3	-	-	mA
	Three-State Leakage Current		$V_O = 0V, 5V$	-	±0.2	±5	µA
TIMING CHARACTERISTICS							
Conversion Timing	Maximum Conversion Speed		CLK = Square Wave	25	35	-	MSPS
	Auto-Balance Time (ϕ1)			20	-	-	ns
	Sample Time (ϕ2)			20	-	5000	ns
Output Timing	Data Valid Delay		(Note 4)	-	30	40	ns
	Data Hold Time		(Note 4)	15	25	-	ns
	Output Enable Time			-	15	-	ns
	Output Disable Time			-	10	-	ns
POWER SUPPLY CHARACTERISTICS							
Device Current, I_{AA}			Continuous Clock	-	5.5	-	mA
			Continuous ϕ2	-	0.4	-	mA
			Continuous ϕ1	-	2	-	mA
Device Current, I_{DD}			Continuous Clock	-	1.5	-	mA
	$V_{AA}+ = 5V$, $V_{SS} = \overline{CE1} = V_{AA}- = CLK = GND$		Continuous ϕ2	-	5	10	mA
	$V_{AA}+ = 7V$		Continuous ϕ1	-	5	20	mA

NOTES:

1. Full scale input range, $V_{REF}+ - V_{REF}-$, may be in the range of 0.5V to $V_{AA}+ - V_{AA}-$ volts. Linearity errors increase at lower full scale ranges, however.
2. Input current is due to energy transferred to the input at the start of the sample period. The average value is dependent on input and V_{DD} voltage.
3. The CLK input is a CMOS inverter with a 50kΩ feedback resistor. It operates from the $V_{AA}+$ and $V_{AA}-$ supplies. It may be AC-coupled with a $1V_{P-P}$ minimum source.
4. Parameter not tested, but guaranteed by design or characterization.

Timing Diagrams

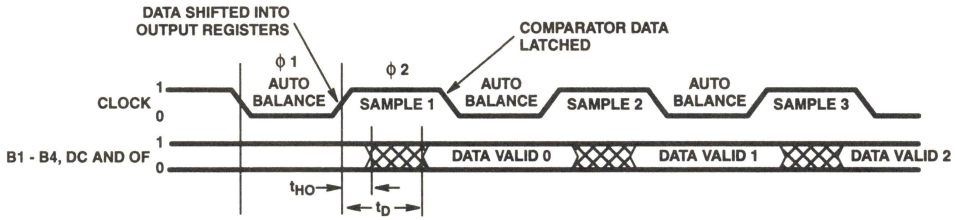


FIGURE 1. TIMING DIAGRAM

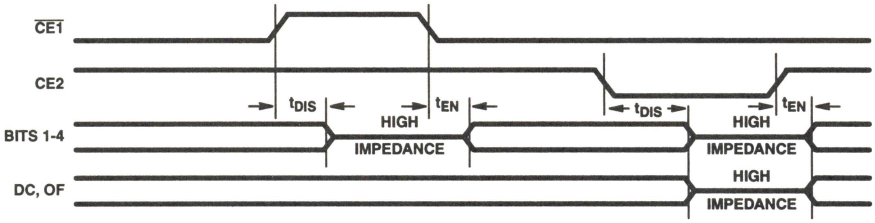


FIGURE 2. OUTPUT ENABLE/DISABLE TIMING

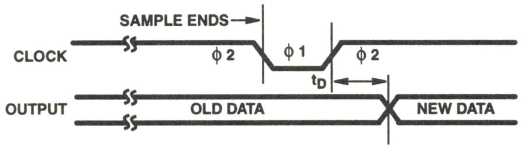


FIGURE 3A.

With ϕ2 as standby state (fastest method, but standby limited to 5µs maximum)

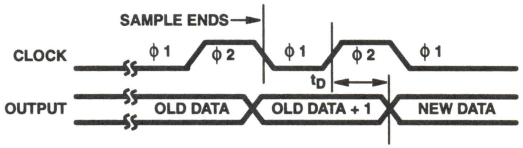


FIGURE 3B.

With ϕ1 as standby state (indefinite standby, double pulse needed)

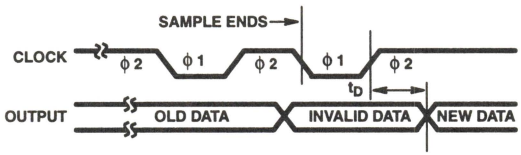


FIGURE 3C.

With ϕ2 as standby state (indefinite standby, lower power than 3B)

FIGURE 3. PULSE-MODE TIMING DIAGRAMS

Typical Performance Curves

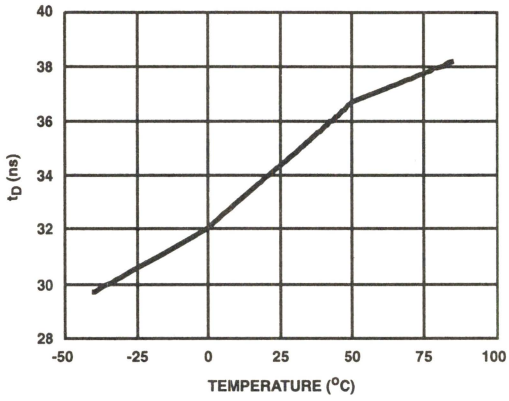


FIGURE 4. DATA DELAY vs TEMPERATURE

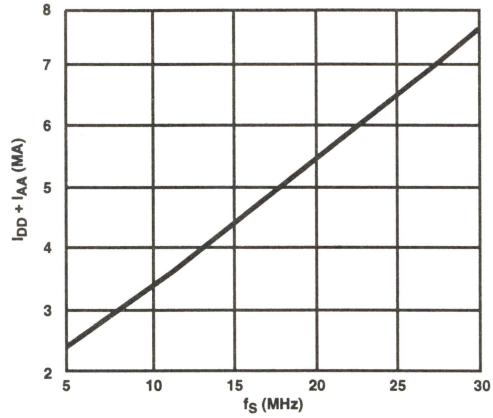


FIGURE 5. DEVICE CURRENT vs SAMPLE FREQUENCY

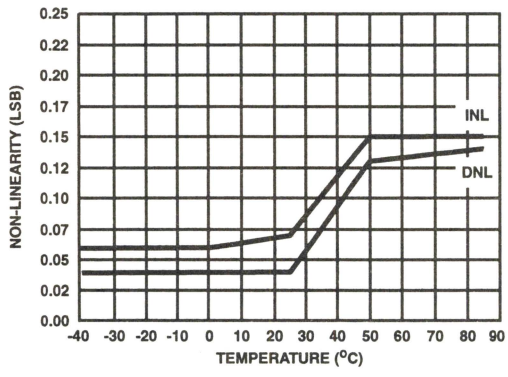


FIGURE 6. NON-LINEARITY vs TEMPERATURE

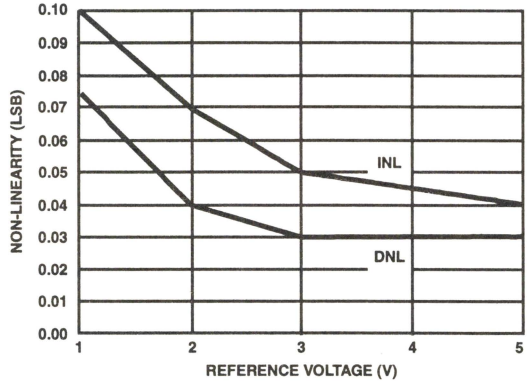


FIGURE 7. NON-LINEARITY vs REFERENCE VOLTAGE

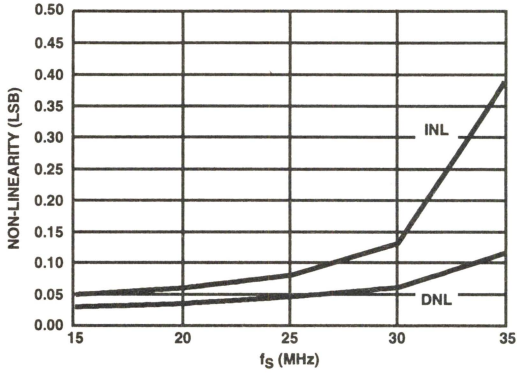


FIGURE 8. NON-LINEARITY vs SAMPLE FREQUENCY

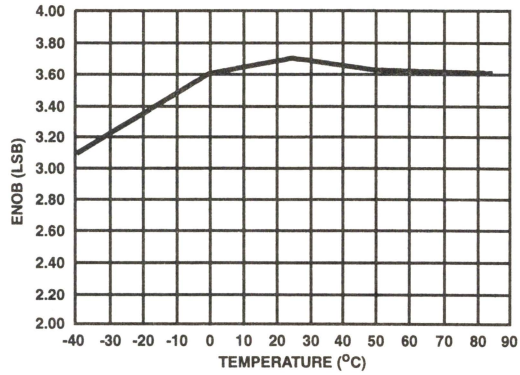


FIGURE 9. EFFECTIVE BITS vs TEMPERATURE

Typical Performance Curves (Continued)

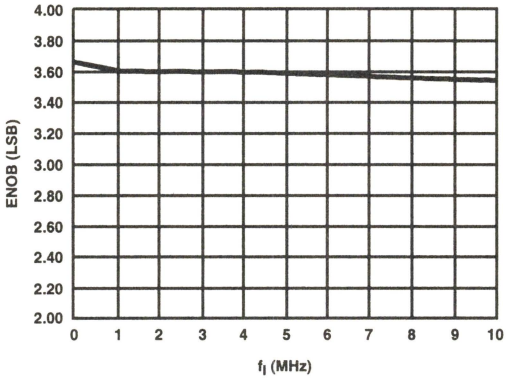


FIGURE 10. EFFECTIVE BITS vs INPUT FREQUENCY

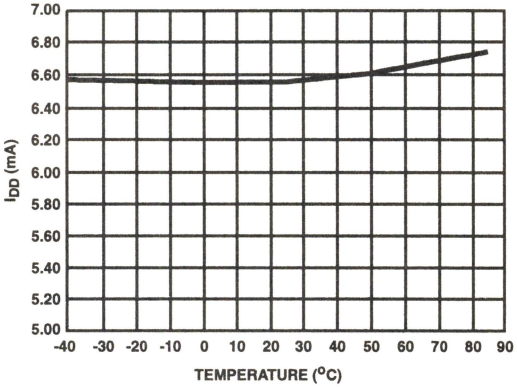


FIGURE 11. DEVICE CURRENT vs TEMPERATURE

Pin Descriptions

PIN NUMBER	NAME	DESCRIPTION	
1	Bit 1	Bit 1 (LSB).	Output Data Bits (High = True)
2	Bit 2	Bit 2.	
3	Bit 3	Bit 3.	
4	Bit 4	Bit 4 (MSB).	
5	DC	Data Change.	
6	OF	Overflow.	
7	CE2	Three-State Output Enable Input, active low. See the Chip Enable Truth Table.	
8	V_{SS}	Digital Ground.	
9	$\overline{CE1}$	Three-State Output Enable Input, active high. See the Chip Enable Truth Table.	
10	$V_{AA}+$	Analog Power Supply, +5V.	
11	V_{IN}	Analog Signal Input.	
12	$V_{REF}+$	Reference Voltage Positive Input.	
13	$V_{REF}-$	Reference Voltage Negative Input.	
14	$V_{AA}-$	Analog Ground.	
15	CLK	Clock Input.	
16	V_{DD}	Digital Power Supply, +5V.	

CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	BIT 1 - BIT 4	DC, OF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't Care

TABLE 1. OUTPUT CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE (V)					OUTPUT CODE					DECIMAL COUNT
	$V_{REF}+ = 1V$ $V_{REF}- = -1V$	1.6V 0V	2V 0V	3.2V 0V	4.8V 0V	OF	B4	B3	B2	B1	
Zero	-1.000	0	0	0	0	0	0	0	0	0	0
1 LSB	-0.875	0.1	0.125	0.2	0.3	0	0	0	0	1	1
2 LSB	-0.750	0.2	0.250	0.4	0.6	0	0	0	1	0	2
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
$^1/_2$ Full Scale -1 LSB	-0.125	0.7	0.875	1.4	2.1	0	0	1	1	1	7
$^1/_2$ Full Scale	0	0.8	1.000	1.6	2.4	0	1	0	0	0	8
$^1/_2$ Full Scale +1 LSB	0.125	0.9	1.125	1.8	2.7	0	1	0	0	1	9
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
Full Scale -1 LSB	0.750	1.4	1.750	2.8	4.2	0	1	1	1	0	14
Full Scale	0.875	1.5	1.875	3.0	4.5	0	1	1	1	1	15
Overflow	1.000	1.6	2.000	3.2	4.8	1	1	1	1	1	31
Step Size	0.125	0.1	0.125	0.2	0.3						

NOTE:

1. The voltages listed are the ideal centers of each output code shown as a function of its associated reference voltage. See Ideal Transfer Curve Figure 6. The output code should exist for an input equal to the ideal center voltage $\pm^1/_2$ of the step size.

Description

Device Operation

A sequential parallel technique is used by the HI3304 converter to obtain its high speed operation. The sequence consists of the "Auto Balance" phase and the "Sample Unknown" phase (Refer to the circuit diagram). Each conversion takes one clock cycle (see Note). The "Auto Balance" (ϕ1) occurs during the Low period of the clock cycle, and the "Sample Unknown" (ϕ2) occurs during the High period of the clock cycle.

NOTE: This device requires only a single-phase clock. The terminology of ϕ1 and ϕ2 refers to the High and Low periods of the same clock.

During the "Auto Balance" phase, a transmission-gate switch is used to connect each of 16 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{TAP}(N) = [(V_{REF}/16) \times N] - [V_{REF}/(2 \times 16)]$$
$$= V_{REF}\,[(2N - 1)/32]$$

Where: $V_{TAP}(N)$ = Reference ladder tap voltage at point N.

V_{REF} = Voltage across $V_{REF}-$ to $V_{REF}+$

N = Tap number (1 through 16)

The other side of the capacitor is connected to a single-stage inverting amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately $(V_{DD} - V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and V_{IN} is switched to all 16 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators whose tap voltages were lower than V_{IN} will drive the comparator outputs to a "low" state. All comparators whose tap voltages were higher than V_{IN} will drive the comparator outputs to a "high" state. A second, capacitor-coupled, auto-zeroed amplifier further amplifies the outputs.

The status of all these comparator amplifiers are stored at the end of this phase (ϕ2), by a secondary latching amplifier stage. Once latched, the status of the 16 comparators is decoded by a 16 to 5 bit decode array and the results are clocked into a storage register at the rising edge of the next ϕ2.

If the input is greater than 31/32 x V_{REF}, the overflow output will go "high". (The bit outputs will remain high). If the output differs from that of the previous conversion, the data change output will go "high".

A three-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B4 when it is in a high state. CE2 will independently disable B1 through B4 and the OF and DC buffers when it is in the low state.

Continuous Clock Operation

One complete conversion cycle can be traced through the HI3304 via the following steps. (Refer to timing diagram Figure 3). The rising edge of the clock input will start a "sample" phase. During this entire "High" state of the clock, the 16 comparators will track the input voltage and the 16 latches will track the comparator outputs. At the falling edge of the clock, all 16 comparator outputs are captured by the 16 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this "Low" state of the clock the output of the latches propagates through the decode array and a 6-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 6-bit code is shifted into the output registers and appears with time delay t_D as valid data at the output of the three-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse Mode Operation

For sampling high speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of three ways. The fastest method is to keep the converter in the Sample Unknown phase, $\phi 2$, during the standby state. The device can now be pulsed through the Auto Balance phase with as little as 20ns. The analog value is captured on the leading edge of $\phi 1$ and is transferred into the output registers on the trailing edge of $\phi 1$. We are now back in the standby state, $\phi 2$, and another conversion can be started within 20ns, but not later than 5µs due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between $\phi 2$ and $\phi 1$, the lower the power consumption. (See Timing Diagram Figure 3A).

The second method uses the Auto Balance phase, $\phi 1$, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two $\phi 2$ pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second $\phi 2$ pulse is needed to transfer the date into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes place in 40ns, but the repetition rate may be as slow as desired. The disadvantage to this method is the slightly higher device dissipation due to the low ratio of $\phi 2$ to $\phi 1$. (See Timing Diagram Figure 3B).

For applications requiring both indefinite standby and lowest power, standby can be in the $\phi 2$ (Sample Unknown) state with two $\phi 1$ pulses to generate valid data (see Figure 3C). The conversion process now takes 60ns. [Note that the above numbers do not include the t_D (Output Delay) time.]

Increased Accuracy

In most case the accuracy of the HI3304 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, two adjustments can be made to obtain better accuracy; i.e., offset trim and gain trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a DC shift to V_{IN} or by the offset trim of the op amp. When this is not possible the V_{REF}- input can be adjusted to produce an offset trim.

The theoretical input voltage to produce the first transition is $^1/_2$ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = {}^1/_2 \text{ LSB} = {}^1/_2(V_{REF}/16)$$
$$= V_{REF}/32$$

Adjust offset by applying this input voltage and adjusting the V_{REF}- voltage or input amplifier offset until an output code alternating between 0 and 1 occurs.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 15 to overflow transition. That voltage is $^1/_2$ LSB less than V_{REF}+ and is calculated as follows:

$$V_{IN} \text{ (15 to 16 transition)} = V_{REF} - V_{REF}/32$$
$$= V_{REF} (31/32)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 15 to overflow transition. Now adjust V_{REF}+ until that transition occurs on the outputs.

Layout, Input and Supply Considerations

The HI3304 should be mounted on a ground-planed, printed-circuit board, with good high-frequency decoupling capacitors mounted as close as possible. If the supply is noisy, decouple V_{AA}+ with a resistor as shown in Figure 12A. The HI3304 outputs current spikes to its input at the start of the auto-balance and sample clock phases. A low impedance source, such as a locally-terminated 50Ω coax cable, should be used to drive the input terminal. A fast-settling buffer such as the HA-5033, HA-5242, or CA3450 should be used if the source is high impedance. The V_{REF} terminals also have current spikes, and should be well bypassed.

Care should be taken to keep digital signals away from the analog input, and to keep digital ground currents away from the analog ground. If possible, the analog ground should be connected to digital ground only at the HI3304.

Bipolar Operation

The HI3304, with separate analog (V_{AA}+, V_{AA}-) and digital (V_{DD}, V_{SS}) supply pins, allows true bipolar or negative input operation. The V_{AA}- pin may be returned to a negative supply (observing maximum voltage ratings to V_{AA}+ or V_{DD} and recommended rating to V_{SS}), thus allowing the V_{REF}- potential also to be negative. Figure 12B shows operation with an input range of -1V to +1V. Similarly, V_{AA}+ and V_{REF}+ could be maintained at a higher voltage than V_{DD}, for an input range above the digital supply.

Digital Input and Output Levels

The clock input is a CMOS inverter operating from and with logic input levels determined by the V_{AA} supplies. If V_{AA}+ or V_{AA}- are outside the range of the digital supplies, it may be necessary to level shift the clock input to meet the required 30% to 70% of V_{AA} input swing. Figure 12B shows an example for a negative V_{AA}-.

An alternate way of driving the clock is to capacitively couple the pin from a source of at least $1V_{P-P}$. An internal 50kΩ feedback resistor will keep the DC level at the intrinsic trip point. Extremely non-symmetrical clock waveforms should be avoided, however.

The remaining digital inputs and outputs are referenced to V_{DD} and V_{SS}. If TTL or other lower voltage sources are to drive the HI3304, either pull-up resistors or CD74HCT series "QMOS" buffers are recommended.

5-Bit Resolution

To obtain 5-bit resolution, two HI3304s can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enable controls - all of which are available on the HI3304.

The first step for connecting a 5-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 13. Since the absolute-resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the fifth bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 4) are now connected in parallel to complete the circuitry.

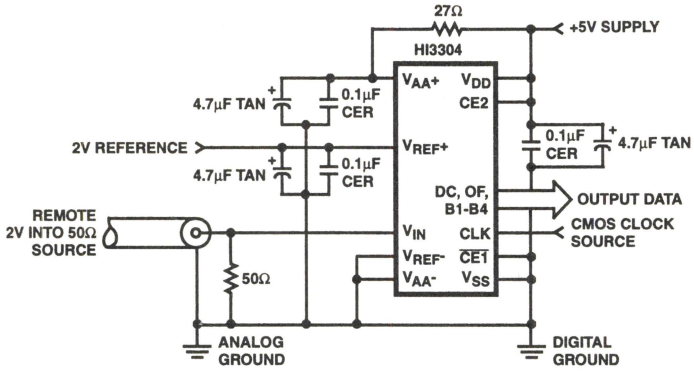


FIGURE 12A. TYPICAL HI3304 UNIPOLAR CIRCUIT CONFIGURATION

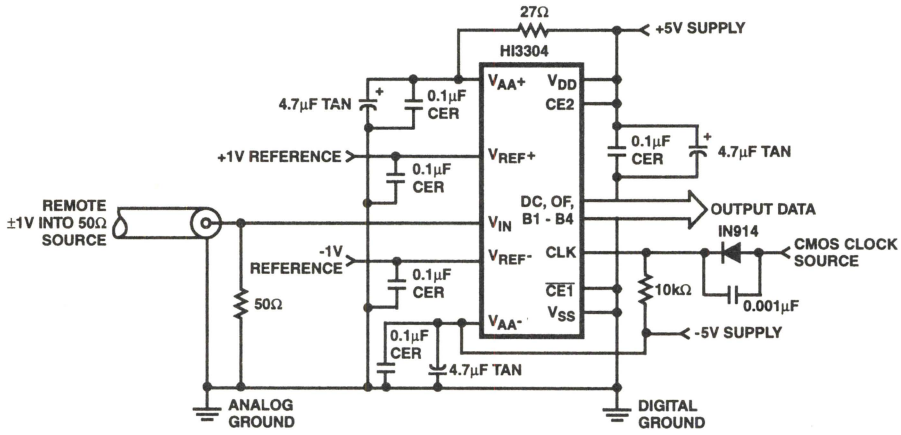


FIGURE 12B. TYPICAL HI3304 BIPOLAR CIRCUIT CONFIGURATION

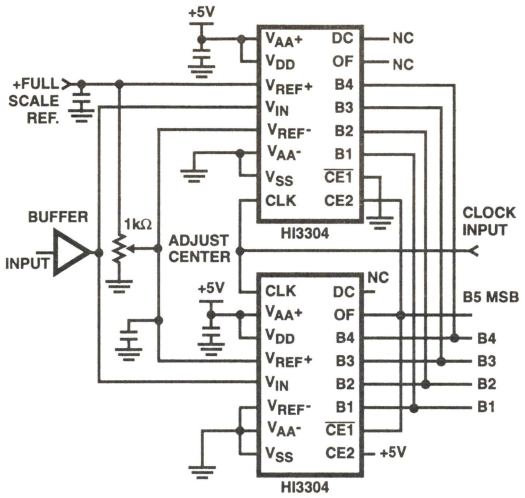


FIGURE 13. TYPICAL HI3304 5-BIT CONFIGURATION

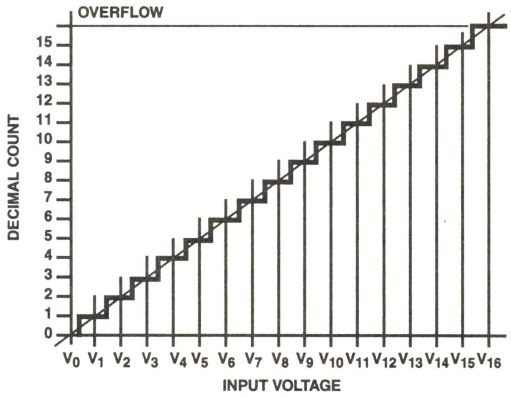


FIGURE 14. IDEAL TRANSFER CURVE

Definitions

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI3304. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from fullscale for all these tests.

Signal-to-Noise (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$ENOB = (SINAD - 1.76 + V_{CORR})/6.02$,

where: $V_{CORR} = 0.5dB$.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

Operating and Handling Considerations

HANDLING

All inputs and outputs of CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

OPERATING

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause the power supply voltages to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} or $V_{AA}+$ nor less than V_{SS} or $V_{AA}-$ (depending upon which supply the protection network is referenced. See Maximum Ratings). Input currents must not exceed 20mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to any supply potential may damage CMOS devices by exceeding the maximum device dissipation.

HARRIS SEMICONDUCTOR

HI3306

August 1997

6-Bit, 15 MSPS, Flash A/D Converter

Features

- CMOS Low Power (Typ) 55mW
- Parallel Conversion Technique
- Single Power Supply Voltage . . . . . 3V to 7.5V
- Sampling Rate with Single 5V Supply 15MHz
- 6-Bit Latched Three-State Output with Overflow Bit
- Linearity (INL, DNL):
  - HI3306JIP/15 . . . . . ±0.5 LSB
  - HI3306JIP/10 . . . . . ±0.5 LSB
  - HI3306JIB/15 . . . . . ±0.5 LSB
  - HI3306JIB/10 . . . . . ±0.5 LSB
- Sampling Rate:
  - HI3306JIP/15 . . . . . 15MHz (67ns)
  - HI3306JIP/10 . . . . . 10MHz (100ns)
  - HI3306JIB/15 . . . . . 15MHz (67ns)
  - HI3306JIB/10 . . . . . 10MHz (100ns)

Applications

- Video Digitizing
- Digital Communication Systems
- High Speed Data Acquisition
- Radar Signal Processing

Description

The HI3306 family are CMOS parallel (FLASH) analog-to-digital converters designed for applications demanding both low power consumption and high speed digitization. Digitizing at 15MHz, for example, requires only about 55mW.

The HI3306 family operates over a wide, full scale signal input voltage range of 1V up to the supply voltage. Power consumption is as low as 15mW, depending upon the clock frequency selected. The HI3306 offers improved linearity at a lower reference voltage and high operating speed with a 5V supply.

The overflow bit makes possible the connection of two or more HI3306s in series to increase the resolution of the conversion system.

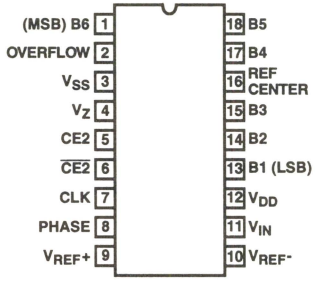
Sixty-four paralleled auto balanced comparators measure the input voltage with respect to a known reference to produce the parallel bit outputs in the HI3306. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

Ordering Information

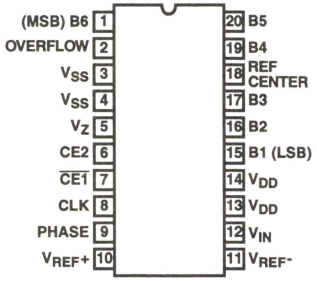
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI3306JIP/15	-40 to 85	18 Ld PDIP	E18.3
HI3306JIP/10	-40 to 85	18 Ld PDIP	E18.3
HI3306JIB/15	-40 to 85	20 Ld SOIC	M20.3
HI3306JIB/10	-40 to 85	20 Ld SOIC	M20.3

Pinouts

HI3306 (PDIP)
TOP VIEW



HI3306 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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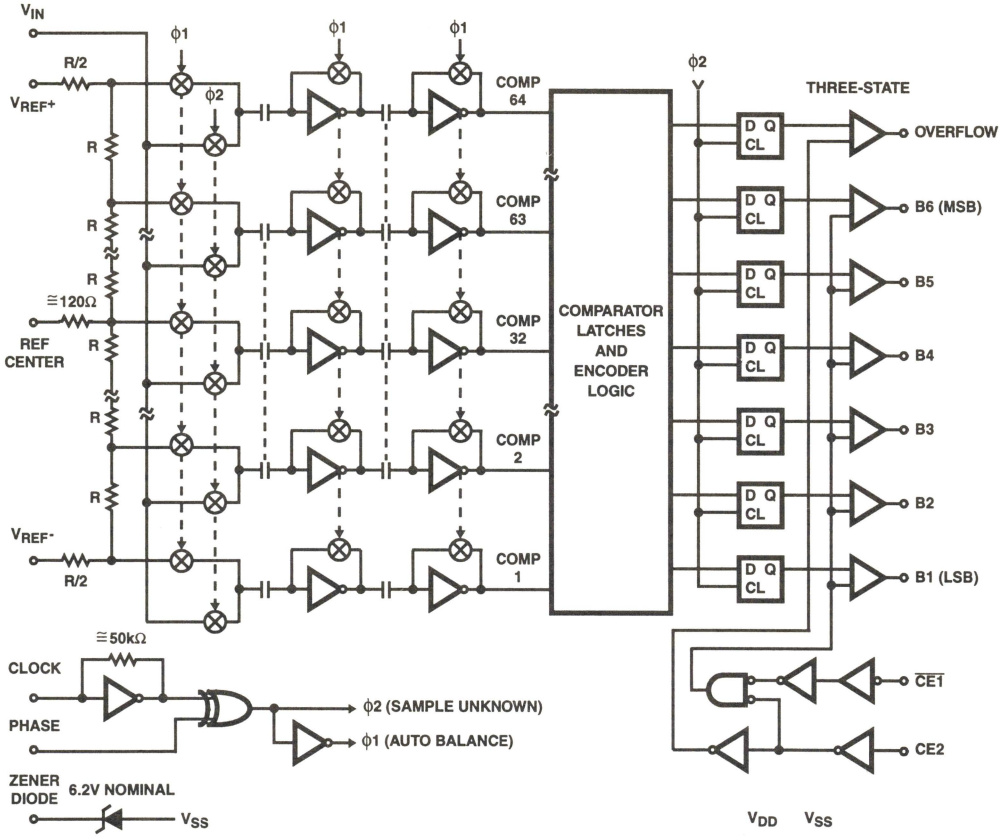
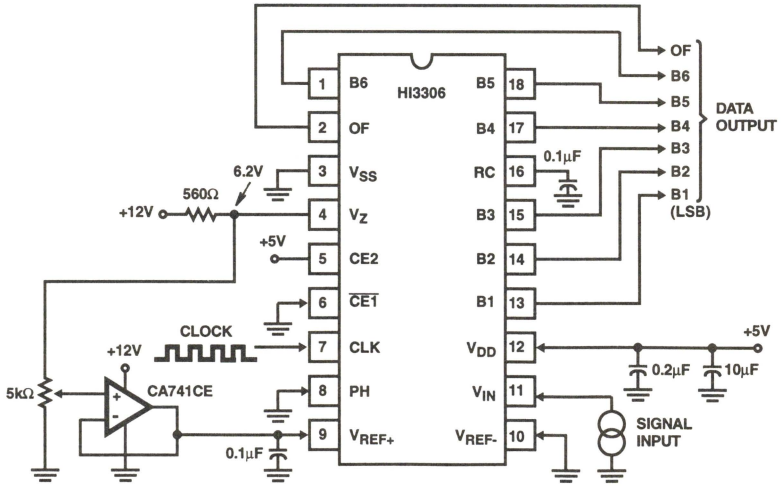
File Number **4136.1**

Functional Block Diagram



Typical Application Circuit



Absolute Maximum Ratings

DC Supply Voltage Range, V_{DD}
Voltage Referenced to V_{SS} Terminal . . . . . -0.5V to +8.5V
Input Voltage Range
All Inputs Except Zener. . . . . -0.5V to V_{DD} + 0.5V
DC Input Current
CLK, PH, $\overline{CE1}$, CE2, V_{IN} . . . . . ±20mA

Operating Conditions

Supply Voltage Range . . . . . .3V to 8V
Temperature Range (T_A) . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	75
SOIC Package	100

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = 25°C, V_{DD} = 5V, V_{REF}+ = 4.8V, V_{SS} = V_{REF}- = GND, Clock = 15MHz Square Wave for HI3306XXX/15, 10MHz for HI3306XXX/10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		6	-	-	Bits
Integral Linearity Error, INL		-	±0.25	±0.5	LSB
Differential Linearity Error, DNL		-	±0.25	±0.5	LSB
Offset Error (Unadjusted)	(Note 1)	-	±0.5	±1	LSB
Gain Error (Unadjusted)	(Note 2)	-	±0.5	±1	LSB
Gain Temperature Coefficient		-	+0.1	-	mV/°C
Offset Temperature Coefficient		-	-0.1	-	mV/°C
DYNAMIC CHARACTERISTICS Input Signal Level 0.5dB Below Full Scale					
Maximum Conversion Speed HI3306XXX/10		10	13	-	MSPS
HI3306XXX/15		15	20	-	MSPS
Maximum Conversion Speed HI3306XXX/10	(Note 4) $\phi1, \phi2 \geq$ Minimum	12	-	-	MSPS
HI3306XXX/15		18	-	-	MSPS
Allowable Input Bandwidth	(Note 4)	DC	-	$f_{CLOCK/2}$	MHz
-3dB Input Bandwidth		-	30	-	MHz
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_S = 15MHz, f_{IN} = 100kHz	-	34.6	-	dB
	f_S = 15MHz, f_{IN} = 5MHz	-	33.4	-	dB
Signal to Noise Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_S = 15MHz, f_{IN} = 100kHz	-	34.2	-	dB
	f_S = 15MHz, f_{IN} = 5MHz	-	29.0	-	dB
Total Harmonic Distortion, THD	f_S = 15MHz, f_{IN} = 100kHz	-	-46.0	-	dBc
	f_S = 15MHz, f_{IN} = 5MHz	-	-30.0	-	dBc
Effective Number of Bits, ENOB	f_S = 15MHz, f_{IN} = 100kHz	-	5.5	-	Bits
	f_S = 15MHz, f_{IN} = 5MHz	-	4.5	-	Bits
ANALOG INPUTS					
Positive Full Scale Input Range	(Notes 3, 4)	1	4, 8	V_{DD} + 0.5	V
Negative Full Scale Input Range	(Notes 3, 4)	-0.5	0	V_{DD} - 1	V
Input Capacitance		-	15	-	pF

Electrical Specifications $T_A = 25^oC$, $V_{DD} = 5V$, $V_{REF}+ = 4.8V$, $V_{SS} = V_{REF}- = GND$, Clock = 15MHz Square Wave for HI3306XXX/15, 10MHz for HI3306XXX/10 **(Continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Current		$V_{IN} = 4.92V$, $V_{DD} = 5V$	-	-	±500	µA
INTERNAL VOLTAGE REFERENCE						
Zener Voltage		$I_Z = 10mA$	5.4	6.2	7.4	V
Zener Dynamic Impedance		$I_Z = 10mA, 20mA$	-	12	25	Ω
Zener Temperature Coefficient			-	-0.5	-	$mV/^oC$
REFERENCE INPUTS						
Resistor Ladder Impedance			650	1100	1550	Ω
DIGITAL INPUTS						
Maximum V_{IN}, Logic 0		All Digital Inputs (Note 4)	-	-	$0.3 \times V_{DD}$	V
Maximum V_{IN}, Logic 1		All Digital Inputs (Note 4)	$0.7 \times V_{DD}$	-	-	V
Digital Input Current		Except CLK, $V_{IN} = 0V, 5V$	-	±1	±5	µA
Digital Input Current		CLK Only	-	±100	±200	µA
DIGITAL OUTPUTS						
Digital Output Three-State Leakage		$V_{OUT} = 0V, 5V$	-	±1	±5	µA
Digital Output Source Current		$V_{OUT} = 4.6V$	-1.6	-	-	mA
Digital Output Sink Current		$V_{OUT} = 0.4V$	3.2	-	-	mA
TIMING CHARACTERISTICS						
Auto Balance Time (ϕ1)	HI3306XXX/10		50	-	∞	ns
	HI3306XXX/15		33	-	∞	
Sample Time (ϕ2)	HI3306XXX/10	(Note 4)	33	-	5000	ns
	HI3306XXX/15		22	-	5000	ns
Aperture Delay			-	8	-	ns
Aperture Jitter			-	100	-	ps_{P-P}
Output Data Valid Delay, t_D	HI3306XXX/10		-	35	50	ns
	HI3306XXX/15		-	30	40	ns
Output Data Hold Time, t_H		(Note 4)	15	25	-	ns
Output Enable Time, t_{EN}			-	20	-	ns
Output Disable Time, t_{DIS}			-	15	-	ns
POWER SUPPLY CHARACTERISTICS						
I_{DD} Current, Refer to Figure 4	HI3306XXX/10	Continuous Conversion (Note 4)	-	11	20	mA
	HI3306XXX/15		-	14	25	mA
I_{DD} Current		Continuous ϕ1	-	7.5	15	mA

NOTES:

1. OFFSET ERROR is the difference between the input voltage that causes the 00 to 01 output code transition and $(V_{REF}+ - V_{REF}-)/128$.
2. GAIN ERROR is the difference the input voltage that causes the $3F_{16}$ to overflow output code transition and $(V_{REF}+ - V_{REF}-) \times 127/128$.
3. The total input voltage range, set by $V_{REF}+$ and $V_{REF}-$, may be in the range of 1 to $(V_{DD} + 1)$ V.
4. Parameter not tested, but guaranteed by design or characterization.

Timing Waveforms

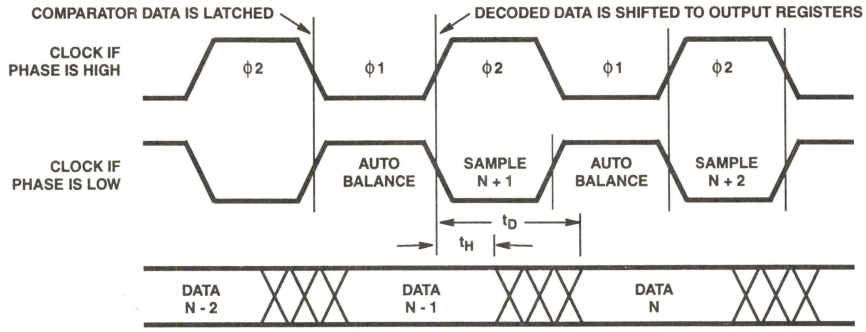


FIGURE 1. INPUT-TO-OUTPUT

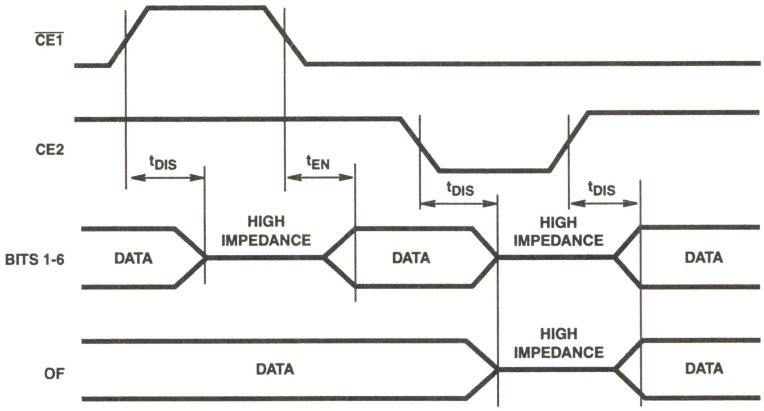


FIGURE 2. OUTPUT ENABLE

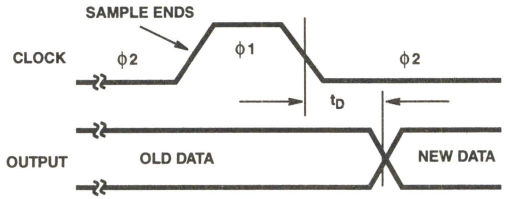


FIGURE 3A.

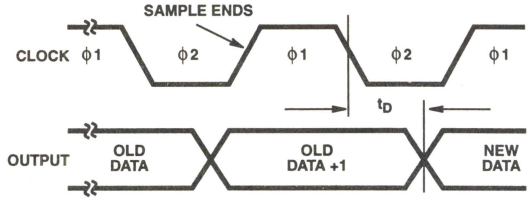


FIGURE 3B.

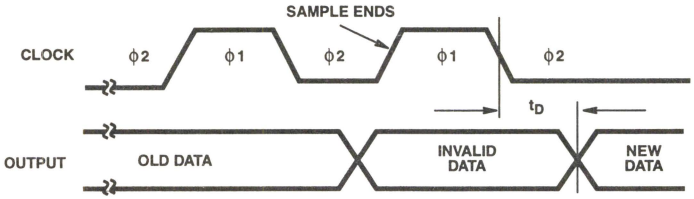


FIGURE 3C.

FIGURE 3. PULSE MODE

Typical Performance Curves

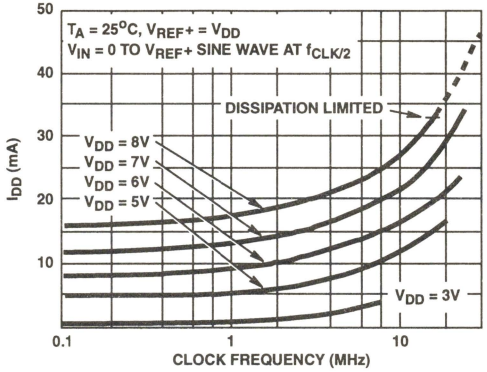


FIGURE 4. TYPICAL I_{DD} AS A FUNCTION OF V_{DD}

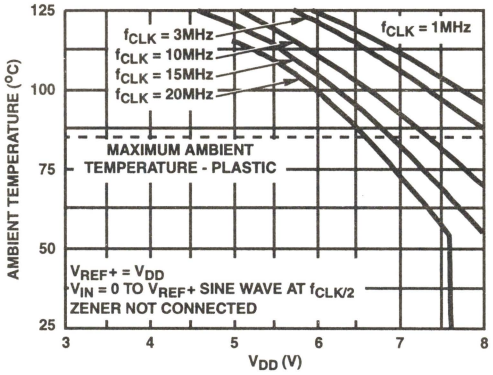


FIGURE 5. TYPICAL MAXIMUM AMBIENT TEMPERATURE AS A FUNCTION OF SUPPLY VOLTAGE

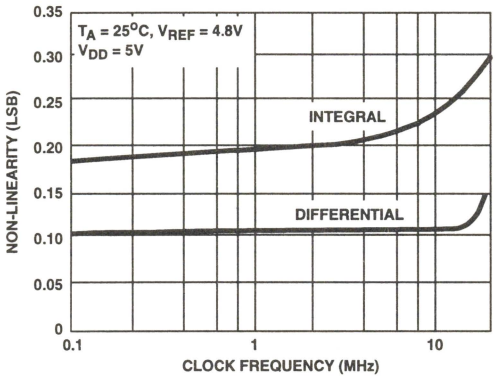


FIGURE 6. TYPICAL NON-LINEARITY AS A FUNCTION OF CLOCK SPEED

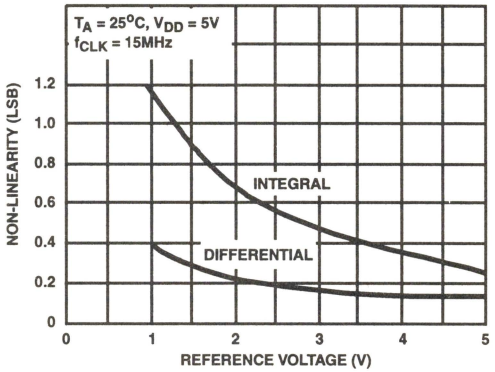


FIGURE 7. TYPICAL NON-LINEARITY AS A FUNCTION OF REFERENCE VOLTAGE

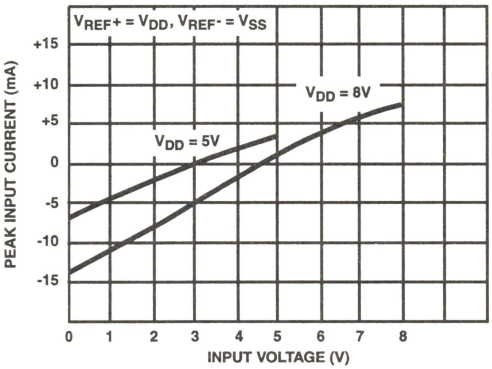


FIGURE 8. TYPICAL PEAK INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

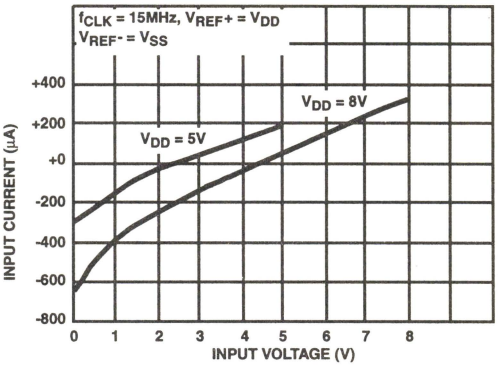


FIGURE 9. TYPICAL AVERAGE INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

Typical Performance Curves (Continued)

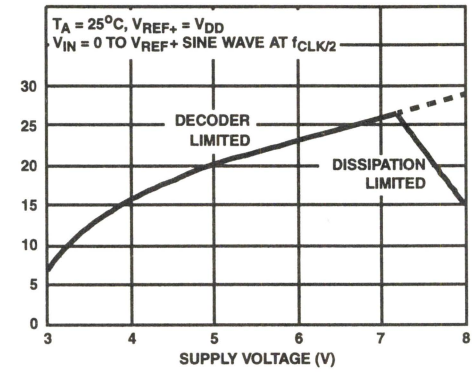


FIGURE 10. TYPICAL MAXIMUM CLOCK FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

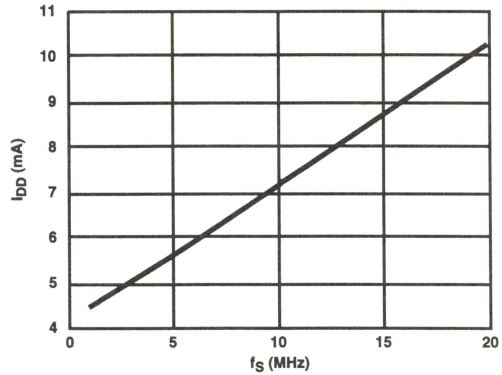


FIGURE 11. DEVICE CURRENT vs SAMPLE FREQUENCY

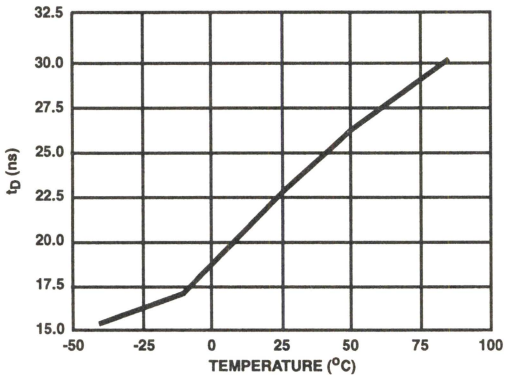


FIGURE 12. DATA DELAY vs TEMPERATURE

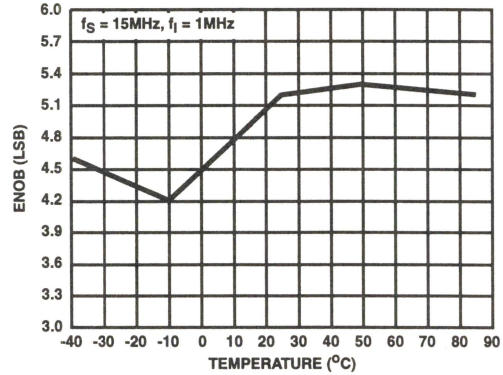


FIGURE 13. ENOB vs TEMPERATURE

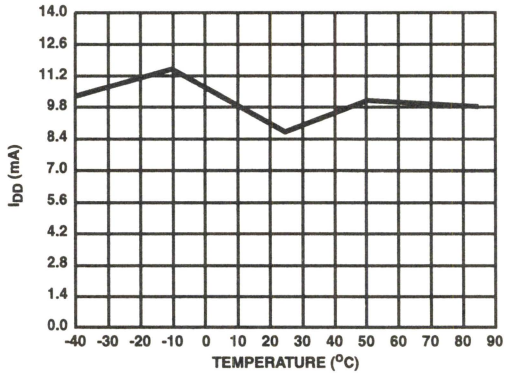


FIGURE 14. I_{DD} vs TEMPERATURE

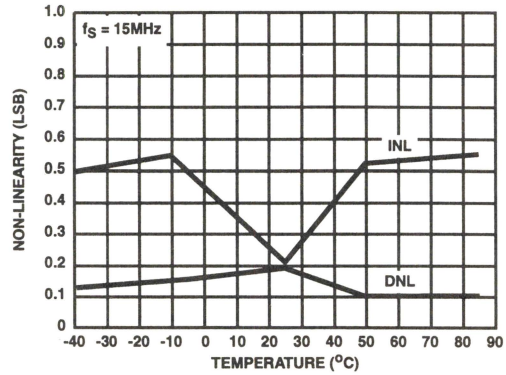


FIGURE 15. NON-LINEARITY vs TEMPERATURE

Typical Performance Curves (Continued)

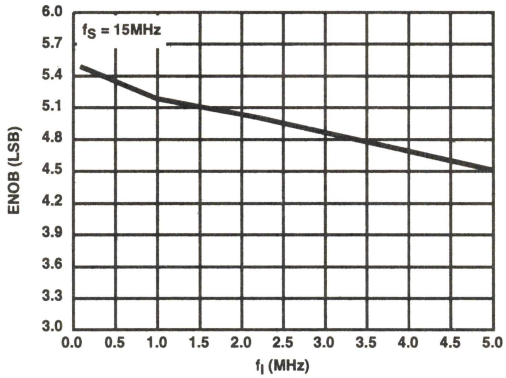


FIGURE 16. ENOB vs INPUT FREQUENCY

Pin Descriptions

PIN NUMBER		NAME	DESCRIPTION
PDIP	SOIC		
1	1	B6	Bit 6, Output (MSB).
2	2	OF	Overflow, Output.
3	3, 4	V_{SS}	Digital Ground.
4	5	V_Z	Zener Reference Output.
5	6	CE2	Three-State Output Enable Input, Active Low. See Table 1.
6	7	$\overline{CE1}$	Three-State Output Enable Input, Active High. See Table 1.
7	8	CLK	Clock Input.
8	9	Phase	Sample clock phase control input. When PHASE is low, "Sample Unknown" occurs when the clock is low and "Auto Balance" occurs when the clock is high (see text).
9	10	$V_{REF}+$	Reference Voltage Positive Input.
10	11	$V_{REF}-$	Reference Voltage Negative Input.
11	12	V_{IN}	Analog Signal Input.
12	13, 14	V_{DD}	Power Supply, +5V.
13	15	B1	Bit 1, Output (LSB).
14	16	B2	Bit 2, Output.
15	17	B3	Bit 3, Output.
16	18	REF(CTR)	Reference Ladder Midpoint.
17	19	B4	Bit 4, Output.
18	20	B5	Bit 5, Output.

TABLE 1. CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	B1 - B6	OF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't care

TABLE 2. OUTPUT CODE TABLE

CODE DESCRIPTION	(NOTE 1) INPUT VOLTAGE V_{REF} 6.40 (V)	V_{REF} 5.12 (V)	V_{REF} 4.80 (V)	V_{REF} 3.20 (V)	BINARY OUTPUT CODE (LSB) OF	B6	B5	B4	B3	B2	B1	DECIMAL COUNT
Zero	0.00	0.00	0.00	0.00	0	0	0	0	0	0	0	0
1 LSB	0.10	0.08	0.075	0.05	0	0	0	0	0	0	1	1
2 LSB	0.20	0.16	0.15	0.10	0	0	0	0	0	1	0	2
•		•						•				•
•		•						•				•
•		•						•				•
•		•						•				•
$^1/_2$ Full Scale - 1 LSB	3.10	2.48	2.325	1.55	0	0	1	1	1	1	1	31
$^1/_2$ Full Scale	3.20	2.56	2.40	1.60	0	1	0	0	0	0	0	32
$^1/_2$ Full Scale + 1 LSB	3.30	2.64	2.475	1.65	0	1	0	0	0	0	1	33
•		•						•				•
•		•						•				•
•		•						•				•
•		•						•				•
Full Scale - 1 LSB	6.20	4.96	4.65	3.10	0	1	1	1	1	1	0	62
Full Scale	6.30	5.04	4.725	3.15	0	1	1	1	1	1	1	63
Overflow	6.40	5.12	4.80	3.20	1	1	1	1	1	1	1	127

NOTE:

1. The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Device Operation

A sequential parallel technique is used by the HI3306 converter to obtain its high speed operation. The sequence consists of the "Auto Balance" phase $\phi 1$ and the "Sample Unknown" phase $\phi 2$. (Refer to the circuit diagram.) Each conversion takes one clock cycle (see Note). With the phase control low, the "Auto Balance" ($\phi 1$) occurs during the High period of the clock cycle, and the "Sample Unknown" ($\phi 2$) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, a transmission-gate switch is used to connect each of 64 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{TAP}(N) = [(V_{REF}/64) \times N] - [V_{REF}/(2 \times 64)],$$

$$= V_{REF}[(2N - 1)/126],$$

Where: $V_{TAP}(N)$ = reference ladder tap voltage at point N,

V_{REF} = voltage across V_{REF}- to V_{REF}+,

N = tap number (I through 64).

NOTE: This device requires only a single-phase clock. The terminology of $\phi 1$ and $\phi 2$ refers to the High and Low periods of the same clock.

The other side of the capacitor is connected to a single-stage inverting amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately, $(V_{DD} - V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted,

and V_{IN} is switched to all 64 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators whose tap voltages were lower than V_{IN} will drive the comparator outputs to a "low" state. All comparators whose tap voltages were higher than V_{IN} will drive the comparator outputs to a "high" state. A second, capacitor-coupled, auto-zeroed amplifier further amplifies the outputs.

The status of all these comparator amplifiers are stored at the end of this phase ($\phi 2$), by a secondary latching amplifier stage. Once latched, the status of the 64 comparators is decoded by a 64-bit 7-bit decode array and the results are clocked into a storage register at the rising edge of the next $\phi 2$.

A three-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B6 when it is in a high state. CE2 will independently disable B1 through B6 and the overflow buffers when it is in the low state (Table 1).

To facilitate usage of this device a phase-control input is provided which can effectively complement the clock as it enters the chip. Also, an on-board Zener is provided for use as a reference voltage.

Continuous Clock Operation

One complete conversion cycle can be traced through the HI3306 via the following steps. (Refer to timing diagram, Figure 1.) With the phase control in a "High" state, the rising edge of the clock input will start a "sample" phase. During this entire "High" state of the clock, the 64 comparators will track the input voltage and the 64 latches will track the comparator outputs. At the falling edge of the clock, after the specified aperture delay, all 64 comparator outputs are captured by the 64 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this "Low" state of the clock the output of the latches propagates through the decode array and a 7-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 7-bit code is shifted into the output registers and appears with time delay to as valid data at the output of the three-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse Mode Operation

For sampling high speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of three ways. The fastest method is to keep the converter in the Sample Unknown phase, $\phi 2$, during the standby state. The device can now be pulsed through the Auto Balance phase with a single pulse. The analog value is captured on the leading edge of $\phi 1$ and is transferred into the output registers on the trailing edge of $\phi 1$. We are now back in the standby state, $\phi 2$, and another conversion can be started, but not later than 5µs due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between $\phi 2$ and $\phi 1$, the lower the power consumption. (See Timing Waveform, Figure 3.)

The second method uses the Auto Balance phase, $\phi 1$, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two $\phi 2$ pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second $\phi 2$ pulse is needed to transfer the data into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes slightly longer, but the repetition rate may be as slow as desired. The disadvantage to this method is the higher device dissipation due to the low ratio of $\phi 2$ to $\phi 1$. (See Timing Waveform, Figure 3B.)

For applications requiring both indefinite standby and lowest power, standby can be in the $\phi 2$ (Sample Unknown) state with two $\phi 1$ pulses to generate valid data (see Figure 3C). Valid data now appears two full clock cycles after starting the conversion process.

Analog Input Considerations

The HI3306 input terminal is characterized by a small capacitance (see Specifications) and a small voltage-dependent current (See Typical Performance Curves). The signal-source impedance should be kept low, however, when operating the HI3306 at high clock rates.

The HI3306 outputs a short (less than 10ns) current spike of up to several mA amplitude (See Typical Performance Curves) at the beginning of the sample phase. (To a lesser extent, a spike also appears at the beginning of auto balance.) The driving source must recover from the spike by the end of the same phase, or a loss of accuracy will result.

A locally terminated 50Ω or 75Ω source is generally sufficient to drive the HI3306. If gain is required, a high speed, fast settling operational amplifier, such as the HA-5033, HA-2542, or HA5020 is recommended.

Digital Input And Output Interfacing

The two chip-enable and the phase-control inputs are standard CMOS units. They should be driven from less than $0.3 \times V_{DD}$ to at least $0.7 \times V_{DD}$. This can be done from 74HC series CMOS (QMOS), TTL with pull-up resistors, or, if V_{DD} is greater than the logic supply, open collector or open drain drivers plus pull-ups. (See Figure 20.)

The clock input is more critical to timing variations, such as $\phi 1$ becoming too short, for instance. Pull-up resistors should generally be avoided in favor of active drivers. The clock input may be capacitively coupled, as it has an internal 50kΩ feedback resistor on the first buffer stage, and will seek its own trip point. A clock source of at least $1V_{P-P}$ is adequate, but extremely non-symmetrical waveforms should be avoided.

The output drivers have full rail-to-rail capability. If driving CMOS systems with V_{DD} below the V_{DD} of the HI3306, a CD74HC4050 or CD74HC4049 should be used to step down the voltage. If driving LSTTL systems, no step-down should be necessary, as most LSTTLs will take input swings up to 10V to 15V.

Although the output drivers are capable of handling typical data bus loading, the capacitor charging currents will produce local ground disturbances. For this reason, an external bus driver is recommended.

Increased Accuracy

In most cases the accuracy of the HI3306 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, three adjustments can be made to obtain better accuracy; i.e., offset trim, gain trim, and midpoint trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a DC shift to V_{IN} or by the offset trim of the operational amplifier. When this is not possible the V_{REF}- input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is $^1/_2$ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = {}^1/_2 \text{ LSB} = {}^1/_2(V_{REF}/64)$$
$$= V_{REF}/128.$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50Ω pot connected between V_{REF}- and ground will accomplish the adjustment. Set V_{IN} to $^1/_2$ LSB and trim the pot until the 0 to 1 transition occurs.

If V_{IN} for the first transition is greater than the theoretical, then the 50Ω pot should be connected between V_{REF} and a negative voltage of about 2 LSBs. The trim procedure is as stated previously.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the operational amplifier. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 63 to overflow transition. That voltage is $^1/_2$ LSB less than V_{REF}+ and is calculated as follows:

$$V_{IN} \text{ (63 to 64 transition)} = V_{REF} - V_{REF}/128$$
$$= V_{REF}(127/128)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overflow transition. Now adjust V_{REF}+ until that transition occurs on the outputs.

Midpoint Trim

The reference center (RC) is available to the user as the midpoint of the resistor ladder. To trim the midpoint, the offset and gain trims should be done first. The theoretical transition from count 31 to 32 occurs at $31\,^1/_2$ LSBs. That voltage is as follows:

$$V_{IN} \text{ (31 to 32 transition)} = 31.5\ (V_{REF}/64)$$
$$= V_{REF}(63/128)$$

An adjustable voltage follower can be connected to the RC pin or a 2kΩ pot can be connected between V_{REF}+ and V_{REF}- with the wiper connected to RC. Set V_{IN} to the 31 to 32 transition voltage, then adjust the voltage follower or the pot until the transition occurs on the output bits.

The Reference Center point can also be used to create unique transfer functions. The user must remember, however, that there is approximately 120Ω in series with the RC pin.

Applications

7-Bit Resolution

To obtain 7-bit resolution, two HI3306s can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enabler controls - all of which are available on the HI3306.

The first step for connecting a 7-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 17. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the seventh bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 6) are now connected in parallel to complete the circuitry.

Doubled Sampling Speed

The phase control and both positive and negative true chip enables allow the parallel connection of two HI3306s to double the sampling speed. Figure 18 shows this configuration. One converter samples on the positive phase of the clock, and the second on the negative. The outputs are also alternately enabled. Care should be taken to provide a near square-wave clock it operating at close to the maximum clock speed for the devices.

8-Bit to 12-Bit Conversion Techniques

To obtain 8-bit to 12-bit resolution and accuracy, use a feed-forward conversion technique. Two A/D converters will be needed to convert up to 11 bits; three A/D converters to convert 12 bits. The high speed of the HI3306 allows 12-bit conversions in the 500ns to 900ns range.

The circuit diagram of a high-speed 12-bit A/D converter is shown in Figure 19. In the feed-forward conversion method two sequential conversions are made. Converter A first does a coarse conversion to 6 bits. The output is applied to a 6-bit D/A converter whose accuracy level is good to 12 bits. The D/A converter output is then subtracted from the input voltage, multiplied by 32, and then converted by a second flash A/D converter, which is connected in a 7-bit configuration. The answers from the first and second conversions are added together with bit 1 of the first conversion overlapping bit 7 of the second conversion.

When using this method, take care that:

- The linearity of the first converter is better than $^1/_2$ LSB.
- An offset bias of 1 LSB (1/64) Is subtracted from the first conversion since the second converter is unipolar.

- The D/A converter and its reference are accurate to the total number of bits desired for the final conversion (the A/D converter need only be accurate to 6 bits).

The first converter can be offset-biased by adding a 20Ω resistor at the bottom of the ladder and increasing the reference voltage by 1 LSB. If a 6.4V reference is used in the system, for example, then the first HI3306 will require a 6.5V reference.

Definitions

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the converter. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests.

Signal-to-Noise (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR})/6.02,$$

where: $V_{CORR} = 0.5dB$.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

Operating and Handling Considerations

HANDLING

All inputs and outputs of Harris CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in AN6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

OPERATING

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 20mA even when the power supply is off. The Zener (pin 4) is the only terminal allowed to exceed V_{DD}.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

Application Circuits

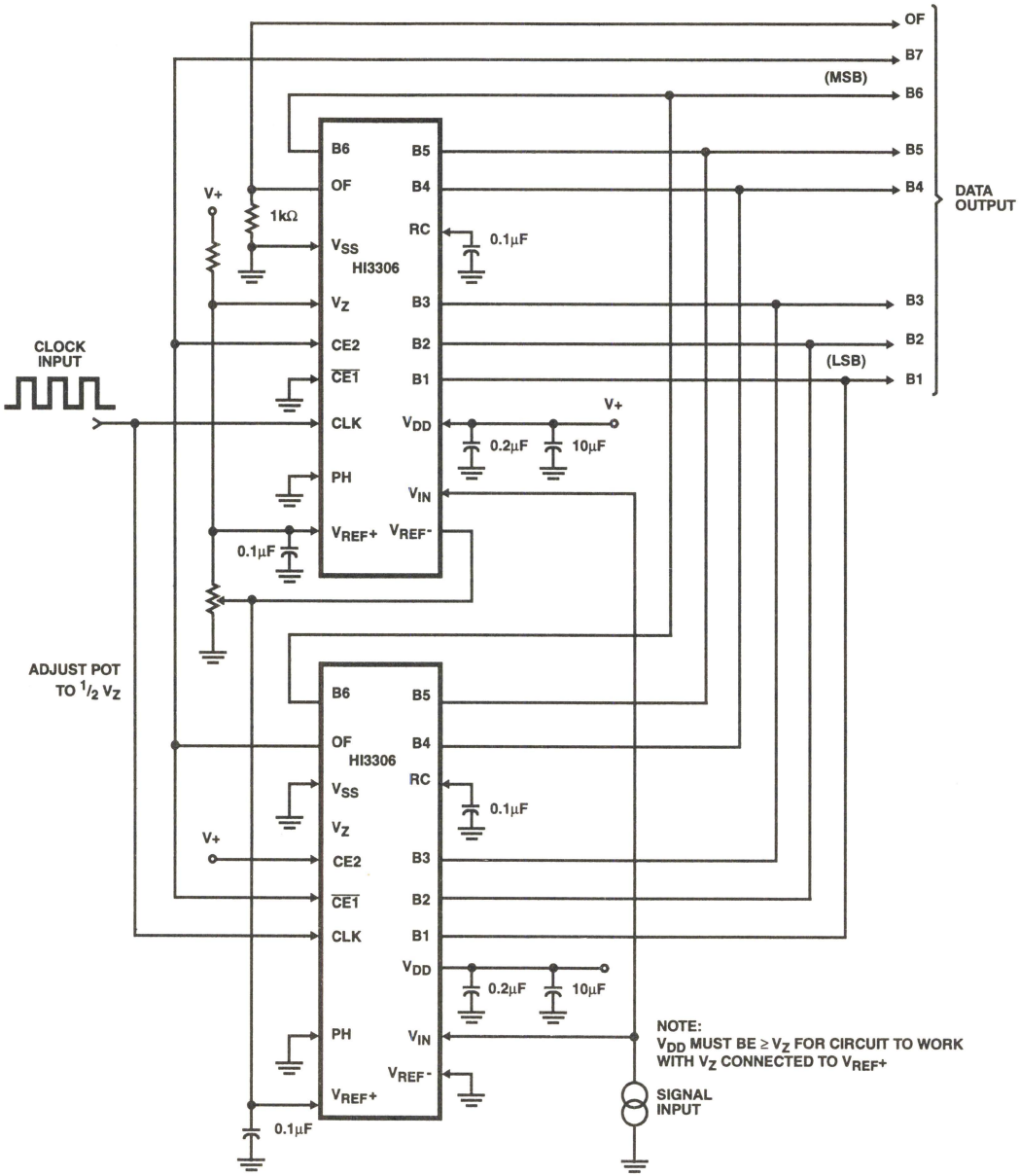


FIGURE 17. TYPICAL HI3306 7-BIT RESOLUTION CONFIGURATION

Application Circuits (Continued)

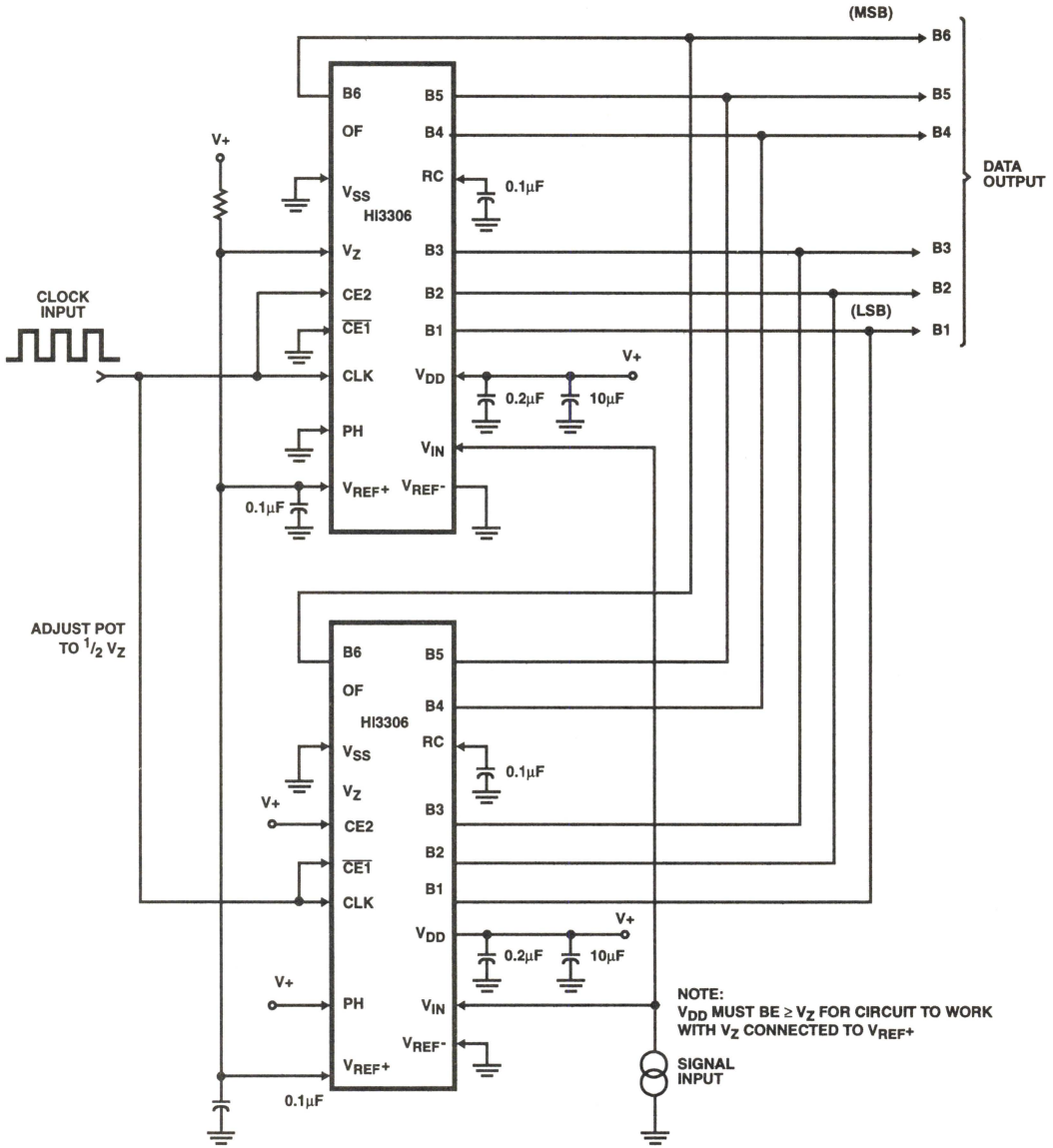


FIGURE 18. TYPICAL HI3306 6-BIT RESOLUTION CONFIGURATION WITH DOUBLE SAMPLING RATE CAPABILITY

Application Circuits (Continued)

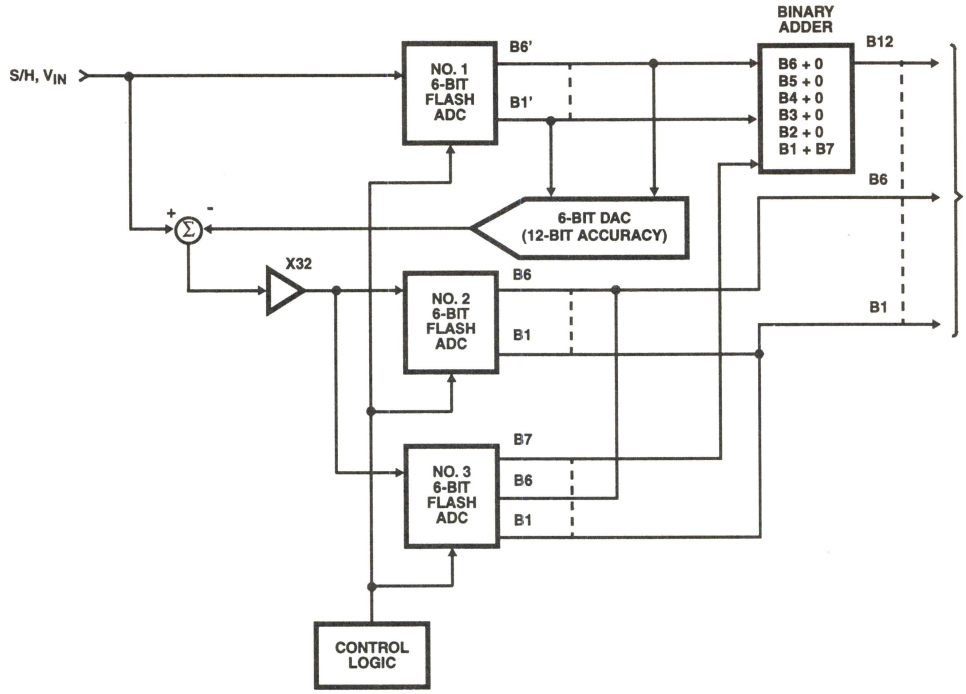


FIGURE 19. TYPICAL HI3306, 800ns, 12-BIT ADC SYSTEM

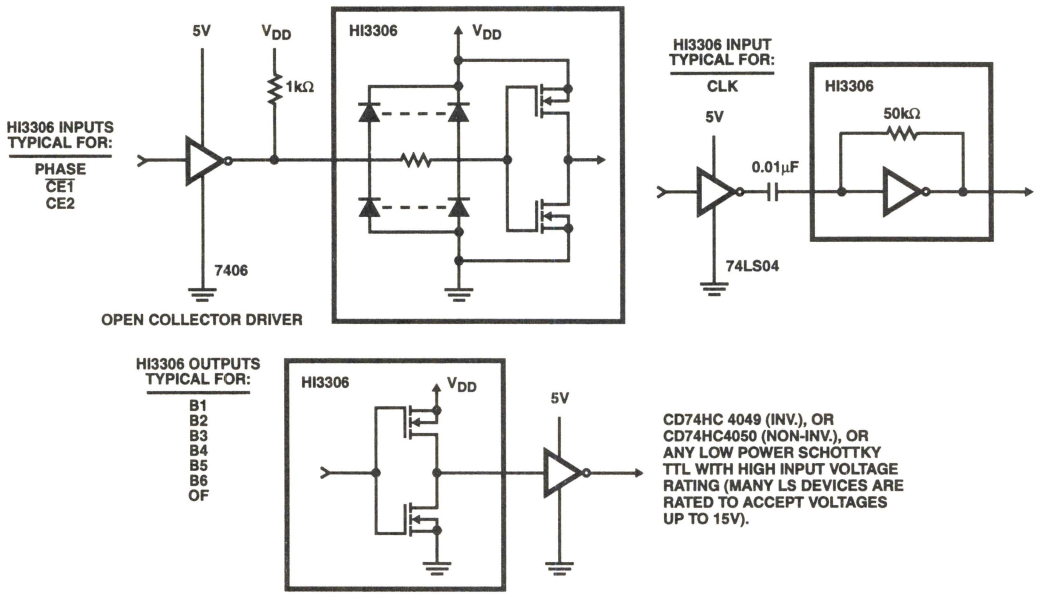


FIGURE 20. 5V LOGIC INTERFACE CIRCUIT FOR V_{DD} > 5.5V

August 1997

8-Bit, 15 MSPS, Flash A/D Converter

Features

- CMOS Low Power (Typ) 150mW
- Parallel Conversion Technique
- Sampling Rate at 5V Supply 15MHz
- 8-Bit Latched Three-State Output with Overflow Bit
- Accuracy (Typ) . . . . . ±1 LSB
- Single Supply Voltage . . . . . 4V to 7.5V
- Linearity (INL):
  - HI3318JIP . . . . . ±1.5 LSB
  - HI3318JIB . . . . . ±1.5 LSB
- Sampling Rate:
  - HI3318JIP 15MHz (67ns)
  - HI3318JIB 15MHz (67ns)
- Video Digitizing
- High-Speed A/D Conversion
- Medical Imaging
- Radar Signal Processing
- Digital Communications Systems

Description

The HI3318 is a CMOS parallel (FLASH) analog-to-digital converter designed for applications demanding both low power consumption and high speed digitization.

The HI3318 operates over a wide full scale input voltage range of 4V up to 7.5V with maximum power consumption depending upon the clock frequency selected. When operated from a 5V supply at a clock frequency of 15MHz, the typical power consumption of the HI3318 is 150mW.

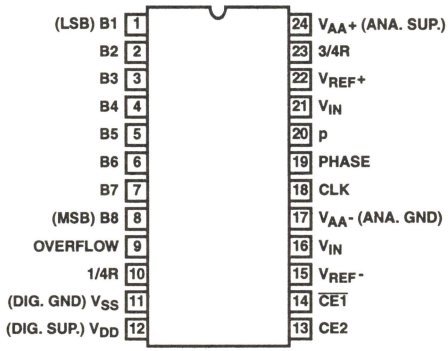
256 paralleled auto balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel bit outputs in the HI3318. 255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3318JIP	-40 to 85	24 Ld PDIP	E24.6
HI3318JIB	-40 to 85	24 Ld SOIC	M24.3

Pinout

HI3318
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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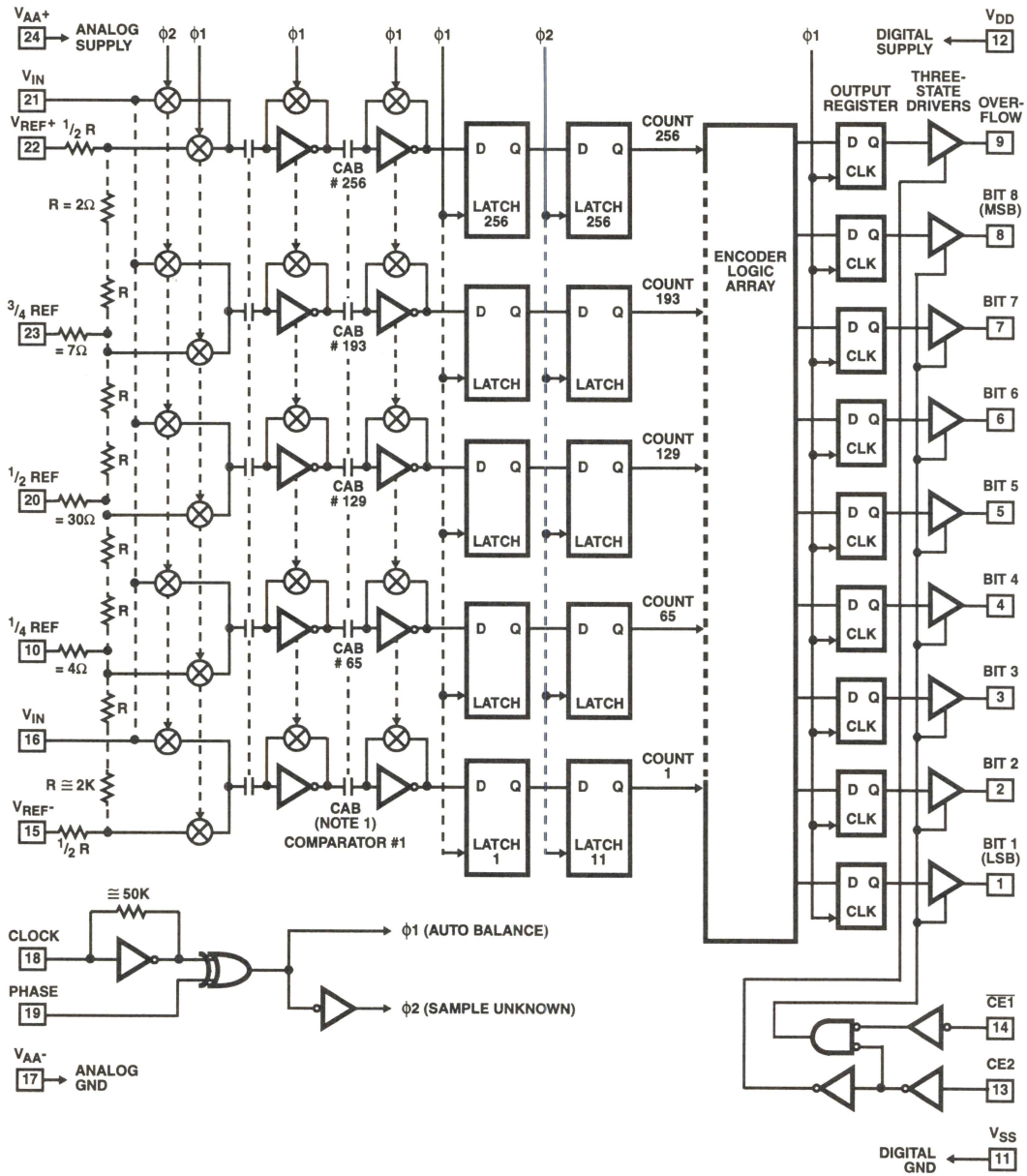
Functional Block Diagram



NOTE:

1. Cascaded Auto Balance (CAB).

Absolute Maximum Ratings $T_A = 25^oC$

DC Supply Voltage Range (V_{DD} or $V_{AA}+$) . . . . . -0.5V to +8V
(Referenced to V_{SS} or $V_{AA}-$ Terminal, Whichever is More Negative)
Input Voltage Range
CE2 and $\overline{CE1}$ . . . . . $V_{AA}-$ -0.5V to V_{DD} + 0.5V
Clock, Phase, $V_{REF}-$, $^1/_2$ Ref. . . . . $V_{AA}-$ -0.5V to $V_{AA}+$ + 0.5V
Clock, Phase, $V_{REF}-$, $^1/_4$ Ref. . . . . $V_{SS}-$ -0.5V to V_{DD} + 0.5V
V_{IN}, $^3/_4$ REF, $V_{REF}+$ . . . . . $V_{AA}-$ -0.5V to $V_{AA}-$ + 7.5V
Output Voltage Range, ... V_{SS} - 0.5V to V_{DD} + 0.5V
Bits 1-8, Overflow (Outputs Off)
DC Input Current . . . . . ±20mA
Clock, Phase, $\overline{CE1}$, CE2, V_{IN}, Bits 1-8, Overflow
Recommended $V_{AA}+$ Operating Range . . . . . V_{DD} ±1V
Recommended $V_{AA}-$ Operating Range . . . . . V_{SS} ±1V

Operating Conditions

Operating Voltage Range (V_{DD} or $V_{AA}+$) . . . 4V (Min) to 7.5V (Max)
Temperature Range (T_A) . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}(^oC/W)$
PDIP Package	60
SOIC Package	75

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

At 25^oC, $V_{AA}+ = V_{DD} = 5V$, $V_{REF}+ = 6.4V$, $V_{REF}- = V_{AA}- = V_{SS}$, CLK = 15MHz, All Reference Points Adjusted, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		8	-	-	Bits
Integral Linearity Error		-	-	± 1.5	LSB
Differential Linearity Error		-	-	+1, -0.8	LSB
Offset Error, Unadjusted	$V_{IN} = V_{REF}- + ^1/_2$ LSB	-0.5	4.5	6.4	LSB
Gain Error, Unadjusted	$V_{IN} = V_{REF}+ - ^1/_2$ LSB	-1.5	0	1.5	LSB
DYNAMIC CHARACTERISTICS					
Maximum Input Bandwidth	(Note 1) HI3318	2.5	5.0	-	MHz
Maximum Conversion Speed	CLK = Square Wave	15	17	-	MSPS
Signal to Noise Ratio, SNR	f_S = 15MHz, f_{IN} = 100kHz	-	47	-	dB
$= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_S = 15MHz, f_{IN} = 4MHz	-	43	-	dB
Signal to Noise Ratio, SINAD	f_S = 15MHz, f_{IN} = 100kHz	-	45	-	dB
$= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_S = 15MHz, f_{IN} = 4MHz	-	35	-	dB
Total Harmonic Distortion, THD	f_S = 15MHz, f_{IN} = 100kHz	-	-46	-	dBc
	f_S = 15MHz, f_{IN} = 4MHz	-	-36	-	dBc
Effective Number of Bits, ENOB	f_S = 15MHz, f_{IN} = 100kHz	-	7.2	-	Bits
	f_S = 15MHz, f_{IN} = 4MHz	-	5.5	-	Bits
Differential Gain Error	Unadjusted	-	2	-	%
Differential Phase Error	Unadjusted	-	1	-	%
ANALOG INPUTS					
Full Scale Range, V_{IN} and ($V_{REF}+$) - ($V_{REF}-$)	Notes 2, 4	4	-	7	V
Input Capacitance, V_{IN}		-	30	-	pF
Input Current, V_{IN}, (See Text)	V_{IN} = 5.0V, $V_{REF}+$ = 5.0V	-	-	3.5	mA
REFERENCE INPUTS					
Ladder Impedance		270	500	800	Ω

Electrical Specifications At 25°C, $V_{AA}+ = V_{DD} = 5V$, $V_{REF}+ = 6.4V$, $V_{REF}- = V_{AA}- = V_{SS}$, CLK = 15MHz, All Reference Points Adjusted, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS					
Low Level Input Voltage, V_{OL}					
$\overline{CE1}$, CE2	Note 4	-	-	$0.2V_{DD}$	V
Phase, CLK	Note 4	-	-	$0.2V_{AA}$	V
High Level Input Voltage, V_{IN}					
$\overline{CE1}$, CE2	Note 4	$0.7V_{DD}$	-	-	V
Phase, CLK	Note 4	$0.7V_{AA}$	-	-	V
Input Leakage Current, I_I (Except CLK Input)	Note 3	-	±0.2	±5	µA
Input Capacitance, C_I		-	3	-	pF
DIGITAL OUTPUTS					
Output Low (Sink) Current	$V_O = 0.4V$	4	10	-	mA
Output High (Source) Current	$V_O = 4.5V$	-4	-6	-	mA
Three-State Output Off-State Leakage Current, I_{OZ}		-	±0.2	±5	µA
Output Capacitance, C_O		-	4	-	pF
TIMING CHARACTERISTICS					
Auto Balance Time, $\phi1$		33	-	∞	ns
Sample Time, $\phi2$	Note 4	25	-	500	ns
Aperture Delay		-	15	-	ns
Aperture Jitter		-	100	-	ps
Data Valid Time, t_D	Note 4	-	50	65	ns
Data Hold Time, t_H	Note 4	25	40	-	ns
Output Enable Time, t_{EN}		-	18	-	ns
Output Disable Time, t_{DIS}		-	18	-	ns
POWER SUPPLY CHARACTERISTICS					
Device Current ($I_{DD} + I_A$) (Excludes I_{REF})	Continuous Conversion (Note 4)	-	30	60	mA
	Auto Balance ($\phi1$)	-	30	60	mA

NOTES:

1. A full scale sine wave input of greater than $f_{CLK}/2$ or the specified input bandwidth (whichever is less) may cause an erroneous code. The -3dB bandwidth for frequency response purposes is greater than 30MHz.
2. V_{IN} (Full Scale) or $V_{REF}+$ should not exceed $V_{AA}+ + 1.5V$ for accuracy.
3. The clock input is a CMOS inverter with a 50kΩ feedback resistor and may be AC coupled with $1V_{P-P}$ minimum source.
4. Parameter not tested, but guaranteed by design or characterization.

Timing Waveforms

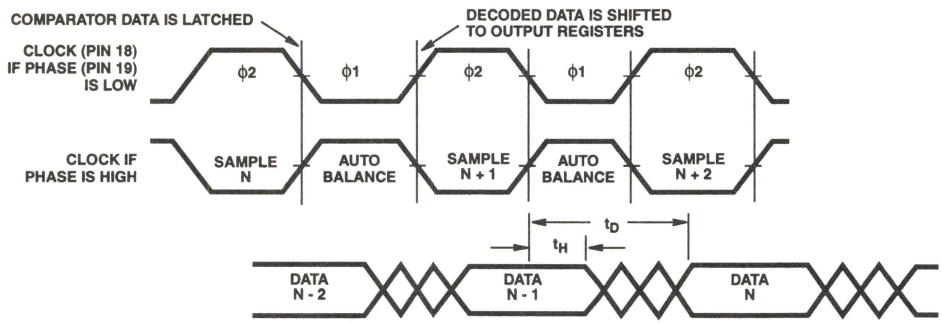


FIGURE 1. INPUT TO OUTPUT TIMING DIAGRAM

Timing Waveforms (Continued)

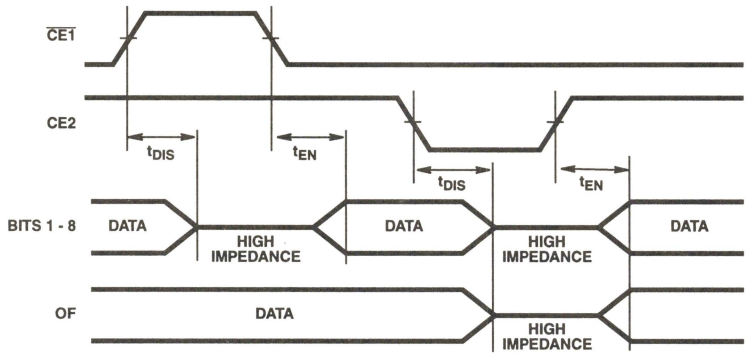


FIGURE 2. OUTPUT ENABLE TIMING DIAGRAM

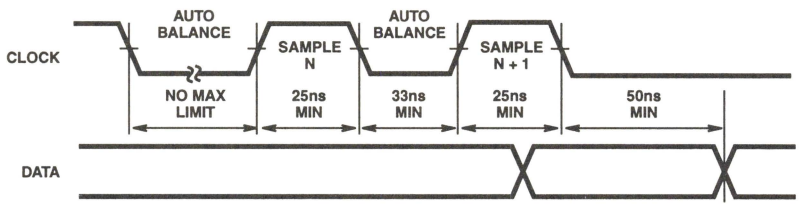


FIGURE 3A. STANDBY IN INDEFINITE AUTO BALANCE (SHOWN WITH PHASE = LOW)

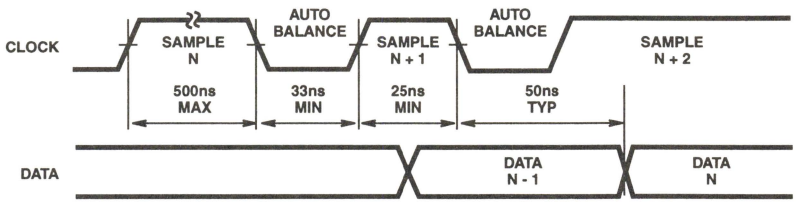


FIGURE 3B. STANDBY IN SAMPLE (SHOWN WITH PHASE = LOW)

FIGURE 3. PULSE MODE OPERATION

Typical Performance Curves

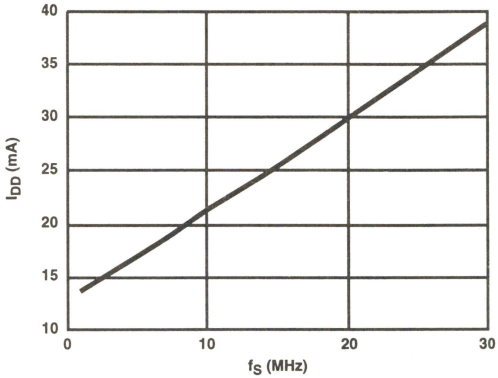


FIGURE 4. DEVICE CURRENT vs SAMPLE FREQUENCY

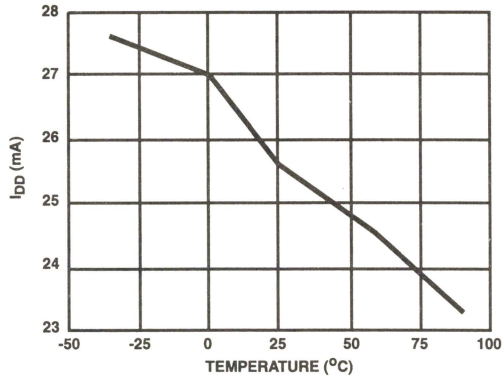


FIGURE 5. DEVICE CURRENT vs TEMPERATURE

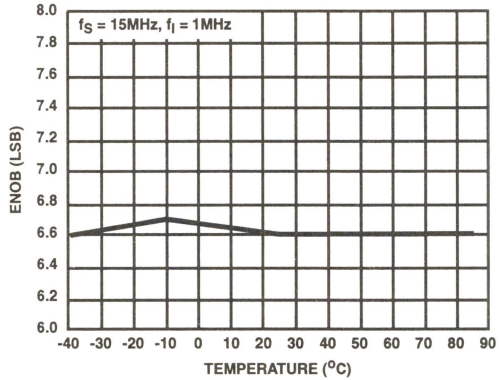


FIGURE 6. ENOB vs TEMPERATURE

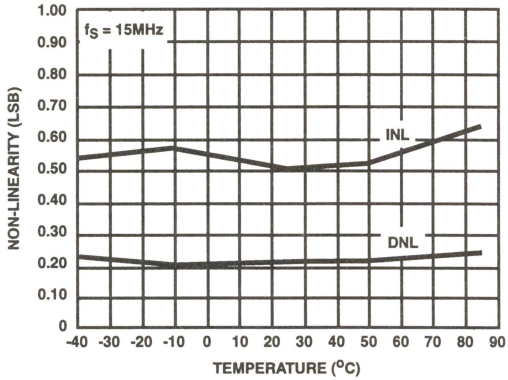


FIGURE 7. NON-LINEARITY vs TEMPERATURE

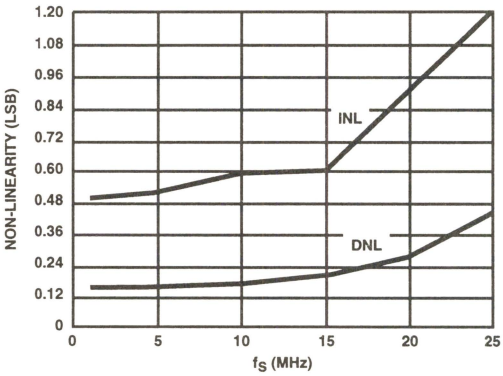


FIGURE 8. NON-LINEARITY vs SAMPLE FREQUENCY

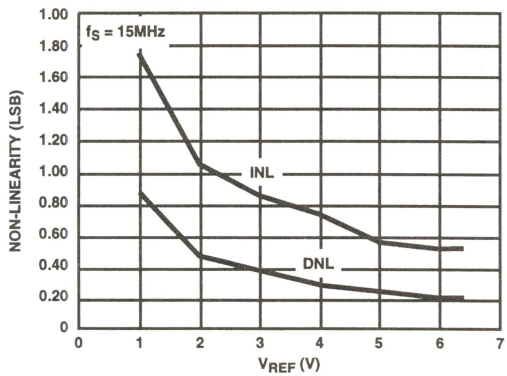


FIGURE 9. NON-LINEARITY vs REFERENCE VOLTAGE

Typical Performance Curves (Continued)

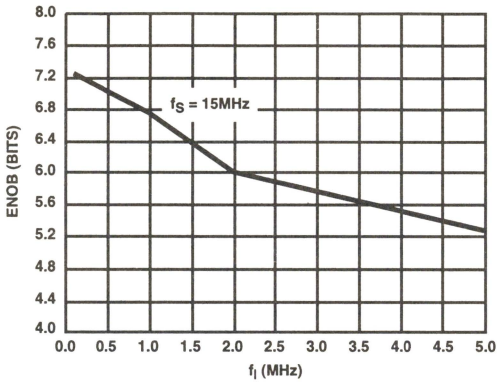


FIGURE 10. ENOB vs INPUT FREQUENCY

Pin Descriptions

PIN	NAME	DESCRIPTION	
1	B1	Bit 1 (LSB)	Output Data Bits (High = True)
2	B2	Bit 2	
3	B3	Bit 3	
4	B4	Bit 4	
5	B5	Bit 5	
6	B6	Bit 6	
7	B7	Bit 7	
8	B8	Bit 8 (MSB)	
9	OF	Overflow	
10	$^1/_4$ R	Reference Ladder $^1/_4$ Point	
11	V_{SS}	Digital Ground	
12	V_{DD}	Digital Power Supply, +5V	
13	CE2	Three-State Output Enable Input, Active Low, See Truth Table.	
14	$\overline{CE1}$	Three-State Output Enable Input Active High. See Truth Table.	
15	V_{REF}-	Reference Voltage Negative Input	
16	V_{IN}	Analog Signal Input	
17	V_{AA}-	Analog Ground	
18	CLK	Clock Input	
19	PHASE	Sample clock phase control input. When PHASE is low, "Sample Unknown" occurs when the clock is low and "Auto Balance" occurs when the clock is high (see text).	
20	$^1/_2$ R	Reference Ladder Midpoint	
21	V_{IN}	Analog Signal Input	
22	V_{REF}+	Reference Voltage Positive Input	
23	$^3/_4$ R	Reference Ladder $^3/_4$ Point	
24	V_{AA}+	Analog Power Supply, +5V	

CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	B1 - B8	OF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't Care

Theory of Operation

A sequential parallel technique is used by the HI3318 converter to obtain its high speed operation. The sequence consists of the "Auto-Balance" phase, ϕ1, and the "Sample Unknown" phase, ϕ2. (Refer to the circuit diagram.) Each conversion takes one clock cycle (see Note). With the phase control (pin 19) high, the "Auto-Balance" (ϕ1) occurs during the high period of the clock cycle, and the "Sample Unknown" (ϕ2) occurs during the low period of the clock cycle.

NOTE: The device requires only a single phase clock The terminology of ϕ1 and ϕ2 refers to the high and low periods of the same clock.

During the "Auto-Balance" phase, a transmission switch is used to connect each of the first set of 256 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{TAP}(N) = [(N/256)\,V_{REF}] - (1/512)\,V_{REF}]$$
$$= [(2N - 1)/512]\,V_{REF},$$

Where:

V_{TAP} (n) = reference ladder tap voltage at point n,
V_{REF} = voltage across V_{REF}- to V_{REF}+,
N = tap number (1 through 256).

The other side of these capacitors are connected to single-stage amplifiers whose outputs are shorted to their inputs by switches. This balances the amplifiers at their intrinsic trip points, which is approximately (V_{AA}+ - V_{AA}-)/2. The first set of capacitors now charges to their associated tap voltages.

At the same time a second set of commutating capacitors and amplifiers is also auto-balanced. The balancing of the second-

stage amplifier at its intrinsic trip point removes any tracking differences between the first and second amplifier stages. The cascaded auto-balance (CAB) technique, used here, increases comparator sensitivity and temperature tracking.

In the "Sample Unknown" phase, all ladder tap switches and comparator shorting switches are opened. At the same time V_{IN} is switched to the first set of commutating capacitors. Since the other end of the capacitors are now looking into an effectively open circuit, any input voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators that had tap voltages greater than V_{IN} will go to a "high" state at their outputs. All comparators that had tap voltages lower than V_{IN} will go to a "low" state.

The status of all these comparator amplifiers is AC coupled through the second-stage comparator and stored at the end of this phase ($\phi 2$) by a latching amplifier stage. The latch feeds a second latching stage, triggered at the end of $\phi 1$. This delay allows comparators extra settling time. The status of the comparators is decoded by a 256 to 9-bit decoder array, and the results are clocked into a storage register at the end of the next $\phi 2$.

A 3-stage buffer is used at the output of the 9 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B6 when it is in a high state. CE2 will independently disable B1 through B8 and the OF buffers when it is in the low state.

To facilitate usage of this device, a phase control input is provided which can effectively complement the clock as it enters the chip.

Continuous-Clock Operation

One complete conversion cycle can be traced through the HI3318 via the following steps. (Refer to timing diagram.) With the phase control in a "low" state, the rising edge of the clock input will start a "sample" phase. During this entire "high" state of the clock, the comparators will track the input voltage and the first-stage latches will track the comparator outputs. At the falling edge of the clock, all 256 comparator outputs are captured by the 256 latches. This ends the "sample" phase and starts the "auto-balance" phase for the comparators. During this "low" state of the clock, the output of the latches settles and is captured by a second row of latches when the clock returns high. The second-stage latch output propagates through the decode array, and a 9-bit code appears at the D inputs of the output registers. On the next falling edge of the clock, this 9-bit code is shifted into the output registers and appears with time delay t_D as valid data at the output of the three-state drivers. This also marks the end of the next "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse-Mode Operation

The HI3318 needs two of the same polarity clock edges to complete a conversion cycle: If, for instance, a negative going clock edge ends sample "N", then data "N" will appear after the next negative going edge. Because of this requirement, and because there is a maximum sample time of 500ns (due to capacitor droop), most pulse or intermittent sample applications will require double clock pulsing.

If an indefinite standby state is desired, standby should be in auto-balance, and the operation would be as in Figure 3A.

If the standby state is known to last less than 500ns and lowest average power is desired, then operation could be as in Figure 3B.

Increased Accuracy

In most cases the accuracy of the HI3318 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, five adjustments can be made to obtain better accuracy, i.e., offset trim; gain trim; and $^1/_4$, $^1/_2$ and $^3/_4$ point trim.

Offset Trim

In general, offset correction can be done in the preamp circuitry by introducing a dc shift to V_{IN} or by the offset trim of the op amp. When this is not possible the V_{REF}- input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is $^1/_2$ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = {}^1/_2 \text{ LSB} = {}^1/_2 (V_{REF}/256)$$
$$= V_{REF}/512.$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50Ω pot connected between V_{REF}- and ground will accomplish the adjustment. Set V_{IN} to $^1/_2$ LSB and trim the pot until the 0-to-1 transition occurs.

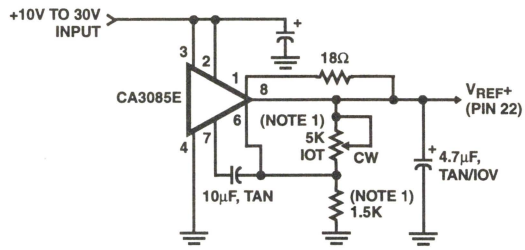
If V_{IN} for the first transition is greater than the theoretical, then the 50Ω pot should be connected between V_{REF}- and a negative voltage of about 2 LSBs. The trim procedure is as stated previously.

Gain Trim

In general, the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 255 to overflow transition. That voltage is $^1/_3$ LSB less than V_{REF}+ and is calculated as follows:

$$V_{IN} \text{ (255 to 256 transition)} = V_{REF} - V_{REF}/512$$
$$= V_{REF}(511/512).$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 255 to overflow transition. Now adjust V_{REF}+ until that transition occurs on the outputs.

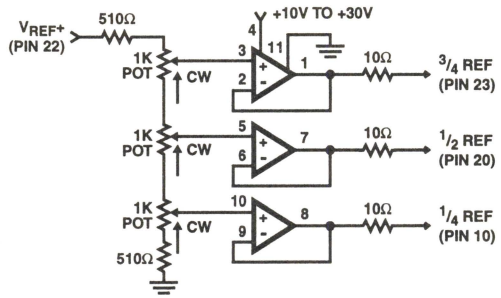


NOTE: Bypass V_{REF}+ to analog GND near A/D with 0.1µF ceramic cap. Parts noted should have low temperature drift.

FIGURE 11. TYPICAL VOLTAGE REFERENCE SOURCE FOR DRIVING V_{REF}+ INPUT

1/4 Point Trims

The 1/4, 1/2 and 3/4 points on the reference ladder are brought out for linearity adjusting or if the user wishes to create a nonlinear transfer function. The 1/4 points can be driven by the reference drivers shown (Figure 12) or by 2-K pots connected between $V_{REF}+$ and $V_{REF}-$. The 1/2 (mid-) point should be set first by applying an input of 257/512 x (V_{REF}) and adjusting for an output changing from 128 to 129. Similarly the 1/4 and 3/4 points can be set with inputs of 129/512 and 385/512 x (V_{REF}) and adjusting for counts of 192 to 193 and 64 to 65. (Note that the points are actually 1/4, 1/2 and 3/4 of full scale +1 LSB.)



NOTES:

1. All Op Amps = 3/4 CA324E.
2. Bypass all reference points to analog ground near A/D with 0.1µF ceramic caps.
3. Adjust V_{REF+} first, then 1/3, 3/4 and 1/4 points.

FIGURE 12. TYPICAL 1/4 POINT DRIVERS FOR ADJUSTING LINEARITY (USE FOR MAXIMUM LINEARITY)

9-Bit Resolution

To obtain 9-bit resolution, two HI3318s can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enable controls, all of which are available on the HI3318.

The first step for connecting a 9-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 13. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the ninth bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the CE1 control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 8) are now connected in parallel to complete the circuitry. The complete circuit for a 9-bit A/D converter is shown in Figure 14.

Grounding/Bypassing

The analog and digital supply grounds of a system should be kept separate and only connected at the A/D. This keeps digital ground noise out of the analog data to be converted. Reference drivers, input amps, reference taps, and the V_{AA} supply should be bypassed at the A/D to the analog side of the ground. See Figure 15 for a block diagram of this concept. All capacitors shown should be low impedance 0.1µF ceramics and should be mounted as close to the A/D as possible. If $V_{AA}+$ is derived from V_{DD}, a small (10Ω resistor or inductor and additional filtering (4.7µF tantalum) may be used to keep digital noise out of the analog system.

Input Loading

The HI3318 outputs a current pulse to the V_{IN} terminal at the start of every sample period. This is due to capacitor charging and switch feedthrough and varies with input voltage and sampling rate. The signal source must be capable of recovering from the pulse before the end of the sample period to guarantee a valid signal for the A/D to convert. Suitable high speed amplifiers include the HA-5033, HA-2542; and CA3450. Figure 16 is an example of an amplifier which recovers fast enough for sampling at 15MHz.

Output Loading

The CMOS digital output stage, although capable of driving large loads, will reflect these loads into the local ground. It is recommended that a local QMOS buffer such as CD74HC541 E be used to isolate capacitive loads.

Definitions

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the converter. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests.

Signal-to-Noise (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR})/6.02,$$

where: $V_{CORR} = 0.5dB$.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

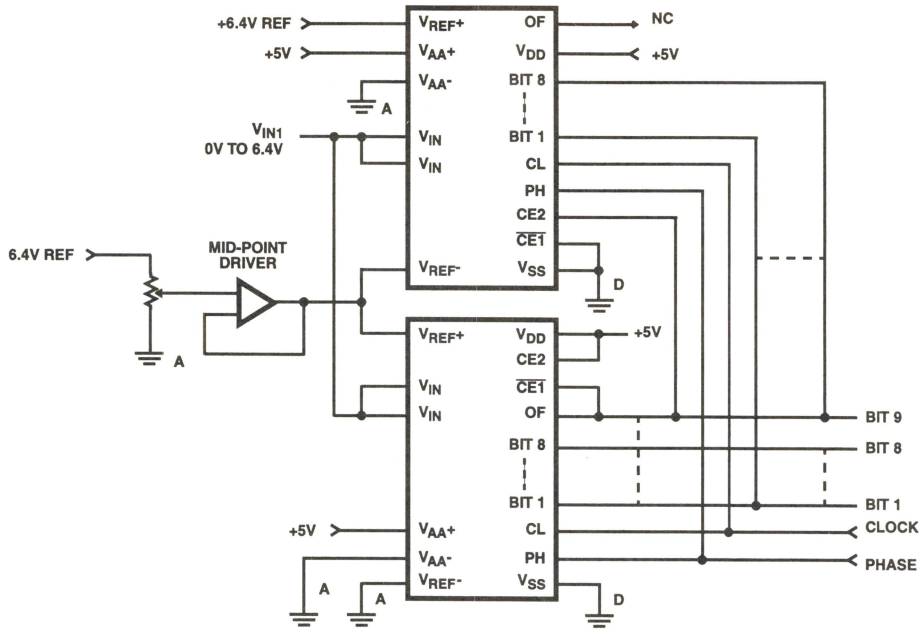


FIGURE 13. USING TWO HI3318s FOR 9-BIT RESOLUTION

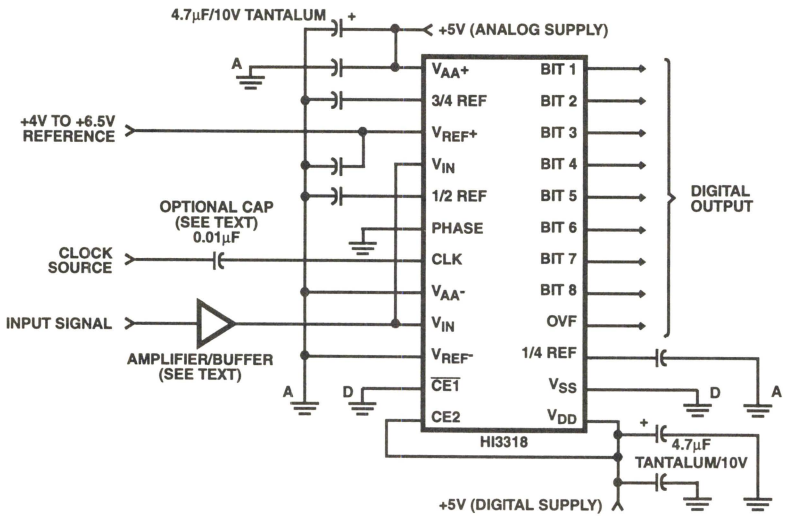


FIGURE 14. TYPICAL CIRCUIT CONFIGURATION FOR THE HI3318 WITH NO LINEARITY ADJUST

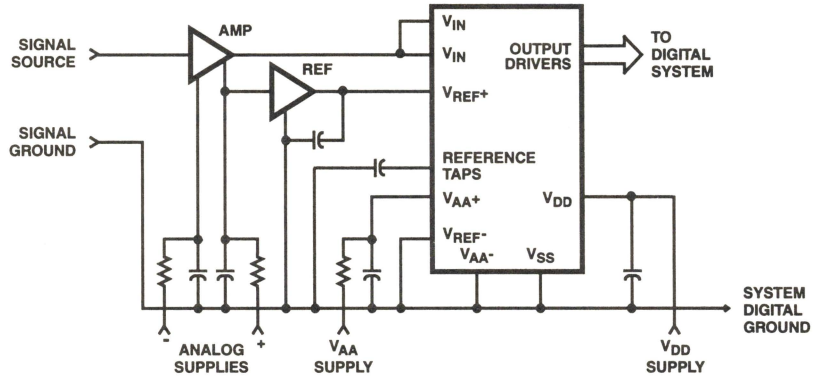
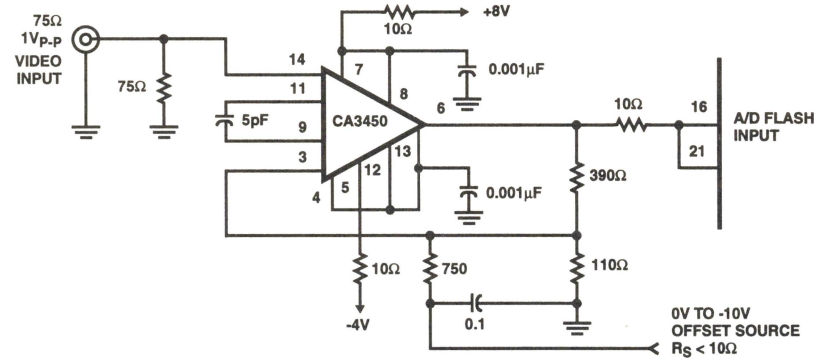


FIGURE 15. TYPICAL SYSTEM GROUNDING/BYPASSING



NOTE: Ground-planing and tight layout are extremely important.

FIGURE 16. TYPICAL HIGH BANDWIDTH AMPLIFIER FOR DRIVING THE HI3318

TABLE 1. OUTPUT CODE TABLE

CODE DESCRIPTION	(NOTE 1) INPUT VOLTAGE		BINARY OUTPUT CODE									DECIMAL COUNT
	V_{REF} 6.40V (V)	V_{REF} 5.12V (V)	OF	MSB B8	B7	B6	B5	B4	B3	B2	LSB B1	
Zero	0.00	0.00	0	0	0	0	0	0	0	0	0	0
1 LSB	0.025	0.02	0	0	0	0	0	0	0	0	1	1
2 LSB	0.05	0.04	0	0	0	0	0	0	0	1	0	2
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
$^1/_4$ Full Scale	1.60	1.28	0	0	1	0	0	0	0	0	0	64
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
$^1/_2$ Full Scale - 1 LSB	3.175	2.54	0	0	1	1	1	1	1	1	1	127
$^1/_2$ Full Scale	3.20	2.56	0	1	0	0	0	0	0	0	0	128
$^1/_2$ Full Scale + 1 LSB	3.225	2.58	0	1	0	0	0	0	0	0	1	129
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
$^3/_4$ Full Scale	4.80	3.84	0	1	1	0	0	0	0	0	0	192
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
Full Scale - 1 LSB	6.35	5.08	0	1	1	1	1	1	1	1	0	254
Full Scale	6.375	5.10	0	1	1	1	1	1	1	1	1	255
Over Flow	6.40	5.12	1	1	1	1	1	1	1	1	1	511

NOTE: 1. The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Reducing Power

Most power is consumed while in the auto-balance state. When operating at lower than 15MHz clock speed, power can be reduced by stretching the sample ($\phi 2$) time. The constraints are a minimum balance time ($\phi 1$) of 33ns, and a maximum sample time of 500ns. Longer sample times cause droop in the auto-balance capacitors. Power can also be reduced in the reference string by switching the reference on only during auto-balance.

Clock Input

The Clock and Phase inputs feed buffers referenced to $V_{AA}+$ and $V_{AA}-$. Phase should be tied to one of these two potentials, while the clock (if DC coupled) should be driven at least from 0.2 to 0.7 x ($V_{AA}+$ - $V_{AA}-$). The clock may also be AC coupled with at least a $1V_{P-P}$ swing. This allows TTL drive levels or 5V QMOS levels when $V_{AA}+$ is greater than 5V.

HARRIS SEMICONDUCTOR

HI5662

ADVANCE INFORMATION

August 1997

Dual 8-Bit, 60 MSPS, A/D Converter with Internal Voltage Reference

Features

- Sampling Rate ..... 60 MSPS
- TBD Bits at f_{IN} = 10MHz
- Low Power at 60 MSPS 600mW
- Wide Full Power Input Bandwidth 250MHz
- On Chip Sample and Holds
- Internal Band-gap Voltage Reference 2.5V
- Fully Differential or Single-Ended Analog Inputs
- Single Supply Voltage .....+5V
- TTL/CMOS Compatible Digital Inputs
- CMOS Compatible Digital Outputs..... 3.0/5.0V
- Offset Binary Digital Data Output Format

Applications

- Wireless Local Loop
- I/Q Demodulation
- Medical Imaging
- High Speed Data Acquisition

Description

The HI5662 is a monolithic, Dual 8-bit, analog-to-digital converter fabricated in a CMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 60 MSPS speed is made possible by a fully differential pipelined architecture with both an internal sample and hold and internal band-gap voltage reference.

The HI5662 has excellent dynamic performance while consuming only 600mW power at 60 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles.

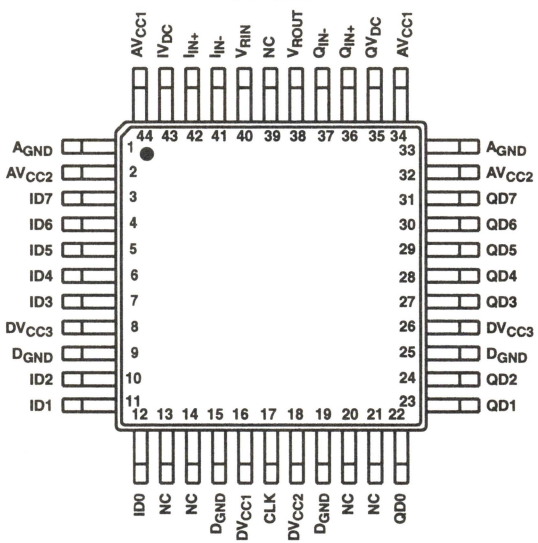
Refer to the HI5762 data sheet for 10-bit resolution.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5662IN	-40 to 85	44 Ld MQFP	Q44.10x10
HI5662EVAL1	25	Evaluation Board	

Pinout

HI5662 (MQFP)
TOP VIEW



4 A/D CONVERTERS HIGH SPEED

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 4317

HARRIS SEMICONDUCTOR

HI-5701

August 1997

6-Bit, 30 MSPS, Flash A/D Converter

Features

- 30 MSPS with No Missing Codes
- Full Power Input Bandwidth 20MHz
- No Missing Codes Over Temperature
- Sample and Hold Not Required
- Single Supply Voltage . . . . . +5V
- Power Dissipation (Max) 300mW
- CMOS/TTL Compatible
- Overflow Bit
- /883 Version Available

Applications

- Video Digitizing
- Radar Systems
- Communication Systems
- High Speed Data Acquisition Systems

Description

The HI-5701 is a monolithic, 6-bit, CMOS flash Analog-to-Digital Converter. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 30 MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5701 delivers ±0.7 LSB differential nonlinearity while consuming only 250mW (Typ) at 30 MSPS. Microprocessor compatible data output latches are provided which present valid data to the output bus 1.5 clock cycles after the convert command is received. An overflow bit is provided to allow the series connection of two converters to achieve 7-bit resolution.

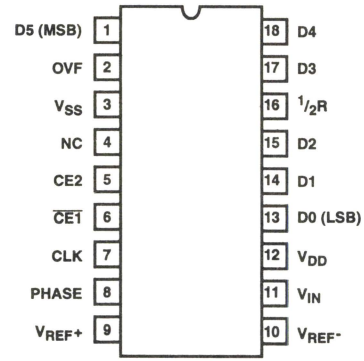
The HI-5701 is available in Commercial and Industrial temperature ranges and is supplied in 18 lead Plastic DIP and SOIC packages.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3-5701K-5	0 to 70	18 Ld PDIP	E18.3
HI9P5701K-5	0 to 70	18 Ld SOIC	M18.3
HI3-5701B-9	-40 to 85	18 Ld PDIP	E18.3
HI9P5701B-9	-40 to 85	18 Ld SOIC	M18.3
HI5701-EV	25	Evaluation Board	

Pinout

HI-5701
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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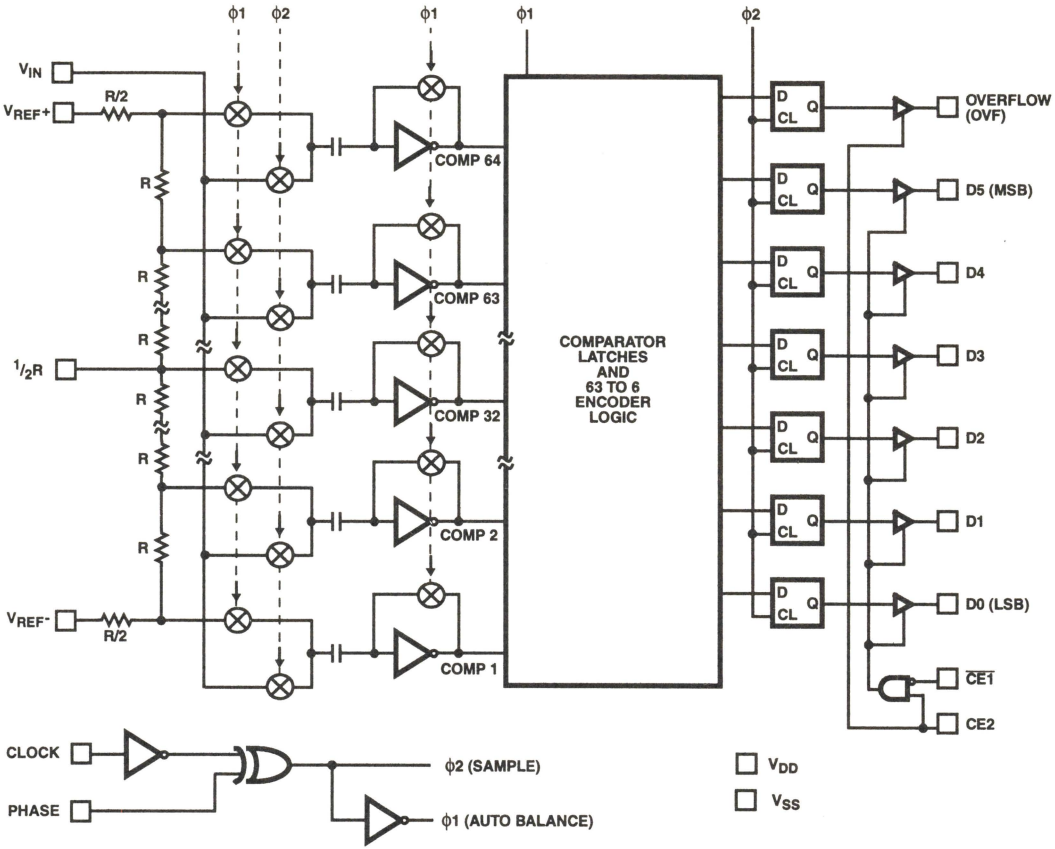
File Number 2937.6

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{DD} to V_{SS} . . . . . $(V_{SS} - 0.5) < V_{DD} < +7V$
Analog and Reference Input Pins . . . . . $(V_{SS} - 0.5) < V_{INA} < (V_{DD} +0.5V)$
Digital I/O Pins . . . . . $(V_{SS} - 0.5) < V_{I/O} < (V_{DD} +0.5V)$

Operating Conditions

Operating Temperature Range
HI3-5701-5 . . . . . 0^oC to 70^oC
HI9P5701-9 . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	75
SOIC Package	105

Maximum Power Dissipation at 70^oC 635mW
Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{DD} = +5.0V; $V_{REF}+$ = +4.0V; $V_{REF}-$ = V_{SS} = GND; f_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	25°C			(NOTE 2) 0°C TO 70°C -40°C TO 85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
SYSTEM PERFORMANCE							
Resolution		6	-	-	6	-	Bits
Integral Linearity Error, INL (Best Fit Line)	f_S = 20MHz	-	±0.5	±1.25	-	±2.0	LSB
	f_S = 30MHz	-	±1.5	-	-	-	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_S = 20MHz	-	±0.3	±0.6	-	±0.75	LSB
	f_S = 30MHz	-	±0.7	-	-		LSB
Offset Error, V_{OS} (Adjustable to Zero)	f_S = 20MHz (Note 2)	-	±0.5	±2.0	-	±2.5	LSB
	f_S = 30MHz	-	±0.5	-	-	-	LSB
Full Scale Error, FSE (Adjustable to Zero)	f_S = 20MHz (Note 2)	-	±0.25	±2.0	-	±2.5	LSB
	f_S = 30MHz	-	±0.25	-	-	-	LSB
DYNAMIC CHARACTERISTICS							
Maximum Conversion Rate	No Missing Codes	30	40	-	30	-	MSPS
Minimum Conversion Rate	No Missing Codes (Note 2)	-	-	0.125	-	0.125	MSPS
Full Power Input Bandwidth	f_S = 30MHz	-	20	-	-	-	MHz
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_S = 1MHz, f_{IN} = 100kHz	-	36	-	-	-	dB
	f_S = 30MHz, f_{IN} = 4MHz	-	31	-	-	-	dB
Signal to Noise Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_S = 1MHz, f_{IN} = 100kHz	-	35	-	-	-	dB
	f_S = 30MHz, f_{IN} = 4MHz	-	30	-	-	-	dB
Total Harmonic Distortion	f_S = 1MHz, f_{IN} = 100kHz	-	-44	-	-	-	dBc
	f_S = 30MHz, f_{IN} = 4MHz	-	-38	-	-	-	dBc
Differential Gain	f_S = 14.32MHz, f_{IN} = 3.58MHz	-	2	-	-	-	%
Differential Phase	f_S = 14.32MHz, f_{IN} = 3.58MHz	-	2	-	-	-	Degree

Electrical Specifications V_{DD} = +5.0V; V_{REF+} = +4.0V; V_{REF-} = V_{SS} = GND; f_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	25°C			(NOTE 2) 0°C TO 70°C -40°C TO 85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
ANALOG INPUTS							
Analog Input Resistance, R_{IN}	V_{IN} = 4V	-	30	-	-	-	MΩ
Analog Input Capacitance, C_{IN}	V_{IN} = 0V	-	20	-	-	-	pF
Analog Input Bias Current, IB	V_{IN} = 0V, 4V	-	0.01	±1.0	-	±1.0	µA
REFERENCE INPUTS							
Total Reference Resistance, R_L		250	370	-	235	-	Ω
Reference Resistance Tempco, T_C		-	+0.266	-	-	-	Ω/°C
DIGITAL INPUTS							
Input Logic High Voltage, V_{IH}		2.0	-	-	2.0	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	-	0.8	V
Input Logic High Current, I_{IH}	V_{IN} = 5V	-	-	1.0	-	1.0	µA
Input Logic Low Current, I_{IL}	V_{IN} = 0V	-	-	1.0	-	1.0	µA
Input Capacitance, C_{IN}		-	7	-	-	-	pF
DIGITAL OUTPUTS							
Output Logic Sink Current, I_{OL}	V_O = 0.4V	3.2	-	-	3.2	-	mA
Output Logic Source Current, I_{OH}	V_O = 4.5V	-3.2	-	-	-3.2	-	mA
Output Leakage, I_{OFF}	CE2 = 0V	-	-	±1.0	-	±1.0	µA
Output Capacitance, C_{OUT}	CE2 = 0V	-	5.0	-	-	-	pF
TIMING CHARACTERISTICS							
Aperture Delay, t_{AP}		-	6	-	-	-	ns
Aperture Jitter, t_{AJ}		-	30	-	-	-	ps
Data Output Enable Time, t_{EN}	(Note 2)	-	12	20	-	20	ns
Data Output Disable Time, t_{DIS}	(Note 2)	-	11	20	-	20	ns
Data Output Delay, t_{OD}	(Note 2)	-	14	20	-	20	ns
Data Output Hold, t_H	(Note 2)	5	10	-	5	-	ns
POWER SUPPLY REJECTION							
Offset Error PSRR, ΔV_{OS}	V_{DD} = 5V ±10%	-	±0.1	±1.0	-	±1.5	LSB
Gain Error PSRR, ΔFSE	V_{DD} = 5V ±10%	-	±0.1	±1.0	-	±1.5	LSB
POWER SUPPLY CURRENT							
Supply Current, I_{DD}	f_S = 30MHz	-	50	60	-	75	mA

NOTES:

2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

3. Parameter guaranteed by design or characterization and not production tested.

Timing Waveforms

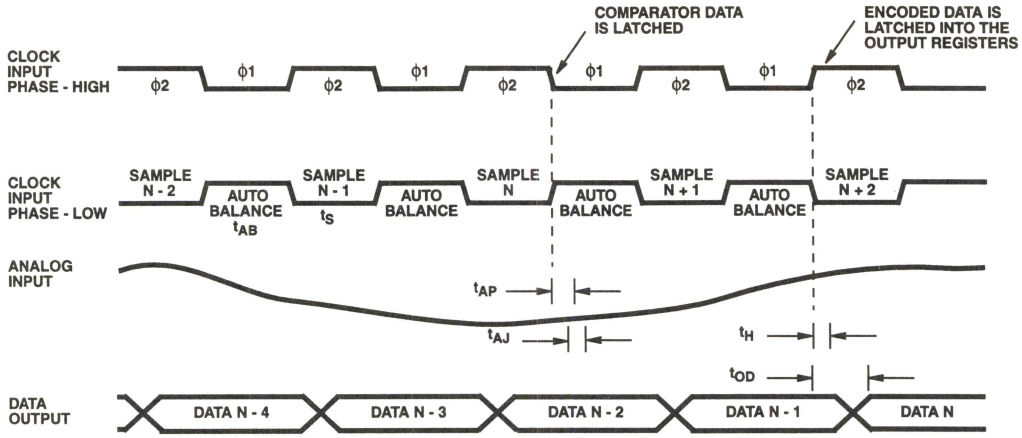


FIGURE 1. INPUT-TO-OUTPUT TIMING

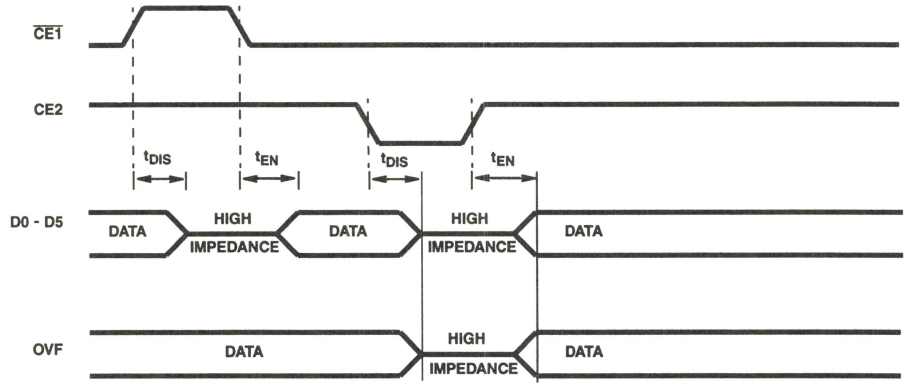


FIGURE 2. OUTPUT ENABLE TIMING

Typical Performance Curves

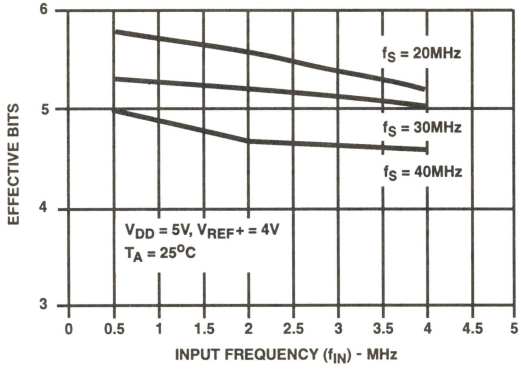


FIGURE 3. EFFECTIVE NUMBER OF BITS vs f_{IN}

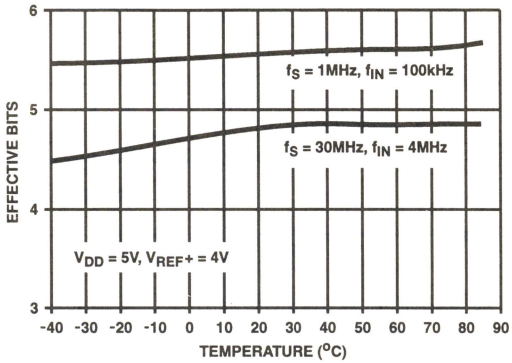


FIGURE 4. ENOB vs TEMPERATURE

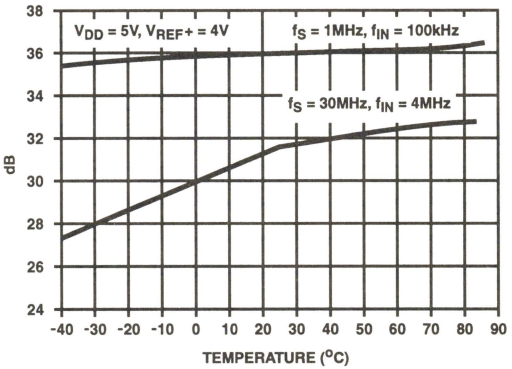


FIGURE 5. SNR vs TEMPERATURE

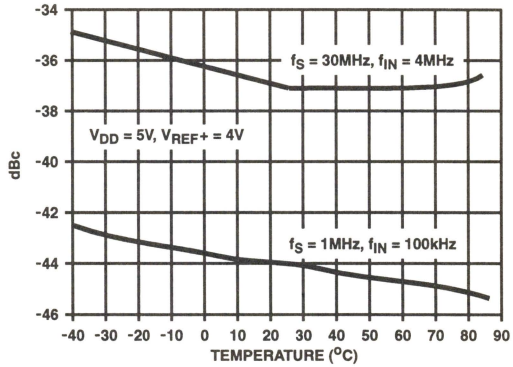


FIGURE 6. TOTAL HARMONIC DISTORTION vs TEMPERATURE

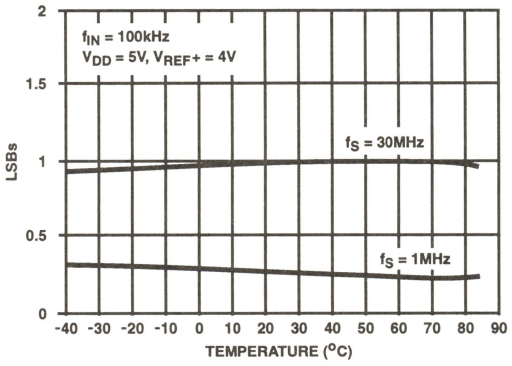


FIGURE 7. INL vs TEMPERATURE

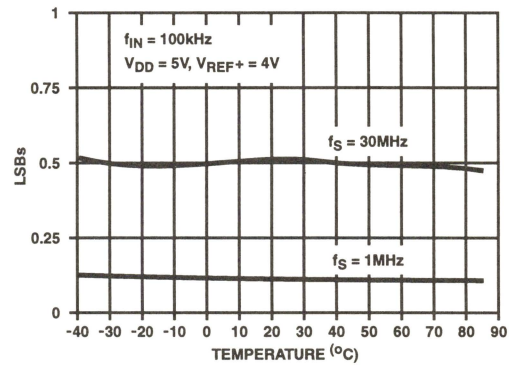


FIGURE 8. DNL vs TEMPERATURE

Typical Performance Curves (Continued)

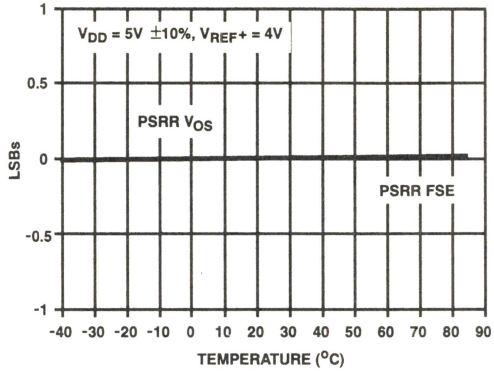


FIGURE 9. POWER SUPPLY REJECTION vs TEMPERATURE

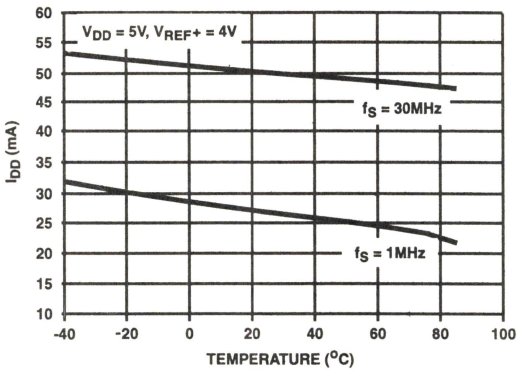


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

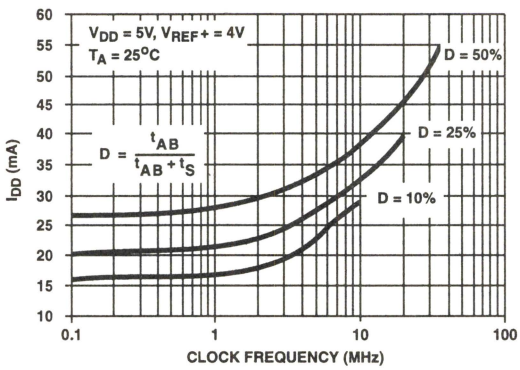


FIGURE 11. SUPPLY CURRENT vs CLOCK AND DUTY CYCLE

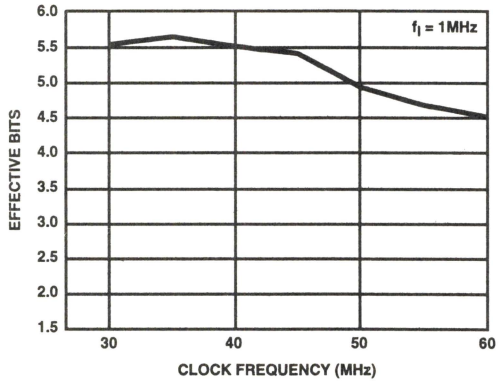


FIGURE 12. EFFECTIVE NUMBER OF BITS vs CLOCK FREQUENCY

TABLE 1. PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1	D5	Bit 6, Output (MSB).
2	OVF	Overflow, Output.
3	V_{SS}	Digital Ground.
4	NC	No Connection.
5	CE2	Three-State Output Enable Input, Active High (See Table 2).
6	$\overline{CE1}$	Three-State Output Enable Input, Active Low (See Table 2).
7	CLK	Clock Input.
8	PHASE	Sample Clock Phase Control Input. When Phase is Low, Sample Unknown (ϕ1) Occurs When the Clock is Low and Auto Balance (ϕ2) Occurs When the Clock is High (See Text).
9	$V_{REF}+$	Reference Voltage Positive Input.
10	$V_{REF}-$	Reference Voltage Negative Input.
11	V_{IN}	Analog Signal Input.
12	V_{DD}	Power Supply, +5V.
13	D0	Bit 1, Output (LSB).
14	D1	Bit 2, Output.
15	D2	Bit 3, Output.
16	$^1/_2$ R2	Reference Ladder Midpoint.
17	D3	Bit 4, Output.
18	D4	Bit 5, Output.

TABLE 2. CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	D0 - D5	OVF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't Care

Theory of Operation

The HI-5701 is a 6-bit analog-to-digital converter based on a parallel CMOS "flash" architecture. This flash technique is an extremely fast method of A/D conversion because all bit decisions are made simultaneously. In all, 64 comparators are used in the HI-5701; 63 comparators to encode the output word, plus an additional comparator to detect an overflow condition.

The CMOS HI-5701 works by alternately switching between a "Sample" mode and an "Auto Balance" mode. Splitting up the comparison process in this CMOS technique offers a number of significant advantages. The offset voltage of each CMOS comparator is dynamically canceled with each conversion cycle such that offset voltage drift is virtually eliminated during operation. The block diagram and timing diagram illustrate how the HI-5701 CMOS flash converter operates.

The input clock which controls the operation of the HI-5701 is first split into a non-inverting ϕ1 clock and an inverting ϕ2 clock. These two clocks, in turn, synchronize all internal timing of analog switches and control logic within the converter.

In the "Auto Balance" mode (ϕ1), all ϕ1 switches close and ϕ2 switches open. The output of each comparator is momentarily tied to its own input, self-biasing the comparator midway between V_{SS} and V_{DD} and presenting a low impedance to a small input capacitor. Each capacitor, in turn, is connected to a reference voltage tap from the resistor ladder. The Auto Balance mode quickly precharges all 64 input capacitors between the self-bias voltage and each respective tap voltage.

In the "Sample" mode (ϕ2), all ϕ1 switches open and ϕ2 switches close. This places each comparator in a sensitive high gain amplifier configuration. In this open loop state, the input impedance is very high and any small voltage shift at the input will drive the output either high or low. The ϕ2 state also switches each input capacitor from its reference tap to the input signal. This instantly transfers any voltage difference between the reference tap and input voltage to the comparator input. All 64 comparators are thus driven simultaneously to a defined logic state. For example, if the input voltage is at mid-scale, capacitors precharged near zero during ϕ1 will push comparator inputs higher than the self bias voltage at ϕ2; capacitors precharged near the reference voltage push the respective comparator inputs lower than the bias point. In general, all capacitors precharged by taps above the input voltage force a "low" voltage at comparator inputs; those precharged below the input voltage force "high" inputs at the comparators.

During the next ϕ1 state, comparator output data is latched into the encoder logic block and the first stage of encoding takes place. The following ϕ2 state completes the encoding process. The 6 data bits (plus overflow bit) are latched into the output flip-flops at the next falling clock edge. The Overflow bit is set if the input voltage exceeds $V_{REF}+ - {}^1/_2$ LSB. The output bus may be either enabled or disabled according to the state of $\overline{CE1}$ and CE2 (See Table 2). When disabled, output bits assume a high impedance state.

As shown in the timing diagram, the digital output word becomes valid after the second ϕ1 state. There is thus a one and a half cycle pipeline delay between input sample and digital output. "Data Output Delay" time indicates the slight time delay for data to become valid at the end of the ϕ1 state. Refer to the Glossary of Terms for other definitions.

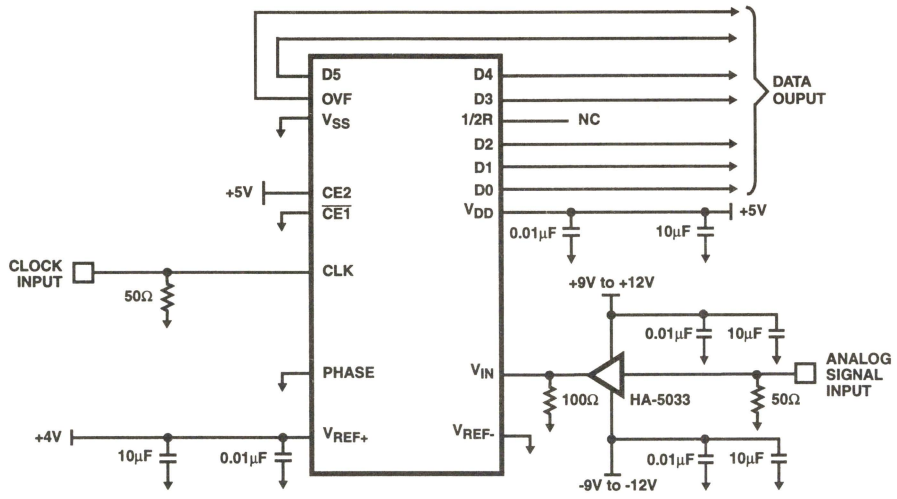


FIGURE 13. TEST CIRCUIT

Application Information

Voltage Reference

The reference voltage is applied across the resistor ladder at the input of the converter, between $V_{REF}+$ and $V_{REF}-$. In most applications, $V_{REF}-$ is simply tied to analog ground such that the reference source drives $V_{REF}+$. The reference must be capable of supplying enough current to drive the minimum ladder resistance of 235Ω over temperature.

The HI-5701 is specified for a reference voltage of 4.0V, but will operate with voltages as high as the V_{DD} supply. In the case of 4.0V reference operation, the converter encodes the analog input into a binary output in LSB increments of $(V_{REF}+ - V_{REF}-)/64$, or 62.5mV. Reducing the reference voltage reduces the LSB size proportionately and thus increases linearity errors. The minimum practical reference voltage is about 2V. Because the reference voltage terminals are subjected to internal transient currents during conversion, it is important to drive the reference pins from a low impedance source and to decouple thoroughly. Again, ceramic and tantalum (0.01µF and 10µF) capacitors near the package pin are recommended. It is not necessary to decouple the $^1/_2$R tap point pin for most applications.

It is possible to elevate $V_{REF}-$ from ground if necessary. In this case, the $V_{REF}-$ pin must be driven from a low impedance reference capable of sinking the current through the resistor ladder. Careful decoupling is again recommended.

Digital Control and Interface

The HI-5701 provides a standard high speed interface to external CMOS and TTL logic families. Four digital inputs are provided to control the function of the converter. The clock and phase inputs control the sample and auto balance modes. The digital outputs change state on the clock phase which begins the sample mode. Two chip enable inputs control the three-state outputs of output bits D0 through D5 and the Overflow OVF bit. As indicated in Table 2, all output bits are high impedance when CE2 is low, and output bits D0 through D5 are independently controlled by $\overline{CE1}$.

Although the Digital Outputs are capable of handling typical data bus loading, the bus capacitance charge/discharge currents will produce supply and local ground disturbances. Therefore, an external bus driver is recommended.

Clock

The clock should be properly terminated to digital ground near the clock input pin. Clock frequency defines the conversion frequency and controls the converter as described in the "Theory of Operation" section. The Auto Balance ϕ1 half cycle of the clock may be reduced to 16ns; the Sample ϕ2 half cycle may be varied from a minimum of 16ns to a maximum of 8µs.

TABLE 3. PHASE CONTROL

CLOCK	PHASE	INTERNAL GENERATION
0	0	Sample Unknown (ϕ2)
0	1	Auto Balance (ϕ1)
1	0	Auto Balance (ϕ1)
1	1	Sample Unknown (ϕ2)

Gain and Offset Adjustment

In applications where accuracy is of utmost importance, three adjustments can be made; i.e., offset, gain, and midpoint trim. In general, offset and gain correction can be done in the preamp circuitry.

Offset Adjustment

The preferred offset correction method is to introduce a DC component to V_{IN} of the converter. An alternate method is to adjust the $V_{REF}-$ input to produce the desired offset adjustment. The theoretical input voltage to produce the first transition is $^1/_2$ LSB.

V_{IN} (0 to 1 transition) = $^1/_2$ LSB = $^1/_2(V_{REF}/64) = V_{REF}/128$.

Gain Adjustment

In general, full scale error correction can be done in the preamp circuitry by adjusting the gain of the op amp. An alternate method is to adjust the $V_{REF}+$ input voltage. This adjustment is performed by setting V_{IN} to the 63 to overflow transition. The theoretical input voltage to produce the transition is $^1/_2$ LSB less than $V_{REF}+$ and is calculated as follows:

V_{IN} (63 to 64 transition) = V_{REF} - (V_{REF}/128) = V_{REF}(127/128).

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overflow transition. Now adjust $V_{REF}+$ until that transition occurs on the outputs.

Midpoint Trim

The reference center ($^1/_2$R) is available to the user as the midpoint of the resistor ladder. The $^1/_2$R point can be used to improve linearity or create unique transfer functions. The offset and gain trims should be done prior to adjusting the midpoint. The theoretical transition from count 31 to 32 occurs at 31.5 LSBs. That voltage is calculated as follows:

V_{IN} (31 to 32 transition) = 31.5(V_{REF}/64) = V_{REF}(63/128).

An adjustable voltage follower can be used to drive the $^1/_2$R pin. Set V_{IN} to the 31 to 32 transition voltage, then adjust the voltage follower until the transition occurs on the output bits.

Signal Source

A current pulse is present at the analog input (V_{IN}) at the beginning of every sample and auto balance period. The transient current is due to comparator charging and switch feed through in the capacitor array. It varies with the amplitude of the analog input and the sampling rate.

The signal source must be capable of recovering from the transient prior to the end of the sample period to ensure a valid signal for conversion. Suitable broad band amplifiers or buffers which exhibit low output impedance and high output drive include the HFA-0005, HA-5004, HA-5002, and HA-5033.

The signal source may drive above or below the power supply rails, but should not exceed 0.5V beyond the rails or damage may occur. Input voltages of -0.5V to +$^1/_2$ LSB are converted to all zeros; input voltages of $V_{REF}+$ - $^1/_2$ LSB to V_{DD} + 0.5 are converted to all ones with the Overflow bit set.

Power Supply

The HI-5701 operates nominally from a 5V supply, but will function from 3V to 6V. The supply should be well regulated and "clean" of significant noise, especially high frequency noise. It is recommended that power supply decoupling capacitors be placed as close to the supply pin as possible. A combination of 0.01µF ceramic and 10µF tantalum capacitors is recommended for this purpose as shown in the test circuit Figure 13.

Reducing Power Consumption

Power dissipation in the HI-5701 is related to clock frequency and clock duty cycle. For a fixed 50% clock duty cycle, power may be reduced by lowering the clock frequency. For a given conversion frequency, power may be reduced by shortening the Auto Balance ϕ1 portion of the clock duty cycle.

TABLE 3. OUTPUT CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE† $V_{REF}+$ = 4V $V_{REF}-$ = 0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB						LSB
			OVF	D5	D4	D3	D2	D1	D0
Overflow (OVF)	4.000	127	1	1	1	1	1	1	1
Full Scale (FS)	3.9063	63	0	1	1	1	1	1	1
FS - 1 LSB	3.8438	62	0	1	1	1	1	1	0
	•					•			
	•					•			
						•			
$^3/_4$ FS	2.9688	48	0	1	1	0	0	0	0
	•					•			
	•					•			
	•					•			
$^1/_2$ FS	1.9688	32	0	1	0	0	0	0	0
	•					•			
	•					•			
	•					•			
$^1/_4$ FS	0.9688	16	0	0	1	0	0	0	0
	•					•			
	•					•			
	•					•			
1 LSB	0.0313	1	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0

† The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage.

Glossary of Terms

Aperture Delay, is the time delay between the external sample command (the rising edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter, t_{AJ}, This is the RMS variation in the aperture delay due to variation of internal $\phi 1$ and $\phi 2$ clock path delays and variation between the individual comparator switching times.

Differential Linearity Error, DNL, The differential linearity error is the difference in LSBs between the spacing of the measured midpoint of adjacent codes and the spacing of ideal midpoints of adjacent codes. The ideal spacing of each midpoint is 1 LSB. The range of values possible is from -1 LSB (which implies a missing code) to greater than +1 LSB.

Full Power Input Bandwidth, Full power bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Full Scale Error, FSE, is the difference between the actual input voltage of the 63 to 64 code transition and the ideal value of $V_{REF}+ - 1.5$ LSB. This error is expressed in LSBs.

Integral Linearity Error, INL, The integral linearity error is the difference in LSBs between the measured code centers and the ideal code centers. The ideal code centers are calculated using a best fit line through the converter's transfer function.

LSB, Least Significant Bit = $(V_{REF}+ - V_{REF}-)/64$. All HI-5701 specifications are given for a 62.5mV LSB size $V_{REF}+ = 4V$, $V_{REF}- = 0V$.

Offset Error, V_{OS}, Offset error is the difference between the actual input voltage of the 0 to 1 code transition and the ideal value of $V_{REF}- + 0.5$ LSB. V_{OS} error is expressed in LSBs.

Power Supply Rejection Ratio, PSRR, is expressed in LSBs and is the maximum shift in code transition points due to a power supply voltage shift. This is measured at the 0 to 1 code transition point and the 62 to 63 code transition point with a power supply voltage shift from the nominal value of 5.0V.

Signal to Noise Ratio, SNR, SNR is the ratio in dB of the RMS signal to RMS noise at specified input and sampling frequencies.

Signal to Noise and Distortion Ratio, SINAD, is the ratio in dB of the RMS signal to the RMS sum of the noise and harmonic distortion at specified input and sampling frequencies.

Total Harmonic Distortion, THD, is the ratio in dBc of the RMS sum of the first five harmonic components to the RMS signal for a specified input and sampling frequency.

Die Characteristics

DIE DIMENSIONS:

86.6 mils x 130.7 mils x 19 mils ±1 mil

METALLIZATION:

Type: SiAl
Thickness: 11kÅ ±1kÅ

PASSIVATION:

Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

$<2.0 \times 10^5$ A/cm^2

TRANSISTOR COUNT:

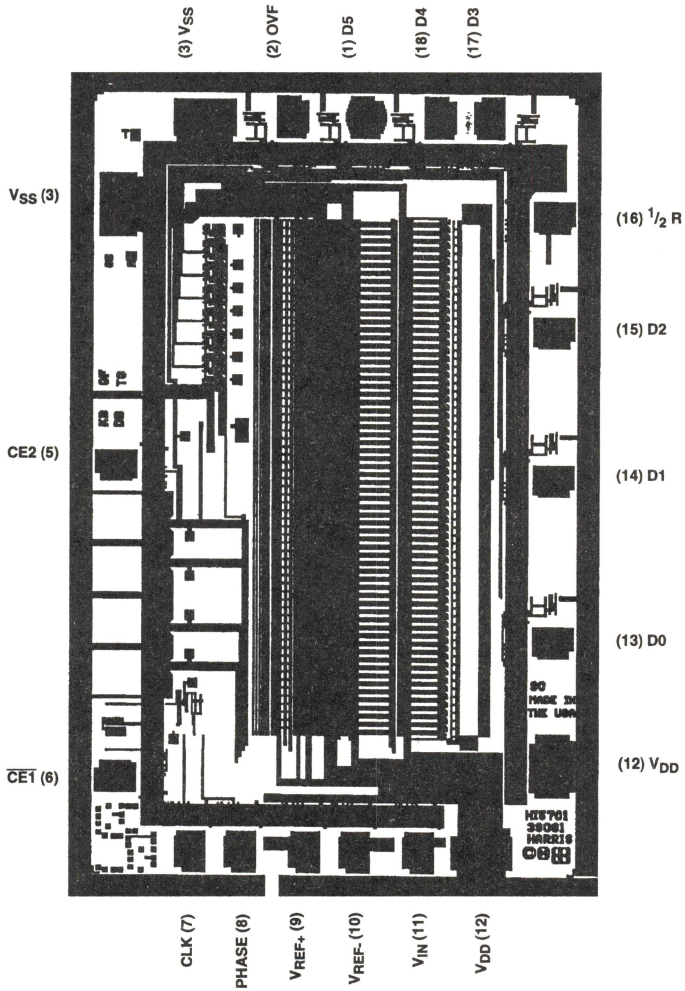
4000

SUBSTRATE POTENTIAL (Powered Up):

V+

Metallization Mask Layout

HI-5701



HARRIS SEMICONDUCTOR

HI5702

August 1997

10-Bit, 40 MSPS A/D Converter

Features

- Sampling Rate ..... 40 MSPS
- 8.3 Bits Guaranteed at f_{IN} = 10MHz
- Low Power
- Wide Full Power Input Bandwidth 250MHz
- Sample and Hold Not Required
- Single-Ended or Differential Input
- Input Signal Range 1.25V
- Single Supply Voltage .....+5V
- TTL Compatible Interface

Applications

- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition

Description

The HI5702 is a monolithic, 10-bit, analog-to-digital converter fabricated in a BiCMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 MSPS speed is made possible by a fully differential pipeline architecture which also eliminates the need for an external sample and hold circuit. The HI5702 has excellent dynamic performance while consuming <650mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles.

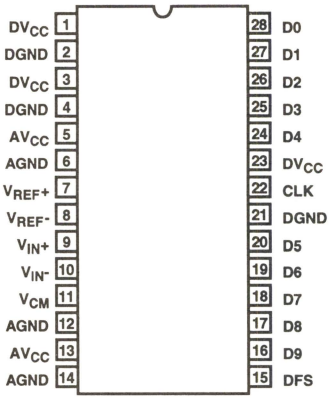
Refer to the HI5703, HI5746, or HI5767 data sheets for lower power consumption.

Ordering Information

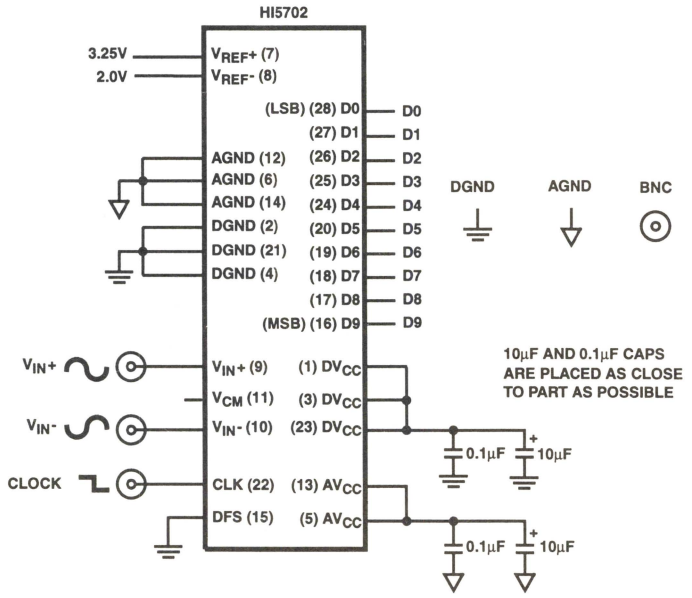
PART NUMBER	SAMPLE RATE	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5702KCB	40 MSPS	0 to 70	28 Ld SOIC (W)	M28.3
HI5702JCB	36 MSPS	0 to 70	28 Ld SOIC (W)	M28.3
HI5702-EV2		25	Evaluation Board	

Pinout

HI5702
(SOIC)
TOP VIEW



Typical Application Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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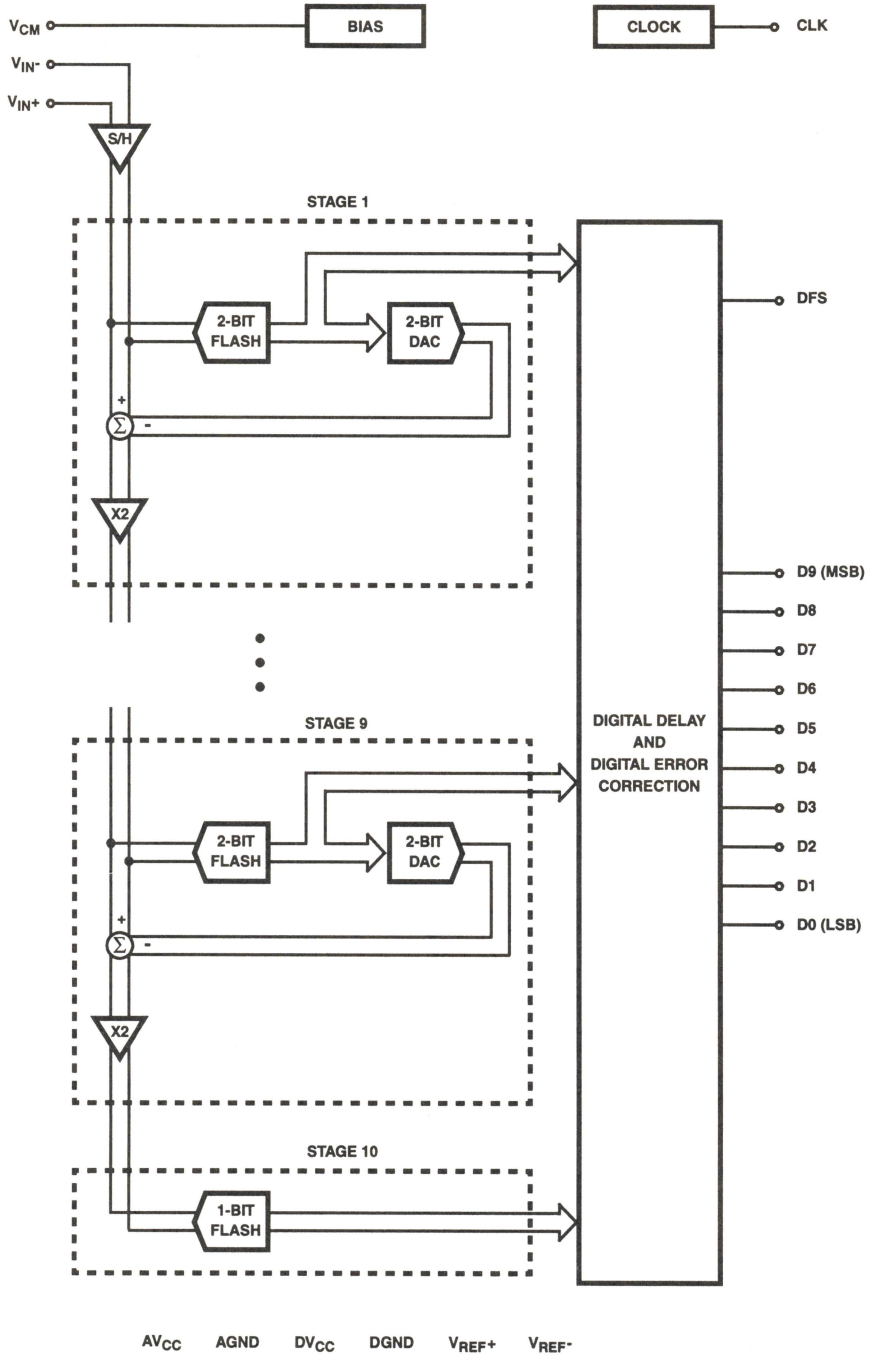
File Number 3745.4

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND . . . . . +6V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{CC}
Analog I/O Pins. . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range
HI5702KCB/JCB . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SOIC Package 70
Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC} = +5V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2V$; f_S = Specified Clock Frequency at 50% Duty Cycle; $C_L = 20pF$; $T_A = 25^oC$; Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±1	±2.0	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1	LSB
Offset Error, V_{OS}	f_{IN} = DC	-	3	-	LSB
Full Scale Error, FSE	f_{IN} = DC	-	2	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	-	MSPS
Maximum Conversion Rate	No Missing Codes HI5702KCB	40	-	-	MSPS
	HI5702JCB	36	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	-	9.0	-	Bits
	f_{IN} = 5MHz	-	9.0	-	Bits
	f_{IN} = 10MHz	8.3	8.8	-	Bits
Signal to Noise and Distribution Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	57	-	dB
	f_{IN} = 5MHz	-	57	-	dB
	f_{IN} = 10MHz	51	56	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	-	56	-	dB
	f_{IN} = 5MHz	-	56	-	dB
	f_{IN} = 10MHz	51	55	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-	-64	-	dBc
	f_{IN} = 5MHz	-	-63	-	dBc
	f_{IN} = 10MHz	-	-60	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-75	-	dBc
	f_{IN} = 5MHz	-	-75	-	dBc
	f_{IN} = 10MHz	-	-73	-	dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-66	-	dBc
	f_{IN} = 5MHz	-	-64	-	dBc
	f_{IN} = 10MHz	-	-63	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz	-	66	-	dBc
	f_{IN} = 5MHz	-	64	-	dBc
	f_{IN} = 10MHz	54	63	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	-59	-	dBc

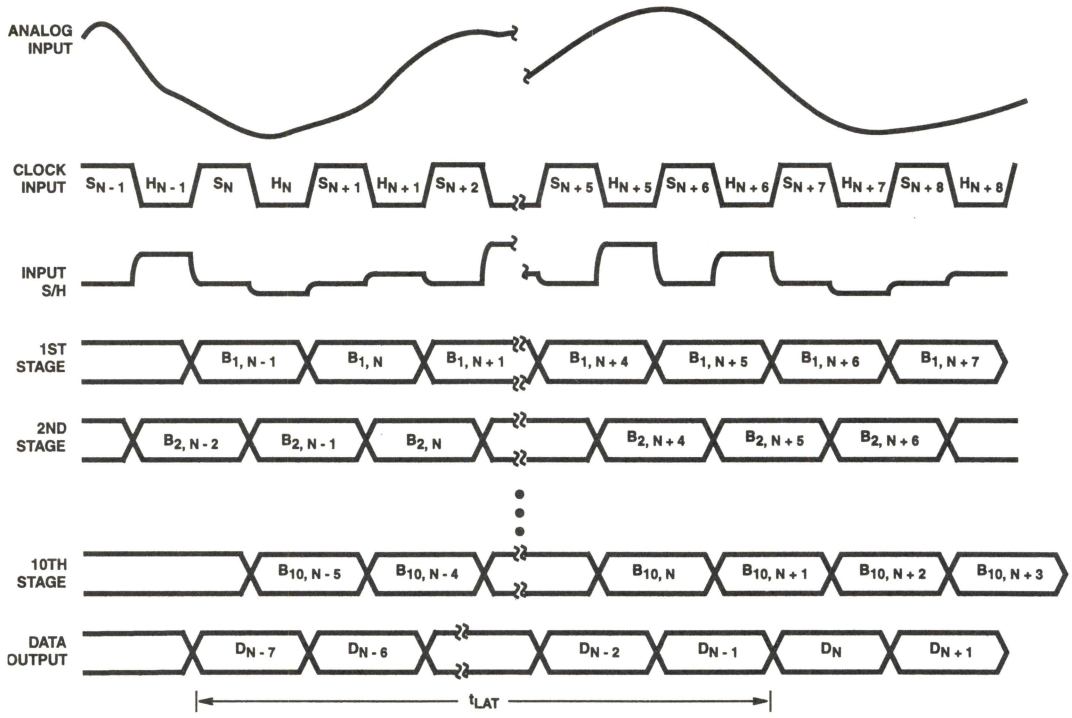
Electrical Specifications $AV_{CC} = DV_{CC} = +5V$; $V_{REF+} = 3.25V$; $V_{REF-} = 2V$; f_S = Specified Clock Frequency at 50% Duty Cycle; $C_L = 20pF$; $T_A = 25^oC$; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Gain Error	f_S = 17.72MHz, 6 Step, Mod Ramp	-	0.5	1	%
Differential Phase Error	f_S = 17.72MHz, 6 Step, Mod Ramp	-	0.25	0.5	Degree
Transient Response		-	1	-	Cycle
Overvoltage Recovery	0.2V Overdrive	-	1	-	Cycle
ANALOG INPUT					
Analog Input Resistance, R_{IN}	(Note 3)	-	1	-	MΩ
Analog Input Capacitance, C_{IN}		-	7	-	pF
Analog Input Bias Current, I_B	(Note 3)	-50	-	+50	µA
Full Power Input Bandwidth		-	250	-	MHz
Analog Input Common Mode Range $(V_{IN+} + V_{IN-}) / 2$	Differential Mode (Note 2)	0.625	-	4.375	V
REFERENCE INPUT					
Total Reference Resistance, R_L		200	400	-	Ω
Reference Current		-	3	6	mA
Positive Reference Input, V_{REF+}	(Note 2)	-	3.25	3.3	V
Negative Reference Input, V_{REF-}	(Note 2)	1.95	2.0	-	V
Reference Common Mode Voltage $(V_{REF+} + V_{REF-}) / 2$	(Note 2)	2.575	2.625	2.675	V
COMMOM MODE VOLTAGE					
Common Mode Voltage Output, V_{CM}		-	2.8	-	V
Max Output Current		-	-	1	mA
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	V_{IN} = 5V	-	-	10.0	µA
Input Logic Low Current, I_{IL}	V_{IN} = 0V	-	-	10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS					
Output Logic Sink Current, I_{OL}	V_O = 0.4V	3.2	-	-	mA
Output Logic Source Current, I_{OH}	V_O = 2.4V	-0.2	-	-	mA
Output Capacitance, C_{OUT}		-	5	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps
Data Output Delay, t_{OD}		-	6	-	ns
Data Output Hold, t_H		-	5	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	7	Cycles
Power-Up Initialization	Data Invalid Time (Note 2)	-	-	20	Cycles
POWER SUPPLY CHARACTERISTICS					
Supply Current, I_{CC}	V_{IN} = 0V	-	120	130	mA
Power Dissipation	V_{IN} = 0V	-	600	650	mW
Offset Error PSRR, ΔV_{OS}	AV_{CC} or DV_{CC} = 5V ±5%	-	0.2	-	LSB
Gain Error PSRR, ΔFSE	AV_{CC} or DV_{CC} = 5V ±5%	-	1	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock off.

Timing Waveforms



NOTES:

1. S_N: N-th sampling period.
2. H_N: N-th holding period.
3. $B_{M,N}$: M-th stage digital output corresponding to N-th sampled input.
4. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5702 INTERNAL CIRCUIT TIMING

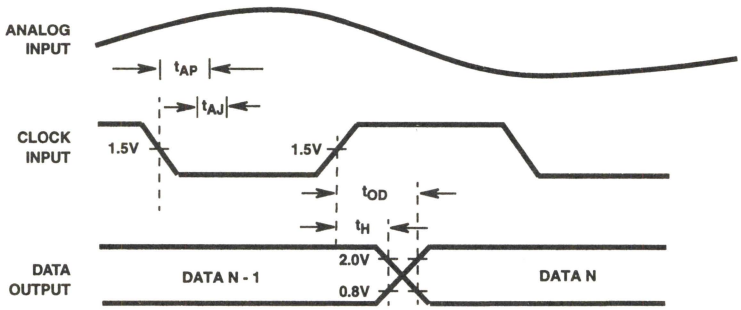


FIGURE 2. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

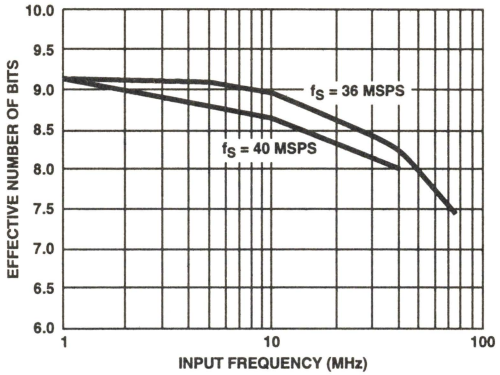


FIGURE 3. ENOB vs INPUT FREQUENCY

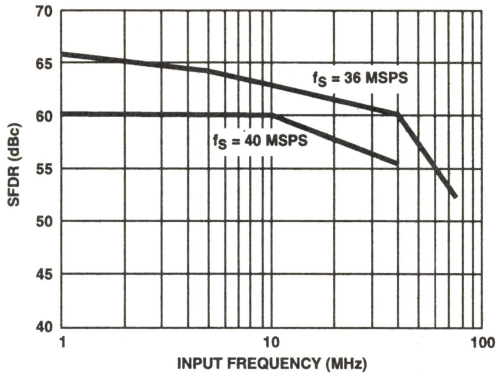


FIGURE 4. SFDR vs INPUT FREQUENCY

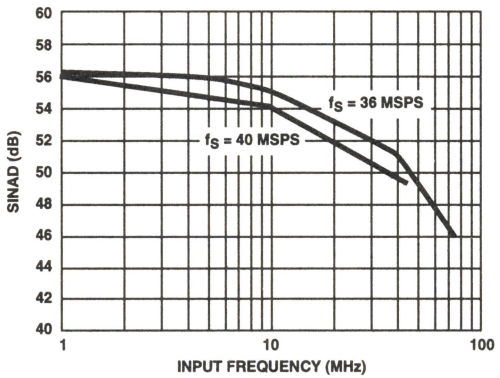


FIGURE 5. SINAD vs INPUT FREQUENCY

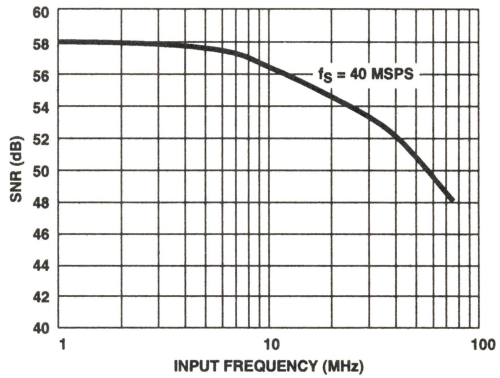


FIGURE 6. SNR vs INPUT FREQUENCY

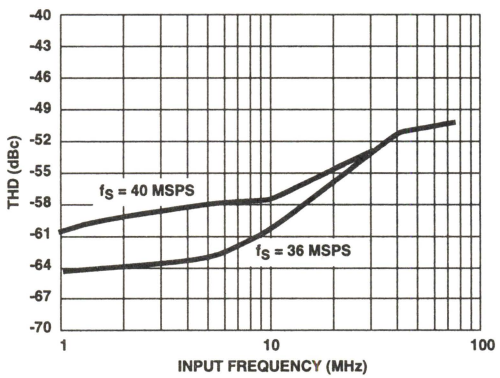


FIGURE 7. THD vs INPUT FREQUENCY

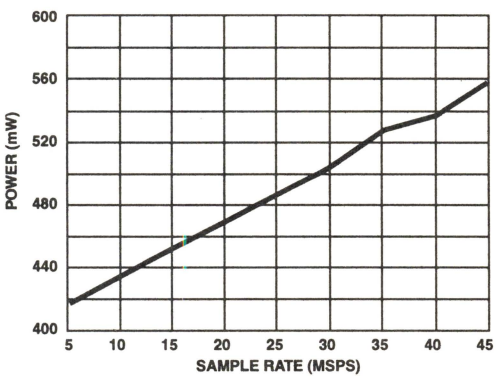


FIGURE 8. POWER DISSIPATION vs SAMPLE RATE

Typical Performance Curves (Continued)

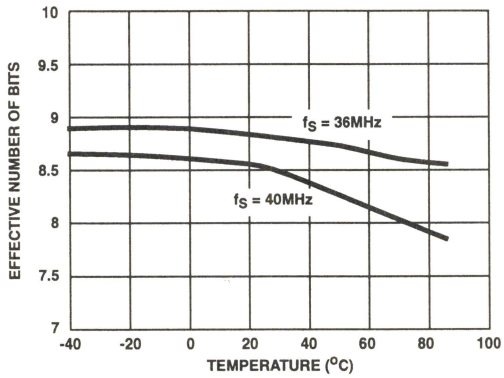


FIGURE 9. ENOB vs TEMPERATURE

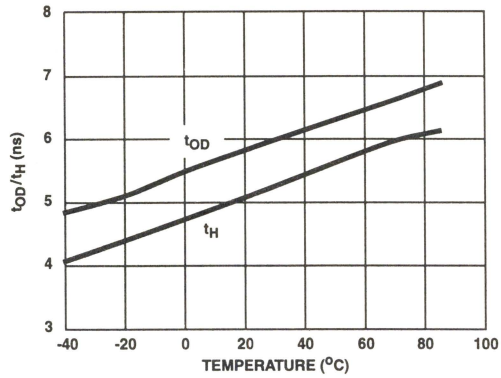


FIGURE 10. t_{OH}/t_D vs TEMPERATURE

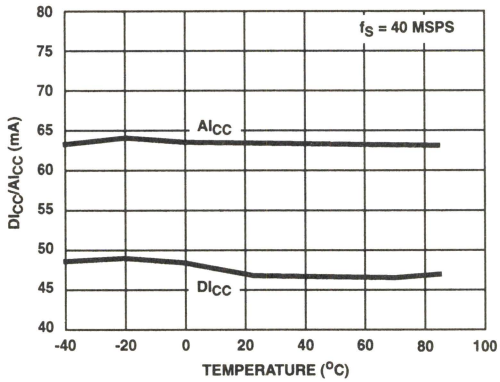


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

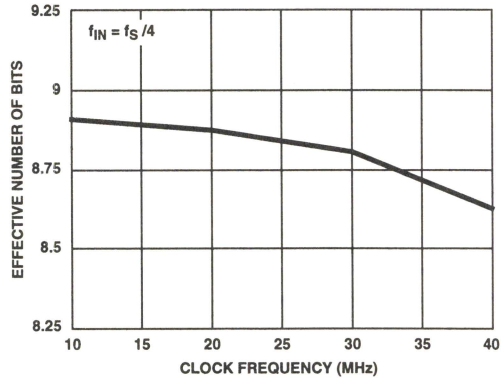


FIGURE 12. ENOB vs SAMPLE RATE WITH FIXED 12.5ns CLOCK PULSE WIDTH

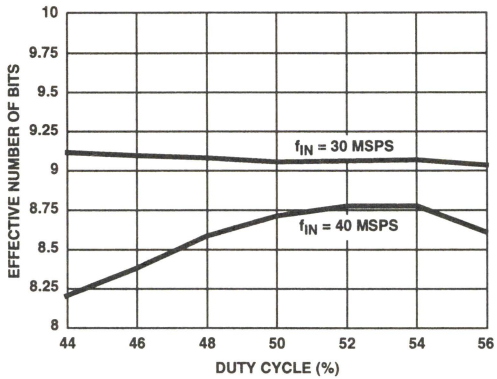


FIGURE 13. ENOB vs DUTY CYCLE

TABLE 1. PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1	DV_{CC}	Digital Supply.
2	DGND	Digital Ground.
3	DV_{CC}	Digital Supply.
4	DGND	Digital Ground.
5	AV_{CC}	Analog Supply.
6	AGND	Analog Ground.
7	V_{REF+}	Positive Reference.
8	V_{REF-}	Negative Reference.
9	V_{IN+}	Positive Analog Input.
10	V_{IN-}	Negative Analog Input.
11	V_{CM}	DC Output Voltage Source.
12	AGND	Analog Ground.
13	AV_{CC}	Analog Supply.
14	AGND	Analog Ground.
15	DFS	Data Format Select.
16	D9	Data Bit 9 Output (MSB).
17	D8	Data Bit 8 Output.
18	D7	Data Bit 7 Output.
19	D6	Data Bit 6 Output.
20	D5	Data Bit 5 Output.
21	DGND	Digital Ground.
22	CLK	Input Clock.
23	DV_{CC}	Digital Supply.
24	D4	Data Bit 4 Output.
25	D3	Data Bit 3 Output.
26	D2	Data Bit 2 Output.
27	D1	Data Bit 1 Output.
28	D0	Data Bit 0 Output (LSB).

Detailed Description

Theory of Operation

The HI5702 is a 10-bit fully differential sampling pipeline A/D converter with digital error correction. Figure 13 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The small values of these components result in a typical full power bandwidth of 250MHz.

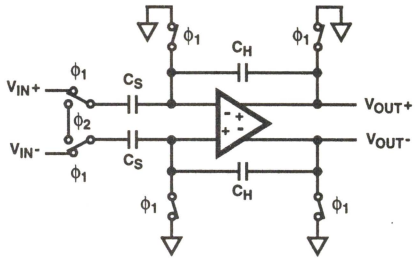


FIGURE 14. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the Functional Block Diagram and the Timing Diagram in Figure 1, nine identical pipeline subconverter stages, each containing a two-bit flash and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the tenth stage being a one bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual sub-converter clock signal is offset by 180 degrees from the previous stage clock signal with the result that alternate stages in the pipeline will perform the same operation.

The two-bit digital output of each stage is fed to a digital delay line controlled by the internal clock. The purpose of the delay line is to align the digital output data to the corresponding sampled analog input signal. This delayed data is fed to the digital error correction circuit which corrects the error in the output data with the information contained in the redundant bits to form the final 10-bit output for the converter.

Because of the pipeline nature of this converter, the data on the bus is output at the 7th cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The output data is synchronized to the external clock by a double buffered latching technique.

The output of the digital correction circuit is available in two's complement or binary format depending on the condition of the Data Format Select (DFS) input.

Analog Input, Differential Connection

The analog input to the HI5702 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 15) will give the best performance for the converter.

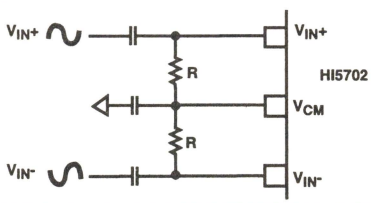


FIGURE 15. AC COUPLED DIFFERENTIAL INPUT

Since the HI5702 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V, which implies the common mode voltage can range of 0.625V to 4.375V. The performance of the ADC does not change significantly with the value of the common mode voltage.

A DC voltage source, V_{CM}, about half way between the top and bottom reference voltages, is made available to the user to help simplify circuit design when using a differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the common mode range over temperature. It has a temperature coefficient of about 200ppm.

Assume the difference between $V_{REF}+$, typically 3.25V, and $V_{REF}-$, typically 2V, is 1.25V in Figure 15. Fullscale is achieved when $V_{IN}+$ and $V_{IN}-$ inputs are $1.25V_{P-P}$, with $V_{IN}-$ being 180 degrees out of phase with $V_{IN}+$. The converter will be at positive fullscale when the $V_{IN}+$ input is at V_{CM} + 0.625V and $V_{IN}-$ is at V_{CM} - 0.625V ($V_{IN}+ - V_{IN}- = 1.25V$). Conversely, the ADC will be at negative fullscale when the $V_{IN}+$ input is equal to V_{CM} - 0.625V and $V_{IN}-$ is at V_{CM} + 0.625V ($V_{IN}+ - V_{IN}- = -1.25V$).

The analog input can be DC coupled as long as the inputs are within the common mode range, Figure 16.

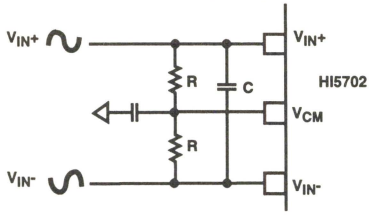


FIGURE 16. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 16 are not absolutely necessary but will improve performance. Values of 100Ω or less are typical. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help common mode any noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well.

Analog Input, Single-Ended Connection

The configuration shown in Figure 17 may be used with a single ended AC coupled input.

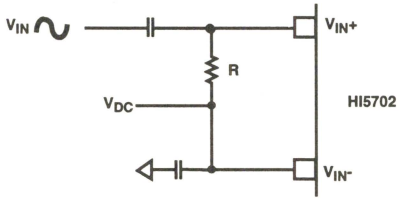


FIGURE 17. AC COUPLED SINGLE ENDED INPUT

Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND.

Again, assume the difference between $V_{REF}+$, typically 3.25V, and $V_{REF}-$, typically 2V, is 1.25V. If V_{IN} is a $2.5V_{P-P}$ sinewave riding on a positive voltage equal to V_{DC}, the converter will be at positive fullscale when $V_{IN}+$ is at V_{DC} + 1.25V and will be at negative fullscale when V_{IN} is equal to V_{DC} - 1.25V. In this case, V_{DC} could range between 1.25V and 3.75V without a significant change in ADC performance. The simplest way to produce V_{DC} is to use the V_{CM} output of the HI5702.

The analog input can be DC coupled as long as the input is within the common mode range, Figure 18.

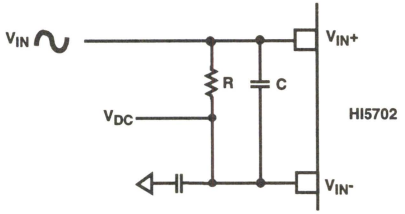


FIGURE 18. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 18 is not absolutely necessary but will improve performance. Values of 100Ω or less are typical. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help common mode any noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well.

A single ended source may give better overall system performance if it is first converted to differential before driving the HI5702. Also refer to the application note AN9413, "Driving the Analog Input of the HI5702". This application note describes several different ways of driving the analog differential inputs.

Reference Input, $V_{REF}-$ $V_{REF}+$

The converter requires two reference voltages connected to the V_{REF} pins. The voltage range of the part with a differential input will be $V_{REF}+ - V_{REF}-$. The HI5702 is tested with $V_{REF}-$ equal to 2V and $V_{REF}+$ equal to 3.25V for an input range of 1.25V. $V_{REF}+$ and $V_{REF}-$ can differ from the above voltages as long as the common mode voltage between the reference pins ($(V_{REF}+ + V_{REF}-) / 2$) does not exceed 2.65V ±50mV and the limits on $V_{REF}+$ and $V_{REF}-$ are not exceeded.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference input pin.

Digital Control and Clock Requirements

The HI5702 provides a standard high-speed interface to external TTL logic families.

In order to ensure rated performance of the HI5702, the duty cycle of the clock should be held at 50%. It must also have low jitter and operate at standard TTL levels.

A Data Format Select (DFS) pin is provided which will determine the format of the digital data. When at logic low the data will be output in offset binary format. When at a logic high the data will be output in a two's complement format. Refer to Table 2 for further information.

Performance of the HI5702 will only be guaranteed at conversion rates above 1 MSPS. This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1 MSPS will have to be performed before valid data is available.

Supply and Ground Considerations

The HI5702 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5702 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the Application Note "Using Harris High Speed A/D Converters" (AN9214) for additional considerations when using high speed converters.

Increased Accuracy

The V_{OS} and FSE errors as reported on the data sheet can be decreased by further calibration of the ADC. It will be assumed that the converter has offset binary coding. See the A/D code table (Table 2) for the ideal code transitions.

The first step would be to center the analog input to the desired midscale voltage. This voltage would then be adjusted up or down in the circuitry driving one side of the input to the HI5702 until the 511 to 512 transition occurs on the digital output.

Next, set the analog input to the HI5702 to the desired positive fullscale voltage. Adjust one side of the reference circuit up or down until the 1022 to 1023 transition occurs on the digital output of the converter.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$ LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for a analog input that is $1^3/_4$ LSBs below positive full-scale with the offset error removed. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection Ratio (PSRR)

Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5702. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full-scale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

TABLE 2. A/D CODE TABLE

CODE DESCRIPTION	(NOTE 1) DIFFERENTIAL INPUT VOLTAGE $V_{REF}+ = 3.25V$ $V_{REF}- = 2.0V$ (V)	OFFSET BINARY OUTPUT CODE (DFS LOW)										TWO'S COMPLEMENT OUTPUT CODE (DFS HIGH)									
		MSB									LSB	MSB									LSB
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale (FS)	1.25V	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
FS - $1^3/_4$ LSB	1.2479V	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
$^1/_2$ FS + $^1/_4$ LSB	0.3mV	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$^1/_2$ FS - $^3/_4$ LSB	2.1mV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$1^1/_4$ LSB	-1.2485V	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
Zero	-1.25V	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

NOTE:

1. The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

where: $V_{CORR} = 0.5dB$

V_{CORR} adjusts the ENOB for the amount the input is below fullscale.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present on the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are $(f_1 + f_2)$, $(f_1 - f_2)$, $(2f_1)$, $(2f_2)$, $(2f_1 + f_2)$, $(2f_1 - f_2)$, $(f_1 + 2f_2)$, $(f_1 - 2f_2)$. The ADC is tested with each tone 6dB below full scale.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component in the spectrum below $f_S/2$.

Transient Response

Transient response is measured by providing a full scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Overvoltage Recovery

Overvoltage Recovery is measured by providing a full scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Video Definitions

Differential gain and Differential Phase are two commonly found video specifications for characterizing the distortion of a chrominance (3.58MHz) signal as it is offset through the input voltage range of an ADC.

Differential Gain (DG)

Differential Gain is the peak difference in chrominance amplitude (in percent) at two different DC levels.

Differential Phase (DP)

Differential Phase is the peak difference in chrominance phase (in degrees) at two different DC levels.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AD})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

This is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the data on the bus is output at 7th cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 7 cycles.

Power-Up Initialization

This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.

HFA1135	HI5702	HSP9501	HI5780	HA5020
HFA1245	HI5703	HSP48410	HI1171	HA2842
	HI5746	HSP48908		HFA1115
	HI5767	HSP48212		
		HSP43891		
		HSP43168		
		HSP43216		

HFA1135: 350MHz Op Amp with Output Limiting
HFA1245: Dual 350MHz Op Amp with Disable/Enable
HI5702: 10-Bit, 40 MSPS, A/D Converter
HI5703: Low Power, 10-Bit, 40 MSPS, A/D Converter
HI5746: Low Power, CMOS, 10-Bit, 40 MSPS A/D Converter
HI5767: Low Power, CMOS, 10-Bit, 40 MSPS A/D Converter, with Voltage Reference
HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48212: Digital Video Mixer
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HI5780: 10-Bit, 80MHz, Video D/A Converter
HI1171: 8-Bit, 40MHz, Video D/A Converter
HFA5020: 100MHz Video Op Amp
HA2842: High Output Current, Video Op Amp
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 19. 10-BIT VIDEO IMAGING COMPONENTS

HFA3600	HI5702	HSP43168	HI5721	HFA1115
HFA3102	HI5703	HSP43216	HI5780	
HFA3101	HI5746	HSP43891	HI20201	
HFA1100	HI5767	HSP50016	HI20203	
		HSP50110		
		HSP50210		

HFA3600: Low Noise Amplifier/Mixer
HFA3102: Dual Long-Tailed Pair Transistor Array
HFA3101: Gilbert Cell Transistor Array
HFA1100: 850MHz Op Amp
HI5702: 10-Bit, 40 MSPS, A/D Converter
HI5703: Low Power, 10-Bit, 40 MSPS, A/D Converter
HI5746: Low Power, CMOS, 10-Bit, 40 MSPS A/D Converter
HI5767: Low Power, CMOS, 10-Bit, 40 MSPS A/D Converter, with Voltage Reference
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP50016: Digital Down Converter
HSP50110: Digital Quadrature Tuner
HSP50210: Digital Costas Loop
HI5721: 10-Bit, 125MHz, Communications D/A Converter
HI5780: 10-Bit, 80MHz, D/A Converter
HI20201: 10-Bit, 160MHz, High Speed D/A Converter
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 20. 10-BIT COMMUNICATIONS COMPONENTS

Die Characteristics

DIE DIMENSIONS:

159.4 mils x 175.2 mils x 19 mils ±1 mil

METALLIZATION:

Type: AlSiCu
Thickness: 11kÅ ±1kÅ

SUBSTRATE POTENTIAL (Powered Up):

GND (0.0V)

PASSIVATION:

Type: Sandwich Passivation
Nitride + Undoped Silicon Glass (USG)
Thickness: Nitride 4.2kÅ, USG 8kÅ
Total 12.2kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.6×10^4 A/cm^2

TRANSISTOR COUNT:

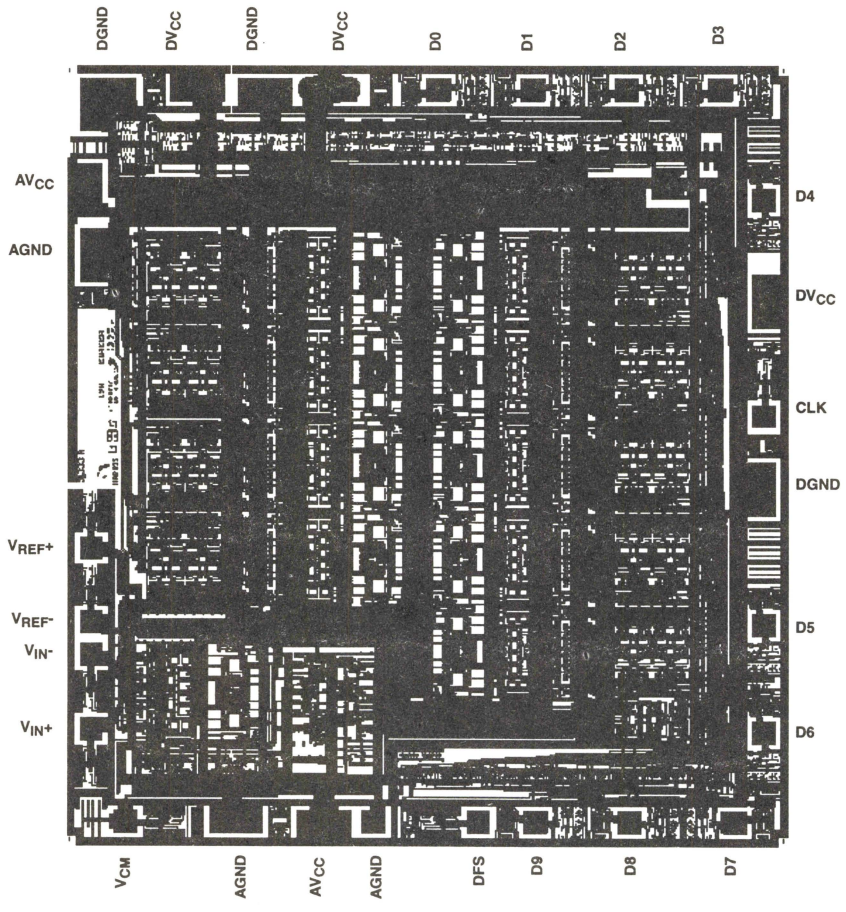
4514

DIE DIMENSIONS:

Silver Filled Epoxy

Metallization Mask Layout

HI5702



August 1997

10-Bit, 40 MSPS A/D Converter

Features

- Sampling Rate . . . . . 40 MSPS
- 8.55 Bits Guaranteed at f_{IN} = 10MHz
- Low Power
- Wide Full Power Input Bandwidth 250MHz
- On Chip Sample and Hold
- Fully Differential or Single-Ended Analog Input
- Single Supply Voltage . . . . . +5V
- TTL Compatible Interface
- 3.3V Digital Outputs Available

Applications

- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition
- Additional Reference Documents
  - AN9534 Using the HI5703 Evaluation Board
  - AN9413 Driving the Analog Input of the HI5702
  - AN9214 Using Harris High Speed A/D Converters

Description

The HI5703 is a monolithic, 10-bit, analog-to-digital converter fabricated in Harris's BiCMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 MSPS speed is made possible by a fully differential pipeline architecture with an internal sample and hold.

The HI5703 has excellent dynamic performance while consuming only 400mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles. It is pin-to-pin compatible with the HI5702.

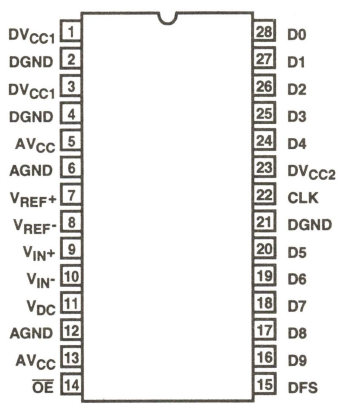
For lower power consumption or internal reference, please refer to the HI5746 or HI5767.

Ordering Information

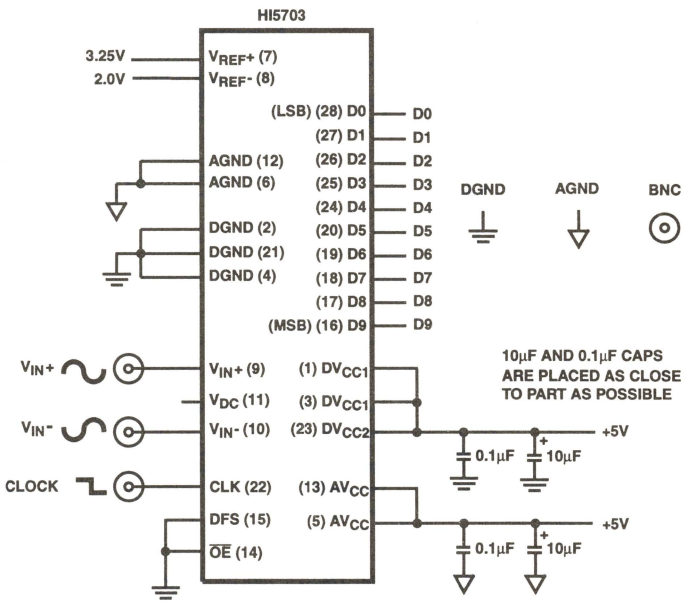
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI5703KCB	0 to 70	28 Ld SOIC (W)	M28.3
HI5703EVAL	25	Evaluation Board	

Pinout

HI5703
(SOIC)
TOP VIEW

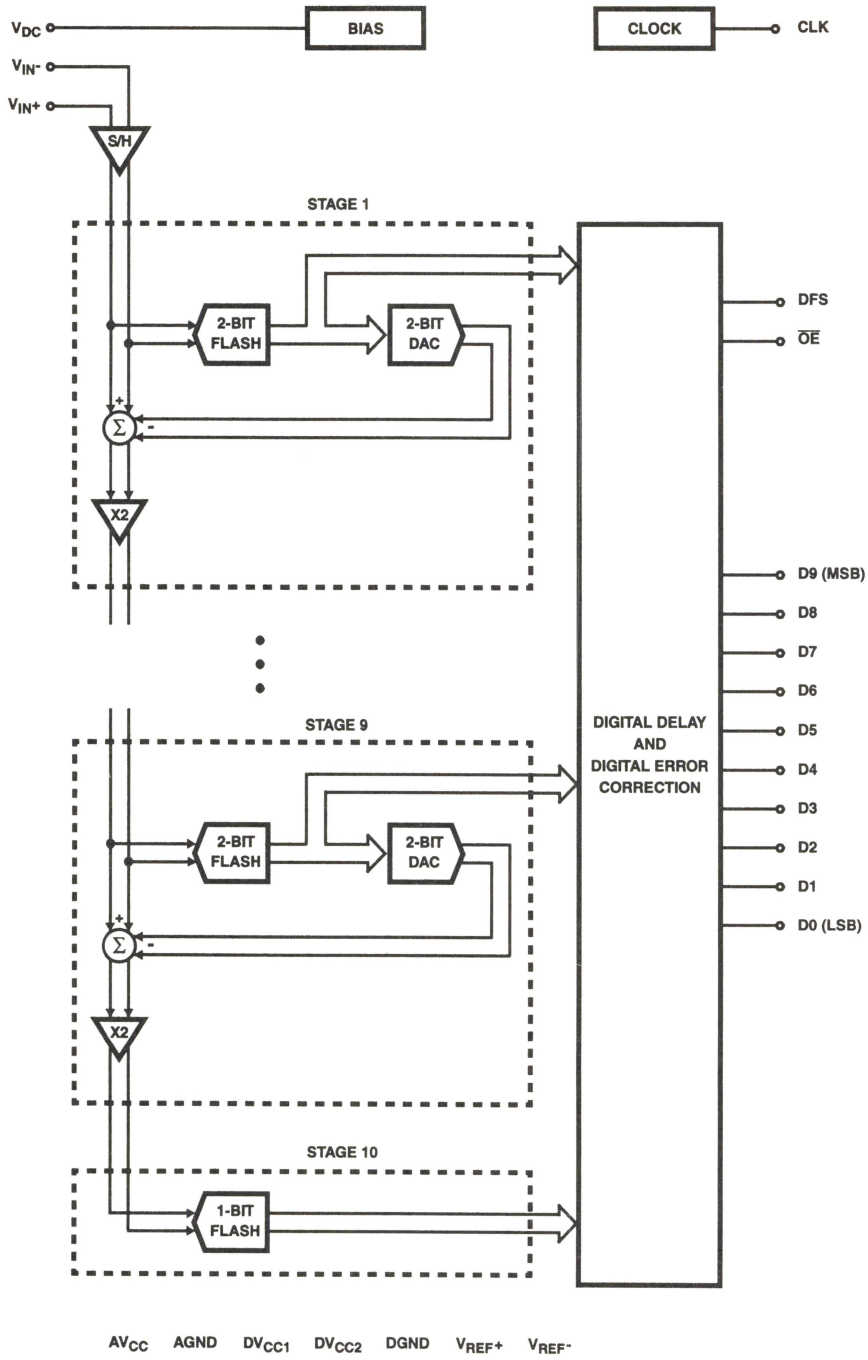


Typical Application Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND . . . . . +6V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{CC}
Analog I/O Pins . . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range, HI5703KCB . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	70

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2.0V$; $f_S = 40$ MSPS at 50% Duty Cycle; $C_L = 20pF$; $T_A = 25^oC$; Differential Analog Input; Unless Otherwise Specified

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±1	±2.0	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1	LSB
Offset Error, V_{OS}	f_{IN} = DC	-	4	-	LSB
Full Scale Error, FSE	f_{IN} = DC	-	1	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	1	MSPS
Maximum Conversion Rate	No Missing Codes	40	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	-	9.2	-	Bits
	f_{IN} = 5MHz	-	9.2	-	Bits
	f_{IN} = 10MHz	8.55	8.9	-	Bits
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	57	-	dB
	f_{IN} = 5MHz	-	57	-	dB
	f_{IN} = 10MHz	53.2	55	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	-	58	-	dB
	f_{IN} = 5MHz	-	58	-	dB
	f_{IN} = 10MHz	53.2	57	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-	-64	-	dBc
	f_{IN} = 5MHz	-	-63	-	dBc
	f_{IN} = 10MHz	-	-60	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-75	-	dBc
	f_{IN} = 5MHz	-	-75	-	dBc
	f_{IN} = 10MHz	-	-73	-	dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-66	-	dBc
	f_{IN} = 5MHz	-	-64	-	dBc
	f_{IN} = 10MHz	-	-63	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz	-	66	-	dBc
	f_{IN} = 5MHz	-	64	-	dBc
	f_{IN} = 10MHz	54	63	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	-59	-	dBc
Differential Gain Error	f_S = 17.72MHz, 6 Step, Mod Ramp	-	0.5	-	%
Differential Phase Error	f_S = 17.72MHz, 6 Step, Mod Ramp	-	0.1	-	Degree
Transient Response		-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive	-	1	-	Cycle

Electrical Specifications $AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2.0V$; $f_S = 40$ MSPS at 50% Duty Cycle; $C_L = 20pF$; $T_A = 25^oC$; Differential Analog Input; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range ($V_{IN+} - V_{IN-}$)		-	±1.25	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	2.5	-	V
Analog Input Resistance, R_{IN}	(Note 3)	-	1	-	MΩ
Analog Input Capacitance, C_{IN}		-	7	-	pF
Analog Input Bias Current, I_{B+} or I_{B-}	(Note 3)	-10	-	+10	µA
Differential Analog Input Bias Current $I_{B\ DIFF} = (I_{B+} - I_{B-})$		-	±0.5	-	µA
Analog Input Common Mode Voltage Range $(V_{IN+} + V_{IN-}) / 2$	Differential Mode (Note 1)	0.625	-	4.375	V
Full Power Input Bandwidth (FPBW)		-	250	-	MHz
REFERENCE INPUT					
Total Reference Resistance, R_L		300	400	500	Ω
Reference Current		2.5	3.125	4.2	mA
Positive Reference Voltage Input, $V_{REF}+$	(Note 2)	-	3.25	3.3	V
Negative Reference Voltage Input, $V_{REF}-$	(Note 2)	1.95	2.0	-	V
Reference Common Mode Voltage $(V_{REF}+ + V_{REF}-) / 2$	(Note 2)	2.575	2.625	2.675	V
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	2.8	-	V
Max Output Current		-	-	1	mA
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	$V_{IH} = 5V$	-	-	10.0	µA
Input Logic Low Current, I_{IL}	$V_{IL} = 0V$	-	-	10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS					
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$; $DV_{CC2} = 5V$	1.6	-	-	mA
Output Logic Source Current, I_{OH}	$V_O = 2.4V$; $DV_{CC2} = 5V$	-0.2	-	-	mA
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/5V$; $DV_{CC2} = 5V$	-	±1	±10	µA
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$; $DV_{CC2} = 3.3V$	1.6	-	-	mA
Output Logic Source Current, I_{OH}	$V_O = 2.4V$; $DV_{CC2} = 3.3V$	-0.2	-	-	mA
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/3.3V$; $DV_{CC2} = 3.3V$	-	±1	±10	µA
Output Capacitance, C_{OUT}		-	5	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps
Data Output Delay, t_{OD}		-	7	-	ns
	$AV_{CC} = DV_{CC1} = 5V$ ±10%, $DV_{CC2} = 3.3V$ ±5%, $0^oC \le T_A \le 70^oC$	5	7	18	ns
Data Output Hold, t_H		-	4	-	ns
Data Output Enable Time, t_{EN}		-	7	-	ns
Data Output Enable Time, t_{DIS}		-	7	-	ns
Clock Pulse Width (Low)	40 MSPS Clock	11.875	12.5	13.125	ns
Clock Pulse Width (High)	40 MSPS Clock	11.875	12.5	13.125	ns

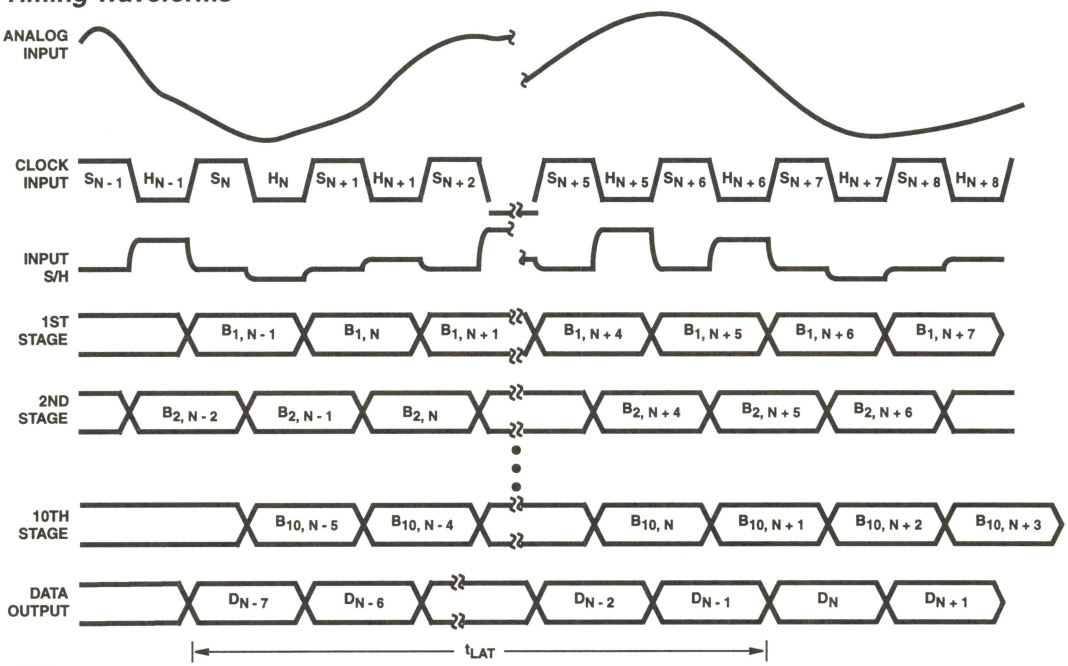
Electrical Specifications $AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2.0V$; $f_S = 40$ MSPS at 50% Duty Cycle; $C_L = 20pF$; $T_A = 25^oC$; Differential Analog Input; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	7	Cycles
Power-Up Initialization	Data Invalid Time (Note 2)	-	-	20	Cycles
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, AV_{CC}		4.75	5.0	5.25	V
Digital Supply Voltage, DV_{CC1}		4.75	5.0	5.25	V
Digital Output Supply Voltage, DV_{CC2}	At 3.30V	3.135	3.3	3.465	V
	At 5.0V	4.75	5.0	5.25	V
Total Supply Current, I_{CC}	$V_{IN}+ - V_{IN}- = +1.25V$ and DFS = "0"	-	80	-	mA
Analog Supply Current, AI_{CC}	$V_{IN}+ - V_{IN}- = +1.25V$ and DFS = "0"	-	48	-	mA
Digital Supply Current, DI_{CC1}	$V_{IN}+ - V_{IN}- = +1.25V$ and DFS = "0"	-	30	-	mA
Digital Output Supply Current, DI_{CC2}	$V_{IN}+ - V_{IN}- = +1.25V$ and DFS = "0"	-	2	-	mA
Power Dissipation	$V_{IN}+ - V_{IN}- = +1.25V$ and DFS = "0"	-	400	-	mW
Offset Error Sensitivity, ΔV_{OS}	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±1.5	-	LSB
Full Scale Error Sensitivity, ΔFSE	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±0.2	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock low and DC input.

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M, N}$: M-th stage digital output corresponding to N-th sampled input.
7. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5703 INTERNAL CIRCUIT TIMING

Timing Waveforms (Continued)

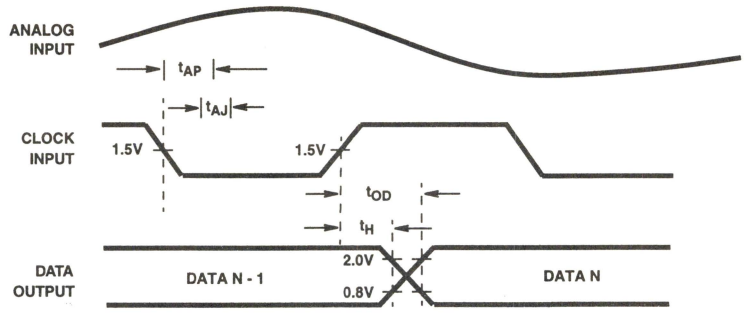


FIGURE 2. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

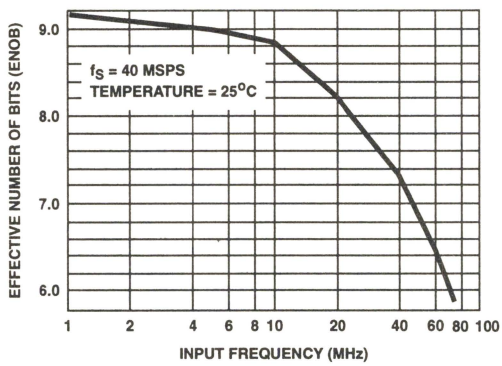
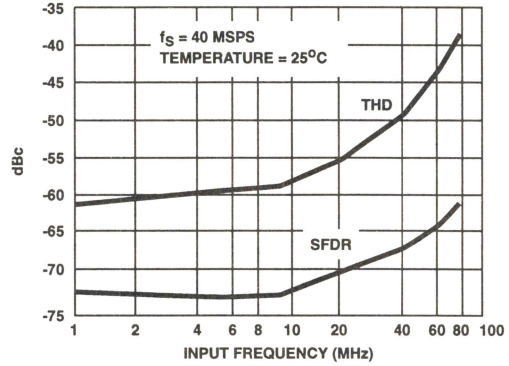


FIGURE 3. EFFECTIVE NUMBER OF BITS (ENOB) vs INPUT FREQUENCY



NOTE: SFDR depicted here does not include any harmonic distortion.

FIGURE 4. TOTAL HARMONIC DISTORTION (THD) AND SPURIOUS FREE DYNAMIC RANGE (SFDR) vs INPUT FREQUENCY

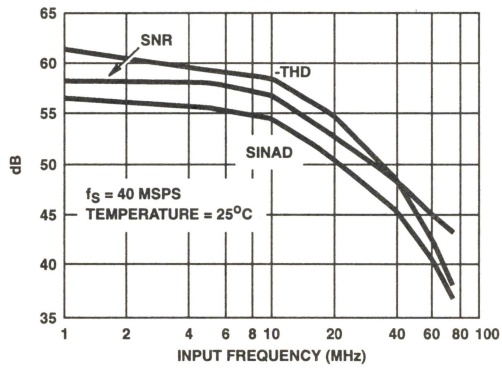


FIGURE 5. SINAD, SNR, AND -THD vs INPUT FREQUENCY

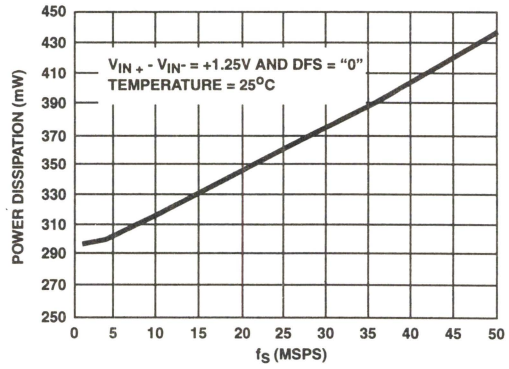


FIGURE 6. POWER DISSIPATION vs SAMPLE FREQUENCY

Typical Performance Curves (Continued)

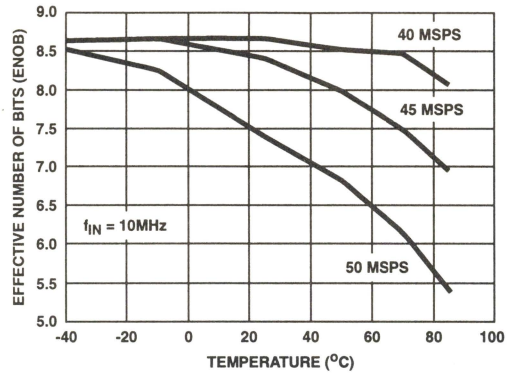


FIGURE 7. EFFECTIVE NUMBER OF BITS (ENOB) vs TEMPERATURE AND SAMPLE FREQUENCY

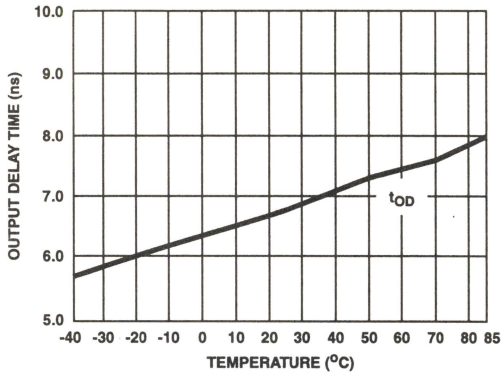


FIGURE 8. OUTPUT DELAY TIME (T_{OD}) vs TEMPERATURE

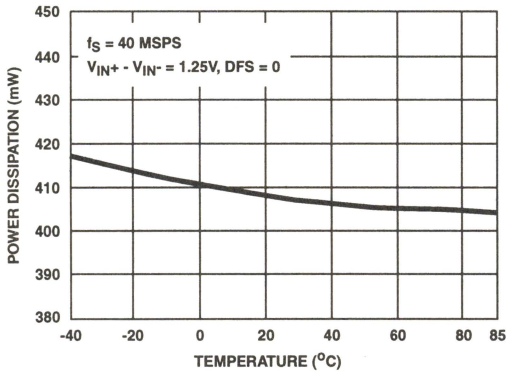


FIGURE 9. POWER DISSIPATION vs TEMPERATURE

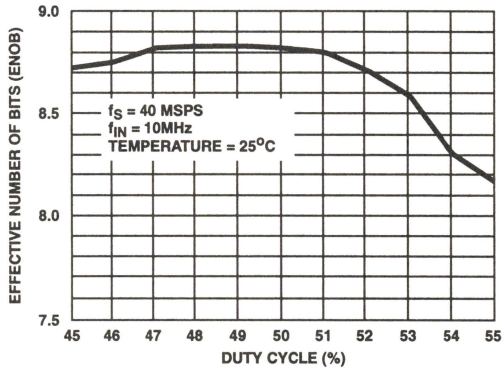


FIGURE 10. EFFECTIVE NUMBER OF BITS (ENOB) vs DUTY CYCLE (T_H/T_{TOTAL})

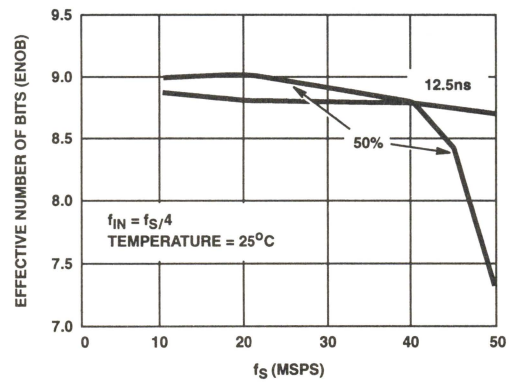


FIGURE 11. EFFECTIVE NUMBER OF BITS (ENOB) vs SAMPLE FREQUENCY

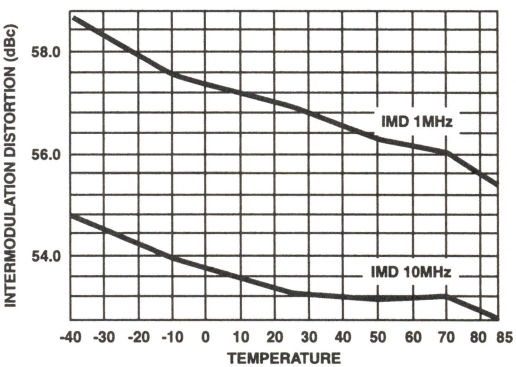


FIGURE 12. INTERMODULATION DISTORTION (IMD) vs TEMPERATURE

Typical Performance Curves (Continued)

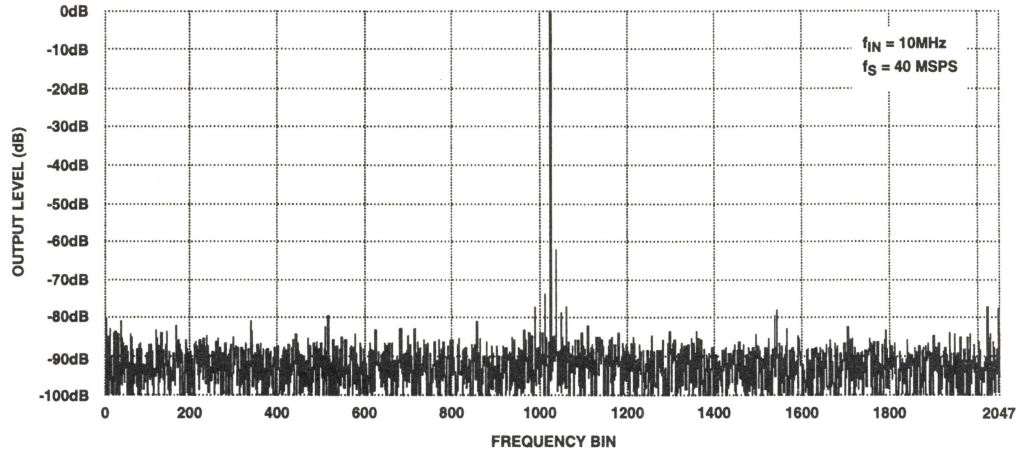


FIGURE 13. 4096 POINT FFT SPECTRAL PLOT

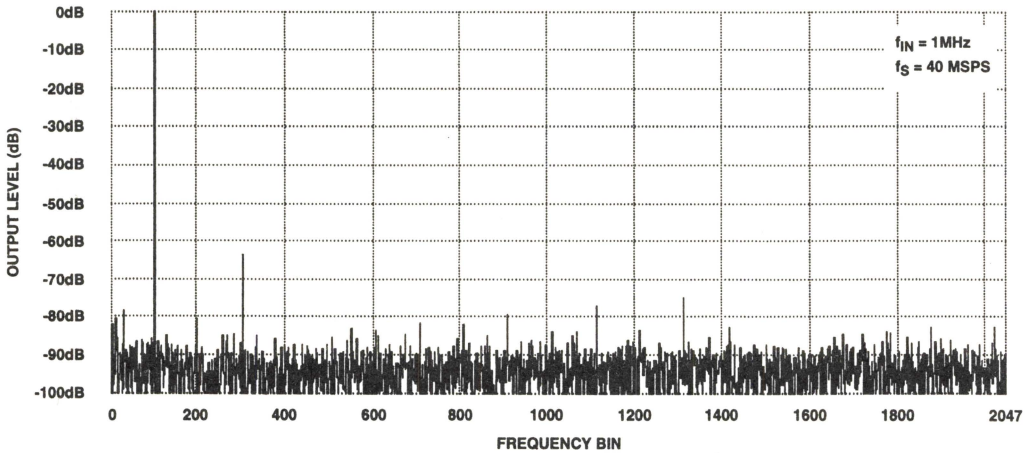


FIGURE 14. 4096 POINT FFT SPECTRAL PLOT

TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	DV_{CC1}	Digital Supply (+5.0V)
2	DGND	Digital Ground
3	DV_{CC1}	Digital Supply (+5.0V)
4	DGND	Digital Ground
5	AV_{CC}	Analog Supply (+5.0V)
6	AGND	Analog Ground
7	$V_{REF}+$	Positive Reference Voltage Input
8	$V_{REF}-$	Negative Reference Voltage Input
9	$V_{IN}+$	Positive Analog Input
10	$V_{IN}-$	Negative Analog Input
11	V_{DC}	DC Bias Voltage Output
12	AGND	Analog Ground
13	AV_{CC}	Analog Supply (+5.0V)
14	$\overline{OE}$	Digital Output Enable Control Input
15	DFS	Data Format Select Input
16	D9	Data Bit 9 Output (MSB)
17	D8	Data Bit 8 Output
18	D7	Data Bit 7 Output
19	D6	Data Bit 6 Output
20	D5	Data Bit 5 Output
21	DGND	Digital Ground
22	CLK	Sample Clock Input
23	DV_{CC2}	Digital Output Supply (+3.3V to +5V)
24	D4	Data Bit 4 Output
25	D3	Data Bit 3 Output
26	D2	Data Bit 2 Output
27	D1	Data Bit 1 Output
28	D0	Data Bit 0 Output (LSB)

Detailed Description

Theory of Operation

The HI5703 is a 10-bit fully differential sampling pipeline A/D converter with digital error correction. Figure 15 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

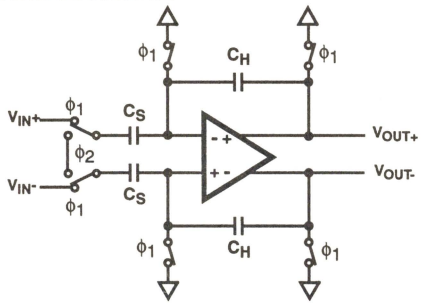


FIGURE 15. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, nine identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the tenth stage being a one bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The two-bit digital output of each stage is fed to a digital delay line controlled by the internal clock. The purpose of the delay line is to align the digital output data to the corresponding sampled analog input signal. This delayed data is fed to the digital error correction circuit which corrects the error in the output data with the information contained in the redundant bits to form the final ten bit output for the converter.

Because of the pipeline nature of this converter, the data on the bus is output at the 7th cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The output data is synchronized to the external clock by a double buffered latching technique.

The digital output bits are available in offset binary or two's complement format, the format being set by the Data Format Select (DFS) input.

Reference Voltage Inputs, $V_{REF}-$ and $V_{REF}+$

The HI5703 requires two reference voltages connected to the V_{REF} pins. The HI5703 is tested with $V_{REF}-$ equal to 2V and $V_{REF}+$ equal to 3.25V for a fully differential input voltage range of ±1.25V. $V_{REF}+$ and $V_{REF}-$ can differ from the above voltages as long as the reference common mode voltage, $((V_{REF}+ + V_{REF}-)/2)$, does not exceed 2.625V ±50mV and the limits on $V_{REF}+$ and $V_{REF}-$ are not exceeded.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference voltage input pins, $V_{REF}+$ and $V_{REF}-$.

Analog Input, Differential Connection

The analog input to the HI5703 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 16 and Figure 17) will give the best performance for the converter.

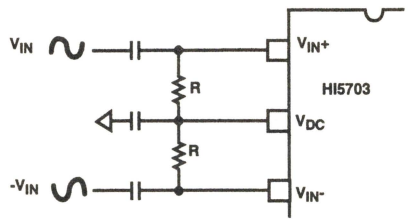


FIGURE 16. AC COUPLED DIFFERENTIAL INPUT

Since the HI5703 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V. For the differential input connection this implies the analog input common mode voltage can range from 0.625V to 4.375V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A DC voltage source, V_{DC}, equal to 2.8V (typical), is made available to the user to help simplify circuit design when using an AC coupled differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the analog input common mode voltage range over temperature. It has a temperature coefficient of approximately +200ppm/^{o}C.

For the AC coupled differential input (Figure 16) assume the difference between V_{REF+}, typically 3.25V, and V_{REF-}, typically 2V, is 1.25V. Fullscale is achieved when the V_{IN+} and V_{IN-} inputs are $1.25V_{P-P}$, with V_{IN-} being 180 degrees out of phase with V_{IN+}. The converter will be at positive fullscale when the V_{IN+} input is at V_{DC} + 0.625V and V_{IN-} is at V_{DC} - 0.625V (V_{IN+} - V_{IN-} = 1.25V). Conversely, the converter will be at negative full scale when the V_{IN+} input is equal to V_{DC} - 0.625V and V_{IN-} is at V_{DC} + 0.625V (V_{IN+} - V_{IN-} = -1.25V).

The analog input can be DC coupled (Figure 17) as long as the inputs are within the analog input common mode voltage range (0.625V ≤ VDC ≤ 4.375V).

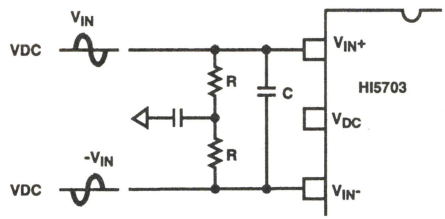


FIGURE 17. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 17 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from V_{IN+} to V_{IN-} will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

Analog Input, Single-Ended Connection

The configuration shown in Figure 18 may be used with a single ended AC coupled input.

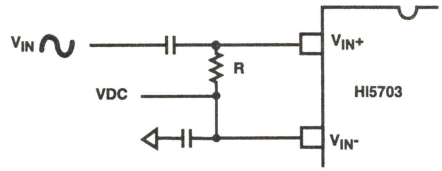


FIGURE 18. AC COUPLED SINGLE ENDED INPUT

Again, assume the difference between V_{REF+}, typically 3.25V, and V_{REF-}, typically 2V, is 1.25V. If V_{IN} is a $2.5V_{P-P}$ sinewave, then V_{IN+} is a $2.5V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive fullscale when V_{IN+} is at VDC + 1.25V and will be at negative fullscale when V_{IN+} is equal to VDC - 1.25V. Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND. In this case, VDC could range between 1.25V and 3.75V without a significant change in ADC performance. The simplest way to produce VDC is to use the V_{DC} output of the HI5703.

The single ended analog input can be DC coupled (Figure 19) as long as the input is within the analog input common mode voltage range.

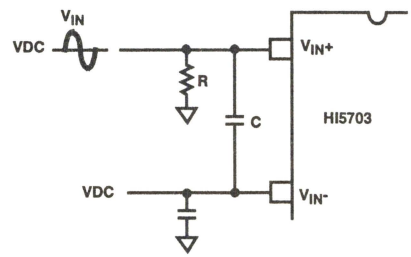


FIGURE 19. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 19 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from V_{IN+} to V_{IN-} will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

A single ended source may give better overall system performance if it is first converted to differential before driving the HI5703. Refer to the application notes AN9534, "Using the HI5703 Evaluation Board", and AN9413, "Driving the Analog Input of the HI5702". Application note AN9413

applies to the HI5703 as well as the HI5702 and describes several different ways of driving the analog differential inputs.

Digital Output Control and Clock Requirements

The HI5703 provides a standard high-speed interface to external TTL logic families.

In order to ensure rated performance of the HI5703, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5703 will only be guaranteed at conversion rates above 1 MSPS. This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1 MSPS will have to be performed before valid data is available.

A Data Format Select (DFS) pin is provided which will determine the format of the digital data outputs. When at logic low, the data will be output in offset binary format. When at logic high, the data will be output in two's complement format. Refer to Table 2 for further information.

The output enable pin, $\overline{OE}$, when pulled high will three-state the digital outputs to a high impedance state. Set the $\overline{OE}$ input to logic low for normal operation.

$\overline{OE}$ INPUT	DIGITAL DATA OUTPUTS
0	Active
1	High Impedance

Supply and Ground Considerations

The HI5703 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The digital data outputs also have a separate supply pin, DV_{CC2}, which can be powered from a 3.3V to 5.0V supply. This allows the outputs to interface with 3.3V logic if so desired.

The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5703 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the application notes "Using Harris High Speed A/D Converters" (AN9214) for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$ LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is $^3/_4$ LSB below positive Fullscale (+FS) with the offset error removed. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Sensitivity

Each of the power supplies are moved plus and minus 5% and the shift in the offset and full scale error (in LSBs) is noted.

TABLE 2. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE ($V_{IN}+ - V_{IN}-$)	OFFSET BINARY OUTPUT CODE (DFS LOW)										TWO'S COMPLEMENT OUTPUT CODE (DFS HIGH)									
		MSB									LSB	MSB									LSB
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) - $^1/_4$ LSB	1.24939V	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
+FS - $1^1/_4$ LSB	1.24695V	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
+$^3/_4$ LSB	1.83mV	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-$^1/_4$ LSB	-0.610mV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-FS + $1^3/_4$ LSB	-1.24573V	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + $^3/_4$ LSB	-1.24817V	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

NOTE:

8. The voltages listed above represent the ideal center of each output code shown as a function of the reference voltage.
9. $V_{REF}+ = 3.25V$ and $V_{REF}- = 2.0V$.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5703. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

where: $V_{CORR} = 0.5$ dB

V_{CORR} adjusts the ENOB for the amount the input is below fullscale.

Signal To Noise and Distortion Ratio (SINAD)

SINAD is the ratio of the measured RMS signal to RMS sum of all the other spectral components below the Nyquist frequency, $f_S/2$, excluding DC.

Signal To Noise Ratio (SNR)

SNR is the ratio of the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components below $f_S/2$ excluding the fundamental, the first five harmonics and DC.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spectral component in the spectrum below $f_S/2$.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present at the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are (f_1+f_2), (f_1-f_2), $(2f_1)$, $(2f_2)$, $(2f_1+f_2)$, $(2f_1-f_2)$, (f_1+2f_2), (f_1-2f_2). The ADC is tested with each tone 6dB below full scale.

Transient Response

Transient response is measured by providing a full scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Over-Voltage Recovery

Over-Voltage Recovery is measured by providing a full scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the analog input frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has an amplitude which swings from -FS to +FS. The bandwidth given is measured at the specified sampling frequency.

Video Definitions

Differential Gain and Differential Phase are two commonly found video specifications for characterizing the distortion of a chrominance signal as it is offset through the input voltage range of an ADC.

Differential Gain (DG)

Differential Gain is the peak difference in chrominance amplitude (in percent) relative to the reference burst.

Differential Phase (DP)

Differential Phase is the peak difference in chrominance phase (in degrees) relative to the reference burst.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the digital data is output on the bus at the 7th cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input sample by 7 cycles.

Power-Up initialization

This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.

HFA1100	HI5702	HSP9501	HI5780	HA5020
HFA1105	HI5703	HSP48410	HI1171	HA2842
HFA1106		HSP48908	CA3338	HFA1115
HFA1135		HSP48212		HFA1212
HFA1145		HSP43891		HFA1412
HFA1245		HSP43168		
		HSP43216		

HFA1100: 850MHz Video Op Amp
HFA1105: 300MHz Video Op Amp
HFA1106: 250MHz Video Op Amp with Bandwidth Limit Control
HFA1135: 350MHz Video Op Amp with Output Limiting
HFA1145: 300MHz Video Op Amp with Output Disable
HFA1245: Dual 350MHz Video Op Amp with Output Disable
HI5702: 10-Bit, 40 MSPS, A/D Converter
HI5703: 10-Bit, 40 MSPS, Low Power A/D Converter
HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48212: Digital Video Mixer
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HI5780: 10-Bit, 80 MSPS, Video D/A Converter
HI1171: 8-Bit, 40 MSPS, Video D/A Converter
CA3338: 8-Bit, 50 MSPS, Video D/A Converter
HA5020: 100MHz Video Op Amp
HA2842: High Output Current, Video Op Amp
HFA1115: 225MHz Programmable Gain Video Buffer with Output Limiting
HFA1212: 350MHz, Dual Programmable Gain Video Buffer
HFA1412: 350MHz, Quad Programmable Gain Video Buffer

In addition, CMOS Logic Families in HC/HCT, AC/ACT, FCT and CD4000 are available.

FIGURE 20. 10-BIT VIDEO IMAGING COMPONENTS

HFA1100	HI5702	HSP43168	HI5721	HFA1112
HFA1110	HI5703	HSP43216	HI5780	HFA1113
HFA3101		HSP43220	HI20201	
HFA3102		HSP43891	HI20203	
HFA3600		HSP50016		
		HSP50110		
		HSP50210		

HFA1100: 850MHz Op Amp
HFA1110: 750MHz Unity Gain Video Buffer
HFA3101: Gilbert Cell Transistor Array
HFA3102: Dual Long-Tailed Pair Transistor Array
HFA3600: Low Noise Amplifier/Mixer
HI5702: 10-Bit, 40 MSPS, A/D Converter
HI5703: 10-Bit, 40 MSPS, Low Power A/D Converter
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HSP43220: Decimating Digital Filter
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP50016: Digital Down Converter
HSP50110: Digital Quadrature Tuner
HSP50210: Digital Costas Loop
HI5721: 10-Bit, 100 MSPS, Communications D/A Converter
HI5780: 10-Bit, 80 MSPS, D/A Converter
HI20201: 10-Bit, 160 MSPS, High Speed D/A Converter
HI20203: 8-Bit, 160 MSPS, High Speed D/A Converter
HFA1112: 850MHz Programmable Gain Video Buffer
HFA1113: 850MHz Programmable Gain Video Buffer with Output Limiting

In addition, CMOS Logic Families in HC/HCT, AC/ACT, FCT and CD4000 are available.

FIGURE 21. 10-BIT COMMUNICATIONS COMPONENTS

HARRIS SEMICONDUCTOR

HI5710A

August 1997

10-Bit, 20 MSPS A/D Converter

Features

- Resolution ±0.5 LSB (DNL) 10-Bit
- Maximum Sampling Frequency . . . . . 20 MSPS
- Low Power Consumption (Reference Current Excluded) 150mW
- Standby Mode Power 5mW
- No Sample and Hold Required
- TTL Compatible Inputs
- Three-State TTL Compatible Outputs
- Single +5V Analog Power Supply
- Single +3.3V or +5V Digital Power Supply

Applications

- Video Digitizing - Multimedia
- Data Communications
- Image Scanners
- Medical Imaging
- Video Recording Equipment
- Camcorders
- QAM Demodulation

Description

The HI5710A is a low power, 10-bit, CMOS analog-to-digital converter. The use of a 2-step architecture realizes low power consumption, 150mW, and a maximum conversion speed of 20MHz with only a 3 clock cycle data latency. The HI5710A can be powered down, disabling the chip and the digital outputs, reducing power to less than 5mW. A built-in, user controllable, calibration circuit is used to provide low linearity error, 1 LSB. The low power, high speed and small package outline make the HI5710A an ideal choice for CCD, battery, and high channel count applications.

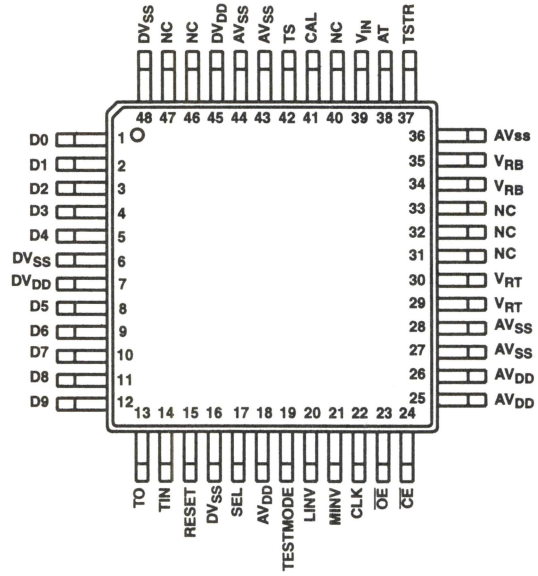
The HI5710A does not require an external sample and hold but requires an external reference and includes force and sense reference pins for increased accuracy. The digital outputs can be inverted, with the MSB controlled separately, allowing for various digital output formats. The HI5710A includes a test mode where the digital outputs can be set to a fixed state to ease in-circuit testing.

Ordering Information

PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5710AJCQ	-20 to 75	48 Ld MQFP	Q48.7x7-S

Pinout

HI5710A (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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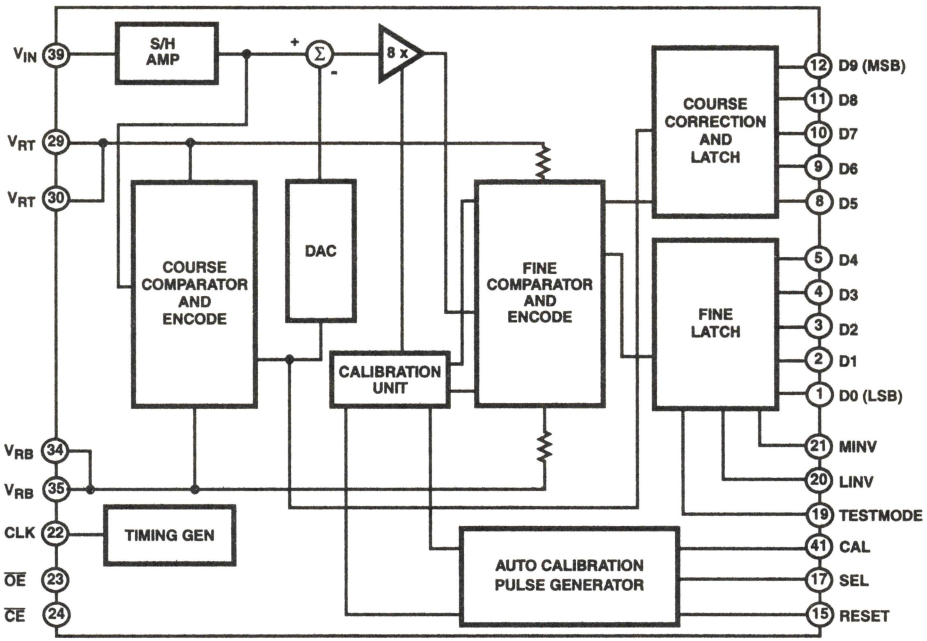
File Number 3921.5

Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{DD}, DV_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Analog Input Voltage, V_{IN} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Digital Input Voltage, V_{IH}, V_{IL} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Digital Output Voltage, V_{OH}, V_{OL} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP Package 111
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range, T_{STG} . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

Operating Conditions

Supply Voltage
AV_{DD}, AV_{SS} . . . . . +5V ±0.25V
DV_{DD}, DV_{SS} . . . . . +3.3V to 5V ±0.25V
|DGND-AGND| . . . . . .0mV to 100mV
Reference Input Voltage
V_{RB} . . . . . .1.8V to 2.8V
V_{RT} . . . . . .3.6V to 4.6V
Analog Input Range, V_{IN} . . . . . (V_{RT} - V_{RB}) (1.8V_{P-P} to 2.8V_{P-P})
Clock Pulse Width
t_{PW1} . . . . . .25ns (Min)
t_{PW0} . . . . . .25ns (Min)
Temperature, T_A . . . . . -20°C to 75°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications f_C = 20 MSPS, AV_{DD} = +5V, DV_{DD} = +3.3V, V_{RB} = 2.0V, V_{RT} = 4.0V, $T_A = 25^oC$ (Note 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE						
Offset Voltage	E_{OT}		40	90	140	mV
	E_{OB}		-120	-70	-20	mV
Integral Non-Linearity, INL		V_{IN} = 2.0V to 4.0V	-	±1.3	±2.0	LSB
Differential Non-Linearity, DNL			-	±0.5	±1.0	LSB
DYNAMIC CHARACTERISTICS						
Maximum Conversion Speed, f_C		f_{IN} = 1kHz Ramp	20	-	-	MSPS
Minimum Conversion Speed, f_C			-	-	0.5	MSPS
Effective Number of Bits, ENOB		f_{IN} = 3MHz	-	8.7	-	Bits
Signal to Noise and Distortion, SINAD		f_{IN} = 100kHz	-	53	-	dB
		f_{IN} = 500kHz	-	52	-	dB
		f_{IN} = 1MHz	-	53	-	dB
		f_{IN} = 3MHz	-	54	-	dB
		f_{IN} = 7MHz	-	47	-	dB
		f_{IN} = 10MHz	-	45	-	dB
Spurious Free Dynamic Range, SFDR		f_{IN} = 100kHz	-	60	-	dB
		f_{IN} = 500kHz	-	59	-	dB
		f_{IN} = 1MHz	-	60	-	dB
		f_{IN} = 3MHz	-	65	-	dB
		f_{IN} = 7MHz	-	50	-	dB
		f_{IN} = 10MHz	-	49	-	dB
Differential Gain Error, DG		NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS	-	1.0	-	%
Differential Phase Error, DP			-	0.3	-	Degree

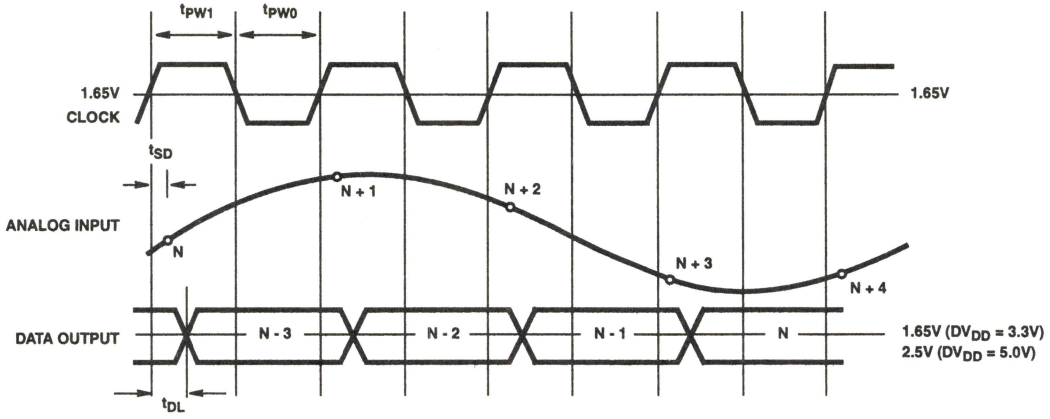
Electrical Specifications f_C = 20 MSPS, AV_{DD} = +5V, DV_{DD} = +3.3V, V_{RB} = 2.0V, V_{RT} = 4.0V, T_A = 25°C (Note 2) **(Continued)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUTS							
Analog Input Bandwidth (-3dB), BW				-	100	-	MHz
Analog Input Current		V_{IN} = 4V		-	-	50	µA
		V_{IN} = 2V		-50	-	-	µA
Analog Input Capacitance, C_{IN}		V_{IN} = 2.5V + 0.07V_{RMS}		-	9	-	pF
REFERENCE INPUT							
Reference Pin Current, I_{RT}		RESET = Low		5	7	11	mA
Reference Pin Current, I_{RB}		RESET = Low		-11	-7	-5	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}				180	280	380	Ω
DIGITAL INPUTS							
Digital Input Voltage	V_{IH}	AV_{DD} = 4.75V to 5.25V		2.3	-	-	V
	V_{IL}			-	-	0.80	V
Digital Input Current	I_{IH}	DV_{DD} = Max	V_{IH} = DV_{DD}	-	-	5	µA
	I_{IL}		V_{IL} = 0V	-	-	5	µA
DIGITAL OUTPUTS							
Digital Output Current	I_{OH}	$\overline{OE}$ = AV_{SS}, DV_{DD} = Min	V_{OH} = DV_{DD} -0.5V	3.5	-	-	mA
	I_{OL}		V_{OL} = 0.4V	3.5	-	-	mA
Digital Output Leakage Current	I_{OZH}	$\overline{OE}$ = AV_{DD}, DV_{DD} = Max	V_{OH} = DV_{DD}	-	-	1	µA
	I_{OZL}		V_{OL} = 0V	-	-	1	µA
TIMING CHARACTERISTICS							
Output Data Delay, t_{DL}		Load is One TTL Gate		8	13	18	ns
Output Enable/Disable Delay	t_{PZL}			10	15	20	ns
	t_{PLZ}			20	25	30	ns
	t_{PZH}			10	15	20	ns
	t_{PHZ}			20	25	30	ns
Sampling Delay, t_{SD}				2	4	6	ns
POWER SUPPLY CHARACTERISTIC							
Analog Supply Current, IA_{DD}		f_{IN} = 1kHz Ramp Wave Input		20	27	34	mA
Digital Supply Current, ID_{DD}				-	3	5	mA
Analog Standby Current		$\overline{CE}$ = High		-	-	1.0	mA
Digital Standby Current				-	-	1.0	µA

NOTE:

2. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams



o = INDICATES POINT AT WHICH ANALOG DATA IS SAMPLED

FIGURE 1.

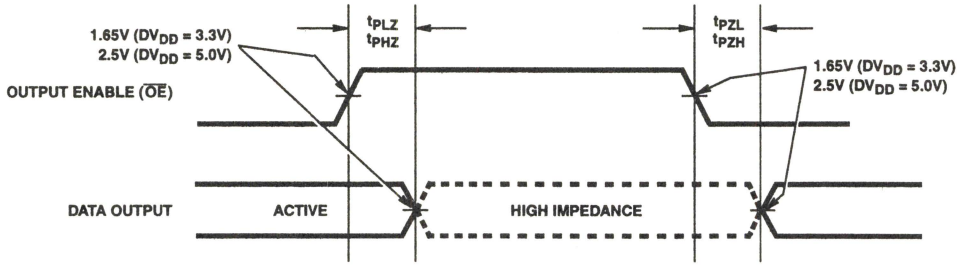


FIGURE 2.

Calibration Timing Diagrams

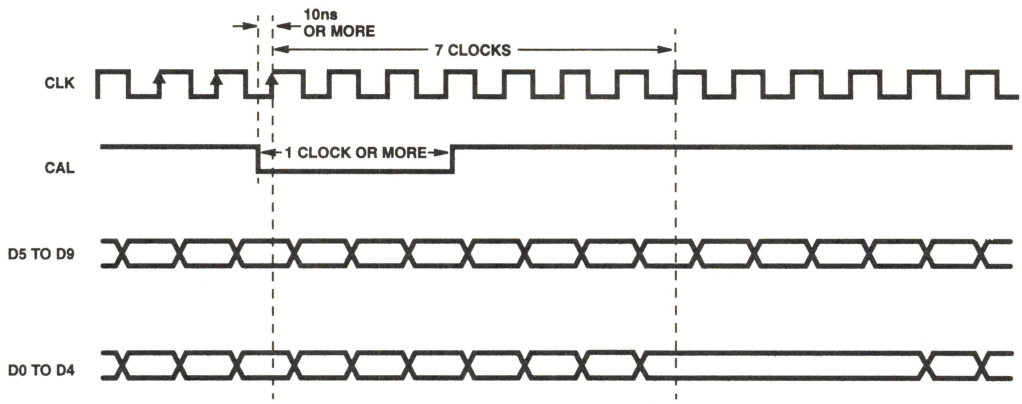


FIGURE 3. EXTERNAL CALIBRATION PULSE TIMING DIAGRAM

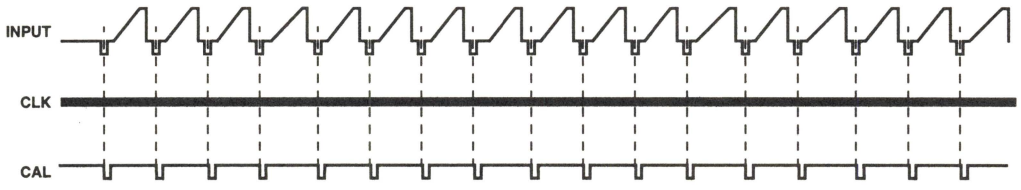


FIGURE 4A. CALIBRATION DURING H SYNC

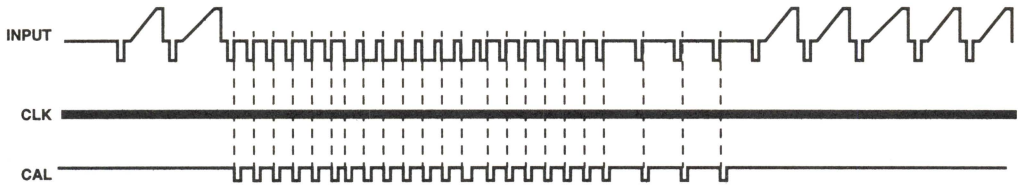


FIGURE 4B. CALIBRATION DURING V SYNC

FIGURE 4. EXAMPLES OF EXTERNAL CALIBRATION PULSE INPUT FOR VIDEO APPLICATIONS

Typical Performance Curves

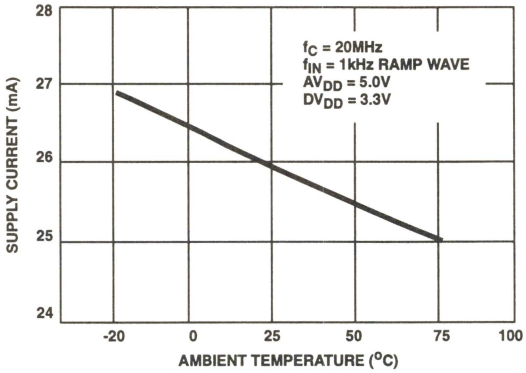


FIGURE 5. SUPPLY CURRENT vs AMBIENT TEMPERATURE

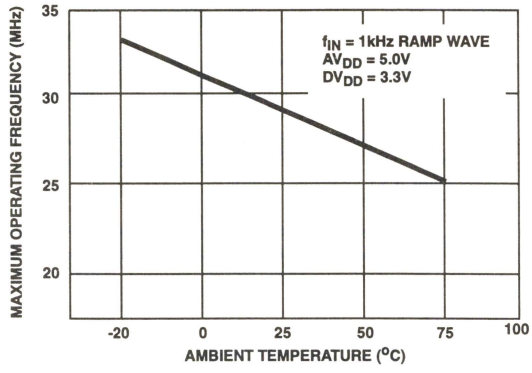


FIGURE 6. MAXIMUM OPERATING FREQUENCY vs AMBIENT TEMPERATURE

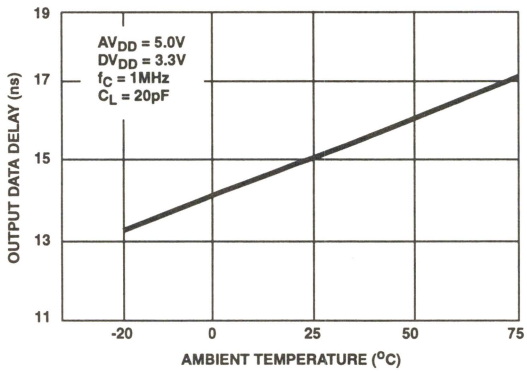


FIGURE 7. OUTPUT DATA DELAY vs AMBIENT TEMPERATURE

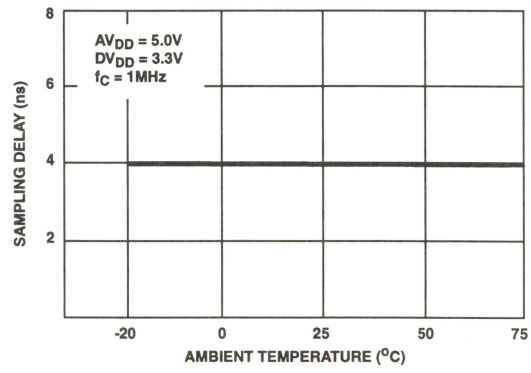


FIGURE 8. SAMPLING DELAY vs AMBIENT TEMPERATURE

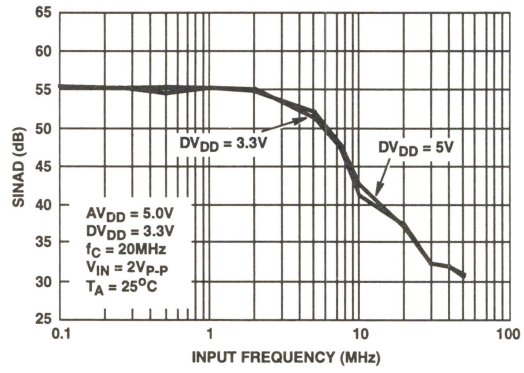


FIGURE 9. SINAD vs INPUT FREQUENCY

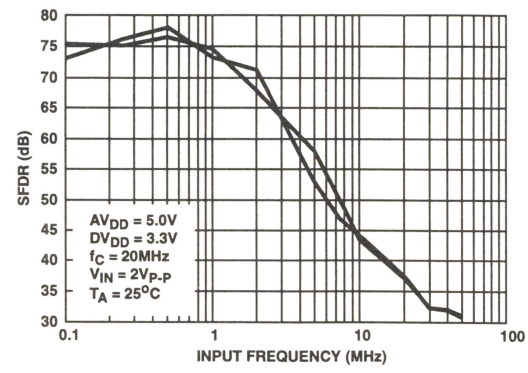


FIGURE 10. SFDR vs INPUT FREQUENCY

Typical Performance Curves (Continued)

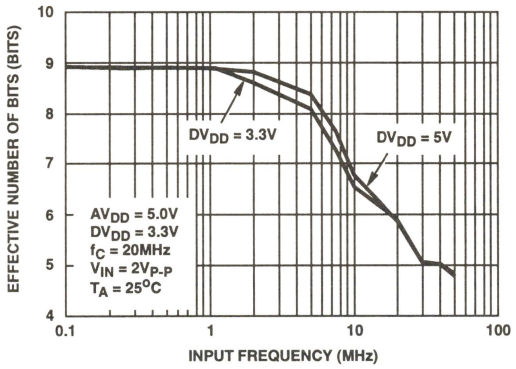


FIGURE 11. EFFECTIVE BITS vs INPUT FREQUENCY

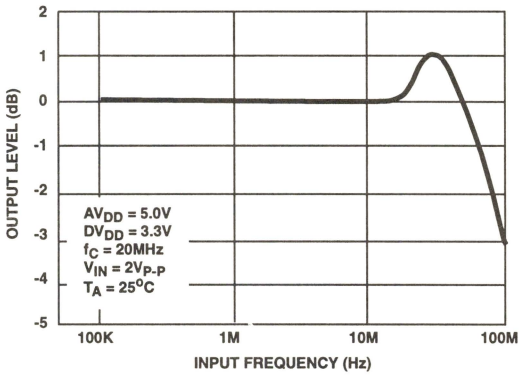


FIGURE 12. INPUT BANDWIDTH

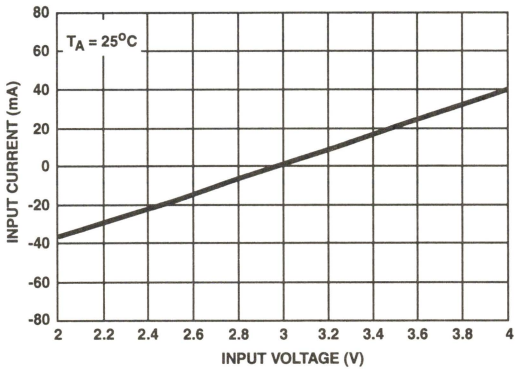


FIGURE 13. ANALOG INPUT CURRENT vs INPUT VOLTAGE

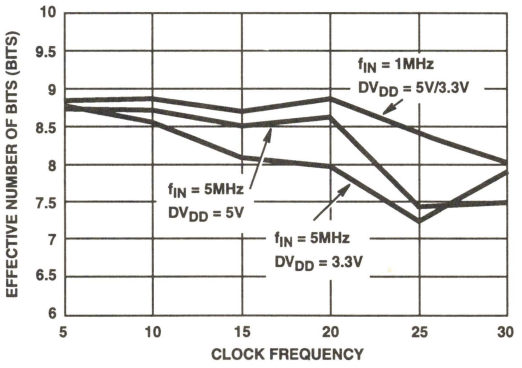


FIGURE 14. ENOB vs CLOCK FREQUENCY

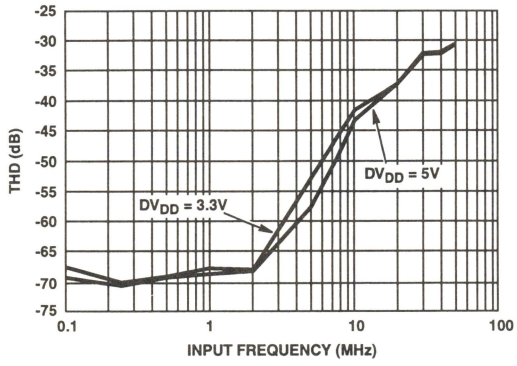


FIGURE 15. THD vs INPUT FREQUENCY

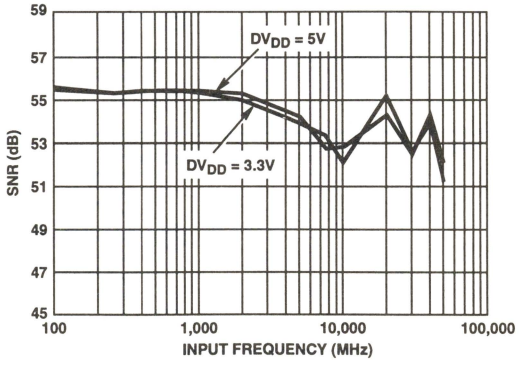
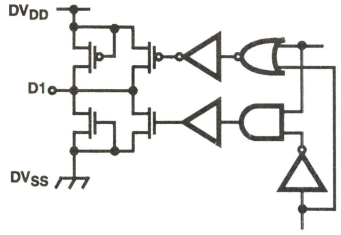
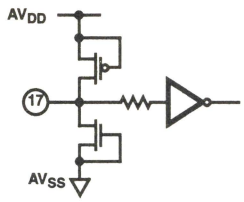
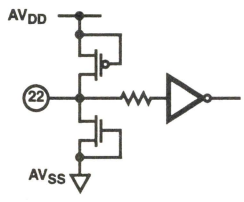
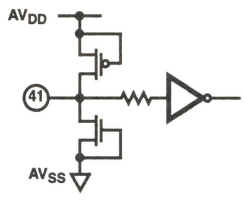
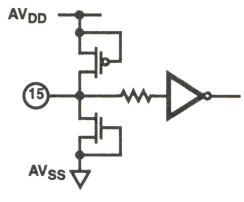
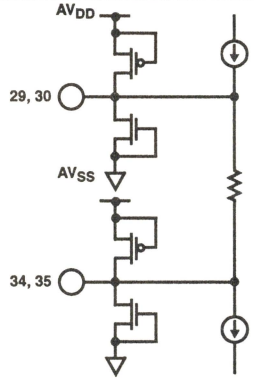
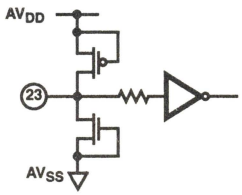
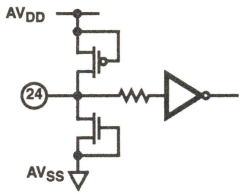
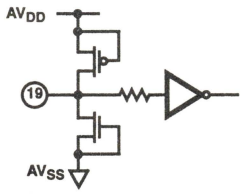
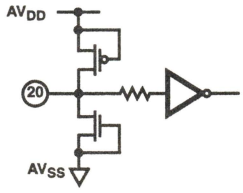


FIGURE 16. SNR vs INPUT FREQUENCY

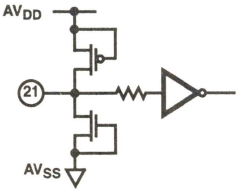
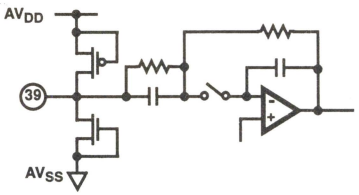
Pin Description and I/O Pin Equivalent Circuit

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 5, 8 to 12	D0 to D9		Digital Outputs: D0 (LSB) to D9 (MSB).
13	TO		Test Pin, Leave Pin Open.
7, 45	DV_{DD}		Digital V_{DD}.
6, 16, 48	DV_{SS}		Digital V_{SS}.
27, 28, 36, 43, 44	AV_{SS}		Analog V_{SS}.
17	SEL		Controls calibration input pulse selection after completion of the internal start-up calibration function. High: Selects the internal auto calibration pulse generation function Low: Selects the external calibration pulse input, CAL pin 41.
22	CLK		Clock Pin.
41	CAL		Calibration Pulse Input, calibration starts on a falling edge, normally high.
15	RESET		Calibration Circuit Reset and Internal Calibration Function Restart, resets with a negative pulse, normally high.
14	TIN		Factory Test Signal Input, normally tied to AV_{SS} or AV_{DD}.

Pin Description and I/O Pin Equivalent Circuit (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
29, 30	V_{RT}		Reference Top, normally 4.0V.
34, 35	V_{RB}		Reference Bottom, normally 2.0V.
38	AT		Factory Test Signal Output, leave pin open.
42	TS		Factory Test Signal Input, tie to AV_{DD}.
37	TSTR		Factory Test Signal Input, tie to AV_{SS}.
23	$\overline{OE}$		D0 to D9 Output Enable. Low: Outputs Enabled. High: High Impedance State.
24	$\overline{CE}$		Chip Enable. Low: Active State. High: Standby State.
19	TESTMODE		Test Mode. High: Normal Output State. Low: Output fixed.
20	LINV		Output Inversion. High: D0 to D8 are inverted. Low: D0 to D8 are normal.

Pin Description and I/O Pin Equivalent Circuit (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
21	MINV		Output Inversion. High: D9 is inverted. Low: D9 is normal.
18, 25, 26	AV_{DD}		Analog V_{DD}.
39	V_{IN}		Analog Input.

A/D OUTPUT CODE TABLE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE										
		MSB										LSB
V_{RT}	1023	1	1	1	1	1	1	1	1	1	1	1
•	•					•						
•	•					•						
•	•					•						
•	512	1	0	0	0	0	0	0	0	0	0	0
•	511	0	1	1	1	1	1	1	1	1	1	1
•	•					•						
•	•					•						
•	•					•						
V_{RB}	0	0	0	0	0	0	0	0	0	0	0	0

NOTE:

3. This table shows the correlation between the analog input voltage and the digital output code. (TESTMODE = 1, MINV and LINV= 0)

DIGITAL OUTPUT DATA FORMAT TABLE

TESTMODE	LINV	MINV	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
1	0	0	N	N	N	N	N	N	N	N	N	N
1	1	0	I	I	I	I	I	I	I	I	I	N
1	0	1	N	N	N	N	N	N	N	N	N	I
1	1	1	I	I	I	I	I	I	I	I	I	I
0	0	0	1	0	1	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0	1	0	1	0	0
0	0	1	1	0	1	0	1	0	1	0	1	1
0	1	1	0	1	0	1	0	1	0	1	0	1

NOTES:

4. This table shows the output state for the combination of TESTMODE, LINV, and MINV states.
5. N: Non-Inverted Output.
6. I: Inverted Output.

Detailed Description

The HI5710A is a two step A/D converter featuring a 5-bit upper comparator group and a 5-bit lower comparator group. A user controllable internal calibration unit is used to improve linearity.

The voltage references must be supplied externally, with V_{RB} and V_{RT} typically being set to 2.0V and 4.0V respectively.

Both chip enable and output enable pins are provided for flexibility and to reduce power consumption. The digital outputs can be inverted by control inputs LINV and MINV, where LINV controls outputs D0 through D8 and MINV controls output D9 (MSB). This allows for various digital output data formats, such as straight binary, inverted binary, offset two's complement or inverted offset two's complement.

Analog Input

The analog input typically requires a $2V_{P-P}$ full scale input signal. The full scale input can range from $1.8V_{P-P}$ to $2.8V_{P-P}$ dependent on the voltage references used.

The input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with an amplifier with sufficient bandwidth and drive capability. Op amps such as the HA5020 should make an excellent input amplifier depending on the application requirements. In order to prevent parasitic oscillation, it may be necessary to insert a resistor between the output of the amplifier and the A/D input. Be sure to consider the amplifiers settling time in CCD applications or where step inputs are expected.

Reference Input

The analog input voltage range of the A/D is set by the voltage difference between the V_{RT} and V_{RB} voltage references. The HI5710A is designed for use with external voltage references of 2.0V and 4.0V on V_{RB} and V_{RT}, respectively. The analog input voltage range of the A/D will now be from 2.0V to 4.0V. The V_{RB} voltage reference range is 1.8V to 2.8V and the V_{RT} voltage reference range is 3.6V to 4.6V. The voltage difference between the V_{RT} and V_{RB} voltage references, (V_{RT} - V_{RB}), can range from 1.8V to 2.8V.

The V_{RT} and V_{RB} voltage reference input pins must be decoupled to analog ground to minimize noise on these references. A 0.1µF capacitor is usually adequate.

Clock Input

The HI5710A samples the input signal on the rising edge of the clock with the digital data being latched at the digital outputs (D0 - D9) after 3 clock cycles. The HI5710A is designed for use with a 50% duty cycle square wave, but a 10% variation should not affect performance.

The clock input can be driven from +3.3V CMOS or +5V TTL/CMOS logic. When using a +3.3V digital supply, HC or AC CMOS logic will work well.

Digital Inputs

The digital inputs can be driven from +3.3V CMOS or +5V TTL/CMOS logic. When using a +3.3V digital supply, HC or AC CMOS logic will work well.

Digital Outputs

The digital outputs are CMOS outputs. The LINV control input will invert outputs D0 through D8 and MINV control input will invert output D9 (MSB). This allows the user to set the digital output data for a number of different digital formats. The outputs can also be three-stated by pulling the $\overline{OE}$ control input high.

The digital output supply can run from +3.3V or +5V. The digital outputs will generate less radiated noise using +3.3V, but the outputs will have less drive capability. The digital outputs will only swing to DV_{DD}, therefore exercise care if interfacing to +5V logic when using a +3.3V supply.

The digital output data can also be set to a fixed, predetermined state, through the use of the TESTMODE, LINV and MINV control input signals, see the Digital Output Data Format table. By setting the TESTMODE pin low, the outputs go to a defined digital pattern. This pattern is varied by the MINV and LINV control inputs. This feature can be used for in-circuit testing of the digital output data bus.

Calibration Function

The HI5710A has a built-in calibration unit which is designed to provide superior linearity by correcting the gain error of the subrange amplification circuitry. In addition to the calibration unit, the HI5710A provides a built-in auto calibration pulse generation function. Figure 20 shows a functional block diagram of the auto calibration pulse generator circuit.

The calibration pulse generation functions provided can be subdivided into four operational areas. The first function is the generation of the calibration pulses required to complete the initial (power-up) calibration process when power is first supplied to the converter. The next two functions accommodated are the generation of periodic calibration pulses, either internally or externally, to maintain calibration. The last function is the provision for externally initiating or re-initiating the power-up calibration process.

Power-up Calibration Function

The initial power-up calibration requires over 600 calibration pulses in order to complete the calibration process when power is first applied to the converter. The power-up calibration function provided by the auto calibration pulse generator automatically generates these pulses internally and completes the initial calibration process. The following five conditions must be satisfied in order for the auto calibration pulse generator power-up calibration process to be initiated :

a) The voltage between AV_{DD} and AV_{SS} is approximately 2.5V or more.

b) The voltage between V_{RT} and V_{RB} is approximately 1.0V or more.

c) The RESET control input pin (Pin 15) must be high (logic 1).

d) The $\overline{CE}$ control input pin (Pin 24) must be low (logic 0).

e) Condition b must be met after condition a.

Once all five of these conditions is satisfied the power-up calibration pulses are generated. These power-up calibration pulses are derived from a divided-by sixteen sample clock

(CLK/16). A 14-bit counter is also counting the CLK/16 signal and when the 14-bit counter reaches the end of its count range the carry out from the counter is used to gate off or mask the CLK/16 power-up calibration pulses.

The time required for the power-up calibration process to be completed after the above five conditions has been met can be calculated using the following equation:

$t_{Power\text{-}Up\ Cal} = (2^4 \times 2^{14})/(f_{CLK}) = 2^{18}/f_{CLK}$.

For example, if the sample clock frequency is 20MHz, the time required for the power-up calibration process to be completed, after the above five conditions has been met, is

$t_{Power\text{-}Up\ Cal} = 2^{18}/f_{CLK} = 2^{18}/20x10^6 = 262,144/20 \times 10^6$,

$t_{Power\text{-}Up\ Cal} = 13.1ms$.

Auto Calibration Pulse Generation Function

The auto calibration pulse generator provides the user with the choice of internal or external periodic calibration pulse generation following the completion of the power-up calibration process. The selection of internal or external periodic calibration pulse generation is made through the use of the SEL control input pin (pin 17). Setting the SEL control input pin high (logic 1) selects the internal periodic calibration pulse generation function. Setting the SEL control input pin low (logic 0) selects the external calibration pulse input pin (CAL, pin 41).

For the case where the internal periodic calibration pulse generation function has been chosen, SEL control input pin high, the auto calibration pulse generator periodically generates calibration pulses internally so that calibration is performed constantly without the need to provide calibration input pulses from an external source. These periodic calibration pulses are derived from the divided-by sixteen sample clock (CLK/16). The CLK/16 signal drives a 24-bit counter which generates a carry-out that is used as the internal calibration pulse. The time between calibration pulses when using the internal auto calibration pulse generator can be calculated using the following equation:

$t_{Internal\ Cal\ Pulse} = (2^4 \times 2^{24})/(f_{CLK}) = 2^{28}/f_{CLK}$.

For example, if the sample clock frequency is 20MHz, the time between internal auto calibration pulses is:

$t_{Internal\ Cal\ Pulse} = 2^{28}/f_{CLK} = 2^{28}/20 \times 10^6 = 268,435,456/20 \times 10^6$,

$t_{Internal\ Cal\ Pulse} = 13.4s$.

Since a calibration is completed once every seven calibration pulses, the time required to complete a calibration cycle is:

$t_{Internal\ Cal\ Cycle} = (7 \times 2^{28})/f_{CLK}$.

Therefore, if the sample clock frequency is 20MHz, the internal calibration cycle is:

$t_{Internal\ Cal\ Cycle} = (7 \times 2^{28})/20 \times 10^6 = 93.95s$.

It should be noted that this method of periodic calibration may not be acceptable if the fixing of the lower five output bits during the calibration (see the discussion below on external calibration pulse input function) would cause problems since the calibration is executed asynchronously without regard to the analog input signal.

External Calibration Pulse Input Function

If the auto calibration pulse generation function cannot be used then periodic calibration can be performed by providing externally input calibration pulses to the CAL input pin (pin 41) and setting the SEL control input pin (pin 17) low. Refer to Figure 3, External Calibration Pulse Timing Diagram, for details on the required timing of the externally supplied calibration pulses.

A setup time of 10ns or longer is required for the CAL input and it must stay low for at least one sample clock (CLK) period. Calibration starts when the falling edge of the externally supplied calibration pulse, input to the CAL pin, is detected. One calibration is completed in 11 sample clock cycles. Seven sample clock cycles after the falling edge of the externally supplied calibration pulse is detected, the calibration circuit takes exclusive possession of the lower comparators, D0 through D4, for four sample clock cycles. During this time, the D0 through D4 outputs are latched with the previous data (cycle seven data). The upper 5 bits, D5 through D9, will operate as usual during the calibration.

The calibration must be done when the part is first powered up, if the sampling frequency changes, when the supplies vary more than 100mV or when (V_{RT} - V_{RB}) changes more than 200mV. Figure 4 shows several possible external calibration pulse timing schemes where the calibration is performed outside the active video interval by using the video sync signal as the externally supplied CAL input. It is not necessary to calibrate as often as these figures show, these are only design ideas. It is also possible to use only the power-up calibration function by leaving the SEL control input pin (pin 17) low and fixing the CAL input pin (pin 41) either high or low. Note, however, that using only the power-up calibration function will require the above restrictions on the sample frequency and the fluctuation range of the power supply voltage and the reference voltage differential be maintained.

Initiating/Re-Initiating Power-up Calibration Function

The power-up calibration function can be initiated/re-initiated after the power supply voltage and the reference voltages are stabilized by using the $\overline{CE}$ (pin 24) or RESET (pin 15) control input pins. This might prove useful in a situation where the turn-on characteristics of the power supply and reference voltages is unstable/indeterminate or where the sequence of power-up does not meet the required conditions stated earlier.

Power, Grounding, and Decoupling

To reduce noise effects, keep the analog and digital grounds separated. Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1µF capacitor close to the input pin. A larger capacitor (1µF to 10µF) should be placed somewhere on the PC board for low frequency decoupling of both analog and digital supplies.

The analog supply should be present before the digital supply to reduce the risk of latch-up. The digital supply can run from +3.3V or +5V. A +3.3V supply generates less radiated noise at the digital outputs, but results in less drive capability. The specifications do not change with digital supply levels. Remember, the digital outputs will only swing to DV_{DD}.

To obtain full expected performance from the converter be sure that the circuit board has a large ground plane to provide as low an impedance as possible. It is recommended that the converter be mounted directly to the circuit board and the use of a socket is highly discouraged.

Test Circuits

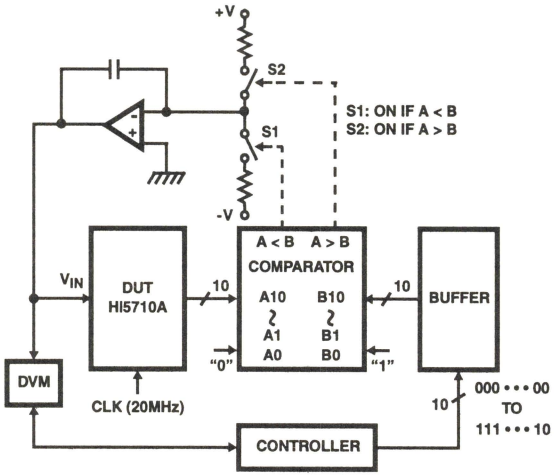


FIGURE 17. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR TEST CIRCUIT

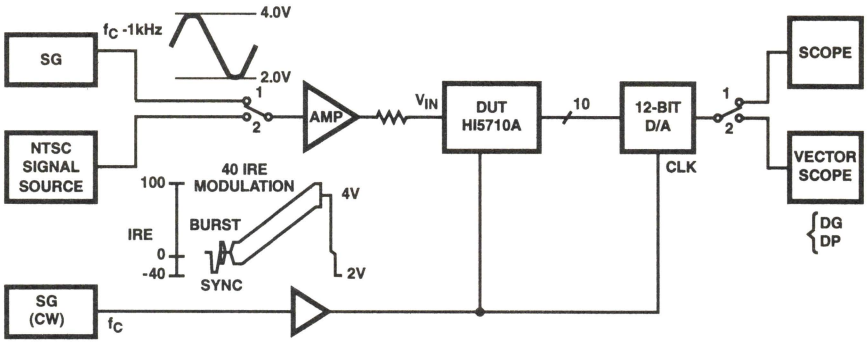


FIGURE 18. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN /PHASE ERROR TEST CIRCUIT

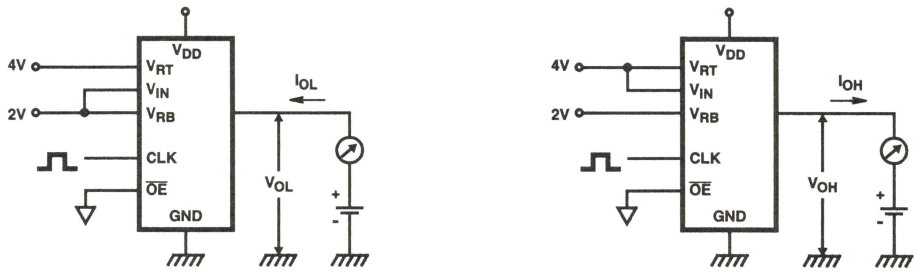


FIGURE 19A. FIGURE 19B.

FIGURE 19. DIGITAL OUTPUT TEST CIRCUIT

Test Circuits (Continued)

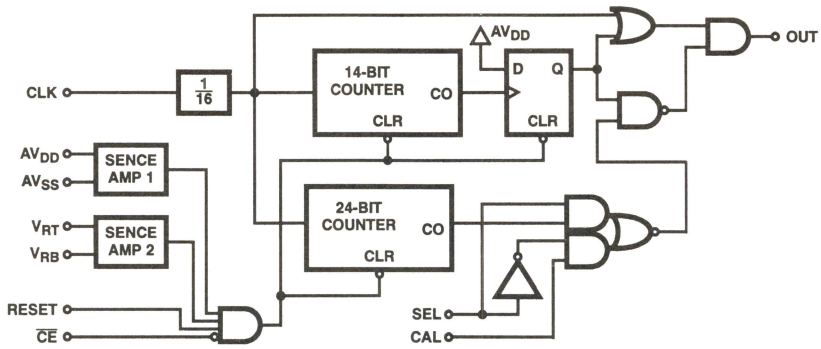


FIGURE 20. CALIBRATION PULSE GENERATION CIRCUIT

Typical Application Circuits

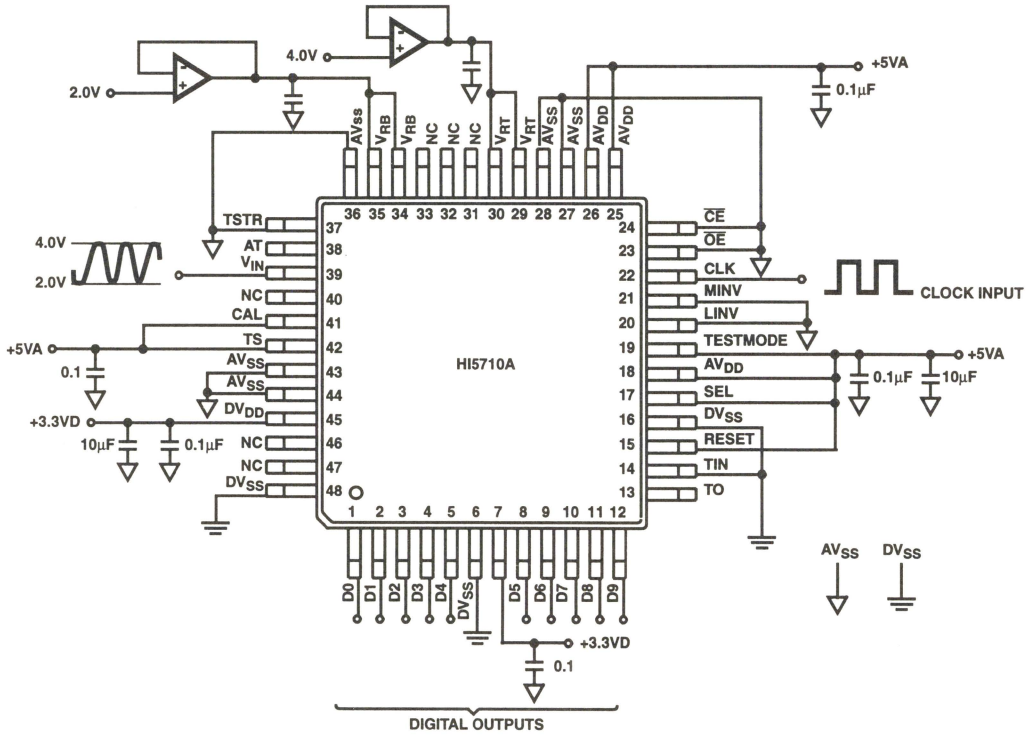


FIGURE 21A. POWER-UP CALIBRATION WITH INTERNAL AUTO CALIBRATION SELECTED

Typical Application Circuits (Continued)

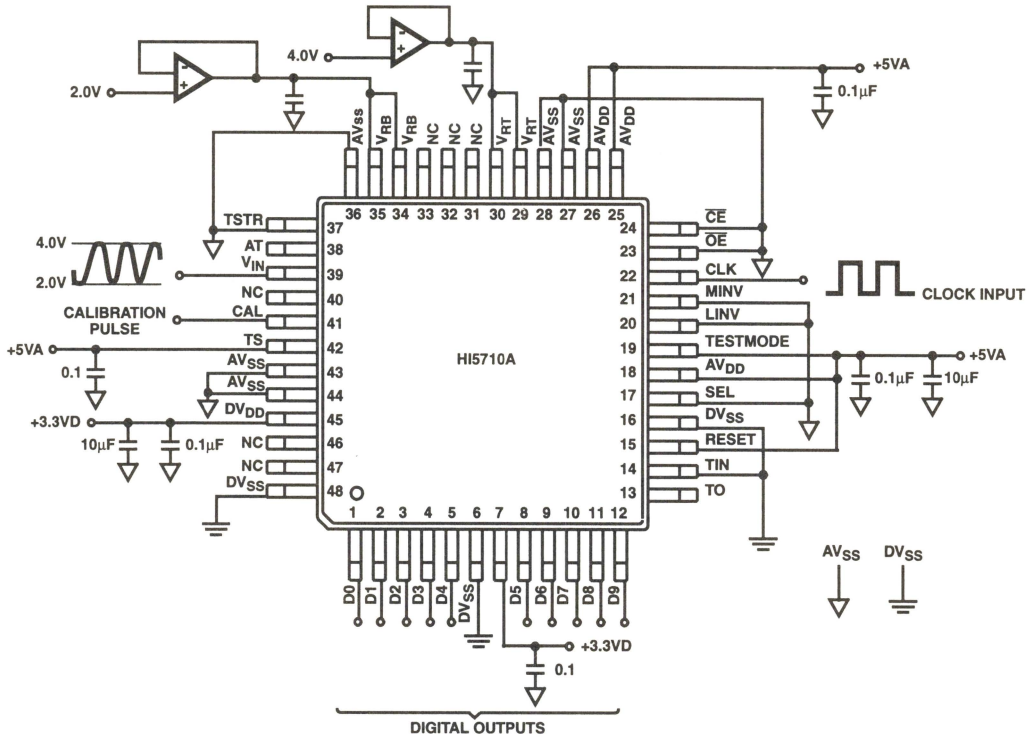


FIGURE 21B. POWER-UP CALIBRATION WITH EXTERNAL CALIBRATION PULSE INPUT SELECTED

Typical Application Circuits (Continued)

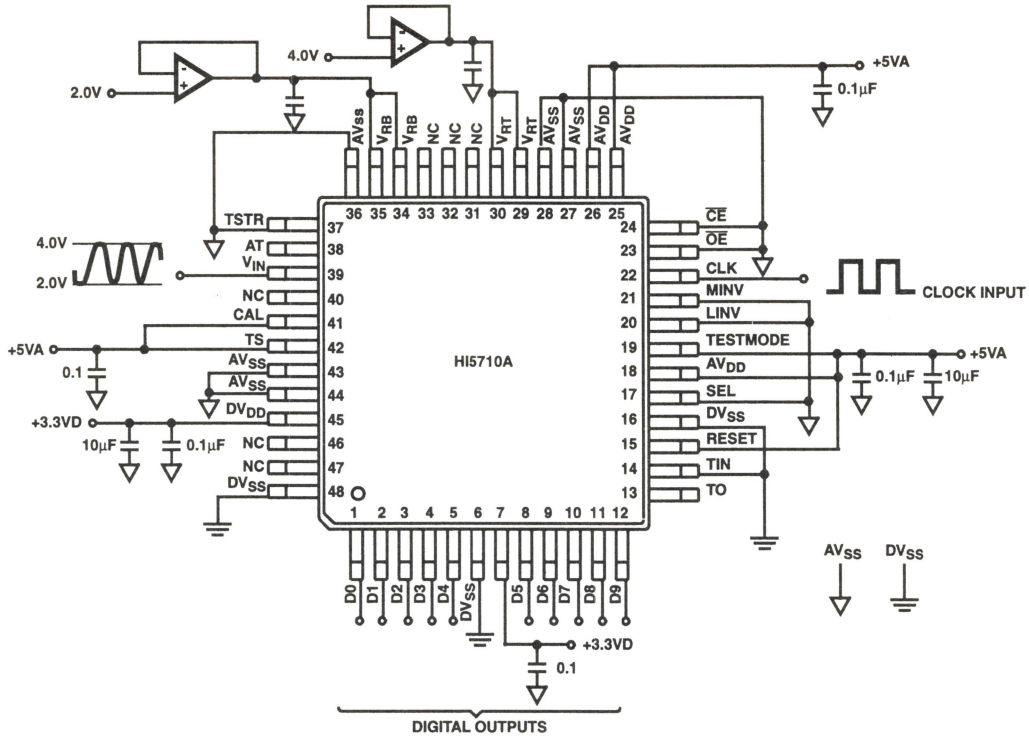


FIGURE 21C. ONLY POWER-UP CALIBRATION BEING UTILIZED

Timing Definitions

Sampling Delay, is the time delay between the external sample command (the rising edge of the clock) and the time at which the analog input signal is actually sampled. This delay is due to internal clock path propagation delays.

Data Latency, after the analog sample is taken, the digital representation is output on the digital data output bus after the 3rd cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding analog input sample is output on the following rising edge of the clock pulse. The digital data output lags the analog input sample by 3 sampling clock cycles.

Power-up Initialization, this time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize some dynamic circuits within the converter.

Static Performance Definitions

Differential Linearity Error, DNL, is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed to have no missing codes over the operating temperature range.

Integral Linearity Error, INL, is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5710A. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 2048 point FFT and analyzed to evaluate the dynamic performance of the A/D. The analog sine wave input signal to the converter is -0.5dB down from full scale for all these tests. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio, SNR, is the measured RMS signal to RMS noise for a specified analog input frequency and sampling frequency. The noise is the RMS sum of all of the spectral components excluding the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio, SINAD, is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits, ENOB, the effective number of bits (ENOB) is calculated from the measured SINAD data. as follows:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02,$$

where: $V_{CORR} = 0.5dB$.

V_{CORR} adjusts the ENOB for the amount the analog input signal is below full scale.

2nd and 3rd Harmonic Distortion, is the ratio of the RMS value of the 2nd and 3rd harmonic component, respectively, to the RMS value of the measured input signal.

Analog Input Bandwidth, is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the differential reference voltage. The bandwidth given is measured at the specified sampling frequency.

HFA1135	HI5710A	HSP9501	HI1171	HA5020
HFA1245	HI5767/2	HSP48410	HI3050	HA2842
HA5020	HI5767/4	HSP48908	HI3338	HFA1115
		HSP48212		
		HSP43891		
		HSP43168		
		HSP43216		

HFA1135: 350MHz Op Amp with Output Limiting
HFA1245: Dual 350MHz Op Amp with Disable/Enable
HA5020: 100MHz Video Op Amp
HI5710A: 10-Bit, 20 MSPS, A/D Converter
HI5767/2/4: 10-Bit, 20/40 MSPS, Low Power A/D Converter with Internal Reference
HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48212: Digital Video Mixer
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HI1171: 8-Bit, 40MHz, Video D/A Converter
HI3338: 8-Bit, 50MHz, Video D/A Converter
HI3050: Triple 10-Bit, 50MHz, Video DAC
HA2842: High Output Current, Video Op Amp
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 22. 10-BIT VIDEO IMAGING COMPONENTS

HFA3600	HI5710A	HSP43168	HI5721	HFA1115
HFA3102	HI5767/2	HSP43216	HI20201	
HFA3101	HI5767/4	HSP43891	HI20203	
HFA1100		HSP50016	HI5780	
		HSP50110		
		HSP50210		

HFA3600: Low Noise Amplifier/Mixer
HFA3102: Dual Long-Tailed Pair Transistor Array
HFA3101: Gilbert Cell Transistor Array
HFA1100: 850MHz Op Amp
HI5710A: 10-Bit, 20 MSPS, A/D Converter
HI5767/2/4: 10-Bit, 20/40 MSPS, Low Power A/D Converter with Internal Reference
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP50016: Digital Down Converter
HSP50110: Digital Quadrature Tuner
HSP50210: Digital Costas Loop
HI5721: 10-Bit, 100MHz, Communications D/A Converter
HI5780: 10-Bit, 80MHz CMOS D/A Converter
HI20201: 10-Bit, 160MHz, High Speed D/A Converter
HI20203: 8-Bit, 160MHz, High Speed D/A Converter
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 23. 10-BIT COMMUNICATIONS COMPONENTS

HARRIS SEMICONDUCTOR

HI5714

August 1997

8-Bit, 40/60/75 MSPS A/D Converter

Features

- Sampling Rate . . . . . 40/60/75 MSPS
- Low Power 325mW
- 7.65 ENOB at 4.43MHz
- Overflow/Underflow Three-State TTL Output
- Operates with Low Level AC Clock
- Very Low Analog Input Capacitance
- No Buffer Amplifier Required
- No Sample and Hold Required
- TTL Compatible I/O
- Pin-Compatible to Philips TDA8714

Applications

- Video Digitizing
- QAM Demodulator
- Digital Cable Setup Box
- Tape Drive/Mass Storage
- Medical Ultrasound Imaging
- Communication Systems

Description

The HI5714 is a high precision, monolithic, 8-bit, Analog-to-Digital Converter fabricated in Harris' advanced HBC10 BiCMOS process.

The HI5714 is optimized for a wide range of applications such as ultrasound imaging, mass storage, instrumentation, and video digitizing, where accuracy and low power consumption are essential. The HI5714 is offered in 40 MSPS, 60 MSPS, and 75 MSPS sample rates.

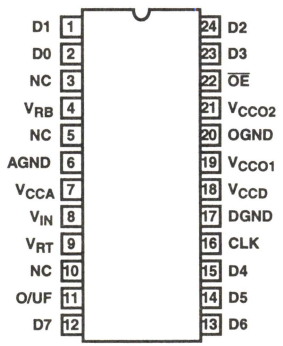
The HI5714 delivers ±0.4 LSB differential nonlinearity while consuming only 325mW power (Typical) at 75 MSPS. The digital inputs and outputs are TTL compatible, as well as allowing for a low-level sine wave clock input.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	SAMPLING FREQUENCY (MHz)	PKG. NO.
HI5714/4CB	0 to 70	24 Ld SOIC	40	M24.3
HI5714/6CB	0 to 70	24 Ld SOIC	60	M24.3
HI5714/7CB	0 to 70	24 Ld SOIC	75	M24.3
HI5714EVAL	25	Evaluation Board		

Pinout

HI5714
(SOIC)
TOP VIEW



4 A/D CONVERTERS HIGH SPEED

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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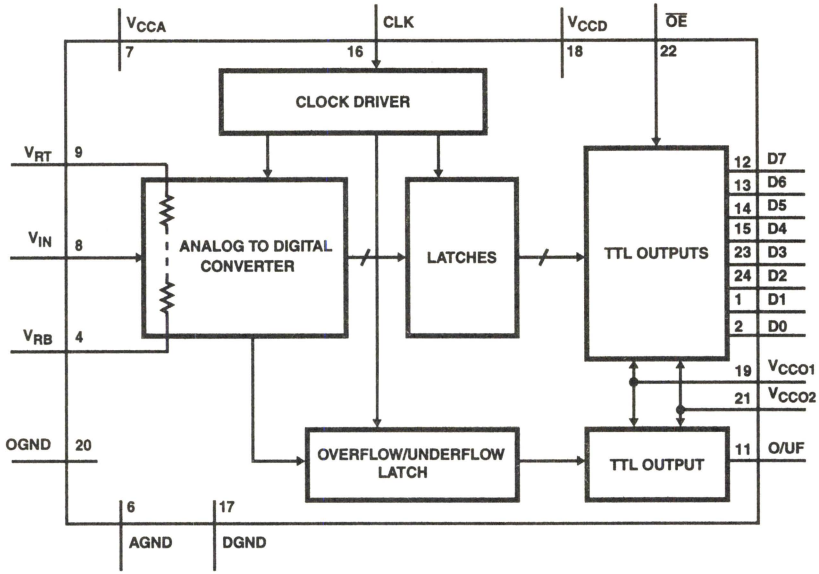
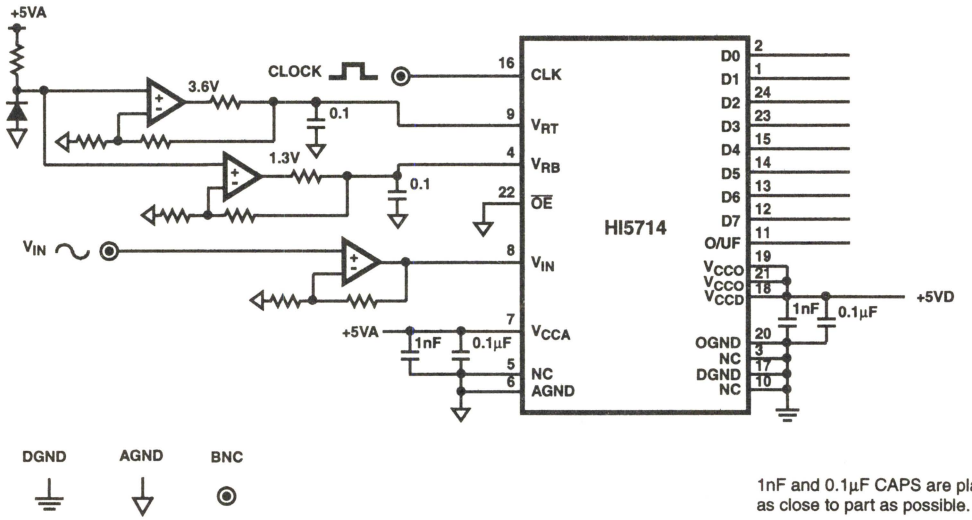
File Number 3973.3

Functional Block Diagram



Typical Application Schematic



1nF and 0.1µF CAPS are placed as close to part as possible.

NOTES:

1. Pin 5 should be connected to AGND and pins 3 and 10 to DGND to reduce noise coupling into the device.
2. Analog and Digital supplies should be separated and decoupled to reduce digital noise coupling into the analog supply.

Absolute Maximum Ratings $T_A = 25^oC$

V_{CCA}, V_{CCD}, V_{CCO} ..... -0.3V to +6.0V
V_{CCA} - V_{CCD} 0.3V
V_{CCO} - V_{CCD} 0.3V
V_{CCA} - V_{CCO} 0.3V
V_{IN}, V_{CLK}, V_{RT}, V_{RB}, $\overline{OE}$ ..... -0.3V to +6.0V
I_{OUT}, Digital Pins 10mA
Input Current, All Pins 1mA
Digital I/O Pins ..... OGND to V_{CCO}

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	75

Maximum Junction Temperature (Plastic Package) ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range
HI5714CB ..... 0^oC to 70^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{CCA} = V_{CCD} = V_{CCO} = +5V$; $V_{RB} = 1.3V$; $V_{RT} = 3.6V$; $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
CLOCK (Referenced to DGND) (Note 1)					
Logic Input Voltage Low, V_{IL}		0	-	0.8	V
Logic Input Voltage High, V_{IH}		2.0	-	V_{CCD}	V
Logic Input Current Low, I_{IL}	$V_{CLK} = 0.4V$	-400	-	-	µA
Logic Input Current High, I_{IH}	$V_{CLK} = 2.7V$	-	-	300	µA
Input Impedance, Z_{IN}	$f_{CLK} = 75MHz$ (Note 8)	-	2	-	kΩ
Input Capacitance, C_{IN}	$f_{CLK} = 75MHz$ (Note 8)	-	4.5	-	pF
$\overline{OE}$ (Referenced to DGND)					
Logic Input Voltage Low, V_{IL}		0	-	0.8	V
Logic Input Voltage High, V_{IH}		2.0	-	V_{CCD}	V
Logic Input Current Low, I_{IL}	$V_{IL} = 0.4V$	-400	-	-	µA
Logic Input Current High, I_{IH}	$V_{IH} = 2.7V$	-	-	20	µA
V_{IN} (Referenced to AGND)					
Input Current Low, I_{IL}	$V_{IN} = 1.2V$	-	0	-	µA
Input Current High, I_{IH}	$V_{IN} = 3.5V$	-	100	180	µA
Input Impedance, Z_{IN}	$f_{IN} = 4.43MHz$	-	10	-	kΩ
Input Capacitance, C_{IN}	$f_{IN} = 4.43MHz$	-	14	-	pF
REFERENCE INPUT					
Bottom Reference Range, V_{RB}		1.2	1.3	1.6	V
Top Reference Range, V_{RT}		3.5	3.6	3.9	V
Reference Range, V_{REF} (V_{RT} - V_{RB})		1.9	2.3	2.7	V
Reference Current, I_{REF}		-	10	-	mA
Reference Ladder Resistance, R_{LAD}		-	240	-	Ω

Electrical Specifications $V_{CCA} = V_{CCD} = V_{CCO} = +5V$; $V_{RB} = 1.3V$; $V_{RT} = 3.6V$; $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
R_{LADTC}		-	0.24	-	$\Omega/^oC$
Bottom Offset Voltage, V_{OB}	(Note 4)	-	255	-	mV
V_{OBTC}	(Note 4)	-	136	-	$\mu V/^oC$
Top Offset Voltage, V_{OT}	(Note 4)	-	-300	-	mV
V_{OTTC}	(Note 4)	-	480	-	$\mu V/^oC$
DIGITAL OUTPUTS (D0 to D7 and O/UF Referenced to OGND)					
Logic Output Voltage Low, V_{OL}	$I_O = 1mA$	0	-	0.4	V
Logic Output Voltage High, V_{OH}	$I_O = -0.4mA$	2.7	-	V_{CCO}	V
Output Leakage Current, I_D	$0.4V < V_{OUT} < V_{CCO}$	-20	-	+20	μA
SWITCHING CHARACTERISTICS (Notes 3, 4) See Figure 9					
Sample Rate, f_{CLK}					
HI5714/7		75	-	-	MHz
HI5714/6		60	-	-	MHz
HI5714/4		40	-	-	MHz
Clock Pulse Width High, t_{CPH}		6	-	-	ns
Clock Pulse Width Low, t_{CPL}		6	-	-	ns
ANALOG SIGNAL PROCESSING ($f_{CLK} = 40MHz$)					
Differential Gain, DG	(Notes 5, 8)	-	1.0	-	%
Differential Phase, DP	(Notes 5, 8)	-	0.05	-	degree
HARMONICS ($f_{CLK} = 75MHz$)					
Second Harmonic, H2	$f_{IN} = 4.43MHz$	-	-63	-	dB
Third Harmonic, H3	$f_{IN} = 4.43MHz$	-	-65	-	dB
Total Harmonic Distortion, THD	$f_{IN} = 4.43MHz$	-	-59	-	dB
Spurious Free Dynamic Range, SFDR	$f_{IN} = 4.43MHz$	-	62	-	dB
Analog Input Bandwidth (-3dB)		-	18	-	MHz
TRANSFER FUNCTION					
Differential Linearity Error, DNL	(Note 6)	-	±0.4	-	LSB
Integral Linearity Error, INL	(Note 6)	-	±0.75	-	LSB
EFFECTIVE NUMBER OF BITS					
ENOB					
HI5714/4 ($f_{CLK} = 40MHz$)	$f_{IN} = 4.43MHz$	-	7.65	-	Bits
	$f_{IN} = 7.5MHz$	-	7.5	-	Bits
HI5714/6 ($f_{CLK} = 60MHz$)	$f_{IN} = 4.43MHz$	-	7.65	-	Bits
	$f_{IN} = 7.5MHz$	-	7.5	-	Bits

Electrical Specifications $V_{CCA} = V_{CCD} = V_{CCO} = +5V$; $V_{RB} = 1.3V$; $V_{RT} = 3.6V$; $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
HI5714/7 (f_{CLK} = 75MHz)	f_{IN} = 4.43MHz	-	7.4	-	Bits
	f_{IN} = 7.5MHz	-	7.15	-	Bits
	f_{IN} = 10MHz	-	6.8	-	Bits
Bit Error Rate, BER	(Note 7)	-	10^{-11}	-	Times/ Sample
TIMING (f_{CLK} = 75MHz) See Figures 1, 2					
Sampling Delay, t_{SD}		-	-	2	ns
Output Hold Time, t_{HD}		5	-	-	ns
Output Delay Time, t_D		-	10	13	ns
Output Enable Delay, t_{PZH}	Enable to High	-	14.6	-	ns
Output Enable Delay, t_{PZL}	Enable to Low	-	17.8	-	ns
Output Disable Delay, t_{PHZ}	Disable from High	-	5.3	-	ns
Output Disable Delay, t_{PLZ}	Disable from Low	-	6.7	-	ns
Aperture Jitter, t_{AJ}		-	50	-	ps
POWER SUPPLY CHARACTERISTICS					
Analog Power Supply Range, V_{CCA}		4.75	5.0	5.25	V
Digital Power Supply Range, V_{CCD}		4.75	5.0	5.25	V
Output Power Supply Range, V_{CCO}		4.75	5.0	5.25	V
Total Supply Current		-	65	75	mA
Supply Current, I_{CCA}		-	30	-	mA
Supply Current, I_{CCD}		-	26	-	mA
Supply Current, I_{CCO}		-	9	-	mA
Power Dissipation		-	325	375	mW

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. The supply voltages V_{CCA} and V_{CCD} may have any value between -0.3V and +6V as long as the difference V_{CCA} - V_{CCD} lies between -0.3V and +0.3V.
3. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock not be less than 1ns.
4. Analog input voltages producing code 00 up to and including FF.

   V_{OB} (Bottom Offset Voltage) is the difference between the analog input which produces data equal to 00 and the Bottom Reference Voltage (V_{RB}).

   V_{OBTC} (Bottom Offset Voltage Temperature Coefficient) is the variation of V_{OB} with temperature.

   V_{OT} (Top Offset Voltage) is the difference between the Top Reference Voltage (V_{RT}) and the analog input which produces data output equal to FF.

   V_{OTTC} (Top Offset Voltage Temperature Coefficient) is the variation of V_{OT} with temperature.
5. Input is standard 5 step video test signal. A 12-bit R reconstruct DAC and VM700 are used for measurement.
6. Full scale sinewave, f_{IN} = 4.43MHz.
7. f_{CLK} = 75MHz, f_{IN} = 4.43MHz, V_{IN} = ±8 LSB at code 128, 50% Clock duty cycle.
8. Parameter is guaranteed by design, not production tested.

Timing Waveforms

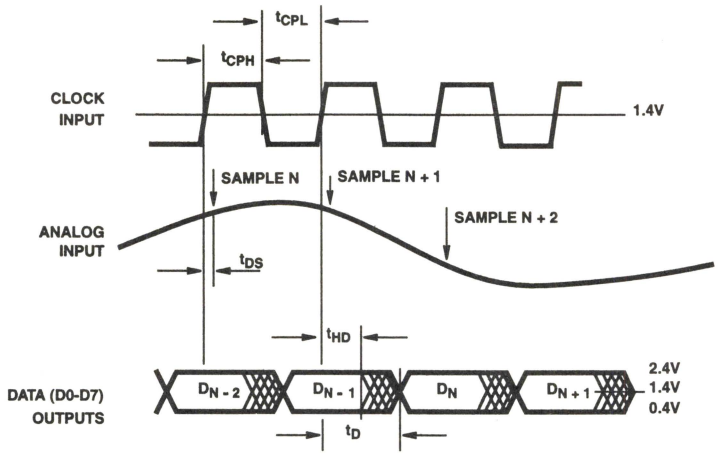


FIGURE 1. INPUT-TO-OUTPUT TIMING

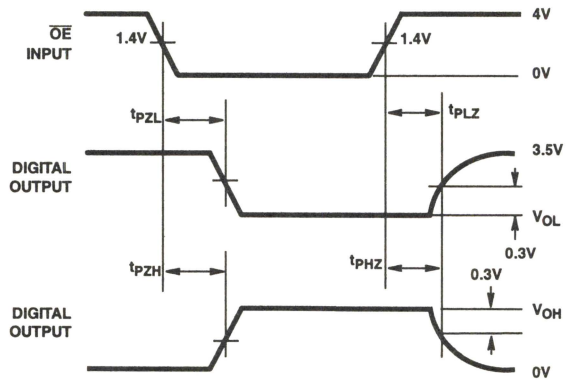


FIGURE 2. THREE-STATE TIMING CIRCUIT

Typical Performance Curves

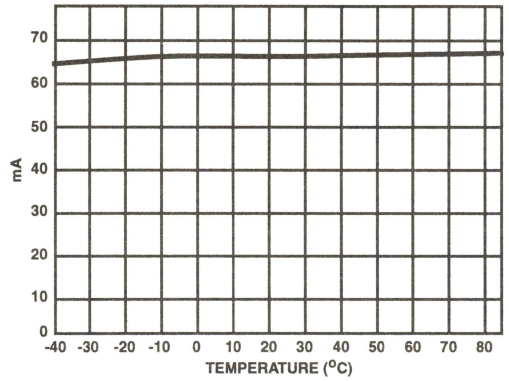


FIGURE 3. TOTAL I_{CC} vs TEMPERATURE

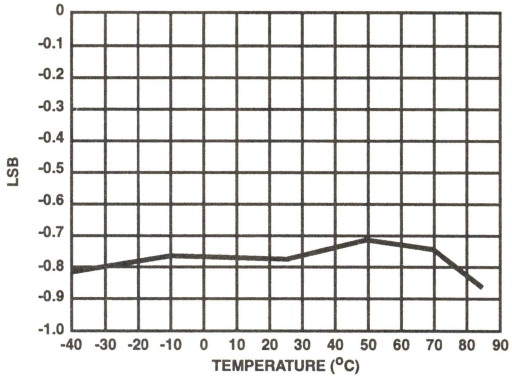


FIGURE 4. INTEGRAL LINEARITY ERROR vs TEMPERATURE

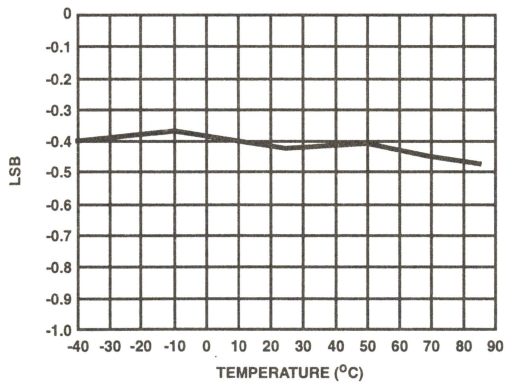


FIGURE 5. DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

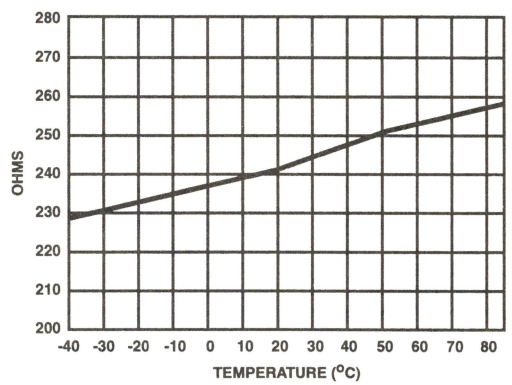


FIGURE 6. REFERENCE RESISTANCE vs TEMPERATURE

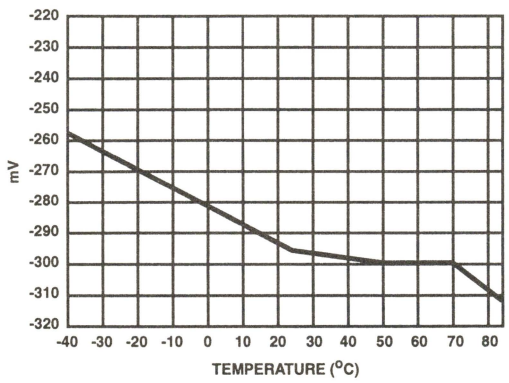


FIGURE 7. V_{OT} vs TEMPERATURE

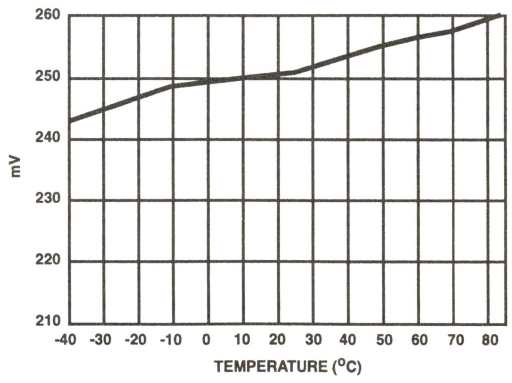


FIGURE 8. V_{OB} vs TEMPERATURE

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 2, 12-15, 23, 24	D0 to D7	Digital Outputs, D0 (LSB) to D7 (MSB).
4	V_{RB}	Bottom Reference Voltage Input. Range: 1.2V to 1.6V.
6	AGND	Analog Ground.
7	V_{CCA}	Analog +5V.
8	V_{IN}	Analog Input.
9	V_{RT}	Top Reference Voltage Input. Range: 3.5V to 3.9V.
11	O/UF	Underflow/Overflow Digital Output. Goes high if the analog input goes above or below the reference (V_{RB}, V_{RT}) minus the offset.
16	CLK	Clock Input.
17	DGND	Digital GND.
18	V_{CCD}	Digital +5V.
19, 21	V_{CCO1}, V_{CCO2}	Digital +5V for Digital Output Stage.
20	OGND	Digital Ground for Digital Output Stage.
22	$\overline{OE}$	Output Enable High: Digital outputs are three-stated. Low: Digital outputs are active.

TABLE 1. A/D CODE TABLE

CODE DESCRIPTION	(NOTE 1) INPUT VOLTAGE V_{RT} = 3.6V V_{RB} = 1.3V	O/UF	BINARY OUTPUT CODE							
			D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.555V	1	0	0	0	0	0	0	0	0
0	1.555V	0	0	0	0	0	0	0	0	0
1	-	0	-	-	-	-	-	-	-	-
-	-	0	-	-	-	-	-	-	-	-
-	-	0	-	-	-	-	-	-	-	-
254	-	0	1	1	1	1	1	1	1	0
255	3.300V	0	1	1	1	1	1	1	1	1
Overflow	>3.300V	1	1	1	1	1	1	1	1	1

NOTE:

1. The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage, including the typical reference offset voltages.

TABLE 2. MODE SELECTION

$\overline{OE}$	D7 to D0	O/UF
1	High Impedance	High Impedance
0	Active: Binary	Active

Detailed Description

Theory of Operation

The HI5714 design utilizes a folding and interpolating architecture. This architecture reduces the number of comparators, reference taps, and latches, thereby reducing power requirements, die size and cost.

A folding A/D converter operates basically like a 2 step subranging converter by using 2 lower resolution converters to do a course and subranged fine conversion. A more complete description is given in the application note "Using the HI5714 Evaluation Module" (AN9517).

Reference Input, V_{RT} and V_{RB}

The HI5714 requires an external reference to be connected to pins 4 and 9, V_{RB} and V_{RT}.

It is recommended that adequate high frequency decoupling be provided at the reference input pin in order to minimize overall converter noise. A 0.1µF and a 1nF capacitor as close as possible to the reference pins work well.

V_{RT} must be kept within the range of 3.5V to 3.9V and V_{RB} within 1.2V to 1.6V. If the reference voltages go outside their respective ranges, the input folding amplifiers may saturate giving erroneous digital data. The range for (V_{RT} - V_{RB}) is 1.9V to 2.7V, which defines the analog input range.

Digital Control and Clock Requirements

The HI5714 provides a standard high-speed interface to external TTL logic families.

The outputs can be three-stated by setting the $\overline{OE}$ input (pin 22) high.

The clock input operates at standard TTL levels as well as a low level sine wave around the threshold level. The HI5714 can operate with clock frequencies from DC to 75MHz. The clock duty cycle should be 50% ±10% to ensure rated performance. Duty cycle variation, within the specified range, has little effect on performance. Due to the clock speed it is important to remember that clock jitter will affect the quality of the digital output data.

The clock can be stopped at any time and restarted at a later time. Once restarted the digital data will be valid at the second rising edge of the clock plus the data delay time.

Digital Outputs and O/UF Output

The digital outputs are standard TTL type outputs. The HI5714 can drive 1 to 3 TTL inputs depending on the input current requirements.

Should the analog input exceed the top or bottom reference the over/underflow output (pin 11) will go high. Should the analog input exceed the top reference voltage, V_{RT}, the digital outputs will remain at all 1s until the analog input goes below V_{RT}. Also, should the analog input go below the bottom reference voltage, V_{RB}, the digital outputs will remain at all 0s until the analog input goes above V_{RT}.

Analog Input

The analog input will accept a voltage within the reference voltage levels, V_{RB} and V_{RT}, minus some offset. The offset is specified in the Electrical Specifications table.

The analog input is relatively high impedance (10kΩ) but should be driven from a low impedance source. The input capacitance is low (14pF) and there is little kickback from the input, so a series resistance is not necessary but it may help to prevent the driving amplifier from oscillating.

The input bandwidth is typically 18MHz. Exceeding 18MHz will result in sparkle at the digital outputs. The bandwidth remains constant at clock rates up to 75MHz.

Supply and Ground Considerations

In order to keep digital noise out of the analog signal path, the HI5714 has separate analog and digital supply and ground pins. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds.

The analog and digital grounds should be tied together at one point near the HI5714. The grounds can be connected directly, through an inductor (ferrite bead), or a low valued resistor. DGND and AGND can be tied together. To help minimize noise, tie pin 5 (NC) to AGND and pins 3 (NC) and 10 (NC) to DGND.

For best performance, the supplies to the HI5714 should be driven by clean, linear regulated supplies. The board should also have good high frequency leaded decoupling capacitors mounted as close as possible to the converter. Capacitor leads must be kept as short as possible (less than $^1/_2$ inch total length). A 0.1µF and a 1nF capacitor as close as possible to the pin works well. Chip capacitors will provide better high frequency decoupling but leaded capacitors appear to be adequate.

If the part is to be powered by a single supply, then the analog supply pins should be isolated by ferrite beads from the digital supply pins. This should help minimize noise on the analog power pins.

Refer to Application Note AN9214, "Using Harris High Speed A/D Converters", for additional considerations when using high speed converters.

Increased Accuracy

Further calibration of the ADC can be done to increase absolute level accuracy. First, a precision voltage equal to the ideal VIN_{-FS} + 0.5 LSB is applied at V_{IN}. Adjust V_{RB} until the 0 to 1 transition occurs on the digital output. Next, a voltage equal to the ideal VIN_{+FS} - 1.5 LSB is applied at V_{IN}. V_{RT} is then adjusted until the 254 to 255 transition occurs on the digital output.

Applications

Figures 3 and 4 show two possible circuit configurations, AC coupled with a DC restore circuit and DC coupled with a DC offset amplifier.

Due to the high clock rate, FCT (TTL/CMOS) or FAST (TTL) glue logic should be used. FCT logic will tend to have large overshoots if not loaded. Long traces (>2 or 3 inches) should be terminated to maintain signal integrity.

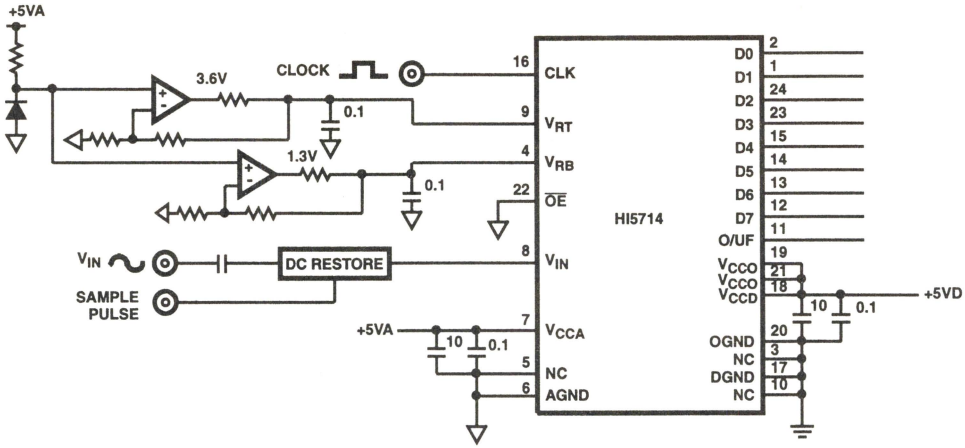


FIGURE 9. TYPICAL AC COUPLED INPUT WITH DC RESTORE

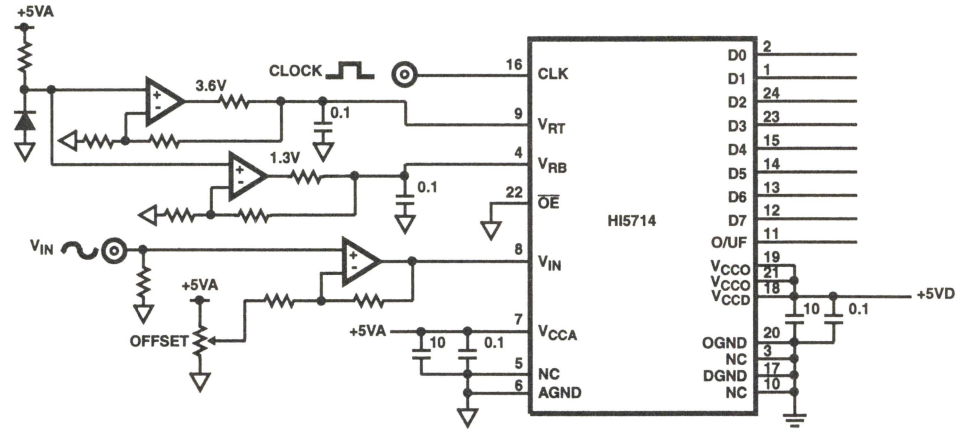
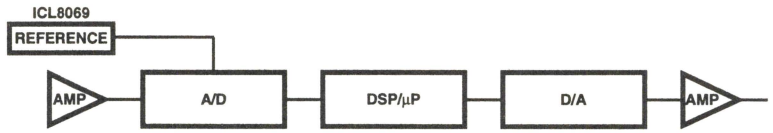


FIGURE 10. TYPICAL DC COUPLED INPUT



HA5020 (Single)	HI5714 (8-Bit)	HSP9501	HI1171 (8-Bit)	HA5020 (Single)
HA5022 (Dual)		HSP48410	CA3338 (8-Bit)	HA2842 (Single)
HA5024 (Quad)		HSP48908	HI5721 (10-Bit)	HFA1115 (Single)
HA5013 (Triple)		HSP48901	HI3050 (10-Bit)	HFA1212 (Dual)
HFA1105 (Single)		HSP48212		HFA1412 (Quad)
HFA1205 (Dual)		HSP43881		
HFA1405 (Quad)		HSP43168		

HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/accumulating Buffer, 10-Bit Pixel Resolution, 4K x 4K Frame Size
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48901: 3 x 3 Image Filter, 30MHz, 8-Bit
HSP48212: Video Mixer
HSP43881: Digital Filter, 30MHz, 1-D and 2-D Fir Filters
HSP43168: Dual Fir Filter, 10-Bit, 33/45MHz

CMOS Logic Available in FCT

FIGURE 11. 8-BIT VIDEO COMPONENTS

Timing Definitions

Aperture Delay: Aperture delay is the time delay between the external sample command (the rising edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter: This is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Latency

After the analog sample is taken, the data on the bus is output at the next rising edge of the clock. This is due to the output latch of the converter. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 1 cycle.

Static Performance Definitions

Offset Error and Full-Scale Error use a measured value of the external voltage reference to determine the ideal plus and minus full-scale values. The results are all displayed in LSBs.

Bottom Offset Voltage (V_{OB})

The first code transition should occur at a level 0.5 LSB above the negative full-scale. Bottom offset voltage is defined as the deviation of the actual code transition from this point.

Top Offset Voltage (V_{OT})

The last code transition should occur for a analog input that is 1.5 LSBs below positive full-scale. Top Offset Voltage is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed to have no missing codes.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5714. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 2048 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is 0.5dB down from full scale for these tests. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

ENOB = (SINAD - 1.76) / 6.02

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the 2nd and 3rd harmonic component respectively to the RMS value of the measured input signal.

Full Power Input Bandwidth

Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the difference between the top reference voltage input and the bottom reference voltage input. The bandwidth given is measured at the specified sampling frequency.

Die Characteristics

DIE DIMENSIONS:

134 mils x 134 mils x 19 mils ±1 mil

METALLIZATION:

Type: AlSiCu
Thickness: M1 - 8kÅ, M2 - 17kÅ

SUBSTRATE POTENTIAL (Powered Up):

GND (0.0V)

PASSIVATION:

Type: Sandwich Passivation*
Undoped Silicon Glass (USG) + Nitride
Thickness: USG - 8kÅ, Nitride - 4.2kÅ
Total 12.2kÅ + 2kÅ

WORST CASE CURRENT DENSITY:

1.6×10^4 A/cm^2

TRANSISTOR COUNT:

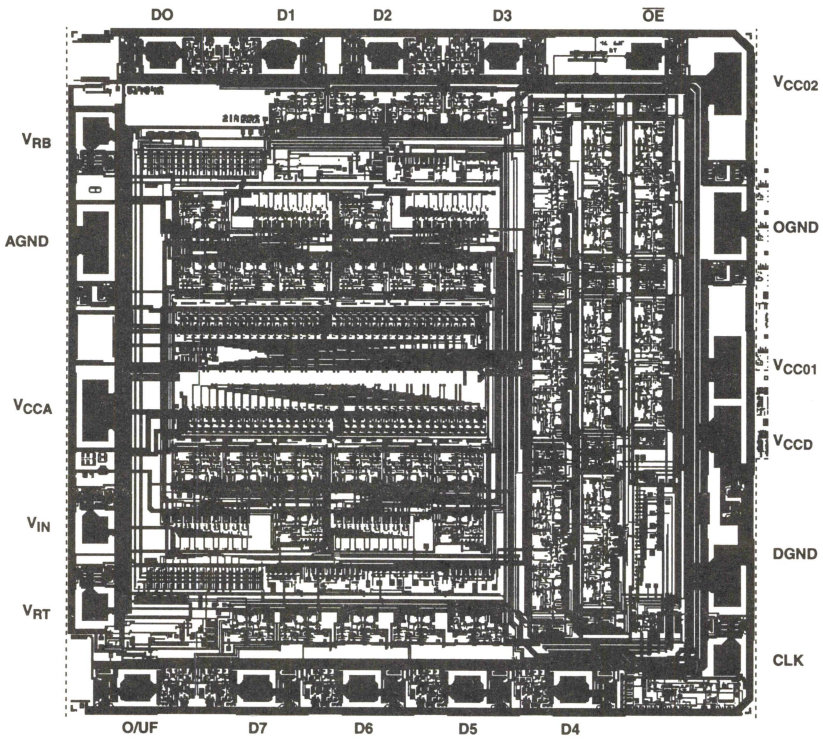
3714

DIE ATTACH:

Silver Filled Epoxy

Metallization Mask Layout

HI5714



HARRIS SEMICONDUCTOR

HI5746

August 1997

10-Bit, 40 MSPS A/D Converter

Features

- Sampling Rate ..... 40 MSPS
- 8.8 Bits at f_{IN} = 10MHz
- Low Power at 40 MSPS 225mW
- Wide Full Power Input Bandwidth 250MHz
- On-Chip Sample and Hold
- Fully Differential or Single-Ended Analog Input
- Single Supply Voltage .....+5V
- TTL/CMOS Compatible Digital Inputs
- CMOS Compatible Digital Outputs..... 3.0/5.0V
- Offset Binary or Two's Complement Output Format

Applications

- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition

Description

The HI5746 is a monolithic, 10-bit, analog-to-digital converter fabricated in a CMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 MSPS speed is made possible by a fully differential pipelined architecture with an internal sample and hold.

The HI5746 has excellent dynamic performance while consuming only 225mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles. It is pin-for-pin functionally compatible with the HI5702 and the HI5703.

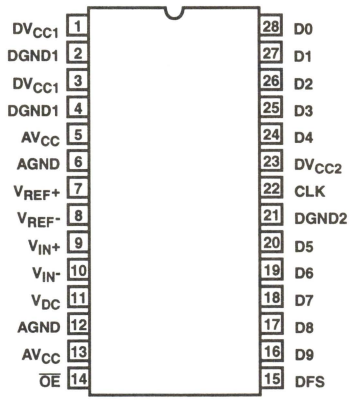
For internal voltage reference, please refer to the HI5767 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5746KCB	0 to 70	28 Ld SOIC (W)	M28.3
HI5746EVAL1	25	Evaluation Board	

Pinout

HI5746
(SOIC)
TOP VIEW



4 A/D CONVERTERS HIGH SPEED

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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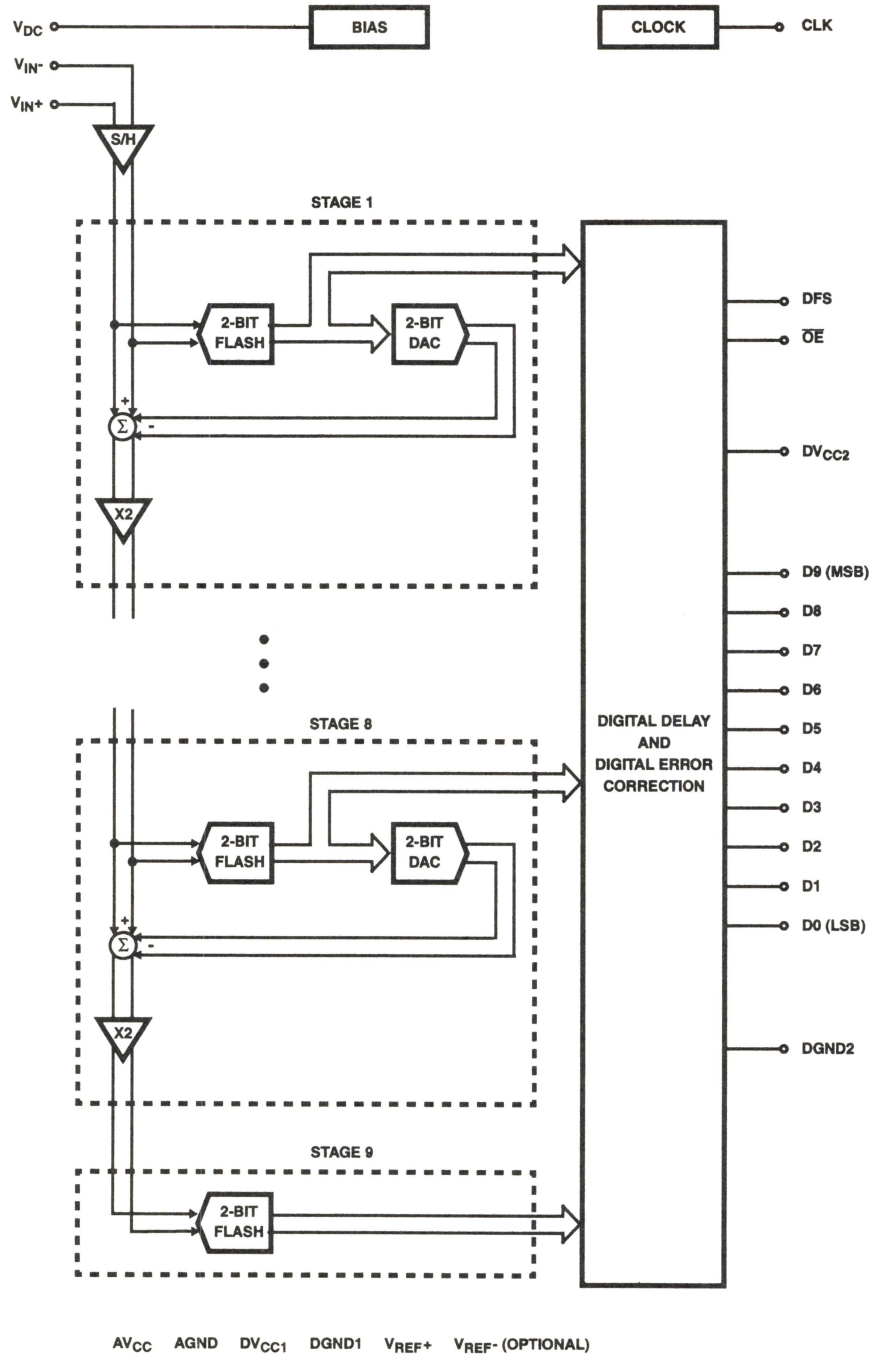
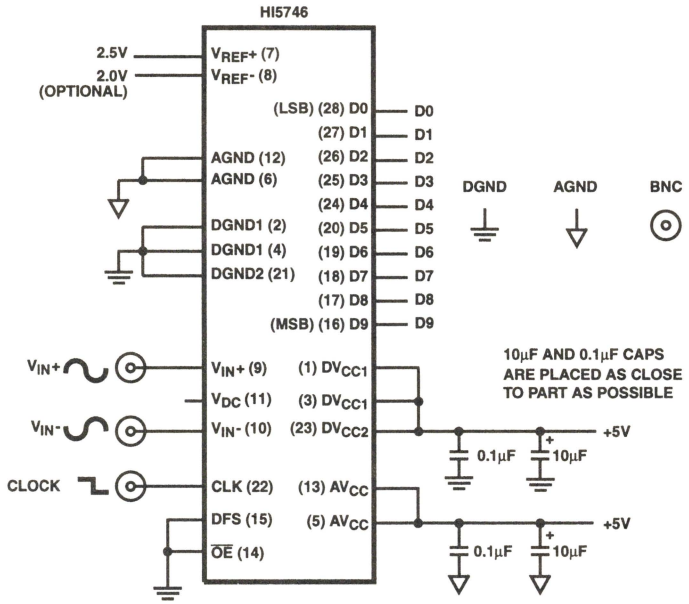
File Number 4129.2

Functional Block Diagram



Typical Application Schematic



Pin Descriptions

PIN NO.	NAME	DESCRIPTION
1	DV_{CC1}	Digital Supply (+5.0V).
2	DGND1	Digital Ground.
3	DV_{CC1}	Digital Supply (+5.0V).
4	DGND1	Digital Ground.
5	AV_{CC}	Analog Supply (+5.0V).
6	AGND	Analog Ground.
7	$V_{REF}+$	+2.5V Positive Reference Voltage Input.
8	$V_{REF}-$	+2.0V Negative Reference Voltage Input (Optional).
9	$V_{IN}+$	Positive Analog Input.
10	$V_{IN}-$	Negative Analog Input.
11	V_{DC}	DC Bias Voltage Output.
12	AGND	Analog Ground.
13	AV_{CC}	Analog Supply (+5.0V).
14	$\overline{OE}$	Digital Output Enable Control Input.

PIN NO.	NAME	DESCRIPTION
15	DFS	Data Format Select Input.
16	D9	Data Bit 9 Output (MSB).
17	D8	Data Bit 8 Output.
18	D7	Data Bit 7 Output.
19	D6	Data Bit 6 Output.
20	D5	Data Bit 5 Output.
21	DGND2	Digital Ground.
22	CLK	Sample Clock Input.
23	DV_{CC2}	Digital Output Supply (+3.0V or +5.0V).
24	D4	Data Bit 4 Output.
25	D3	Data Bit 3 Output.
26	D2	Data Bit 2 Output.
27	D1	Data Bit 1 Output.
28	D0	Data Bit 0 Output (LSB).

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND 6V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{CC}
Analog I/O Pins. . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range
HI5746KCB (Typ) . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	70

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = 5.0V$; $DV_{CC2} = 3.0V$, $V_{REF}+ = 2.5V$; $V_{REF}- = 2.0V$; $f_S = 40$ MSPS at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±1.0	±2.0	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1.0	LSB
Offset Error, V_{OS}	f_{IN} = DC	-40	12	40	LSB
Full Scale Error, FSE	f_{IN} = DC	-	4	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	1	MSPS
Maximum Conversion Rate	No Missing Codes	40	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 10MHz	8.55	8.8	-	Bits
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 10MHz	53.2	54.9	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 10MHz	53.2	55.4	-	dB
Total Harmonic Distortion, THD	f_{IN} = 10MHz	-	-64.6	-	dBc
2nd Harmonic Distortion	f_{IN} = 10MHz	-	-67.8	-	dBc
3rd Harmonic Distortion	f_{IN} = 10MHz	-	-68.3	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 10MHz	-	67.8	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	64	-	dBc
Differential Gain Error	f_S = 17.72 MSPS, 6 Step, Mod Ramp	-	0.8	-	%
Differential Phase Error	f_S = 17.72 MSPS, 6 Step, Mod Ramp	-	0.1	-	Degree
Transient Response	(Note 2)	-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive (Note 2)	-	1	-	Cycle

Electrical Specifications $AV_{CC} = DV_{CC1} = 5.0V$; $DV_{CC2} = 3.0V$, $V_{REF+} = 2.5V$; $V_{REF-} = 2.0V$; $f_S = 40$ MSPS at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range ($V_{IN+} - V_{IN-}$)		-	±0.5	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	1.0	-	V
Analog Input Resistance, R_{IN}	(Note 3)	-	1	-	MΩ
Analog Input Capacitance, C_{IN}		-	10	-	pF
Analog Input Bias Current, I_{B+} or I_{B-}	(Note 3)	-10	-	+10	µA
Differential Analog Input Bias Current $I_{BDIFF} = (I_{B+} - I_{B-})$	(Note 3)	-	±0.5	-	µA
Full Power Input Bandwidth, FPBW		-	250	-	MHz
Analog Input Common Mode Voltage Range $(V_{IN+} + V_{IN-})/2$	Differential Mode (Note 2)	0.25	-	4.75	V
REFERENCE INPUT					
Total Reference Resistance, R_L	V_{REF+} to AGND	-	2.5K	-	Ω
Positive Reference Current, I_{REF+}		-	1.07	-	mA
Negative Reference Current, I_{REF-}		-	21	-	µA
Positive Reference Voltage Input, V_{REF+}	(Note 2)	-	2.5	-	V
Negative Reference Voltage Input, V_{REF-}	(Note 2)	-	2.0	-	V
Reference Common Mode Voltage $(V_{REF+} + V_{REF-})/2$	(Note 2)	-	2.25	-	V
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	3.2	-	V
Maximum Output Current		-	-	0.4	mA
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}	CLK, DFS, $\overline{OE}$	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	CLK, DFS, $\overline{OE}$	-	-	0.8	V
Input Logic High Current, I_{IH}	CLK, DFS, $\overline{OE}$, $V_{IH} = 5V$	-10.0	-	+10.0	µA
Input Logic Low Current, I_{IL}	CLK, DFS, $\overline{OE}$, $V_{IL} = 0V$	-10.0	-	+10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS					
Output Logic High Voltage, V_{OH}	$I_{OH} = 100µA$; $DV_{CC2} = 5V$	4.0	-	-	V
Output Logic Low Voltage, V_{OL}	$I_{OL} = 100µA$; $DV_{CC2} = 5V$	-	-	0.5	V
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/5V$; $DV_{CC2} = 5V$	-	±1	±10	µA
Output Logic High Voltage, V_{OH}	$I_{OH} = 100µA$; $DV_{CC2} = 3V$	2.4	-	-	V

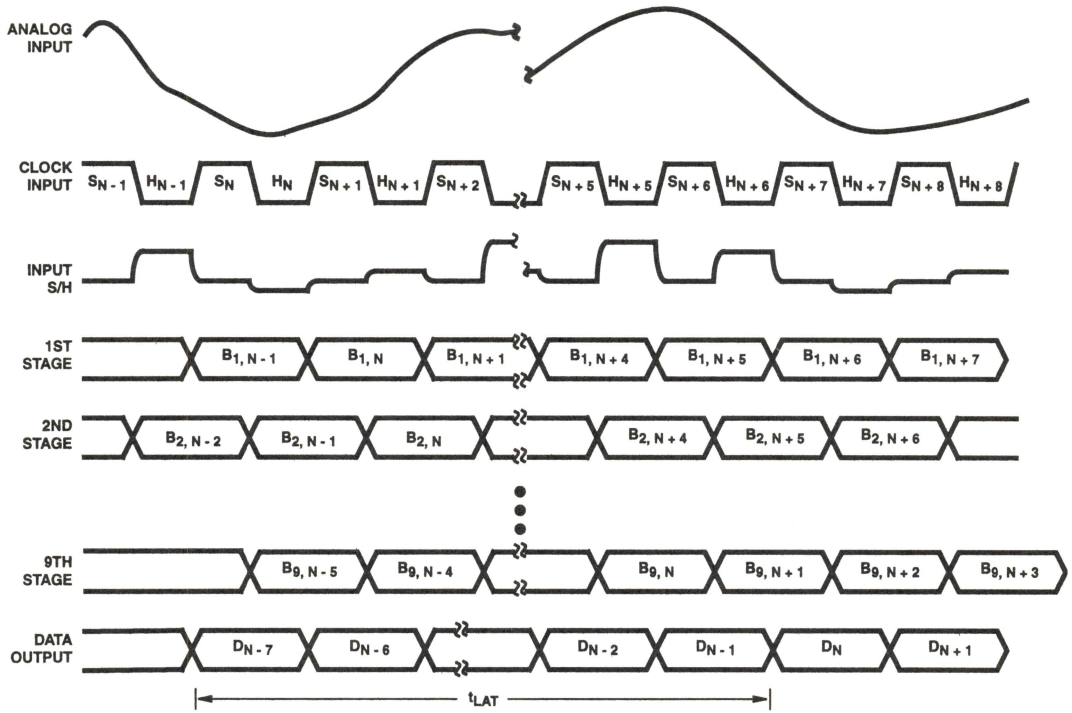
Electrical Specifications $AV_{CC} = DV_{CC1} = 5.0V$; $DV_{CC2} = 3.0V$, $V_{REF}+ = 2.5V$; $V_{REF}- = 2.0V$; $f_S = 40$ MSPS at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic Low Voltage, V_{OL}	$I_{OL} = 100\mu A$; $DV_{CC2} = 3V$	-	-	0.5	V
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/5V$; $DV_{CC2} = 3V$	-	±1	±10	µA
Output Capacitance, C_{OUT}		-	10	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps_{RMS}
Data Output Hold, t_H		-	7	-	ns
Data Output Delay, t_{OD}		-	8	-	ns
Data Output Enable Time, t_{EN}		-	5	-	ns
Data Output Enable Time t_{DIS}		-	5	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	7	Cycles
Power-Up Initialization	Data Invalid Time (Note 2)	-	-	20	Cycles
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, AV_{CC}		4.75	5.0	5.25	V
Digital Supply Voltage DV_{CC1}		4.75	5.0	5.25	V
Digital Output Supply Voltage, DV_{CC2}	At 3.0V	2.7	3.0	3.3	V
	At 5.0V	4.75	5.0	5.25	V
Total Supply Current, I_{CC}	$f_{IN} = 10MHz$ and DFS = "0"	-	46	-	mA
Analog Supply Current, AI_{CC}	$f_{IN} = 10MHz$ and DFS = "0"	-	30	-	mA
Digital Supply Current, DI_{CC}	$f_{IN} = 10MHz$ and DFS = "0"	-	13	-	mA
Output Supply Current, DI_{CC2}	$f_{IN} = 10MHz$ and DFS = "0"	-	3	-	mA
Power Dissipation	$f_{IN} = 10MHz$ and DFS = "0"	-	225	275	mW
Offset Error Sensitivity, ΔV_{OS}	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±0.4	-	LSB
Gain Error Sensitivity, ΔFSE	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±0.8	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock low and DC input.

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M,N}$: M-th stage digital output corresponding to N-th sampled input.
7. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5746 INTERNAL CIRCUIT TIMING

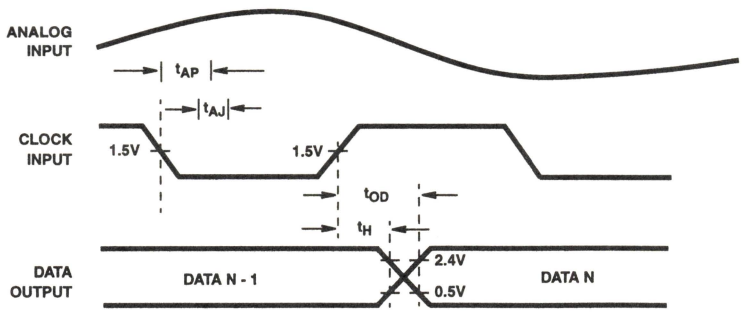


FIGURE 2. INPUT-TO OUTPUT TIMING

Typical Performance Curves

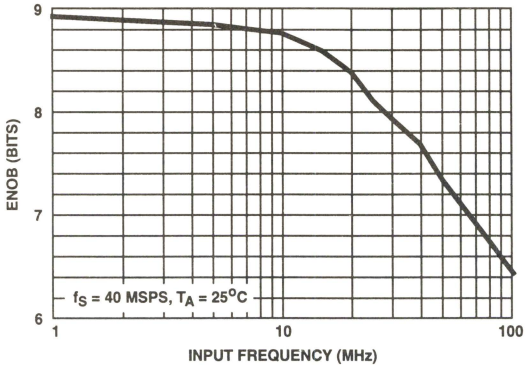


FIGURE 3. EFFECTIVE NUMBER OF BITS (ENOB) vs INPUT FREQUENCY

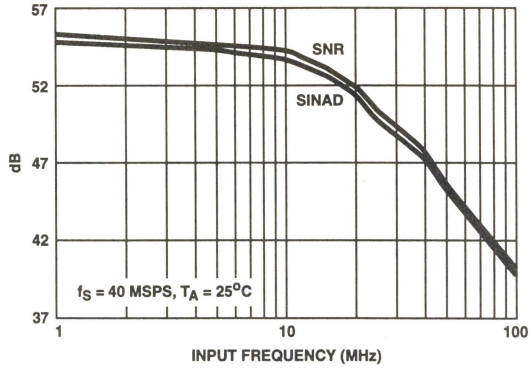
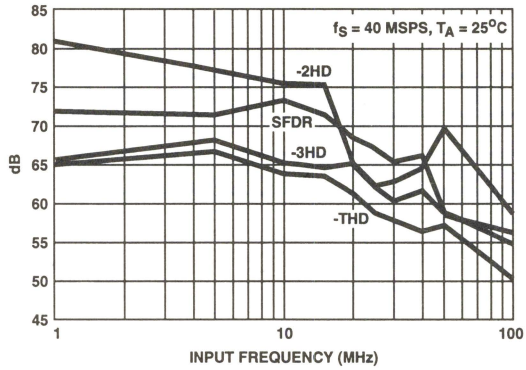


FIGURE 4. SINAD AND SNR vs INPUT FREQUENCY



NOTE: SFDR depicted here does not include any harmonic distortion.

FIGURE 5. -2HD, -3HD, -THD AND SFDR vs INPUT FREQUENCY

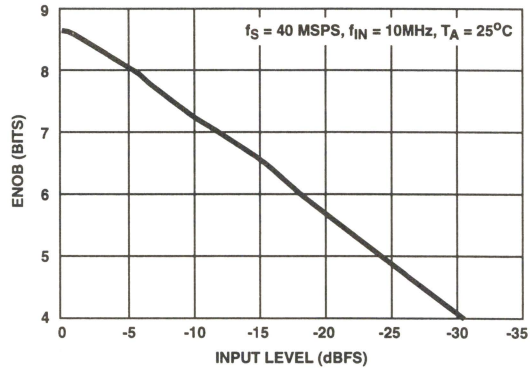


FIGURE 6. EFFECTIVE NUMBER OF BITS (ENOB) vs ANALOG INPUT LEVEL

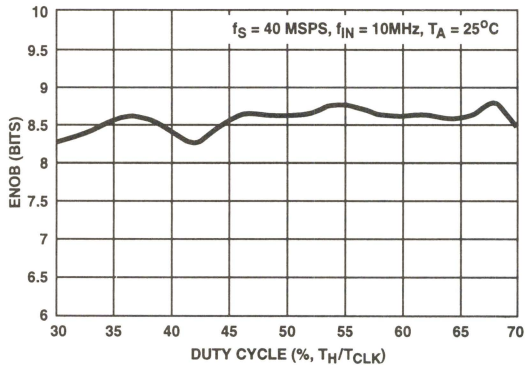


FIGURE 7. EFFECTIVE NUMBER OF BITS (ENOB) vs SAMPLE CLOCK DUTY CYCLE

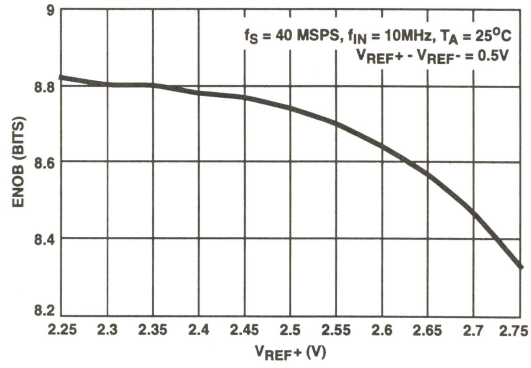


FIGURE 8. EFFECTIVE NUMBER OF BITS (ENOB) vs V_{REF}+

Typical Performance Curves (Continued)

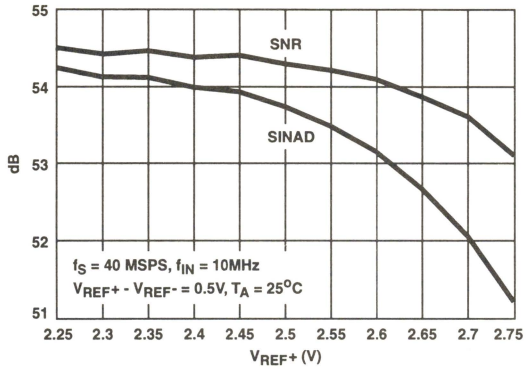
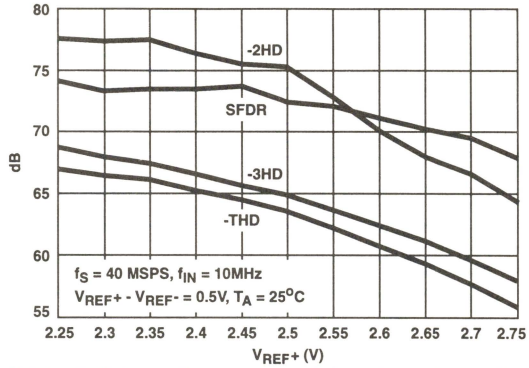


FIGURE 9. SINAD AND SNR vs V_{REF+}



NOTE: SFDR depicted here does not include any harmonic distortion.

FIGURE 10. -2HD, -3HD, -THD AND SFDR vs V_{REF+}

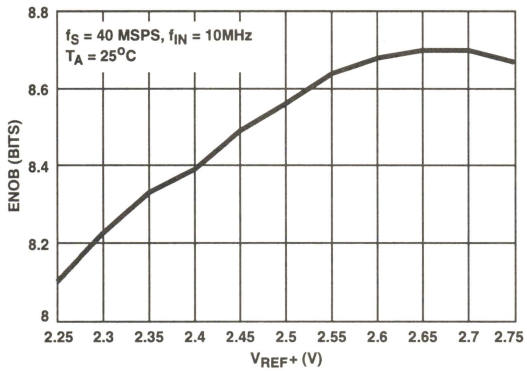


FIGURE 11. EFFECTIVE NUMBER OF BITS (ENOB) vs V_{REF+} (V_{REF-} NOT DRIVEN)

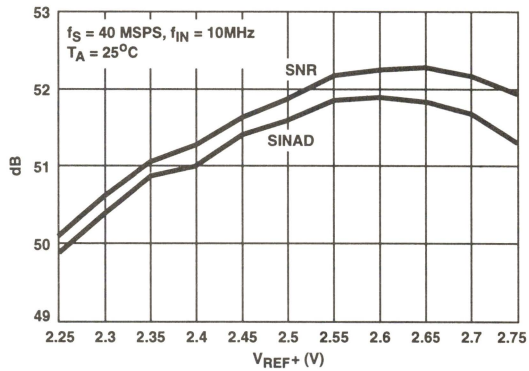


FIGURE 12. SINAD AND SNR vs V_{REF+} (V_{REF-} NOT DRIVEN)

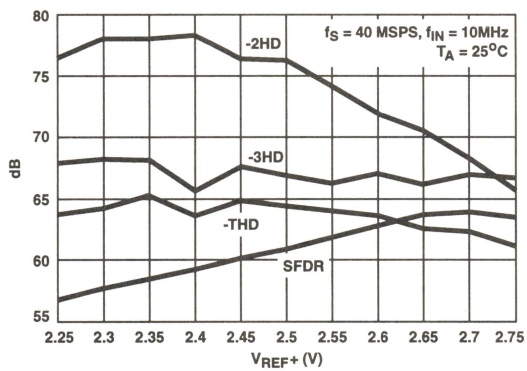


FIGURE 13. -2HD, -3HD, -THD AND SFDR vs V_{REF+} (V_{REF-} NOT DRIVEN)

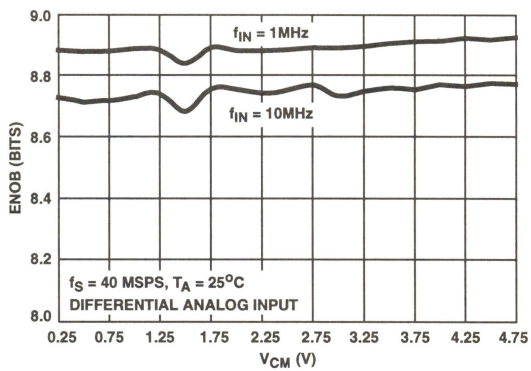


FIGURE 14. EFFECTIVE NUMBER OF BITS (ENOB) vs ANALOG INPUT COMMON MODE VOLTAGE

Typical Performance Curves (Continued)

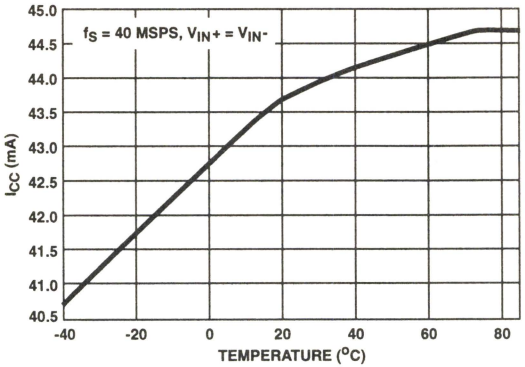


FIGURE 15. TOTAL SUPPLY CURRENT vs TEMPERATURE

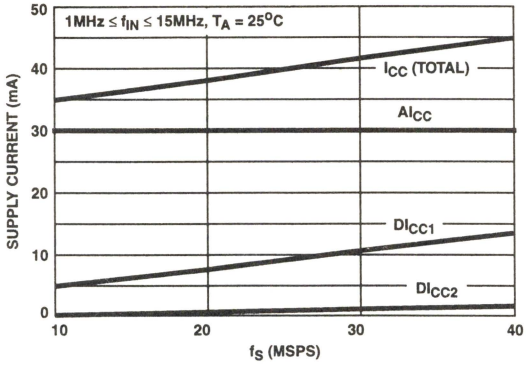


FIGURE 16. SUPPLY CURRENT vs SAMPLE CLOCK FREQUENCY

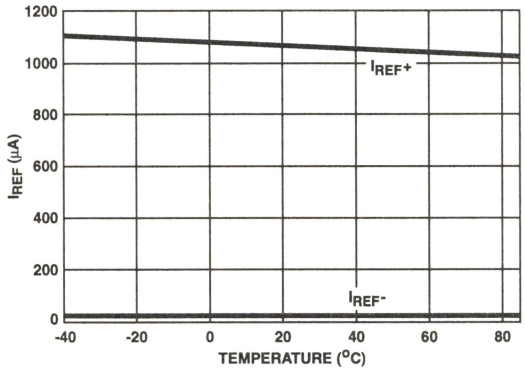


FIGURE 17. REFERENCE CURRENT vs TEMPERATURE

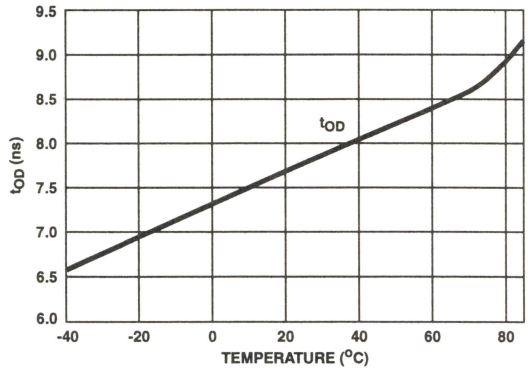


FIGURE 18. DATA OUTPUT DELAY vs TEMPERATURE

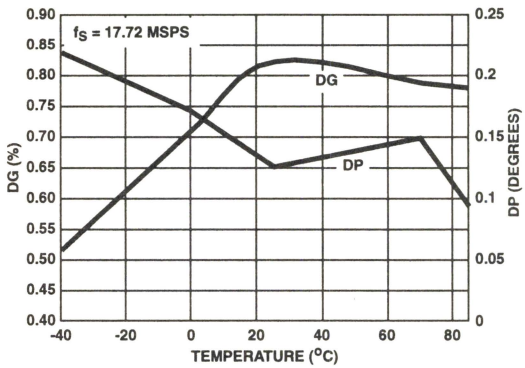


FIGURE 19. DIFFERENTIAL GAIN/PHASE vs TEMPERATURE

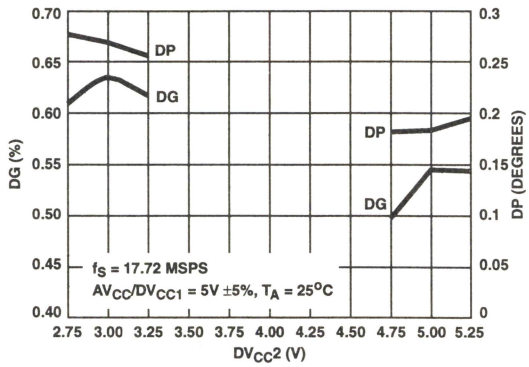


FIGURE 20. DIFFERENTIAL GAIN/PHASE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

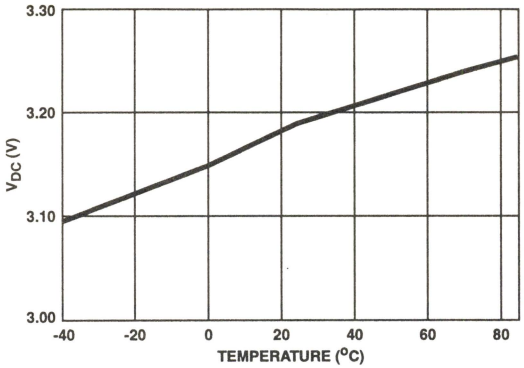


FIGURE 21. DC BIAS VOLTAGE (V_{DC}) vs TEMPERATURE

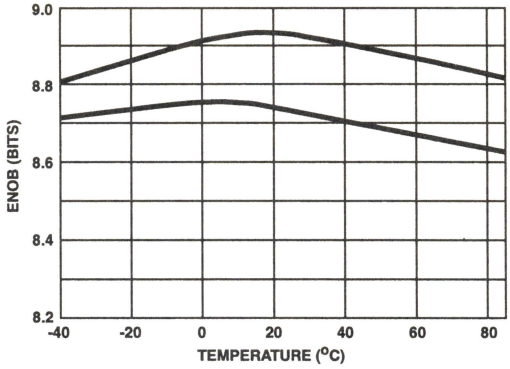


FIGURE 22. EFFECTIVE NUMBER OF BITS F(ENOB) vs TEMPERATURE

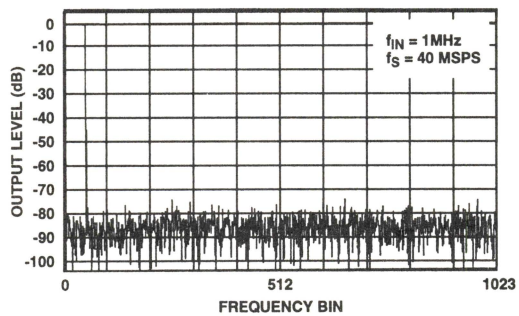


FIGURE 23. 2048 POINT FFT PLOT

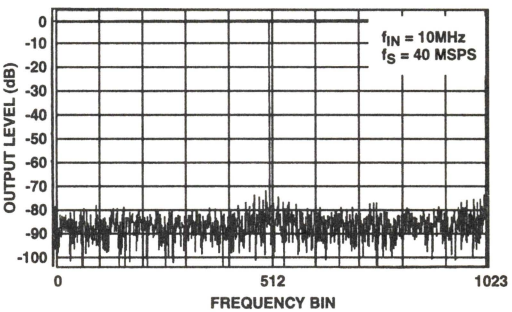


FIGURE 24. 2048 POINT FFT SPECTRAL PLOT

Detailed Description

Theory of Operation

The HI5746 is a 10-bit fully differential sampling pipeline A/D converter with digital error correction logic. Figure 25 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal sampling clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master sampling clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The front end sample-and-hold output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

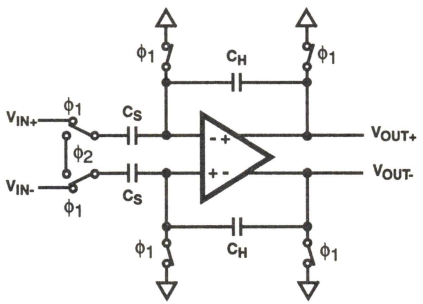


FIGURE 25. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, eight identical pipeline subconverter stages, each containing a two-bit flash converter and a

two-bit multiplying digital-to-analog converter, follow the S/H circuit with the ninth stage being a two bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The output of each of the eight identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the eight identical two-bit subconverter stages with the corresponding output of the ninth stage flash converter before applying the eighteen bit result to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final ten bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital output data is synchronized to the external sampling clock by a double buffered latching technique. The output of the digital error correction circuit is available in two's complement or offset binary format depending on the state of the Data Format Select (DFS) control input (see Table 1, A/D Code Table).

Reference Voltage Inputs, V_{REF}- and V_{REF}+

The HI5746 is designed to accept two external reference voltage sources at the V_{REF} input pins. Typical operation of the converter requires V_{REF}+ to be set at +2.5V and V_{REF}- to be set at 2.0V. However, it should be noted that the input structure of the V_{REF}+ and V_{REF}- input pins consists of a resistive voltage divider with one resistor of the divider (nominally 500Ω) connected between V_{REF}+ and V_{REF}- and the other resistor of the divider (nominally 2000Ω) connected between V_{REF}- and analog ground. This allows the user the option of supplying only the +2.5V V_{REF}+ voltage reference with the +2.0V V_{REF}- being generated internally by the voltage division action of the input structure.

The HI5746 is tested with V_{REF}- equal to +2.0V and V_{REF}+ equal to +2.5V yielding a fully differential analog input voltage range of ±0.5V. V_{REF}+ and V_{REF}- can differ from the above voltages (see the Typical Performance Curves, Figure 8 through Figure 13).

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at **both** of the reference voltage input pins, V_{REF}+ and V_{REF}-.

Analog Input, Differential Connection

The analog input to the HI5746 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 26 and Figure 27) will give the best performance for the converter.

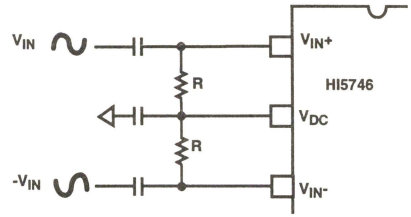


FIGURE 26. AC COUPLED DIFFERENTIAL INPUT

Since the HI5746 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V. For the differential input connection this implies the analog input common mode voltage can range from 0.25V to 4.75V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A DC voltage source, V_{DC}, equal to 3.2V (typical), is made available to the user to help simplify circuit design when using an AC coupled differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent DC bias source and stays well within the analog input common mode voltage range over temperature (see the Typical Performance Curves, Figure 21).

For the AC coupled differential input (Figure 26) assume the difference between V_{REF}+, typically 2.5V, and V_{REF}-, typically 2.0V, is 0.5V. Full scale is achieved when the V_{IN} and -V_{IN} input signals are $0.5V_{P-P}$, with -V_{IN} being 180 degrees out of phase with V_{IN}. The converter will be at positive full scale when the V_{IN}+ input is at V_{DC} + 0.25V and the V_{IN}- input is at V_{DC} - 0.25V (V_{IN}+ - V_{IN}- = +0.5V). Conversely, the converter will be at negative fullscale when the V_{IN}+ input is equal to V_{DC} - 0.25V and V_{IN}- is at V_{DC} + 0.25V (V_{IN}+ - V_{IN}- = -0.5V).

The analog input can be DC coupled (Figure 27) as long as the inputs are within the analog input common mode voltage range (0.25V ≤ VDC ≤ 4.75V).

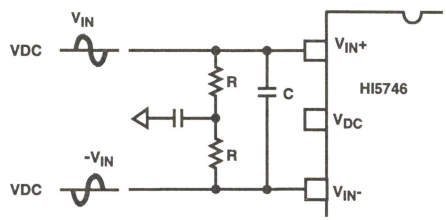


FIGURE 27. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 27 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from V_{IN}+ to V_{IN}- will help filter any high fre-

quency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

Analog Input, Single-Ended Connection

The configuration shown in Figure 28 may be used with a single ended AC coupled input.

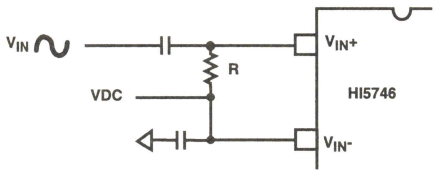


FIGURE 28. AC COUPLED SINGLE ENDED INPUT

Again, assume the difference between V_{REF+}, typically 2.5V, and V_{REF-}, typically 2V, is 0.5V. If V_{IN} is a $1V_{P-P}$ sinewave, then V_{IN+} is a $1V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive full scale when V_{IN+} is at VDC + 0.5V (V_{IN+} - V_{IN-} = +0.5V) and will be at negative full scale when V_{IN+} is equal to VDC - 0.5V (V_{IN+} - V_{IN-} = -0.5V). Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND. In this case, VDC could range between 0.5V and 4.5V without a significant change in ADC performance. The simplest way to produce VDC is to use the DC bias source, V_{DC}, output of the HI5746.

The single ended analog input can be DC coupled (Figure 27) as long as the input is within the analog input common mode voltage range.

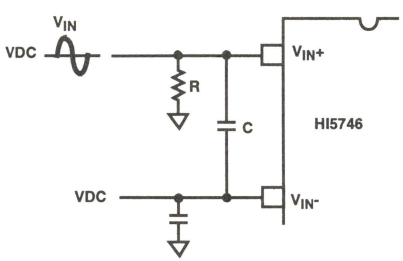


FIGURE 29. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 29 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from V_{IN+} to V_{IN-} will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

A single ended source may give better overall system performance if it is first converted to differential before driving the HI5746.

Digital Output Control and Clock Requirements

The HI5746 provides a standard high-speed interface to external TTL logic families.

In order to ensure rated performance of the HI5746, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5746 will only be guaranteed at conversion rates above 1 MSPS. This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1 MSPS will have to be performed before valid data is available.

A Data Format Select (DFS) pin is provided which will determine the format of the digital data outputs. When at logic low, the data will be output in offset binary format. When at logic high, the data will be output in two's complement format. Refer to Table 1 for further information.

The output enable pin, $\overline{OE}$, when pulled high will three-state the digital outputs to a high impedance state. Set the $\overline{OE}$ input to logic low for normal operation.

$\overline{OE}$ INPUT	DIGITAL DATA OUTPUTS
0	Active
1	High Impedance

Supply and Ground Considerations

The HI5746 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The digital data outputs also have a separate supply pin, DV_{CC2}, which can be powered from a 3V or 5V supply. This allows the outputs to interface with 3V logic if so desired.

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE ($V_{IN}+ - V_{IN}-$)	OFFSET BINARY OUTPUT CODE (DFS LOW)										TWO'S COMPLEMENT OUTPUT CODE (DFS HIGH)									
		MSB									LSB	MSB									LSB
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) -1/4 LSB	0.499756V	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
+FS - 1 1/4 LSB	0.498779V	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
+3/4 LSB	732.422µV	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-1/4 LSB	-244.141µV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-FS + 1 3/4 LSB	-0.498291V	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + 3/4 LSB	-0.499268V	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

NOTES:

8. The voltages listed above represent the ideal center of each output code shown as a function of the reference differential voltage, ($V_{REF}+ - V_{REF}-$) = 0.5V.
9. $V_{REF}+$ = 2.5V and $V_{REF}-$ = 2V.

The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5746 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the application note "Using Harris High Speed A/D Converters" (AN9214) for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level 1/4 LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is 3/4 LSB below positive Full scale (+FS) with the offset error removed. Fullscale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Sensitivity

Each of the power supplies are moved plus and minus 5% and the shift in the offset and full scale error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5746. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from Fullscale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by:

ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02,

where: V_{CORR} = 0.5 dB.

V_{CORR} adjusts the SINAD, and hence the ENOB, for the amount the analog input signal is below fullscale.

Signal To Noise and Distortion Ratio (SINAD)

SINAD is the ratio of the measured RMS signal to RMS sum of all the other spectral components below the Nyquist frequency, $f_S/2$, excluding DC.

Signal To Noise Ratio (SNR)

SNR is the ratio of the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components below $f_S/2$ excluding the fundamental, the first five harmonics and DC.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spectral component in the spectrum below $f_S/2$.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present at the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are (f_1+f_2), (f_1-f_2), $(2f_1)$, $(2f_2)$, $(2f_1+f_2)$, $(2f_1-f_2)$, (f_1+2f_2), (f_1-2f_2). The ADC is tested with each tone 6dB below full scale.

Transient Response

Transient response is measured by providing a full scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Over-Voltage Recovery

Over-Voltage Recovery is measured by providing a full scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the analog input frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has an amplitude which swings from -FS to +FS. The bandwidth given is measured at the specified sampling frequency.

Video Definitions

Differential Gain and Differential Phase are two commonly found video specifications for characterizing the distortion of a chrominance signal as it is offset through the input voltage range of an ADC.

Differential Gain (DG)

Differential Gain is the peak difference in chrominance amplitude (in percent) relative to the reference burst.

Differential Phase (DP)

Differential Phase is the peak difference in chrominance phase (in degrees) relative to the reference burst.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This is due to the pipeline nature of the converter where the analog sample has to ripple through the internal subconverter stages. This delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital data lags the analog input sample by 7 sample clock cycles.

Power-Up Initialization

This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.

HFA1100	HI5703	HSP9501	HI5780	HA5020
HFA1105	HI5746	HSP48410	HI1171	HA2842
HFA1106	HI5767	HSP48908	HI3338	HFA1115
HFA1135		HSP48212		HFA1212
HFA1145		HSP43891		HFA1412
HFA1245		HSP43168		
		HSP43216		

HFA1100: 850MHz Video Op Amp
HFA1105: 300MHz Video Op Amp
HFA1106: 250MHz Video Op Amp with Bandwidth Limit Control
HFA1135: 350MHz Video Op Amp with Output Limiting
HFA1145: 300MHz Video Op Amp with Output Disable
HFA1245: Dual, 350MHz, Video Op Amp with Output Disable
HI5703: 10-Bit, 40 MSPS, Low Power A/D Converter
HI5746: 10-Bit, 40 MSPS, Very Low Power A/D Converter
HI5767: 10-Bit, 40 MSPS A/D Converter with Voltage Reference
HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48212: Digital Video Mixer
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HI5780: 10-Bit, 80 MSPS, Video D/A Converter
HI1171: 8-Bit, 40 MSPS, Video D/A Converter
HI3338: 8-Bit, 50 MSPS, Video D/A Converter
HA5020: 100MHz Video Op Amp
HA2842: High Output Current, Video Op Amp
HFA1115: 225MHz Programmable Gain Video Buffer with Output Limiting
HFA1212: 350MHz Dual Programmable Gain Video Buffer
HFA1412: 350MHz Quad Programmable Gain Video Buffer

In addition, CMOS Logic Families in HC/HCT, AC/ACT, FCT and CD4000 are available.

FIGURE 30. 10-BIT VIDEO IMAGING COMPONENTS

HFA1100	HI5703	HSP43168	HI5721	HFA1112
HFA1110	HI5746	HSP43216	HI5780	HFA1113
HFA3101	HI5767	HSP43220	HI20201	
HFA3102		HSP43891	HI20203	
HFA3600		HSP50016		
		HSP50110		
		HSP50210		

HFA1100: 850MHz Op Amp
HFA1110: 750MHz Unity Gain Video Buffer
HFA3101: Gilbert Cell Transistor Array
HFA3102: Dual Long-Tailed Pair Transistor Array
HFA3600: Low Noise Amplifier/Mixer
HI5703: 10-Bit, 40 MSPS, Low Power A/D Converter
HI5746: 10-Bit, 40 MSPS, Very Low Power A/D Converter
HI5767: 10-Bit, 40 MSPS A/D Converter with Voltage Reference
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HSP43220: Decimating Digital Filter
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP50016: Digital Down Converter
HSP50110: Digital Quadrature Tuner
HSP50210: Digital Costas Loop
HI5721: 10-Bit, 100 MSPS, Communications D/A Converter
HI5780: 10-Bit, 80 MSPS, D/A Converter
HI20201: 10-Bit, 160 MSPS, High Speed D/A Converter
HI20203: 8-Bit, 160 MSPS, High Speed D/A Converter
HFA1112: 850MHz Programmable Gain Video Buffer
HFA1113: 850MHz Programmable Gain Video Buffer with Output Limiting

In addition, CMOS Logic Families in HC/HCT, AC/ACT, FCT and CD4000 are available.

FIGURE 31. 10-BIT COMMUNICATIONS COMPONENTS

HARRIS SEMICONDUCTOR

HI5762

PRELIMINARY

August 1997

Dual 10-Bit, 40/60 MSPS A/D Converter with Internal Voltage Reference

Features

- Sampling Rate ..... 60 MSPS
- 8.3 Bits at f_{IN} = 10MHz
- Low Power at 60 MSPS 600mW
- Wide Full Power Input Bandwidth 250MHz
- On-Chip Sample and Holds
- Internal Band-gap Voltage Reference 2.5V
- Fully Differential or Single-Ended Analog Inputs
- Single Supply Voltage .....+5V
- TTL/CMOS Compatible Digital Inputs
- CMOS Compatible Digital Outputs..... 3.0/5.0V
- Offset Binary Digital Data Output Format

Applications

- Wireless Local Loop
- I/Q Demodulation
- Medical Imaging
- High Speed Data Acquisition

Description

The HI5762 is a monolithic, dual 10-bit, analog-to-digital converter fabricated in a CMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 and 60 MSPS speed is made possible by a fully differential pipelined architecture with both an internal sample and hold and internal band-gap voltage reference.

The HI5762 has excellent dynamic performance while consuming only 600mW power at 60 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles.

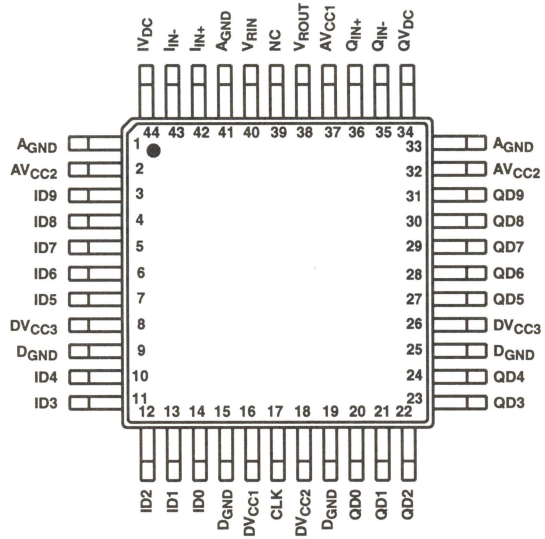
Refer to the HI5662 data sheet for 8-bit resolution.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5762/4IN	-40 to 85	44 Ld MQFP	Q44.10x10
HI5762/6IN	-40 to 85	44 Ld MQFP	Q44.10x10
HI5762EVAL1	25	Evaluation Board	

Pinout

HI5762
(MQFP)
TOP VIEW



4 A/D CONVERTERS HIGH SPEED

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 4318

HARRIS SEMICONDUCTOR

HI5766

August 1997

10-Bit, 60 MSPS A/D Converter

Features

- Sampling Rate ..... 60 MSPS
- 8.3 Bits at f_{IN} = 10MHz
- Low Power at 60 MSPS 260mW
- Wide Full Power Input Bandwidth 250MHz
- On Chip Sample and Hold
- Fully Differential or Single-Ended Analog Input
- Single Supply Voltage .....+5V
- TTL/CMOS Compatible Digital Inputs
- CMOS Compatible Digital Outputs..... 3.0/5.0V
- Offset Binary or Two's Complement Output Format

Applications

- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition

Description

The HI5766 is a monolithic, 10-bit, analog-to-digital converter fabricated in a CMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 60 MSPS speed is made possible by a fully differential pipelined architecture with an internal sample and hold.

The HI5766 has excellent dynamic performance while consuming only 260mW power at 60 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles. It is pin-for-pin functionally compatible with the HI5702, HI5703 and the HI5746.

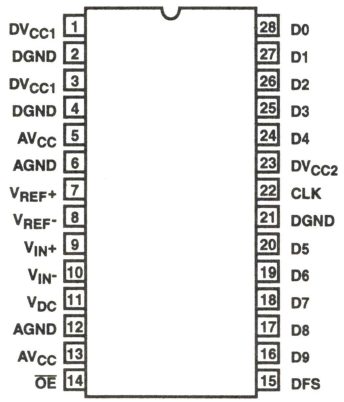
For internal voltage reference, please refer to the HI7567 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5766KCB	0 to 70	28 Ld SOIC (W)	M28.3
HI5766EVAL1	25	Evaluation Board	

Pinout

HI5766
(SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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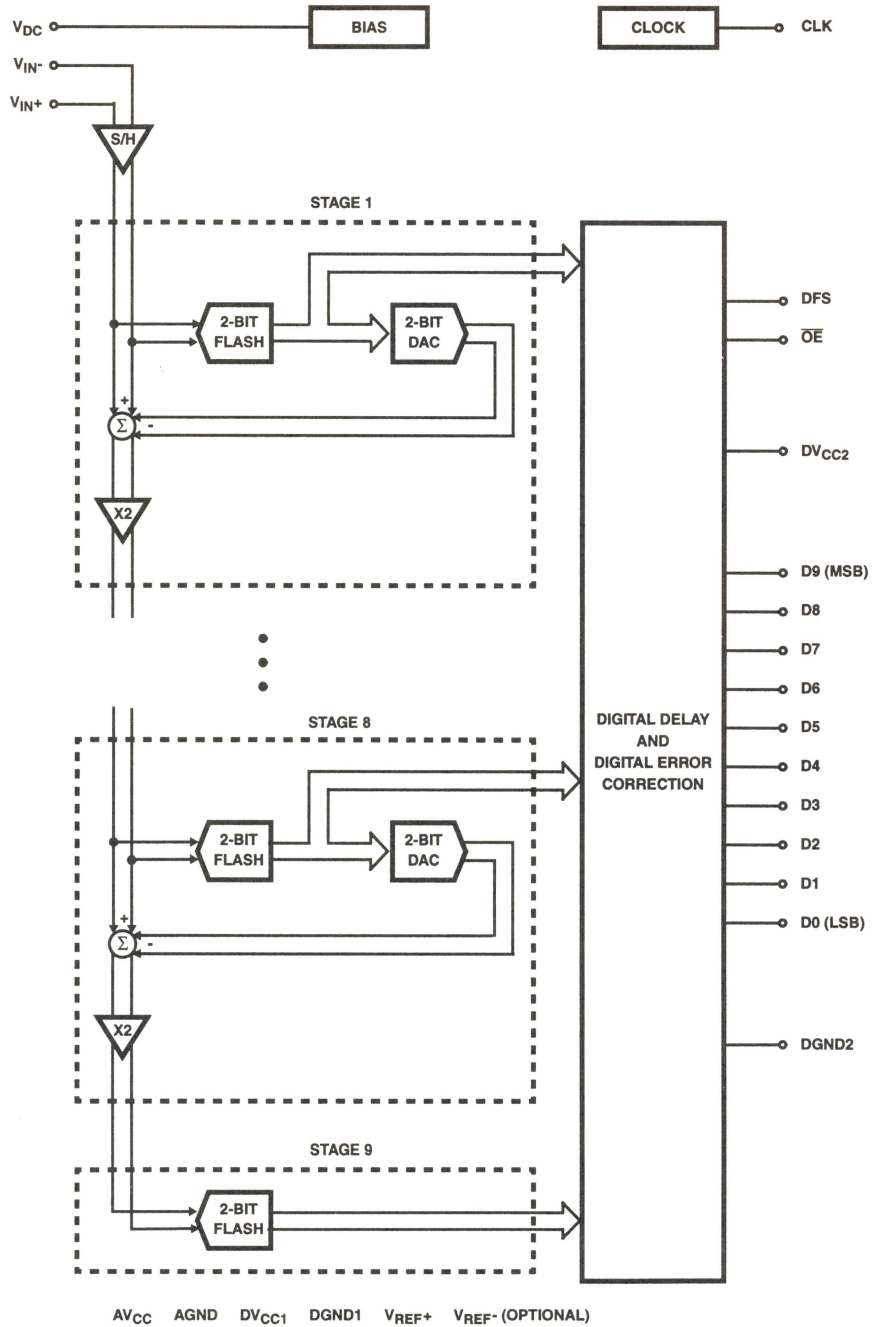
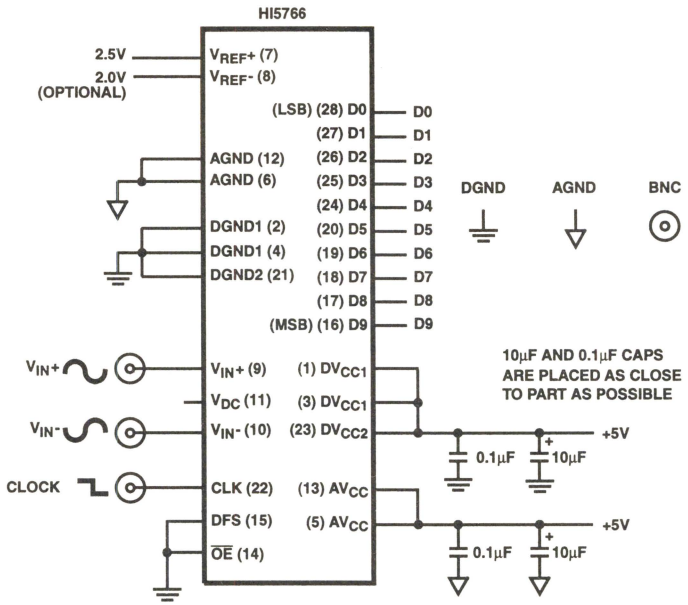
File Number **4130.3**

Functional Block Diagram



Typical Application Schematic



Pin Descriptions

PIN NO.	NAME	DESCRIPTION
1	DV_{CC1}	Digital Supply (+5.0V).
2	DGND1	Digital Ground.
3	DV_{CC1}	Digital Supply (+5.0V).
4	DGND1	Digital Ground.
5	AV_{CC}	Analog Supply (+5.0V).
6	AGND	Analog Ground.
7	V_{REF+}	+2.5V Positive Reference Voltage Input.
8	V_{REF-}	+2.0V Negative Reference Voltage Input (Optional).
9	V_{IN+}	Positive Analog Input.
10	V_{IN-}	Negative Analog Input.
11	V_{DC}	DC Bias Voltage Output.
12	AGND	Analog Ground.
13	AV_{CC}	Analog Supply (+5.0V).
14	$\overline{OE}$	Digital Output Enable Control Input.

PIN NO.	NAME	DESCRIPTION
15	DFS	Data Format Select Input.
16	D9	Data Bit 9 Output (MSB).
17	D8	Data Bit 8 Output.
18	D7	Data Bit 7 Output.
19	D6	Data Bit 6 Output.
20	D5	Data Bit 5 Output.
21	DGND2	Digital Ground.
22	CLK	Sample Clock Input.
23	DV_{CC2}	Digital Output Supply (+3.0V or +5.0V).
24	D4	Data Bit 4 Output.
25	D3	Data Bit 3 Output.
26	D2	Data Bit 2 Output.
27	D1	Data Bit 1 Output.
28	D0	Data Bit 0 Output (LSB).

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND 6V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{CC}
Analog I/O Pins. . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range
HI5766KCB (Typ) . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
HI5766KCB	70

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = 5.0V$, $DV_{CC2} = 3.0V$; $V_{REF}+ = 2.5V$; $V_{REF}- = 2.0V$; $f_S = 60$ MSPS at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±1.0	±2.0	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1.0	LSB
Offset Error, V_{OS}	f_{IN} = DC	-40	12	+40	LSB
Full Scale Error, FSE	f_{IN} = DC	-	4	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	1	MSPS
Maximum Conversion Rate	No Missing Codes	60	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 10MHz	-	8.3	-	Bits
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 10MHz	-	51.7	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 10MHz	-	53.7	-	dB
Total Harmonic Distortion, THD	f_{IN} = 10MHz	-	-56.2	-	dBc
2nd Harmonic Distortion	f_{IN} = 10MHz	-	-61.6	-	dBc
3rd Harmonic Distortion	f_{IN} = 10MHz	-	-58.1	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 10MHz	-	58.1	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	62	-	dBc
Differential Gain Error	f_S = 17.72 MSPS, 6 Step, Mod Ramp	-	0.8	-	%
Differential Phase Error	f_S = 17.72 MSPS, 6 Step, Mod Ramp	-	0.1	-	Degree
Transient Response	(Note 2)	-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive (Note 2)	-	1	-	Cycle
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range ($V_{IN}+ - V_{IN}-$)		-	±0.5	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	1.0	-	V
Analog Input Resistance, R_{IN}	(Note 3)	-	1	-	MΩ

Electrical Specifications $AV_{CC} = DV_{CC1} = 5.0V$, $DV_{CC2} = 3.0V$; $V_{REF}+ = 2.5V$; $V_{REF}- = 2.0V$; $f_S = 60$ MSPS at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input Capacitance, C_{IN}		-	10	-	pF
Analog Input Bias Current, $I_{B}+$ or $I_{B}-$	(Note 3)	-10	-	+10	µA
Differential Analog Input Bias Current $I_{BDIFF} = (I_{B}+ - I_{B}-)$	(Note 3)	-	±0.5	-	µA
Full Power Input Bandwidth, FPBW		-	250	-	MHz
Analog Input Common Mode Voltage Range $(V_{IN}+ + V_{IN}-) / 2$	Differential Mode (Note 2)	0.25	-	4.75	V
REFERENCE INPUT					
Total Reference Resistance, R_L		-	2.5K	-	Ω
Reference Current		-	1.0	-	mA
Positive Reference Voltage Input, $V_{REF}+$	(Note 2)	-	2.5	-	V
Negative Reference Voltage Input, $V_{REF}-$	(Note 2)	-	2.0	-	V
Reference Common Mode Voltage $(V_{REF}+ + V_{REF}-) / 2$	(Note 2)	-	2.25	-	V
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	3.2	-	V
Maximum Output Current		-	-	0.4	mA
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}	CLK, DFS, $\overline{OE}$	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	CLK, DFS, $\overline{OE}$	-	-	0.8	V
Input Logic High Current, I_{IH}	CLK, DFS, $\overline{OE}$, $V_{IH} = 5V$	-10.0	-	+10.0	µA
Input Logic Low Current, I_{IL}	CLK, DFS,$\overline{OE}$, $V_{IL} = 0V$	-10.0	-	+10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS					
Output Logic High Voltage, V_{OH}	$I_{OH} = 100µA$; $DV_{CC2} = 5V$	4.0	-	-	V
Output Logic Low Voltage, V_{OL}	$I_{OL} = 100µA$; $DV_{CC2} = 5V$	-	-	0.5	V
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/5V$; $DV_{CC2} = 5V$	-	±1	±10	µA
Output Logic High Voltage, V_{OH}	$I_{OH} = 100µA$; $DV_{CC2} = 3V$	2.4	-	-	V
Output Logic Low Voltage, V_{OL}	$I_{OL} = 100µA$; $DV_{CC2} = 3V$	-	-	0.5	V
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/5V$; $DV_{CC2} = 3V$	-	±1	±10	µA
Output Capacitance, C_{OUT}		-	10	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps_{RMS}
Data Output Hold, t_H		-	7	-	ns
Data Output Delay, t_{OD}		-	8	-	ns
Data Output Enable Time, t_{EN}		-	5	-	ns
Data Output Enable Time, t_{DIS}		-	5	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	7	Cycles
Power-Up Initialization	Data Invalid Time (Note 2)	-	-	20	Cycles

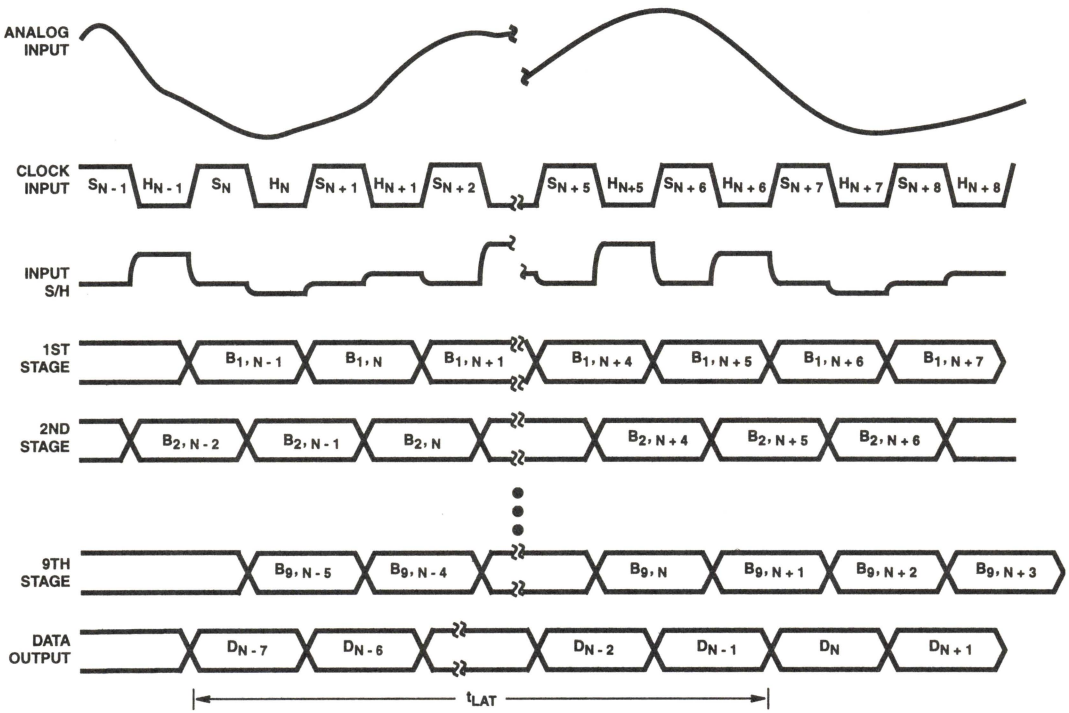
Electrical Specifications $AV_{CC} = DV_{CC1} = 5.0V$, $DV_{CC2} = 3.0V$; $V_{REF}+ = 2.5V$; $V_{REF}- = 2.0V$; $f_S = 60$ MSPS at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25°C, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, AV_{CC}		4.75	5.0	5.25	V
Digital Supply Voltage, DV_{CC1}		4.75	5.0	5.25	V
Digital Output Supply Voltage, DV_{CC2}	At 3.0V	2.7	3.0	3.3	V
	At 5.0V	4.75	5.0	5.25	V
Supply Current, I_{CC}	$V_{IN}+ - V_{IN}- = 1.25V$ and DFS = "0"	-	52	-	mA
Power Dissipation	$V_I+ - V_{IN}- = 1.25V$ and DFS = "0"	-	260	-	mW
Offset Error Sensitivity, ΔV_{OS}	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±0.4	-	LSB
Gain Error Sensitivity, ΔFSE	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±0.8	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock low and DC input.

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M,N}$: M-th stage digital output corresponding to N-th sampled input.
7. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5766 INTERNAL CIRCUIT TIMING

Timing Waveforms

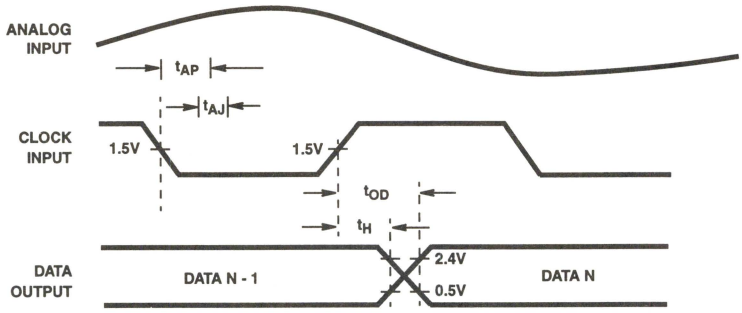


FIGURE 2. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

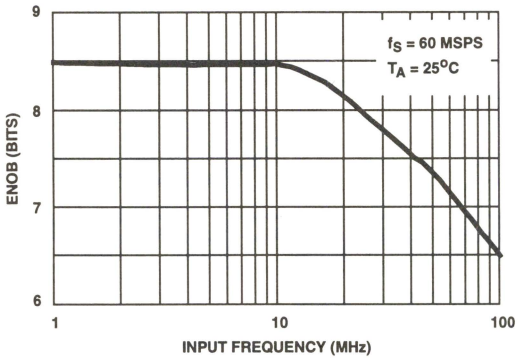


FIGURE 3. EFFECTIVE NUMBER OF BITS (ENOB) vs INPUT FREQUENCY

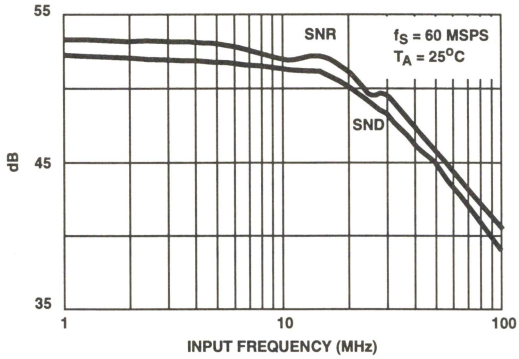
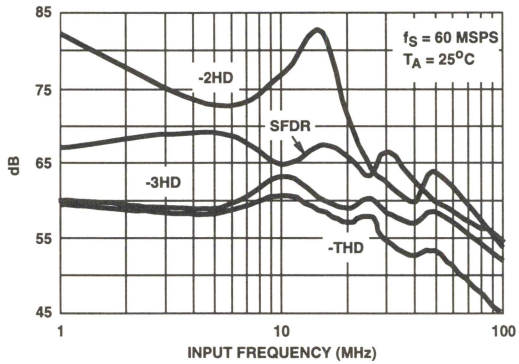


FIGURE 4. SINAD AND SNR vs INPUT FREQUENCY



NOTE: SFDR depicted here does not include any harmonic distortion.

FIGURE 5. -2HD, -3HD, -THD AND SFDR vs INPUT FREQUENCY

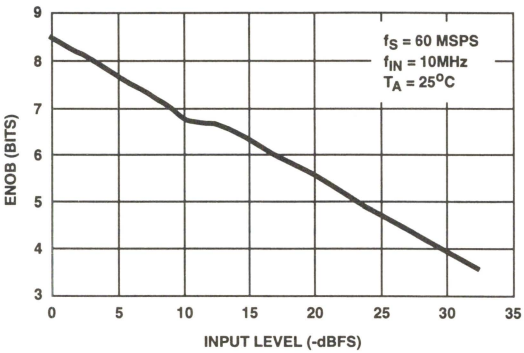


FIGURE 6. EFFECTIVE NUMBER OF BITS (ENOB) vs ANALOG INPUT LEVEL

Typical Performance Curves (Continued)

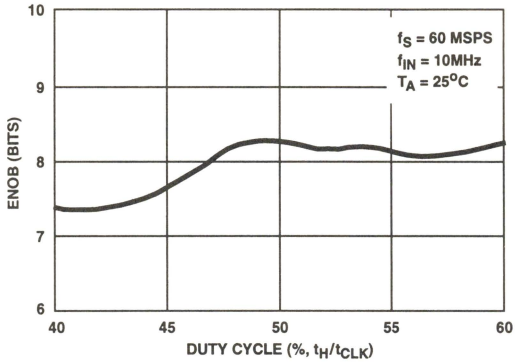


FIGURE 7. EFFECTIVE NUMBER OF BITS (ENOB) vs SAMPLE CLOCK DUTY CYCLE

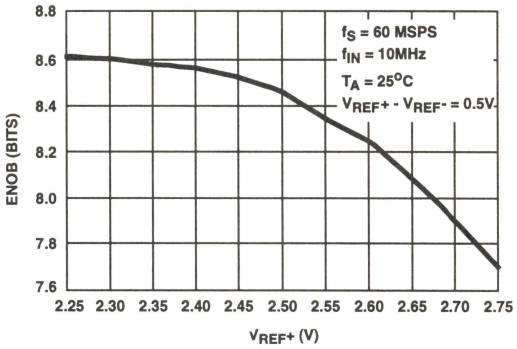


FIGURE 8. EFFECTIVE NUMBER OF BITS (ENOB) vs V_{REF+}

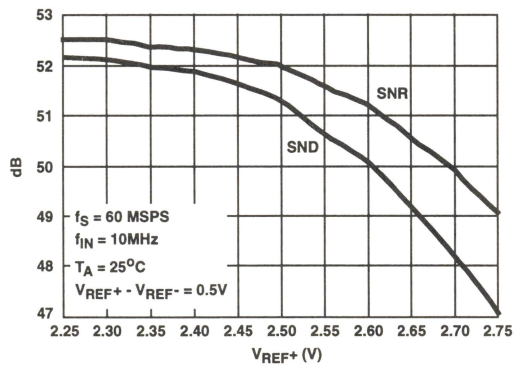
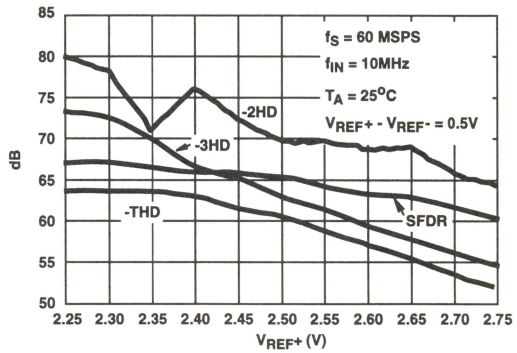


FIGURE 9. SINAD AND SNR vs V_{REF+}



NOTE: SFDR depicted here does not include any harmonic distortion.

FIGURE 10. -2HD, -3HD, -THD AND SFDR vs V_{REF+}

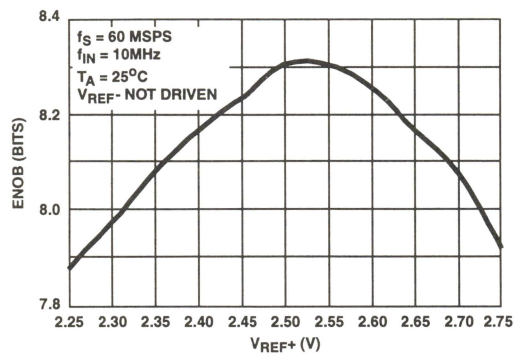


FIGURE 11. EFFECTIVE NUMBER OF BITS (ENOB) vs V_{REF+} (V_{REF-} NOT DRIVEN)

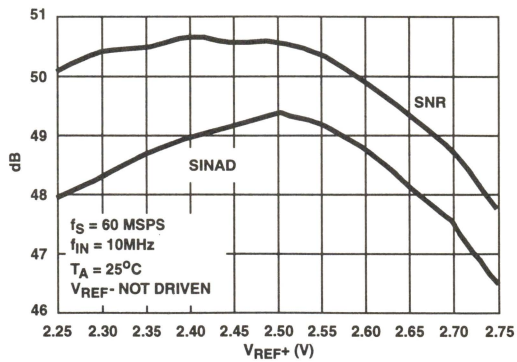


FIGURE 12. SINAD AND SNR vs V_{REF+} (V_{REF-} NOT DRIVEN)

Typical Performance Curves (Continued)

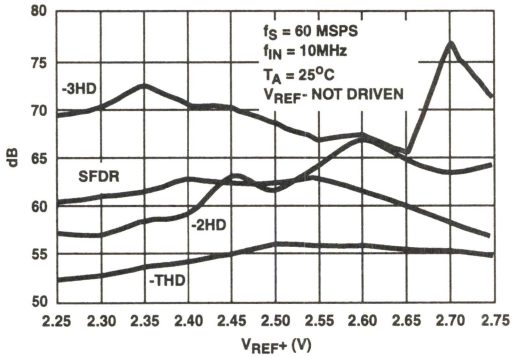


FIGURE 13. -2HD, -3HD, -THD AND SFDR vs V_{REF}+ (V_{REF}- NOT DRIVEN)

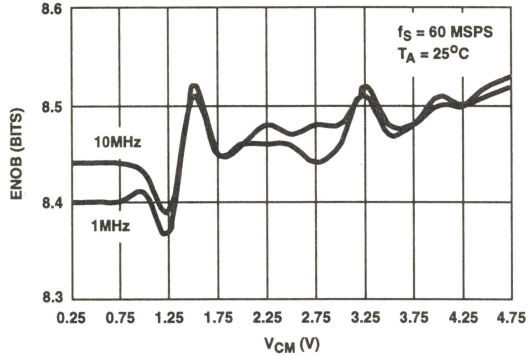


FIGURE 14. EFFECTIVE NUMBER OF BITS (ENOB) vs ANALOG INPUT COMMON MODE VOLTAGE

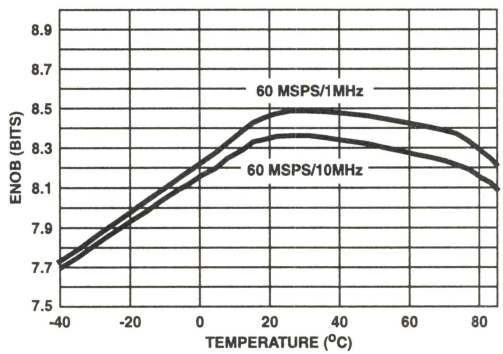


FIGURE 15. EFFECTIVE NUMBER OF BITS (ENOB) vs TEMPERATURE

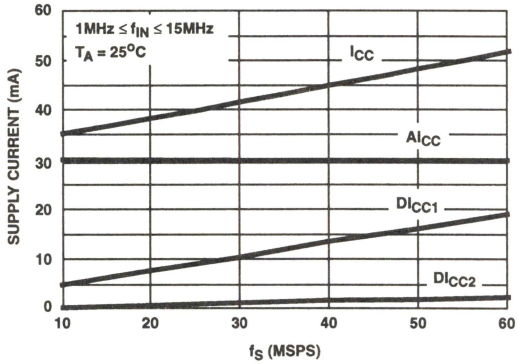


FIGURE 16. SUPPLY CURRENT vs SAMPLE CLOCK FREQUENCY

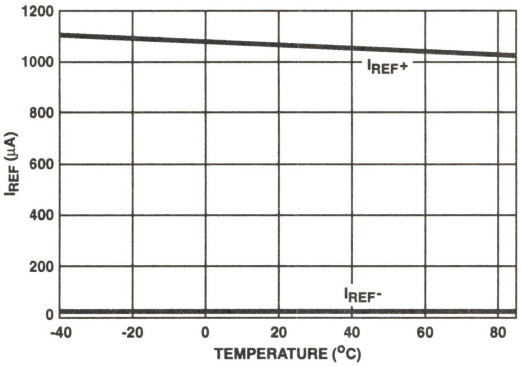


FIGURE 17. REFERENCE CURRENT vs TEMPERATURE

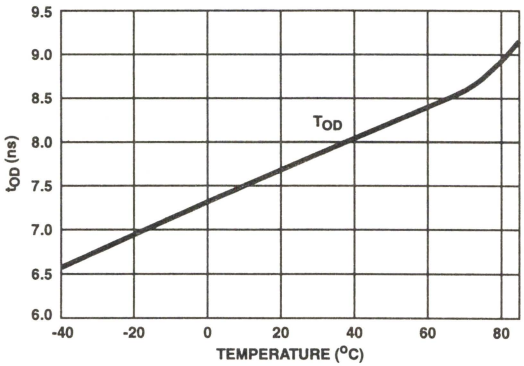


FIGURE 18. DATA OUTPUT DELAY vs TEMPERATURE

Typical Performance Curves (Continued)

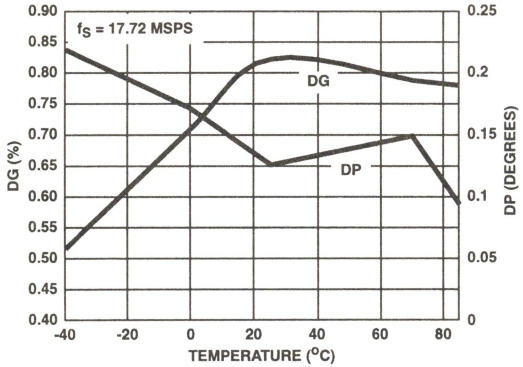


FIGURE 19. DIFFERENTIAL GAIN/PHASE vs TEMPERATURE

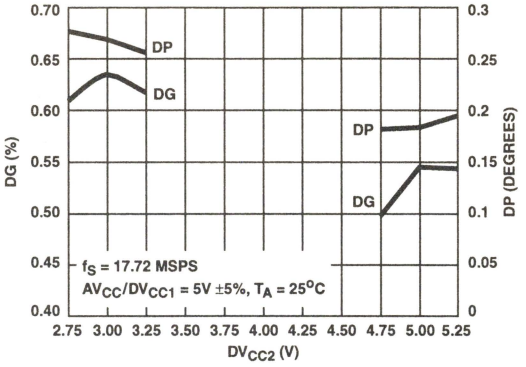


FIGURE 20. DIFFERENTIAL GAIN/PHASE vs SUPPLY VOLTAGE

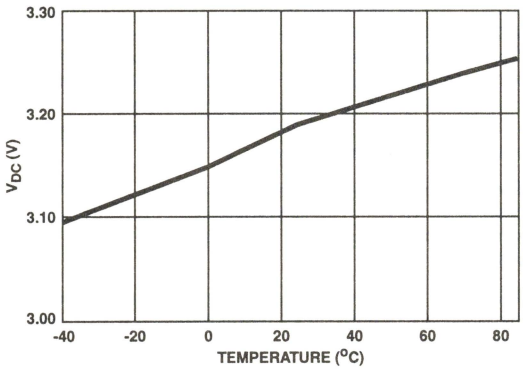


FIGURE 21. DC BIAS VOLTAGE (V_{DC}) vs TEMPERATURE

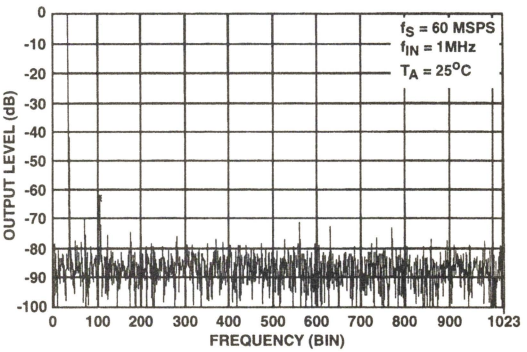


FIGURE 22. 2048 POINT FFT PLOT

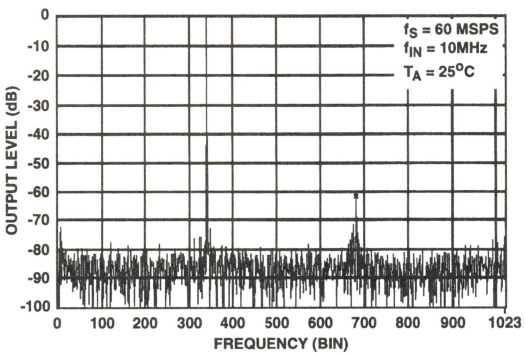


FIGURE 23. 2048 POINT FFT PLOT

Detailed Description

Theory of Operation

The HI5766 is a 10-bit fully differential sampling pipeline A/D converter with digital error correction logic. Figure 3 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal sampling clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master sampling clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The front end sample-and-hold output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

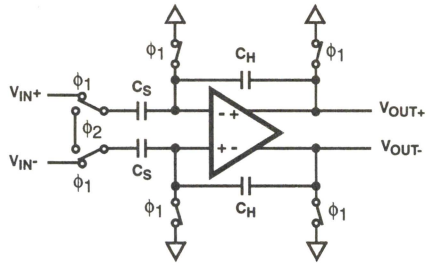


FIGURE 24. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, eight identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the ninth stage being a two bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The output of each of the eight identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the eight identical two-bit subconverter stages with the corresponding output of the ninth stage flash converter before applying the eighteen bit result to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final 10-bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital output data is synchronized to the external sampling clock by a double buffered latching technique. The output of the digital error correction circuit is available in two's complement or offset binary format depending on the state of the Data Format Select (DFS) control input (see Table 1, A/D Code Table).

Reference Voltage Inputs, V_{REF}- and V_{REF}+

The HI5766 is designed to accept two external reference voltage sources at the V_{REF} input pins. Typical operation of the converter requires V_{REF}+ to be set at +2.5V and V_{REF}- to be set at 2.0V. However, it should be noted that the input structure of the V_{REF}+ and V_{REF}- input pins consists of a resistive voltage divider with one resistor of the divider (nominally 500Ω) connected between V_{REF}+ and V_{REF}- and the other resistor of the divider (nominally 2000Ω) connected between V_{REF}- and analog ground. This allows the user the option of supplying only the +2.5V V_{REF}+ voltage reference with the +2.0V V_{REF}- being generated internally by the voltage division action of the input structure.

The HI5766 is tested with V_{REF}- equal to +2.0V and V_{REF}+ equal to +2.5V yielding a fully differential analog input voltage range of ±0.5V. V_{REF}+ and V_{REF}- can differ from the above voltages.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at **both** of the reference voltage input pins, V_{REF}+ and V_{REF}-.

Analog Input, Differential Connection

The analog input to the HI5766 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 4 and Figure 5) will give the best performance for the converter.

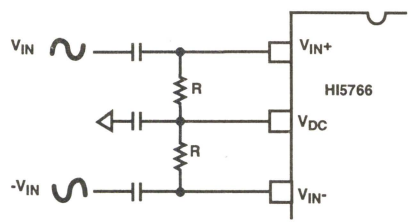


FIGURE 25. AC COUPLED DIFFERENTIAL INPUT

Since the HI5766 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V. For the differential input connection this implies the analog input common mode voltage can range from 0.25V to 4.75V.

The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A DC voltage source, V_{DC}, equal to 3.2V (Typ), is made available to the user to help simplify circuit design when using an AC coupled differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent DC bias source and stays well within the analog input common mode voltage range over temperature.

For the AC coupled differential input (Figure 4) assume the difference between $V_{REF}+$, typically 2.5V, and $V_{REF}-$, typically 2V, is 0.5V. Full scale is achieved when the V_{IN} and $-V_{IN}$ input signals are $0.5V_{P-P}$, with $-V_{IN}$ being 180 degrees out of phase with V_{IN}. The converter will be at positive full scale when the $V_{IN}+$ input is at V_{DC} + 0.25V and the $V_{IN}-$ input is at V_{DC} - 0.25V ($V_{IN}+$ - $V_{IN}-$ = +0.5V). Conversely, the converter will be at negative full scale when the $V_{IN}+$ input is equal to V_{DC} - 0.25V and $V_{IN}-$ is at V_{DC} + 0.25V ($V_{IN}+$ - $V_{IN}-$ = -0.5V).

The analog input can be DC coupled (Figure 5) as long as the inputs are within the analog input common mode voltage range (0.25V ≤ VDC ≤ 4.75V).

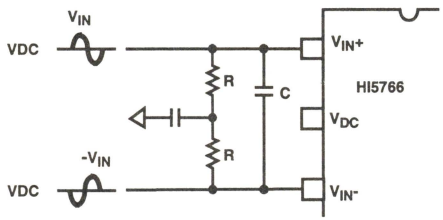


FIGURE 26. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 5 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

Analog Input, Single-Ended Connection

The configuration shown in Figure 6 may be used with a single ended AC coupled input.

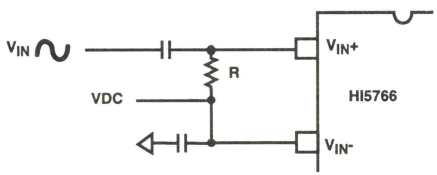


FIGURE 27. AC COUPLED SINGLE ENDED INPUT

Again, assume the difference between $V_{REF}+$, typically 2.5V, and $V_{REF}-$, typically 2V, is 0.5V. If V_{IN} is a $1V_{P-P}$ sinewave, then $V_{IN}+$ is a $1V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive full scale when $V_{IN}+$ is at VDC + 0.5V ($V_{IN}+$ - $V_{IN}-$ = +0.5V) and will be at negative full scale when $V_{IN}+$ is equal to VDC - 0.5V ($V_{IN}+$ - $V_{IN}-$ = -0.5V). Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND. In this case, VDC could range between 0.5V and 4.5V without a significant change in ADC performance. The simplest way to produce VDC is to use the DC bias source, V_{DC}, output of the HI5766.

The single ended analog input can be DC coupled (Figure 7) as long as the input is within the analog input common mode voltage range.

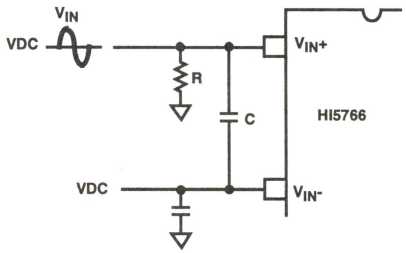


FIGURE 28. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 7 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

A single ended source may give better overall system performance if it is first converted to differential before driving the HI5766.

Digital Output Control and Clock Requirements

The HI5766 provides a standard high-speed interface to external TTL logic families.

In order to ensure rated performance of the HI5766, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5766 will only be guaranteed at conversion rates above 1 MSPS. This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1 MSPS will have to be performed before valid data is available.

A Data Format Select (DFS) pin is provided which will determine the format of the digital data outputs. When at logic low, the data will be output in offset binary format. When at logic high, the data will be output in two's complement format. Refer to Table 1 for further information.

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE ($V_{IN}+ - V_{IN}-$)	OFFSET BINARY OUTPUT CODE (DFS LOW)										TWO'S COMPLEMENT OUTPUT CODE (DFS HIGH)									
		MSB									LSB	MSB									LSB
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) - $^1/_4$ LSB	0.499756V	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
+FS - $1^1/_4$ LSB	0.498779V	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
+ $^3/_4$ LSB	732.422µV	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
- $^1/_4$ LSB	-244.141µV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-FS + $1^3/_4$ LSB	-0.498291V	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + $^3/_4$ LSB	-0.499268V	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

NOTES:

8. The voltages listed above represent the ideal center of each output code shown as a function of the reference differential voltage, ($V_{REF}+ - V_{REF}-$) = 0.5V.
9. $V_{REF}+$ = 2.5V and $V_{REF}-$ = 2V.

The output enable pin, $\overline{OE}$, when pulled high will three-state the digital outputs to a high impedance state. Set the $\overline{OE}$ input to logic low for normal operation.

$\overline{OE}$ INPUT	DIGITAL DATA OUTPUTS
0	Active
1	High Impedance

Supply and Ground Considerations

The HI5766 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The digital data outputs also have a separate supply pin, DV_{CC2}, which can be powered from a 3V or 5V supply. This allows the outputs to interface with 3V logic if so desired.

The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5766 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the application note "Using Harris High Speed A/D Converters" (AN9214) for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$ LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is $^3/_4$ LSBs below positive Full Scale (+FS) with the offset error removed. Full Scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Sensitivity

Each of the power supplies are moved plus and minus 5% and the shift in the offset and full scale error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5766. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from Full scale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

where: V_{CORR} = 0.5 dB.

V_{CORR} adjusts the SINAD, and hence the ENOB, for the amount the analog input signal is below full scale.

Signal To Noise and Distortion Ratio (SINAD)

SINAD is the ratio of the measured RMS signal to RMS sum of all the other spectral components below the Nyquist frequency, $f_S/2$, excluding DC.

Signal To Noise Ratio (SNR)

SNR is the ratio of the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components below $f_S/2$ excluding the fundamental, the first five harmonics and DC.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spectral component in the spectrum below $f_S/2$.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present at the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are (f_1+f_2), (f_1-f_2), $(2f_1)$, $(2f_2)$, $(2f_1+f_2)$, $(2f_1-f_2)$, (f_1+2f_2), (f_1-2f_2). The ADC is tested with each tone 6dB below full scale.

Transient Response

Transient response is measured by providing a full scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Over-Voltage Recovery

Over-Voltage Recovery is measured by providing a full scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the analog input frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has an amplitude which swings from -FS to +FS. The bandwidth given is measured at the specified sampling frequency.

Video Definitions

Differential Gain and Differential Phase are two commonly found video specifications for characterizing the distortion of a chrominance signal as it is offset through the input voltage range of an ADC.

Differential Gain (DG)

Differential Gain is the peak difference in chrominance amplitude (in percent) relative to the reference burst.

Differential Phase (DP)

Differential Phase is the peak difference in chrominance phase (in degrees) relative to the reference burst.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This is due to the pipeline nature of the converter where the analog sample has to ripple through the internal subconverter stages. This delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital data lags the analog input sample by 7 sample clock cycles.

Power-Up Initialization

This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.

HARRIS SEMICONDUCTOR

HI5767

10-Bit, 20/40/60 MSPS A/D Converter with Internal Voltage Reference

August 1997

Features

- Sampling Rate . . . . . 20/40/60 MSPS
- 8.8 Bits at f_{IN} = 10MHz, f_S = 40 MSPS
- Low Power at 40 MSPS 310mW
- Wide Full Power Input Bandwidth 250MHz
- On-Chip Sample and Hold
- Internal 2.5V Band-Gap Voltage Reference
- Fully Differential or Single-Ended Analog Input
- Single Supply Voltage . . . . . .+5V
- TTL/CMOS Compatible Digital Inputs
- CMOS Compatible Digital Outputs. 3.0V/5.0V
- Offset Binary or Two's Complement Output Format

Applications

- Digital Communication Systems
- QAM Demodulators
- Professional Video Digitizing
- Medical Imaging
- High Speed Data Acquisition

Description

The HI5767 is a monolithic, 10-bit, analog-to-digital converter fabricated in a CMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its high sample clock rate is made possible by a fully differential pipelined architecture with both an internal sample and hold and internal band-gap voltage reference.

The 250MHz Full Power Input Bandwidth and superior high frequency performance of the HI5767 converter make it an excellent choice for implementing Digital IF architectures in communications applications.

The HI5767 has excellent dynamic performance while consuming only 310mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles.

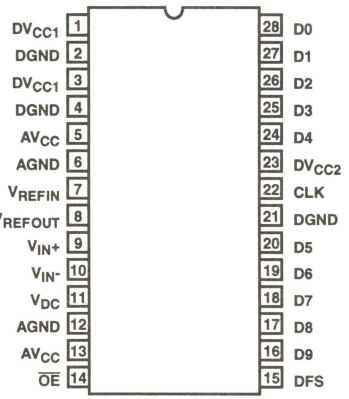
The HI5767 is offered in 20 MSPS, 40 MSPS and 60 MSPS sampling rates.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.	SAMPLING RATE (MSPS)
HI5767/2CB	0 to 70	28 Ld SOIC	M28.3	20
HI5767/4CB	0 to 70	28 Ld SOIC	M28.3	40
HI5767/6CB	0 to 70	28 Ld SOIC	M28.3	60
HI5767EVAL1	25	Evaluation Board		60

Pinout

HI5767 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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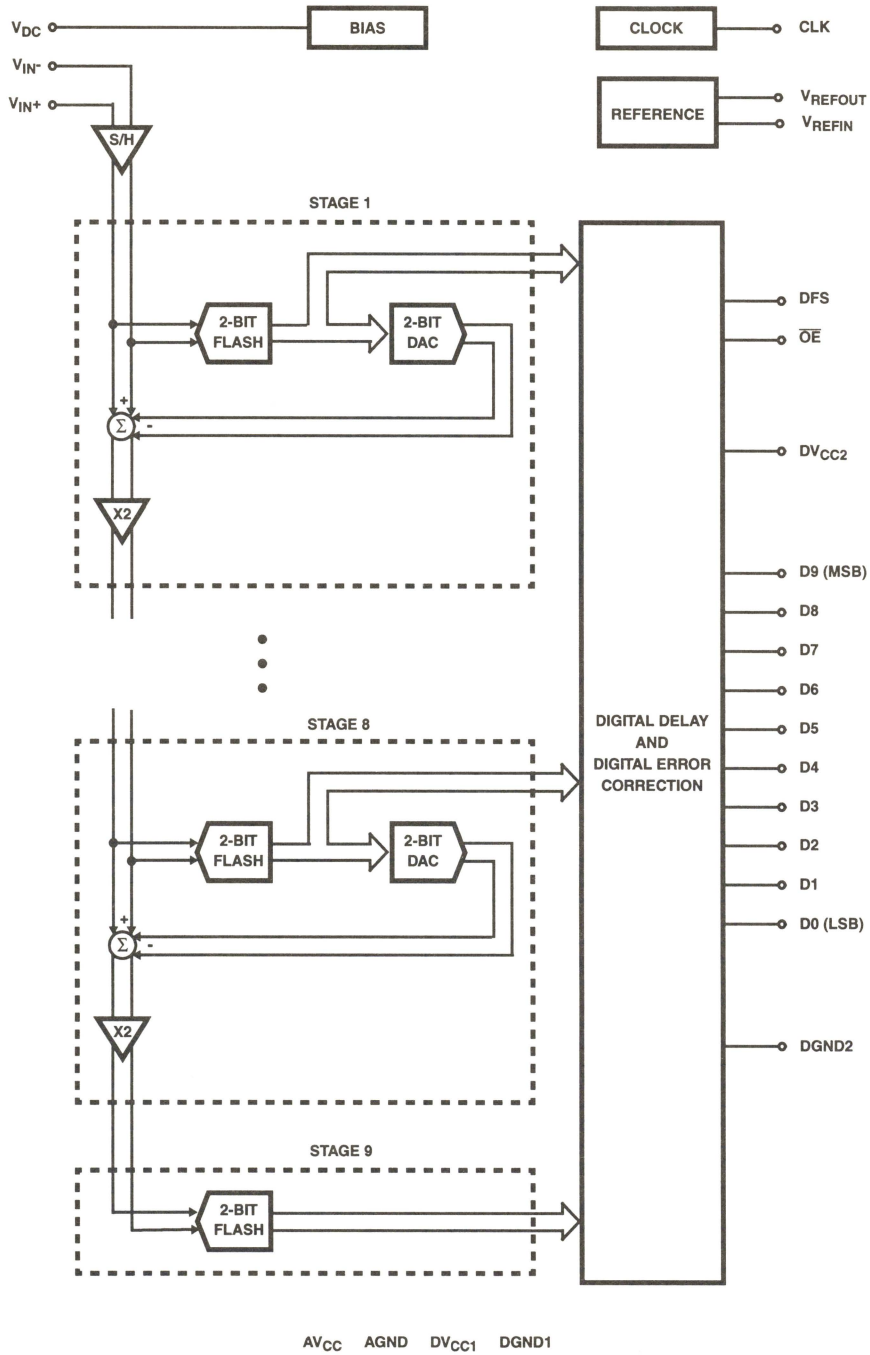
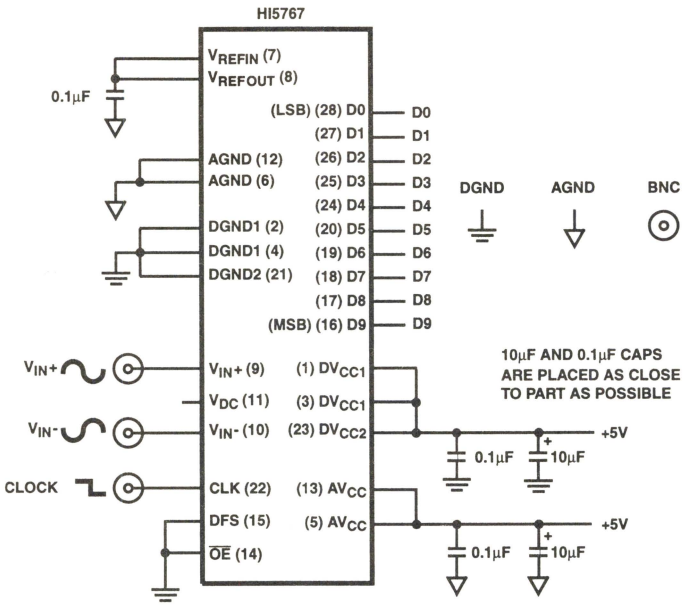
File Number **4319.1**

Functional Block Diagram



Typical Application Schematic



Pin Descriptions

PIN NO.	NAME	DESCRIPTION
1	DV_{CC1}	Digital Supply (+5.0V)
2	DGND1	Digital Ground
3	DV_{CC1}	Digital Supply (+5.0V)
4	DGND1	Digital Ground
5	AV_{CC}	Analog Supply (+5.0V)
6	AGND	Analog Ground
7	V_{REFIN}	+2.5V Reference Voltage Input
8	V_{REFOUT}	+2.5V Reference Voltage Output
9	$V_{IN}+$	Positive Analog Input
10	$V_{IN}-$	Negative Analog Input
11	V_{DC}	DC Bias Voltage Output
12	AGND	Analog Ground
13	AV_{CC}	Analog Supply (+5.0V)
14	$\overline{OE}$	Digital Output Enable Control Input
15	DFS	Data Format Select Input

PIN NO.	NAME	DESCRIPTION
16	D9	Data Bit 9 Output (MSB)
17	D8	Data Bit 8 Output
18	D7	Data Bit 7 Output
19	D6	Data Bit 6 Output
20	D5	Data Bit 5 Output
21	DGND2	Digital Ground
22	CLK	Sample Clock Input
23	DV_{CC2}	Digital Output Supply (+3.0V or +5.0V)
24	D4	Data Bit 4 Output
25	D3	Data Bit 3 Output
26	D2	Data Bit 2 Output
27	D1	Data Bit 1 Output
28	D0	Data Bit 0 Output (LSB)

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND. 6V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{CC}
Analog I/O Pins. . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range
HI5767/XCB (Typ). . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	75
Maximum Junction Temperature	150^oC
Maximum Storage Temperature Range	-65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = 5.0V$, $DV_{CC2} = 3.0V$; $V_{REFIN} = V_{REFOUT}$; $f_S = 40$ MSPS at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±0.75	±1.75	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.35	±1.0	LSB
Offset Error, V_{OS}	f_{IN} = DC	-40	-	40	LSB
Full Scale Error, FSE	f_{IN} = DC	-	4	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	1	MSPS
Maximum Conversion Rate	No Missing Codes	40	-	-	MSPS
Effective Number of Bits, ENOB					
HI5767/2	$f_S = 20$ MSPS, $f_{IN} = 10$MHz	8.7	9	-	Bit
HI5767/4	$f_S = 40$ MSPS, $f_{IN} = 10$MHz	8.55	8.8	-	Bit
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$					
HI5767/2	$f_S = 20$ MSPS, $f_{IN} = 10$MHz	-	55.9	-	dB
HI5767/4	$f_S = 40$ MSPS, $f_{IN} = 10$MHz	-	54.7	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$					
HI5767/2	$f_S = 20$ MSPS, $f_{IN} = 10$MHz	-	55.9	-	dB
HI5767/4	$f_S = 40$ MSPS, $f_{IN} = 10$MHz	-	55	-	dB
Total Harmonic Distortion, THD					
HI5767/2	$f_S = 20$ MSPS, $f_{IN} = 10$MHz	-	-71	-	dBc
HI5767/4	$f_S = 40$ MSPS, $f_{IN} = 10$MHz	-	-65	-	dBc
2nd Harmonic Distortion					
HI5767/2	$f_S = 20$ MSPS, $f_{IN} = 10$MHz	-	-76	-	dBc
HI5767/4	$f_S = 40$ MSPS, $f_{IN} = 10$MHz	-	-73	-	dBc

Electrical Specifications $AV_{CC} = DV_{CC1} = 5.0V$, $DV_{CC2} = 3.0V$; $V_{REFIN} = V_{REFOUT}$; $f_S = 40$ MSPS at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
3rd Harmonic Distortion					
HI5767/2	$f_S = 20$ MSPS, $f_{IN} = 10$MHz	-	-80	-	dBc
HI5767/4	$f_S = 40$ MSPS, $f_{IN} = 10$MHz	-	-69	-	dBc
Spurious Free Dynamic Range, SFDR					
HI5767/2	$f_S = 20$ MSPS, $f_{IN} = 10$MHz	-	76	-	dBc
HI5767/4	$f_S = 40$ MSPS, $f_{IN} = 10$MHz	-	69	-	dBc
Intermodulation Distortion, IMD	$f_1 = 1$MHz, $f_2 = 1.02$MHz	-	64	-	dBc
Differential Gain Error	$f_S = 17.72$MHz, 6 Step, Mod Ramp	-	0.5	-	%
Differential Phase Error	$f_S = 17.72$MHz, 6 Step, Mod Ramp	-	0.2	-	Degree
Transient Response	(Note 2)	-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive (Note 2)	-	1	-	Cycle
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range ($V_{IN}+ - V_{IN}-$)		-	±0.5	–	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	1.0	-	V
Analog Input Resistance, R_{IN}	(Note 3)	-	1	-	MΩ
Analog Input Capacitance, C_{IN}		-	10	-	pF
Analog Input Bias Current, $I_{B}+$ or $I_{B}-$	(Note 3)	-10	-	+10	µA
Differential Analog Input Bias Current $I_{BDIFF} = (I_{B}+ - I_{B}-)$	(Note 3)		±0.5		µA
Full Power Input Bandwidth, FPBW		-	250	-	MHz
Analog Input Common Mode Voltage Range ($V_{IN}+ + V_{IN}-$) / 2	Differential Mode (Note 2)	0.25	-	4.75	V
INTERNAL REFERENCE VOLTAGE					
Reference Voltage Output, V_{REFOUT} (Loaded)		-	2.47	-	V
Reference Output Current, I_{REFOUT}		-	1	2	mA
Reference Temperature Coefficient		-	120	-	ppm/^oC
REFERENCE VOLTAGE INPUT					
Reference Voltage Input, V_{REFIN}		-	2.5	-	V
Total Reference Resistance, R_{REFIN}		-	2.5	-	kΩ
Reference Input Current, I_{REFIN}		-	1	-	mA
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	3.0	-	V
Maximum Output Current		-	-	0.2	mA
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}	CLK, DFS, $\overline{OE}$	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	CLK, DFS, $\overline{OE}$	-	-	0.8	V

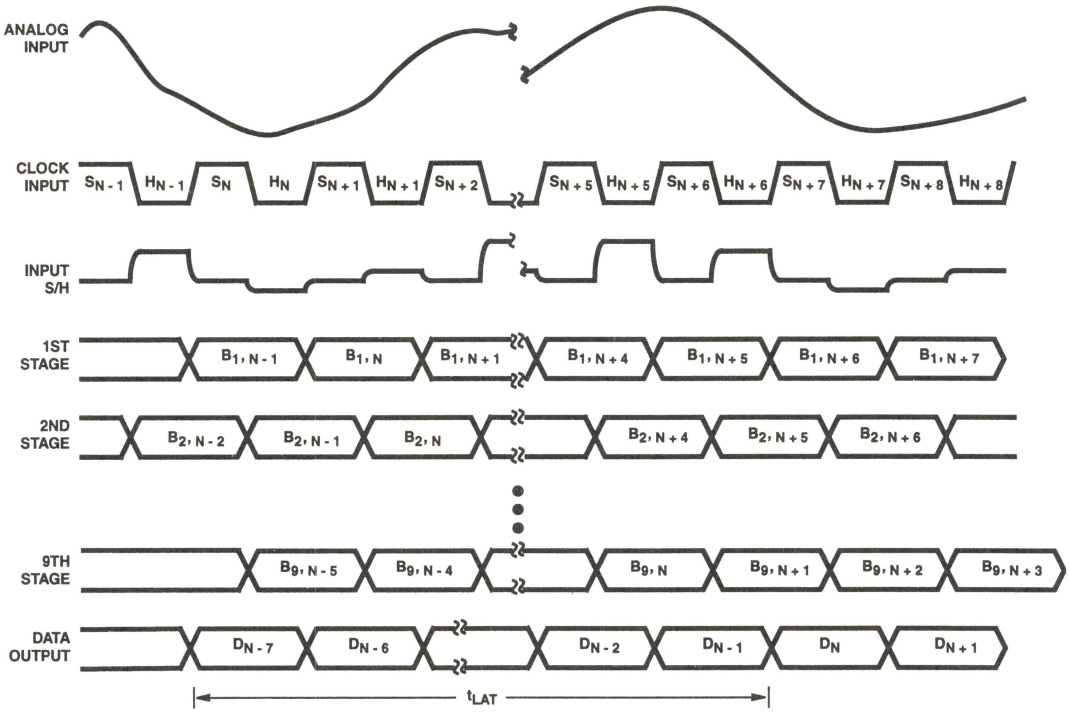
Electrical Specifications $AV_{CC} = DV_{CC1} = 5.0V$, $DV_{CC2} = 3.0V$; $V_{REFIN} = V_{REFOUT}$; $f_S = 40$ MSPS at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Logic High Current, I_{IH}	CLK, DFS, $\overline{OE}$, $V_{IH} = 5V$	-10.0	-	+10.0	µA
Input Logic Low Current, I_{IL}	CLK, DFS, $\overline{OE}$, $V_{IL} = 0V$	-10.0	-	+10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS					
Output Logic High Voltage, V_{OH}	$I_{OH} = 100µA$; $DV_{CC2} = 5V$	4.0	-	-	V
Output Logic Low Voltage, V_{OL}	$I_{OL} = 100µA$; $DV_{CC2} = 5V$	-	-	0.8	V
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/5V$; $DV_{CC2} = 5V$	-10	±1	10	µA
Output Logic High Voltage, V_{OH}	$I_{OH} = 100µA$; $DV_{CC2} = 3V$	2.4	-	-	V
Output Logic Low Voltage, V_{OL}	$I_{OL} = 100µA$; $DV_{CC2} = 3V$	-	-	0.5	V
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/5V$; $DV_{CC2} = 3V$	-10	±1	10	µA
Output Capacitance, C_{OUT}		-	10	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps_{RMS}
Data Output Hold, t_H		-	5	-	ns
Data Output Delay, t_{OD}		-	6	-	ns
Data Output Enable Time, t_{EN}		-	5	-	ns
Data Output Enable Time, t_{DIS}		-	5	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	7	Cycles
Power-Up Initialization	Data Invalid Time (Note 2)	-	-	20	Cycles
Sample Clock Pulse Width (Low)	$f_S = 40$ MSPS	11.3	12.5	-	ns
Sample Clock Pulse Width (High)	$f_S = 40$ MSPS	11.3	12.5	-	ns
Sample Clock Duty Cycle Variation	$f_S = 40$ MSPS	-	±5	-	%
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, AV_{CC}		4.75	5.0	5.25	V
Digital Supply Voltage, DV_{CC1}		4.75	5.0	5.25	V
Digital Output Supply Voltage, DV_{CC2}	At 3.0V	2.7	3.0	3.3	V
	At 5.0V	4.75	5.0	5.25	V
Supply Current, I_{CC}	$f_{IN} = 1MHz$ and DFS = "0"	-	62	-	mA
Power Dissipation	$f_{IN} = 1MHz$ and DFS = "0"	-	310	-	mW
Offset Error Sensitivity, ΔV_{OS}	AV_{CC} or $DV_{CC} = 5V$ ±5%	-	±0.7	-	LSB
Gain Error Sensitivity, ΔFSE	AV_{CC} or $DV_{CC} = 5V$ ±5%	-	±0.1	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock low and DC input.

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M,N}$: M-th stage digital output corresponding to N-th sampled input.
7. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5767 INTERNAL CIRCUIT TIMING

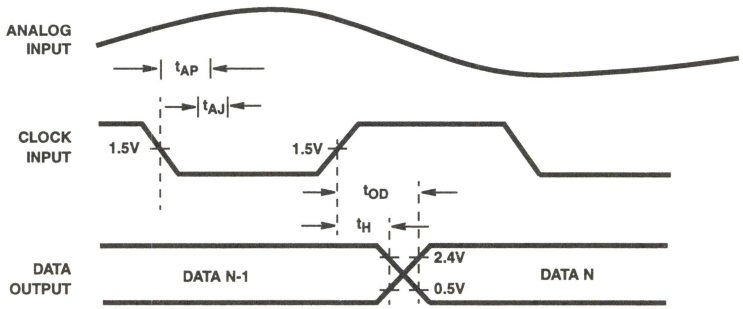


FIGURE 2. INPUT-TO OUTPUT TIMING

Detailed Description

Theory of Operation

The HI5767 is a 10-bit fully differential sampling pipeline A/D converter with digital error correction logic. Figure 3 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal sampling clock which is a non-overlapping two phase signal, Φ_1 and Φ_2, derived from the master sampling clock. During the sampling phase, Φ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of Φ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, Φ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The front end sample-and-hold output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

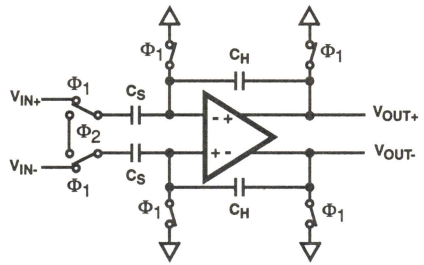


FIGURE 3. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, eight identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the ninth stage being a two bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The output of each of the eight identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the eight identical two-bit subconverter stages with the corresponding output of the ninth stage flash converter before applying the eighteen bit result to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final ten bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital output data is synchronized to the external sampling clock by a double buffered latching technique. The digital output data is available in two's complement or offset binary format depending on the state of the Data Format Select (DFS) control input (see Table 1, A/D Code Table).

Internal Reference Voltage Output, V_{REFOUT}

The HI5767 is equipped with an internal reference voltage generator, therefore, no external reference voltage is required. V_{REFOUT} must be connected to V_{REFIN} when using the internal reference voltage.

An internal band-gap reference voltage followed by an amplifier/buffer generates the precision +2.5V reference voltage used by the converter. A 4:1 array of substrate PNPs generates the "delta-V_{BE}" and a two-stage op-amp closes the loop to create an internal +1.25V band-gap reference voltage. This voltage is then amplified by a wide-band uncompensated operational amplifier connected in a gain-of-two configuration. An external, user-supplied, 0.1µF capacitor connected from the V_{REFOUT} output pin to analog ground is used to set the dominant pole and to maintain the stability of the operational amplifier.

Reference Voltage Input, V_{REFIN}

The HI5767 is designed to accept a +2.5V reference voltage source at the V_{REFIN} input pin. Typical operation of the converter requires V_{REFIN} to be set at +2.5V. The HI5767 is tested with V_{REFIN} connected to V_{REFOUT} yielding a fully differential analog input voltage range of ±0.5V.

The user does have the option of supplying an external +2.5V reference voltage. As a result of the high input impedance presented at the V_{REFIN} input pin, 2.5kΩ typically, the external reference voltage being used is only required to source 1mA of reference input current. In the situation where an external reference voltage will be used an external 0.1µF capacitor **must** be connected from the V_{REFOUT} output pin to analog ground in order to maintain the stability of the internal operational amplifier.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference voltage input pin, V_{REFIN}.

Analog Input, Differential Connection

The analog input to the HI5767 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 4 and Figure 5) will deliver the best performance from the converter.

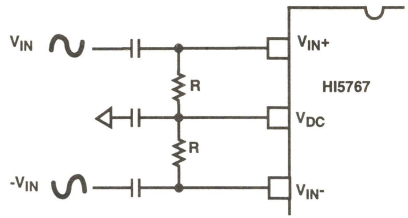


FIGURE 4. AC COUPLED DIFFERENTIAL INPUT

Since the HI5767 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V. For the differential input connection this implies the analog input common mode voltage can range from 0.25V to 4.75V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A DC voltage source, V_{DC}, equal to 3.2V (typical), is made available to the user to help simplify circuit design when using an AC coupled differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent DC bias source and stays well within the analog input common mode voltage range over temperature.

For the AC coupled differential input (Figure 4) and with V_{REFIN} connected to V_{REFOUT}, full scale is achieved when the V_{IN} and $-V_{IN}$ input signals are $0.5V_{P-P}$, with $-V_{IN}$ being 180 degrees out of phase with V_{IN}. The converter will be at positive full scale when the $V_{IN}+$ input is at V_{DC} + 0.25V and the $V_{IN}-$ input is at V_{DC} - 0.25V ($V_{IN}+ - V_{IN}- = +0.5V$). Conversely, the converter will be at negative full scale when the $V_{IN}+$ input is equal to V_{DC} - 0.25V and $V_{IN}-$ is at V_{DC} + 0.25V ($V_{IN}+ - V_{IN}- = -0.5V$).

The analog input can be DC coupled (Figure 5) as long as the inputs are within the analog input common mode voltage range ($0.25V \leq VDC \leq 4.75V$).

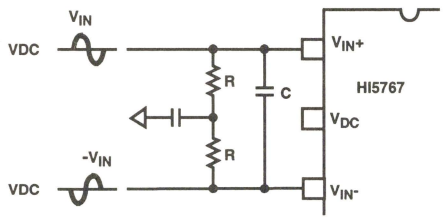


FIGURE 5. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 5 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

Analog Input, Single-Ended Connection

The configuration shown in Figure 6 may be used with a single ended AC coupled input.

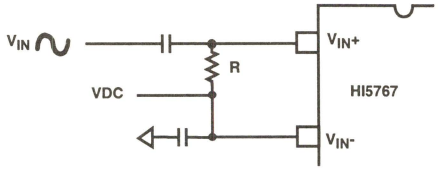


FIGURE 6. AC COUPLED SINGLE ENDED INPUT

Again, with V_{REFIN} connected to V_{REFOUT}, if V_{IN} is a $1V_{P-P}$ sinewave, then $V_{IN}+$ is a $1.0V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive full scale when $V_{IN}+$ is at VDC + 0.5V ($V_{IN}+ - V_{IN}- = +0.5V$) and will be at negative full scale when $V_{IN}+$ is equal to VDC - 0.5V ($V_{IN}+ - V_{IN}- = -0.5V$). Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND. In this case, VDC could range between 0.5V and 4.5V without a significant change in ADC performance. The simplest way to produce VDC is to use the DC bias source, V_{DC}, output of the HI5767.

The single ended analog input can be DC coupled (Figure 7) as long as the input is within the analog input common mode voltage range.

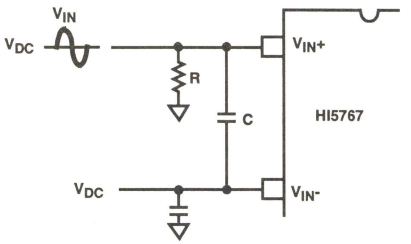


FIGURE 7. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 7 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

A single ended source may give better overall system performance if it is first converted to differential before driving the HI5767.

Digital Output Control and Clock Requirements

The HI5767 provides a standard high-speed interface to external TTL logic families.

In order to ensure rated performance of the HI5767, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5767 will only be guaranteed at conversion rates above 1 MSPS. This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1 MSPS will have to be performed before valid data is available.

A Data Format Select (DFS) pin is provided which will determine the format of the digital data outputs. When at logic low, the data will be output in offset binary format. When at logic high, the data will be output in two's complement format. Refer to Table 1 for further information.

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE ($V_{IN}+ - V_{IN}-$)	OFFSET BINARY OUTPUT CODE (DFS LOW)										TWO'S COMPLEMENT OUTPUT CODE (DFS HIGH)									
		MSB									LSB	MSB									LSB
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) - $^1/_4$ LSB	0.499756V	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
+FS - $1^1/_4$ LSB	0.498779V	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
+ $^3/_4$ LSB	732.422µV	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
- $^1/_4$ LSB	-244.141µV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-FS + $1^3/_4$ LSB	-0.498291V	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + $^3/_4$ LSB	-0.499268V	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

NOTE:

8. The voltages listed above represent the ideal center of each output code shown with V_{REFIN} = +2.5V.

The output enable pin, $\overline{OE}$, when pulled high will three-state the digital outputs to a high impedance state. Set the $\overline{OE}$ input to logic low for normal operation.

$\overline{OE}$ INPUT	DIGITAL DATA OUTPUTS
0	Active
1	High Impedance

Supply and Ground Considerations

The HI5767 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The digital data outputs also have a separate supply pin, DV_{CC2}, which can be powered from a 3.0V or 5.0V supply. This allows the outputs to interface with 3.0V logic if so desired.

The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5767 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the application note "Using Harris High Speed A/D Converters" (AN9214) for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$ LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is $^3/_4$ LSB below Positive Full Scale (+FS) with the offset error removed. Full scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Sensitivity

Each of the power supplies are moved plus and minus 5% and the shift in the offset and full scale error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5767. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is typically -0.5dB down from full scale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

The Effective Number of Bits (ENOB) is calculated from the SINAD data by:

ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02,

where: V_{CORR} = 0.5 dB (Typical).

V_{CORR} adjusts the SINAD, and hence the ENOB, for the amount the analog input signal is backed off from full scale.

Signal To Noise and Distortion Ratio (SINAD)

SINAD is the ratio of the measured RMS signal to RMS sum of all the other spectral components below the Nyquist frequency, $f_S/2$, excluding DC.

Signal To Noise Ratio (SNR)

SNR is the ratio of the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components below $f_S/2$ excluding the fundamental, the first five harmonics and DC.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spectral component in the spectrum below $f_S/2$.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present at the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are (f_1+f_2), (f_1-f_2), ($2f_1$), ($2f_2$), ($2f_1+f_2$), ($2f_1-f_2$), (f_1+2f_2), (f_1-2f_2). The ADC is tested with each tone 6dB below full scale.

Transient Response

Transient response is measured by providing a full-scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Over-Voltage Recovery

Over-Voltage Recovery is measured by providing a full-scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the analog input frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has an amplitude which swings from -FS to +FS. The bandwidth given is measured at the specified sampling frequency.

Video Definitions

Differential Gain and Differential Phase are two commonly found video specifications for characterizing the distortion of a chrominance signal as it is offset through the input voltage range of an ADC.

Differential Gain (DG)

Differential Gain is the peak difference in chrominance amplitude (in percent) relative to the reference burst.

Differential Phase (DP)

Differential Phase is the peak difference in chrominance phase (in degrees) relative to the reference burst.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This is due to the pipeline nature of the converter where the analog sample has to ripple through the internal subconverter stages. This delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital data lags the analog input sample by 7 sample clock cycles.

Power-Up Initialization

This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.

August 1997

12-Bit, 3 MSPS, Sampling A/D Converter

Features

- Throughput Rate ..... 3 MSPS
- 12-Bit, No Missing Codes Over Temperature
- Integral Linearity Error ..... 1.0 LSB
- Buffered Sample and Hold Amplifier
- Precision Voltage Reference
- Input Signal Range ..... ±2.5V
- 20MHz Input BW Allows Sampling Beyond Nyquist
- Zero Latency/No Pipeline Delay

Applications

- High Speed Data Acquisition Systems
- Medical Imaging
- Radar Signal Analysis
- Document and Film Scanners
- Vibration/Waveform Spectrum Analysis
- Digital Servo Control

Description

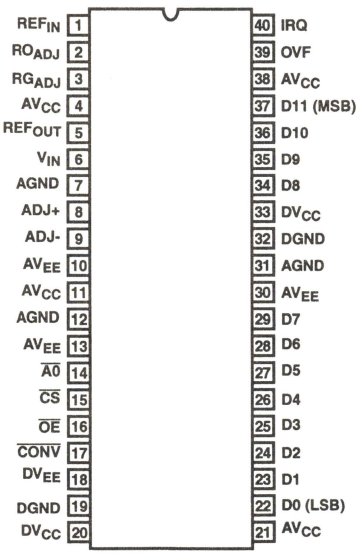
The HI5800 is a monolithic, 12-bit, sampling Analog-to-Digital Converter fabricated in the HBC10 BiCMOS process. It is a complete subsystem containing a sample and hold amplifier, voltage reference, two-step subranging A/D, error correction, control logic, and timing generator. The HI5800 is designed for high speed applications where wide bandwidth, accuracy and low distortion are essential.

Ordering Information

PART NUMBER	LINEARITY	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5800BID	±1 LSB	-40 to 85	40 Ld SBDIP	D40.6
HI5800JCD HI5800KCD	±2 LSB ±1 LSB	0 to 70	40 Ld SBDIP	D40.6
HI5800-EV		25	Evaluation Board	

Pinout

HI5800
(SBDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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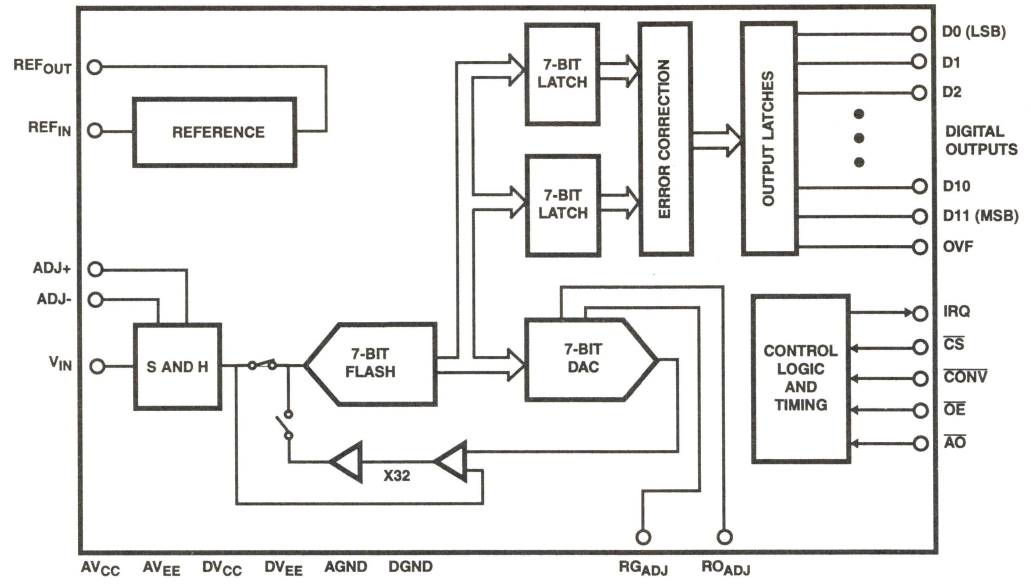
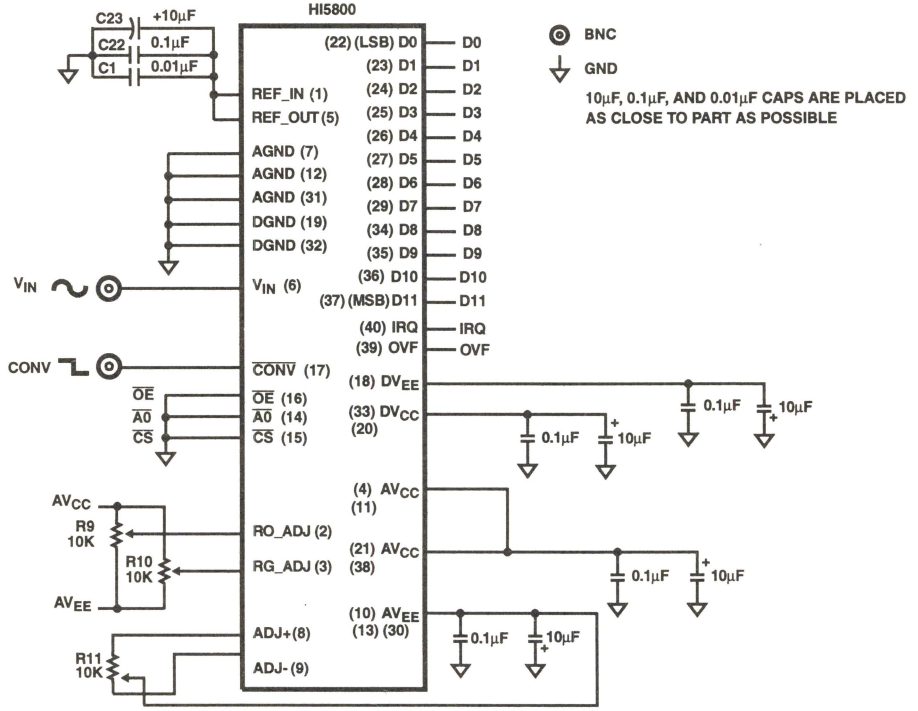
Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltages
- AV_{CC} or DV_{CC} to GND . . . . . +5.5V
- AV_{EE} or DV_{EE} to GND . . . . . -5.5V
- DGND to AGND . . . . . ±0.3V

Analog Input Pins
- Reference Input REF_{IN} . . . . . +2.75V
- Signal Input V_{IN} . . . . . $\pm(REF_{IN} + 0.2V)$

RO_{ADJ}, RG_{ADJ}, ADJ+, ADJ- . . . . . V_{EE} to V_{CC}

Digital I/O Pins . . . . . GND to V_{CC}

Operating Conditions

Temperature Range
- HI5800JCD/KCD . . . . . 0^oC to 70^oC
- HI5800BID . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SBDIP Package	40	15

Maximum Junction Temperature
- SBDIP Package . . . . . 175^oC

Maximum Storage Temperature Range . . . . . -65^oC to 150^oC

Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used Unless Otherwise Specified

PARAMETER	TEST CONDITIONS		HI5800JCD 0°C TO 70°C MIN	HI5800JCD 0°C TO 70°C TYP	HI5800JCD 0°C TO 70°C MAX	HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C MIN	HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C TYP	HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C MAX	UNITS
SYSTEM PERFORMANCE									
Resolution			12	-	-	12	-	-	Bits
Integral Linearity Error, INL	f_S = 3MHz, f_{IN} = 45Hz Ramp		-	0.7	±2	-	±0.5	±1	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_S = 3MHz, f_{IN} = 45Hz Ramp		-	±0.5	±1	-	±0.3	±1	LSB
Offset Error, V_{OS} (Adjustable to Zero)	(Note 8)	JCD, KCD	-	±2	±15	-	±2	±15	LSB
		BID	-	-	-	-	±3	±15	LSB
Full Scale Error, FSE (Adjustable to Zero)	(Note 8)	JCD, KCD	-	±2	±15	-	±2	±10	LSB
		BID	-	-	-	-	±3	±15	LSB
DYNAMIC CHARACTERISTICS (Input Signal Level 0.5dB Below Full Scale)									
Throughput Rate	No Missing Codes		3.0	-	-	3.0	-	-	MSPS
Signal to Noise Ratio (SNR) $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_S = 3MHz, f_{IN} = 20kHz		66	69	-	68	71	-	dB
	f_S = 3MHz, f_{IN} = 1MHz		65	67	-	67	69	-	dB
Signal to Noise Ratio (SINAD) $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_S = 3MHz, f_{IN} = 20kHz		66	68	-	68	71	-	dB
	f_S = 3MHz, f_{IN} = 1MHz		65	67	-	67	68	-	dB
Total Harmonic Distortion, THD	f_S = 3MHz, f_{IN} = 20kHz		-	-74	-70	-	-85	-74	dBc
	f_S = 3MHz, f_{IN} = 1MHz		-	-70	-68	-	-77	-70	dBc
Spurious Free Dynamic Range, SFDR	f_S = 3MHz, f_{IN} = 20kHz		71	76	-	76	86	-	dBc
	f_S = 3MHz, f_{IN} = 1MHz		68	72	-	71	77	-	dBc

Electrical Specifications AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	HI5800JCD 0°C TO 70°C			HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Intermodulation Distortion, IMD	f_S = 3MHz, f1 = 49kHz, f_2 = 50kHz	-	-74	-66	-	-79	-70	dBc
Differential Gain	f_S = 1MHz	-	0.9	-	-	0.9	-	%
Differential Phase	f_S = 1MHz	-	0.05	-	-	0.05	-	Degrees
Aperture Delay, t_{AD}		-	12	20	-	12	20	ns
Aperture Jitter, t_{AJ}		-	10	20	-	10	20	ps
ANALOG INPUT								
Input Voltage Range		-	±2.5	±2.7	-	±2.5	±2.7	V
Input Resistance		1	3	-	1	3	-	MΩ
Input Capacitance		-	5	-	-	5	-	pF
Input Current		-	±1	±10	-	±1	±10	µA
Input Bandwidth		-	20	-	-	20	-	MHz
INTERNAL VOLTAGE REFERENCE								
Reference Output Voltage, REF_{OUT} (Loaded)		2.450	2.500	2.550	2.470	2.500	2.530	V
Reference Output Current	Note 5	2	-	-	2	-	-	mA
Reference Temperature Coefficient		-	20	-	-	13	-	ppm/°C
REFERENCE INPUT								
Reference Input Range		-	2.5	2.6	-	2.5	2.6	V
Reference Input Resistance		-	200	-	-	200	-	Ω
DIGITAL INPUTS								
Input Logic High Voltage, V_{IH}	Note 6	2.0	-	-	2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	-	-	0.8	V
Input Logic Current, I_{IL}	V_{IN} = 0V, 5V	-	±1	±10	-	±1	±10	µA
Digital Input Capacitance, C_{IN}	V_{IN} = 0V	-	5	-	-	5	-	pF
DIGITAL OUTPUTS								
Output Logic High Voltage, V_{OH}	I_{OUT} = -160µA	2.4	4.3	-	2.4	4.3	-	V
Output Logic Low Voltage, V_{OL}	I_{OUT} = 3.2mA	-	0.22	0.4	-	0.22	0.4	V
Output Logic High Current, I_{OH}		-0.160	-6	-	-0.160	-6	-	mA
Output Logic Low Current, I_{OL}		3.2	6	-	3.2	6	-	mA
Output Three-State Leakage Current, I_{OZ}	V_{OUT} = 0V, 5V	-	±1	±10	-	±1	±10	µA
Digital Output Capacitance, C_{OUT}		-	10	-	-	10	-	pF
TIMING CHARACTERISTICS								
Minimum $\overline{CONV}$ Pulse, t_1	(Notes 3, 4)	10	-	-	10	-	-	ns

Electrical Specifications AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS		HI5800JCD 0°C TO 70°C MIN	HI5800JCD 0°C TO 70°C TYP	HI5800JCD 0°C TO 70°C MAX	HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C MIN	HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C TYP	HI5800KCD, HI5800BID 0°C TO 70°C -40°C TO 85°C MAX	UNITS
$\overline{CS}$ to $\overline{CONV}$ Setup Time, t_2	(Note 3)		10	-	-	10	-	-	ns
$\overline{CONV}$ to $\overline{CS}$ Setup Time, t_3	(Note 3)		0	-	-	0	-	-	ns
Minimum $\overline{OE}$ Pulse, t_4	(Notes 3, 5)		15	-	-	15	-	-	ns
$\overline{CS}$ to $\overline{OE}$ Setup Time, t_5	(Note 3)		0	-	-	0	-	-	ns
$\overline{OE}$ to $\overline{CS}$ Setup Time, t_6	(Note 3)		0	-	-	0	-	-	ns
IRQ Delay from Start Convert, t_7	(Note 3)		10	20	25	10	20	25	ns
IRQ Pulse Width, t_8		JCD, KCD	190	200	230	190	200	230	ns
		BID	-	-	-	180	195	230	ns
Minimum Cycle Time for Conversion, t_9			-	325	333	-	325	333	ns
IRQ to Data Valid Delay, t_{10}	(Note 3)		-5	0	+5	-5	0	+5	ns
Minimum $\overline{A0}$ Pulse, t_{11}	(Notes 3, 5)		10	-	-	10	-	-	ns
Data Access from $\overline{OE}$ Low, t_{12}	(Note 3)		10	18	25	10	18	25	ns
LSB, Nibble Delay from $\overline{A0}$ High, t_{13}	(Note 3)		-	10	20	-	10	20	ns
MSB Delay from $\overline{A0}$ Low, t_{14}	(Note 3)		-	14	20	-	14	20	ns
$\overline{CS}$ to Float Delay, t_{15}	(Note 3)		10	18	25	10	18	25	ns
Minimum $\overline{CS}$ Pulse, t_{16}	(Notes 3, 5)		15	-	-	15	-	-	ns
$\overline{CS}$ to Data Valid Delay, t_{17}	(Note 3)		10	18	25	10	18	25	ns
Output Fall 2 Time, t_f	(Note 3)		-	5	20	-	5	20	ns
Output Rise Time, t_r	(Note 3)		-	5	20	-	5	20	ns
POWER SUPPLY CHARACTERISTICS									
IV_{CC}			-	170	220	-	170	220	mA
IV_{EE}			-	150	190	-	150	190	mA
IDV_{CC}			-	24	40	-	24	40	mA
IDV_{EE}			-	2	5	-	2	5	mA
Power Dissipation			-	1.7	2.2	-	1.7	2.2	W
PSRR	V_{CC}, V_{EE} ±5%		-	0.01	-	-	0.01	-	%/%

NOTE:

2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Parameter guaranteed by design or characterization and not production tested.
4. Recommended pulse width for $\overline{CONV}$ is 60ns.
5. Recommended minimum pulse width is 25ns.
6. This is the additional current available from the REF_{OUT} pin with the REF_{OUT} pin driving the REF_{IN} pin.
7. The $\overline{A0}$ pin V_{IH} at -40°C may exceed 2.0V by up to 0.4V at initial power up.
8. Excludes error due to internal reference temperature drift.

Timing Diagrams

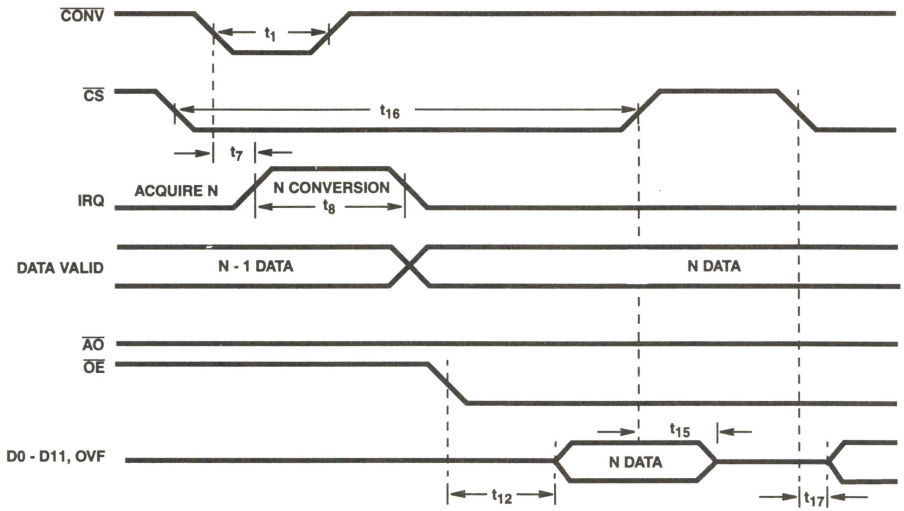


FIGURE 1. SINGLE SHOT TIMING

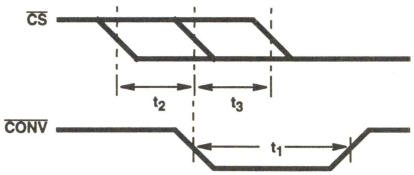


FIGURE 2A. START CONVERSION SETUP TIME

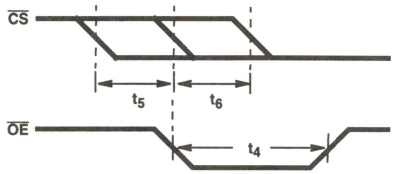


FIGURE 2B. OUTPUT ENABLE SETUP TIME

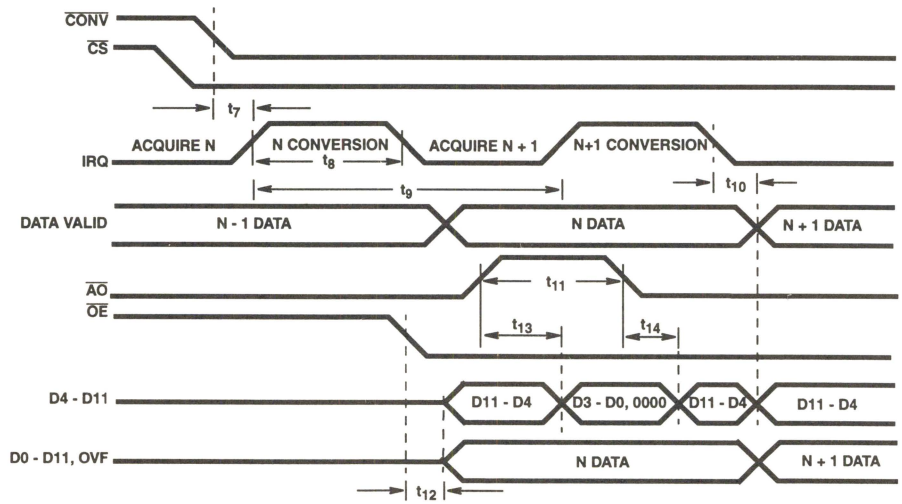


FIGURE 3. CONTINUOUS CONVERSION TIMING

Typical Performance Curves

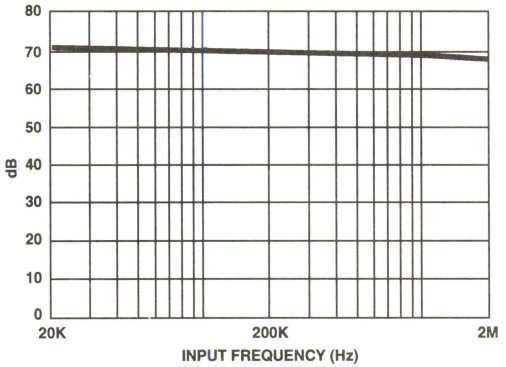


FIGURE 4. TYPICAL SNR vs INPUT FREQUENCY

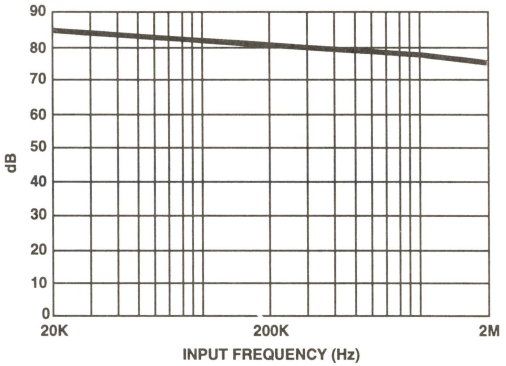


FIGURE 5. TYPICAL THD vs INPUT FREQUENCY

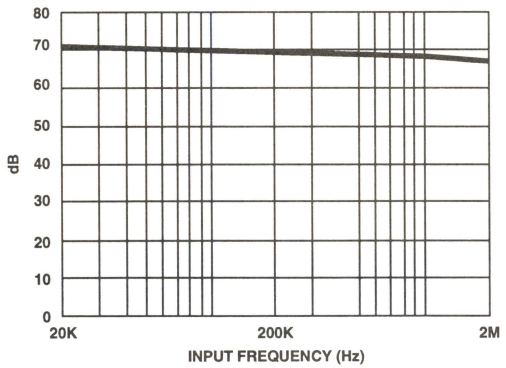


FIGURE 6. TYPICAL SINAD vs INPUT FREQUENCY

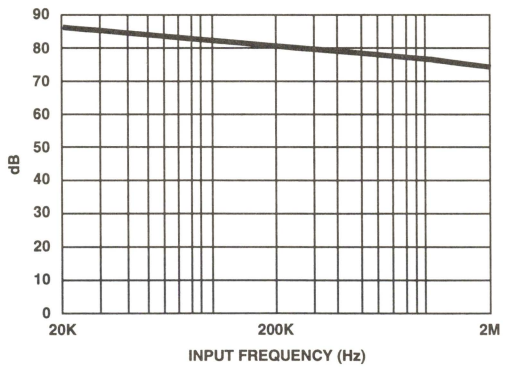


FIGURE 7. TYPICAL SFDR vs INPUT FREQUENCY

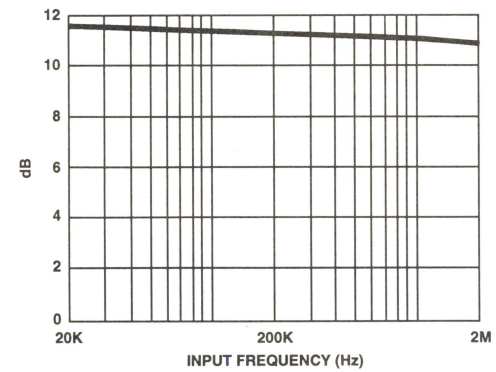


FIGURE 8. TYPICAL EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

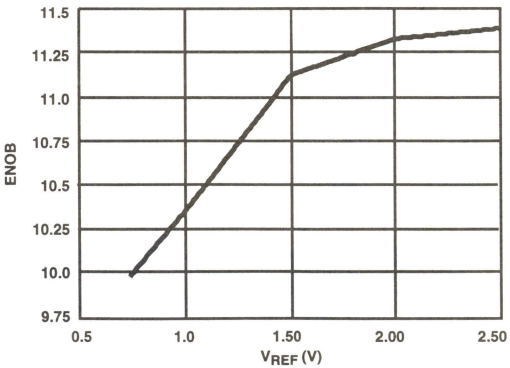


FIGURE 9. EFFECTIVE NUMBER OF BITS vs REFERENCE VOLTAGE (f_S = 3MHz, f_{IN} = 20kHz)

Typical Performance Curves (Continued)

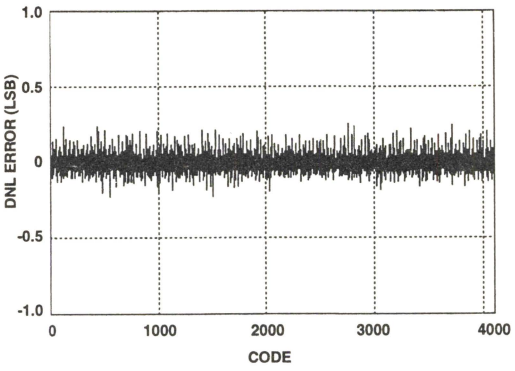


FIGURE 10. DIFFERENTIAL NON-LINEARITY

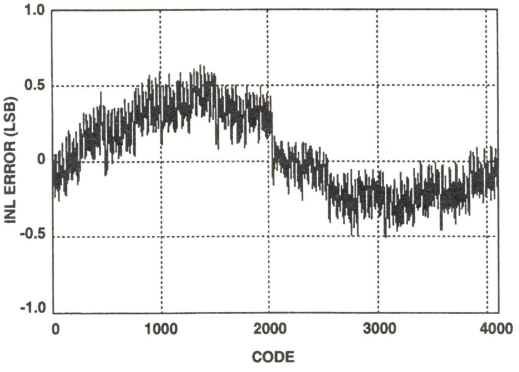


FIGURE 11. INTEGRAL NON-LINEARITY

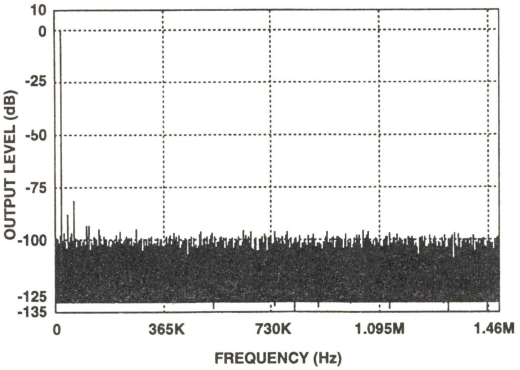


FIGURE 12. FFT SPECTRAL PLOT FOR f_{IN} = 20kHz, f_S = 3MHz

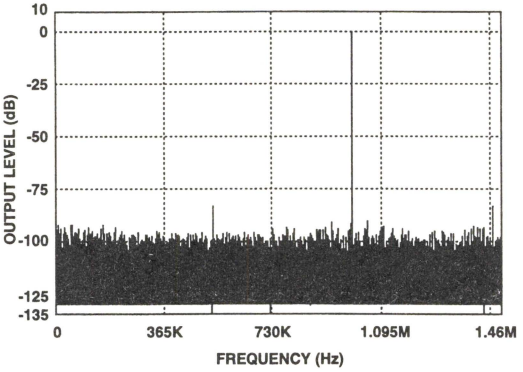


FIGURE 13. FFT SPECTRAL PLOT FOR f_{IN} = 1MHz, f_S = 3MHz

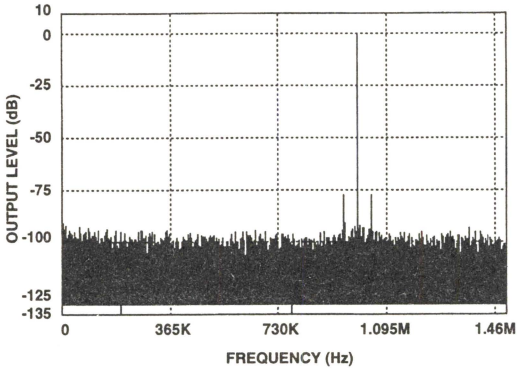


FIGURE 14. FFT SPECTRAL PLOT FOR f_{IN} = 2MHz, f_S = 3MHz

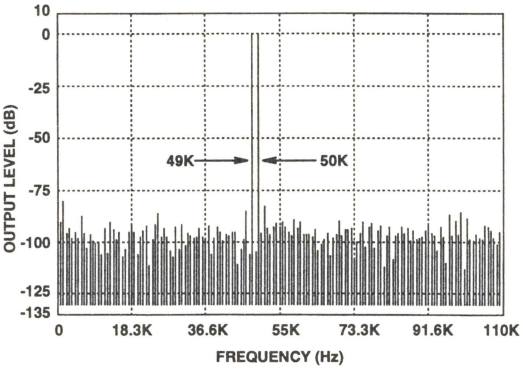


FIGURE 15. INTERMODULATION DISTORTION PLOT FOR f_{IN} = 49kHz, 50kHz at f_S = 3MHz

Pin Descriptions

PIN #	SYMBOL	PIN DESCRIPTION
1	REF_{IN}	External Reference Input.
2	RO_{ADJ}	DAC Offset Adjust (Connect to AGND If Not Used).
3	RG_{ADJ}	DAC Gain Adjust (Connect to AGND If Not Used).
4	AV_{CC}	Analog Positive Power Supply, +5V.
5	REF_{OUT}	Internal Reference Output, +2.5V.
-	NC	No Connection.
6	V_{IN}	Analog Input Voltage.
7	AGND	Analog Ground.
8	ADJ+	Sample/Hold Offset Adjust (Connect to AGND If Not Used).
9	ADJ-	Sample/Hold Offset Adjust (Connect to AGND If Not Used).
10	AV_{EE}	Analog Negative Power Supply, -5V.
11	AV_{CC}	Analog Positive Power Supply, +5V.
12	AGND	Analog Ground.
13	AV_{EE}	Analog Negative Power Supply, -5V.
14	$\overline{A0}$	Output Byte Control Input, active low. When low, data is presented as a 12-bit word or the upper byte (D11 - D4) in 8-bit mode. When high, the second byte contains the lower LSBs (D3 - D0) with 4 trailing zeroes. See Text.
15	$\overline{CS}$	Chip Select Input, active low. Dominates all control inputs.
-	NC	No Connection.
16	$\overline{OE}$	Output Enable Input, active low.
17	$\overline{CONV}$	Convert Start Input. Initiates conversion on the falling edge. If held low, continuous conversion mode overrides and remains in effect until the input goes high.
18	DV_{EE}	Digital Negative Power Supply, -5V.
19	DGND	Digital Ground.
20	DV_{CC}	Digital Positive Power Supply, +5V.
21	AV_{CC}	Analog Positive Power Supply, +5V.
22	D0	Data Bit 0, (LSB).
23	D1	Data Bit 1.
24	D2	Data Bit 2.
25	D3	Data Bit 3.
-	NC	No Connection
26	D4	Data Bit 4.
27	D5	Data Bit 5.
28	D6	Data Bit 6.
29	D7	Data Bit 7.
30	AV_{EE}	Analog Negative Power Supply, -5V.
31	AGND	Analog Ground.
32	DGND	Digital Ground.
33	DV_{CC}	Digital Positive Power Supply, +5V.
34	D8	Data Bit 8.
35	D9	Data Bit 9.
-	NC	No Connection.
36	D10	Data Bit 10.
37	D11	Data Bit 11 (MSB).
38	AV_{CC}	Analog Positive Power Supply, +5V.
39	OVF	Overflow Output. Active high when either an overrange or underrange analog input condition is detected.
40	IRQ	Interrupt ReQuest Output. Goes low when a conversion is complete.

Description

The HI5800 is a 12-bit, two-step, sampling analog-to-digital converter which uses a subranging technique with digital error correction. As illustrated in the block diagram, it uses a sample and hold front end, 7-bit, R-2R D/A converter which is laser trimmed to 14 bits accuracy, a 7-bit BiCMOS flash converter, precision bandgap reference, digital controller and timing generator, error correction logic, output latches and BiCMOS output drivers.

The falling edge of the convert command signal puts the sample and hold (S/H) in the hold mode and the conversion process begins. At this point the Interrupt Request (IRQ) line is set high indicating that a conversion is in progress. The output of the S/H circuit drives the input of the 7-bit flash converter through a switch. After allowing the flash to settle, the intermediate output of the flash is stored in the latches which feed the D/A and error correction logic. The D/A reconstructs the analog signal and feeds the gain amplifier whose summing node subtracts the held signal of the S/H and amplifies the residue by 32. This signal is then switched to the flash for a second pass using the input switch. The output of the second flash conversion is fed directly to the error correction which reconstructs the twelve bit word from the fourteen bit input. The logic also decodes the overflow bit and the polarity of the overflow. The output of the error correction is then gated through the read controller to the output drivers. The data is ready on the bus as soon as the IRQ line goes low.

I/O Control Inputs

The converter has four active low inputs ($\overline{CS}$, $\overline{CONV}$, $\overline{OE}$ and $\overline{A0}$) and fourteen outputs (D0 - D11, IRQ and OVF). All inputs and outputs are TTL compatible and will also interface to the newer TTL compatible families. All four inputs are CMOS high input impedance stages and all outputs are BiMOS drivers capable of driving 100pF loads.

In order to initiate a conversion or read the data bus, $\overline{CS}$ should be held low. The conversion is initiated by the falling edge of the $\overline{CONV}$ command. The $\overline{OE}$ input controls the output bus directly and is independent of the conversion process. The data on the bus changes just before the IRQ goes low. Therefore if the $\overline{OE}$ line is held low all the time, the data on the bus will change just before the IRQ line goes low. The byte control signal $\overline{A0}$ is also independent of the conversion process and the byte can be manipulated anytime. When $\overline{A0}$ is low the 12-bits and overflow word is read on the bus. The bus can also be hooked up such that the upper byte (D11 - D4) is read when $\overline{A0}$ is low. When $\overline{A0}$ is high, the lower byte (D3 - D0) is output on the same eight pins with trailing zeros.

In order to minimize switching noise during a conversion, byte manipulations done using the $\overline{A0}$ signal should be done in the single shot mode and $\overline{A0}$ should be changed during the acquisition phase. For accuracy, allow sufficient time for settling from any glitches before the next conversion.

Once a conversion is started, the converter will complete the conversion and acquisition periods irrespective of the input states. If during these cycles another convert command is issued, it will be ignored until the acquire phase is complete.

Stand Alone Operation

The converter can be operated in a stand alone configuration with bus inputs controlling the converter. The conversion will be started on the negative edge of the convert ($\overline{CONV}$) pulse as long as this pulse is less than the converter throughput rate. If the converter is given multiple convert commands, it will ignore all but the first command until such time when the acquisition period of the next cycle is complete. At this point it will start a new conversion on the first negative edge of the input command. This allows the converter to be synchronized to a multiple of a faster external clock. The new output data of the conversion is available on the same cycle at the negative edge of the IRQ pulse and is valid until the next negative edge of the IRQ pulse. Data may be accessed at any time during these cycles. It should be noted that if the data bus is kept enabled all the time ($\overline{OE}$ is low), then the data will be updating just before the IRQ goes low. During this time, the data may not be valid for a few nanoseconds.

Continuous Convert Mode

The converter can be operated at its maximum rate by taking the $\overline{CONV}$ line low (supplying the first negative edge) and holding it low. This enables the continuous convert mode. During this time, at the end of the internal acquisition period, the converter automatically starts a new conversion. The data will be valid between the IRQ negative edges.

Note that there is no pipeline delay on the data. The output data is available during the same cycle as the conversion and is valid until the next conversion ends. This allows data access to both previous and present conversions in the same cycle.

When initiating a conversion or a series of conversions, the last signal ($\overline{CS}$ and $\overline{CONV}$) to arrive dominates the function. The same condition holds true for enabling the bus to read the data ($\overline{CS}$ and $\overline{OE}$). To terminate the bus operations, the first signal ($\overline{CS}$ and $\overline{OE}$) to arrive dominates the function.

Interrupt Request Output

The interrupt request line (IRQ) goes high at the start of each conversion and goes low to indicate the start of the acquisition. During the time that IRQ is high, the internal sample and hold is in hold mode. At the termination of IRQ, the sample and hold switches to acquire mode which lasts approximately 100ns. If no convert command is issued for a period of time, the sample and hold simply remains in acquire mode tracking the analog input signal until the next conversion cycle is initiated. The IRQ line is the only output that is not three-stateable.

Analog Input, V_{IN}

The analog input of the HI5800 is coupled into the input stage of the Sample and Hold amplifier. The input is a high impedance bipolar differential pair complete with an ESD protection circuit. Typically it has >3MΩ input impedance. With this high input impedance circuit, the HI5800 is easily interfaced to any type of op amp without a requirement for a high drive capability. Adequate precautions should be taken while driving the input from high voltage output op amps to

ensure that the analog input pin is not overdriven above the specified maximum limits. For a +2.5V reference, the analog input range is ±2.5V. This input range scales with the value of the external reference voltage if the internal reference is not used. For best performance, the analog ground pin next to the analog input should be utilized for signal return.

Figures 16 and 17 illustrate the use of an input buffer as a level shifter to convert a unipolar signal to the bipolar input used by the HI5800. Figure 16 is an example of a non-inverting buffer that takes a 0 to 2.5V input and shifts it to ±2.5V. The gain can be calculated from:

$$V_{OUT} = \left[1 + \frac{R2}{(R1 \| R3)}\right] \times V_{IN} - \left[\frac{R1}{R1 + R3}\right] \times V_{OFFSET}$$

$$R1 \| R_3 = \frac{R1R3}{R1 + R3}$$

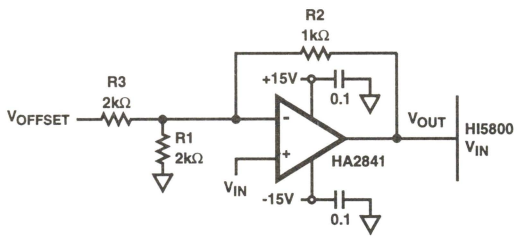


FIGURE 16. NON-INVERTING BUFFER

Figure 17 is an example of an inverting buffer that level shifts a 0V to 5V input to ±2.5V. Its gain can be calculated from:

$$V_{OUT} = (-R2/R1) \times V_{IN} - (R2/R3) \times V_{OFFSET}.$$

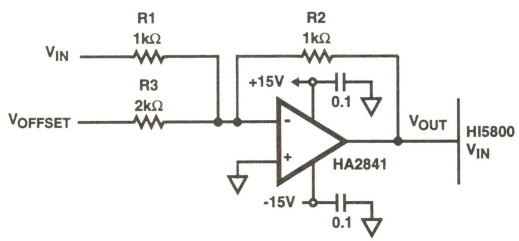


FIGURE 17. INVERTING BUFFER

Note that the correct op amp must be chosen in order to not degrade the overall dynamic performance of the circuit. Recommended op amps are called out in the figures.

Voltage Reference, REF_{OUT}

The HI5800 has a curvature corrected internal band-gap reference generator with a buffer amplifier capable of driving up to 15mA. The band-gap and amplifier are trimmed to give +2.50V. When connected to the reference input pin REF_{IN}, the reference is capable of driving up to 2mA externally. Further loading may degrade the performance of the output voltage. It is recommended that the output of the reference be decoupled with good quality capacitors to reduce the high frequency noise.

Reference Input, REF_{IN}

The converter requires a voltage reference connected to the REF_{IN} pin. This can be the above internal reference or it can be an external reference. It is recommended that adequate high frequency decoupling is provided at the reference input pin in order to minimize overall converter noise.

A user trying to provide an external reference to a HI5800 is faced with two problems. First, the drift of the reference over temperature must be very low. Second, it must be capable of driving the 200Ω input impedance seen at the REF_{IN} pin of the HI5800. Figure 18 is a recommended circuit for doing this that is capable of 2ppm/°C drift over temperature.

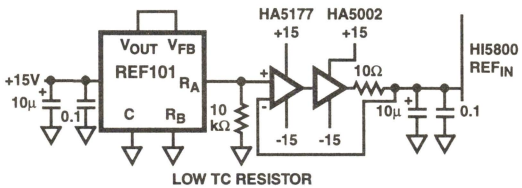


FIGURE 18. EXTERNAL REFERENCE

Supply and Ground Considerations

The HI5800 has separate analog and digital supply and ground pins to help keep digital noise out of the analog signal path. For the best performance, the part should be mounted on a board that provides separate low impedance planes for the analog and digital supplies and grounds. Only connect the two grounds together at one place preferably as close as possible to the part. The supplies should be driven by clean linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the HI5800.

If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Also, it is recommended that the turn-on power supply sequencing be such that the analog positive supply, AI_{CC}, come up first, followed by the remaining supplies.

Refer to the Application Note "Using Harris High Speed A/D Converters" (AN9214) for additional suggestions to consider when using the HI5800.

Error Adjustments

For most applications the accuracy of the HI5800 is sufficient without any adjustments. In applications where accuracy is of utmost importance three external adjustments are possible: S/H offset, D/A offset and D/A gain. Figure 19 illustrates the use of external potentiometers to reduce the HI5800 errors to zero.

The D/A offset (RO_{ADJ}) and S/H offset (ADJ+ and ADJ-) trims adjust the voltage offset of the transfer curve while the D/A gain trim (RG_{ADJ}) adjusts the tilt of the transfer curve around the curve midpoint (code 2048). The 10kΩ potentiometers can be installed to achieve the desired adjustment in the following manner.

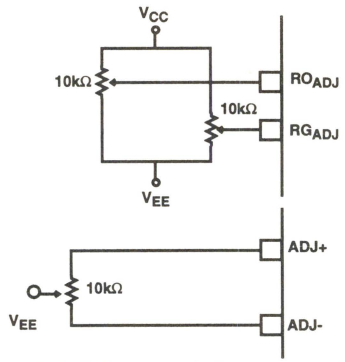


FIGURE 19. D/A OFFSET, D/A GAIN AND S/H OFFSET ADJUSTMENTS

Typically only one of the offset trimpots needs to be used. The offset should first be adjusted to get code 2048 centered at a desired DC input voltage such as 0V. Next the gain trim can be adjusted by trimming the gain pot until the 4094 to 4095 code transition occurs at the desired voltage (2.500V - 1.5 LSBs for a 2.5V reference). The gain trim can also be done by adjusting the gain pot until the code 0 to 1 transition occurs at a particular voltage (-2.5V + 0.5 LSBs for a 2.5V reference). If a nonzero offset is needed, then the offset pot can be adjusted after the gain trim is finished. The gain trim is simplified if an offset trim to zero is done first with a non-zero offset trim done after the gain trim is finished. The D/A offset and S/H offset trimpots have an identical effect on the converter except that the S/H offset is a finer resolution trim. The D/A offset and D/A gain typically have an adjustment range of ±30 LSBs and the S/H offset typically has an adjustment range of ±20 LSBs.

TABLE 1. I/O TRUTH TABLE

INPUTS				OUTPUT	
CS	CONV	OE	A0	IRQ	FUNCTION
1	X	X	X	X	No operation.
0	0	X	X	X	Continuous convert mode.
0	X	0	0	X	Outputs all 12-bits and OVF or upper byte D11 - D4 in 8 bit mode.
0	X	0	1	X	In 8-bit mode, outputs lower LSBs D3 - D0 followed by 4 trailing zeroes and OVF, (See text).
0	1	X	X	0	Converter is in acquisition mode.
0	X	X	X	1	Converter is busy doing a conversion.
0	X	1	X	X	Data outputs and OVF in high impedance state.

X's = Don't Care

TABLE 2. A/D OUTPUT CODE TABLE

CODE DESCRIPTION $LSB = \frac{2\ (REF_{IN})}{4096}$	(NOTE) INPUT VOLTAGE REF_{IN} = 2.5V (V)	OUTPUT DATA (OFFSET BINARY) MSB												LSB
		OVF	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
≥+FS (Full Scale)	≥ +2.5000	1	1	1	1	1	1	1	1	1	1	1	1	1
+FS - 1 LSB	+2.49878	0	1	1	1	1	1	1	1	1	1	1	1	1
$+^3/_4$ FS	+1.8750	0	1	1	1	0	0	0	0	0	0	0	0	0
$+^1/_2$ FS	+1.2500	0	1	1	0	0	0	0	0	0	0	0	0	0
+1 LSB	+0.00122	0	1	0	0	0	0	0	0	0	0	0	0	1
0	0.0000	0	1	0	0	0	0	0	0	0	0	0	0	0
-1 LSB	-0.00122	0	0	1	1	1	1	1	1	1	1	1	1	1
$-^1/_2$ FS	-1.2500	0	0	1	0	0	0	0	0	0	0	0	0	0
$-^3/_4$ FS	-1.8750	0	0	0	1	0	0	0	0	0	0	0	0	0
-FS + 1 LSB	-2.49878	0	0	0	0	0	0	0	0	0	0	0	0	1
≤-FS	≤ -2.5000	1	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: The voltages listed above represent the ideal center of each output code shown as a function of the reference voltage.

If no external adjustments are required the following pins should be connected to analog ground (AGND) for optimum performance: RO_{ADJ}, RG_{ADJ}, ADJ+, and ADJ-.

Typical Application Schematic

A typical application schematic diagram for the HI5800 is shown with the block diagram. The adjust pins are shown with 10kΩ potentiometers used for gain and offset adjustments. These potentiometers may be left out and the respective pins should be connected to ground for best untrimmed performance.

Definitions

Static Performance Definitions

Offset, Full scale, and gain all use a measured value of the internal voltage reference to determine the ideal plus and minus full scale values. The results are all displayed in LSBs.

Offset Error (V_{OS})

The first code transition should occur at a level $^1/_2$ LSB above the negative full scale. Offset is defined as the deviation of the actual code transition from this point. Note that this is adjustable to zero.

Full Scale Error (FSE)

The last code transition should occur for a analog input that is $1^1/_2$ LSBs below positive full scale. Full scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed for no missing codes over all temperature ranges.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection (PSRR)

Each of the power supplies are moved plus and minus 5% and the shift in the offset and full scale error is noted. The number reported is the percent change in these parameters versus full scale divided by the percent change in the supply.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5800. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests. Distortion results are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02,$$

where: $V_{CORR} = 0.5dB$.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present on the inputs. The ratio of the measured signal to the distortion terms is calculated. The IMD products used to calculate the total distortion are (f_2-f_1), (f_2+f_1), $(2f_1-f_2)$, $(2f_1+f_2)$, $(2f_2-f_1)$, $(2f_2+f_1)$, $(3f_1-f_2)$, $(3f_1+f_2)$, $(3f_2-f_1)$, $(3f_2+f_1)$, $(2f_2-2f_1)$, $(2f_2+2f_1)$, $(2f_1)$, $(2f_2)$, $(2f_1)$, $(2f_2)$, $(4f_1)$, $(4f_2)$. The data reflects the sum of all the IMD products.

Full Power Input Bandwidth

Full power input bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Die Characteristics

DIE DIMENSIONS:

202 mils x 283 mils x 19 mils

TRANSISTOR COUNT:

10K

METALLIZATION:

Metal 1: Type: AlSiCu, Thickness: 6kÅ +1500A/-750Å
Metal 2: Type: AlSiCu, Thickness: 16kÅ +2500A/-1100Å

SUBSTRATE POTENTIAL (Powered Up):

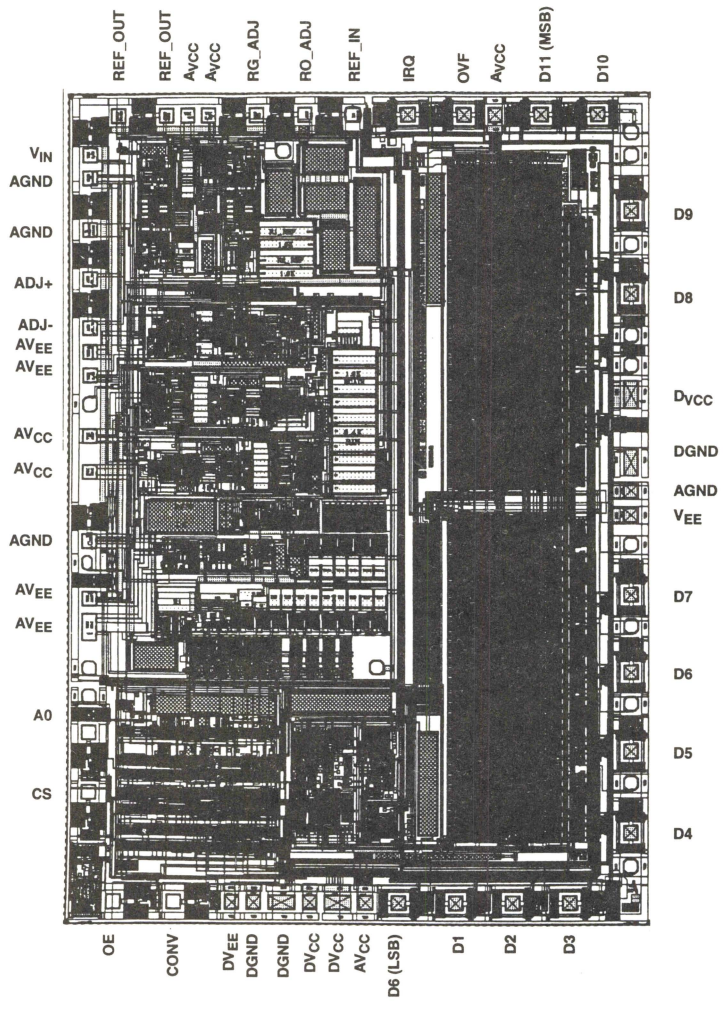
V_{EE}

PASSIVATION:

Type: Sandwich Passivation - Nitride +
Undoped Si Glass (USG)
Thickness: Nitride - 4KÅ, USG - 8KÅ, Total - 12kÅ ±2kÅ

Metallization Mask Layout

HI5800



HI5804

August 1997

12-Bit, 5 MSPS A/D Converter

Features

- Sampling Rate ..... 5 MSPS
- Low Power
- Internal Sample and Hold
- Fully Differential Architecture
- Full Power Input Bandwidth 100MHz
- Low Distortion
- Internal Reference
- TTL/CMOS Compatible Digital I/O
- Digital Outputs ..... 3V to 5V

Applications

- High Speed Data Acquisition Systems
- Digital IF Communication Systems
- Document and Film Scanners
- Medical Imaging
- Radar Signal Analysis
- Vibration/Waveform Spectrum Analysis
- Digital Servo Loop Control
- Reference Literature
  - AN9214 Using Harris High Speed Converters
  - AN9647 Using the HI5804 Evaluation Board

Description

The HI5804 is a monolithic, 12-bit, Analog-to-Digital Converter fabricated in Harris' HBC10 BiCMOS process. It is designed for high speed, high resolution applications where wide bandwidth and low power consumption are essential.

The HI5804 is designed in a fully differential pipelined architecture with a front end differential-in-differential-out sample-and-hold (S/H). The HI5804 has excellent dynamic performance while consuming 300mW power at 5 MSPS.

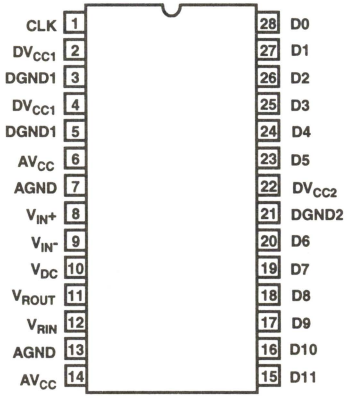
The 100MHz full power input bandwidth is ideal for communication systems and document scanner applications. Data output latches are provided which present valid data to the output bus with a latency of 3 clock cycles. The digital outputs have a separate supply pin which can be powered from a 3.0V to 5.0V supply.

Ordering Information

PART NUMBER	SAMPLE RATE	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5804KCB	5 MSPS	0 to 70	28 Ld SOIC	M28.3
HI5804EVAL		25	Evaluation Board	

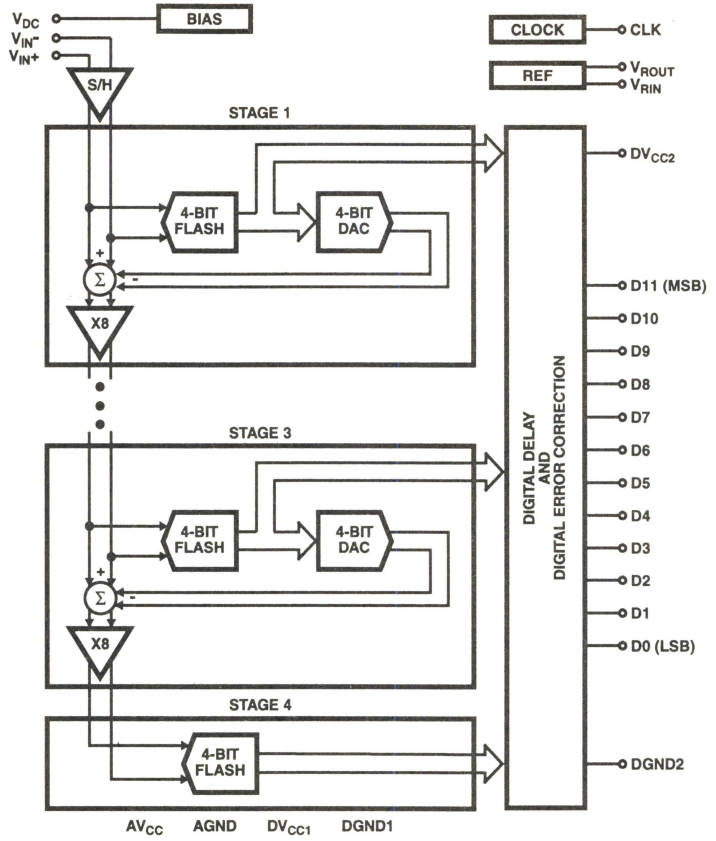
Pinout

HI5804
(SOIC)
TOP VIEW

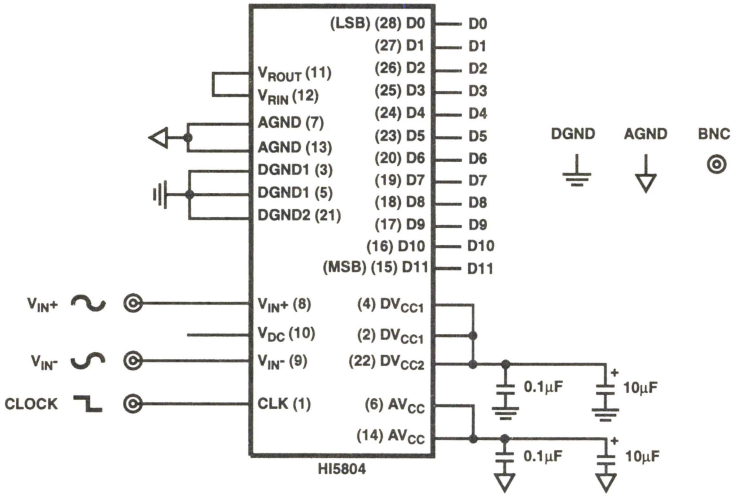


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage, AV_{CC} or DV_{CC} to A_{GND} or D_{GND} . . . . . +6.0V
D_{GND} to A_{GND} 0.3V
Digital I/O Pins . . . . . D_{GND} to DV_{CC}
Analog I/O Pins. . . . . A_{GND} to AV_{CC}

Operating Conditions

Temperature Range, HI5804KCB . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA}(°C/W)
HI5804KCB 70
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$, $f_S = 5$ MSPS at 50% Duty Cycle, $V_{RIN} = 3.5V$, $C_L = 10pF$, $T_A = 25°C$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		12	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±2	-	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1	LSB
Offset Error, V_{OS}	f_{IN} = DC	-	12	-	LSB
Full Scale Error, FSE	f_{IN} = DC	-	24	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	-	MSPS
Maximum Conversion Rate	No Missing Codes	-	5	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	-	10.3	-	Bits
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	64	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	-	65	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-	-70	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-73		dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-73	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz	-	73	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	-66	-	dBc
Transient Response		-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive	-	2	-	Cycle
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range ($V_{IN}+ - V_{IN}-$)		-	±2.0	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	4.0	-	V
Analog Input Resistance, R_{IN}	(Notes 2, 3)	1	-	-	MΩ
Analog Input Capacitance, C_{IN}		-	10	-	pF
Analog Input Bias Current, I_B+ or I_B-		-10	-	+10	µA
Differential Analog Input Bias Current $I_{B\,DIFF} = (I_B+ - I_B-)$		-	±0.5	-	µA
Full Power Input Bandwidth, FPBW		-	100	-	MHz
Analog Input Common Mode Voltage ($V_{IN}+ + V_{IN}-)/2$	Differential Mode (Note 2)	1	2.3	4	V

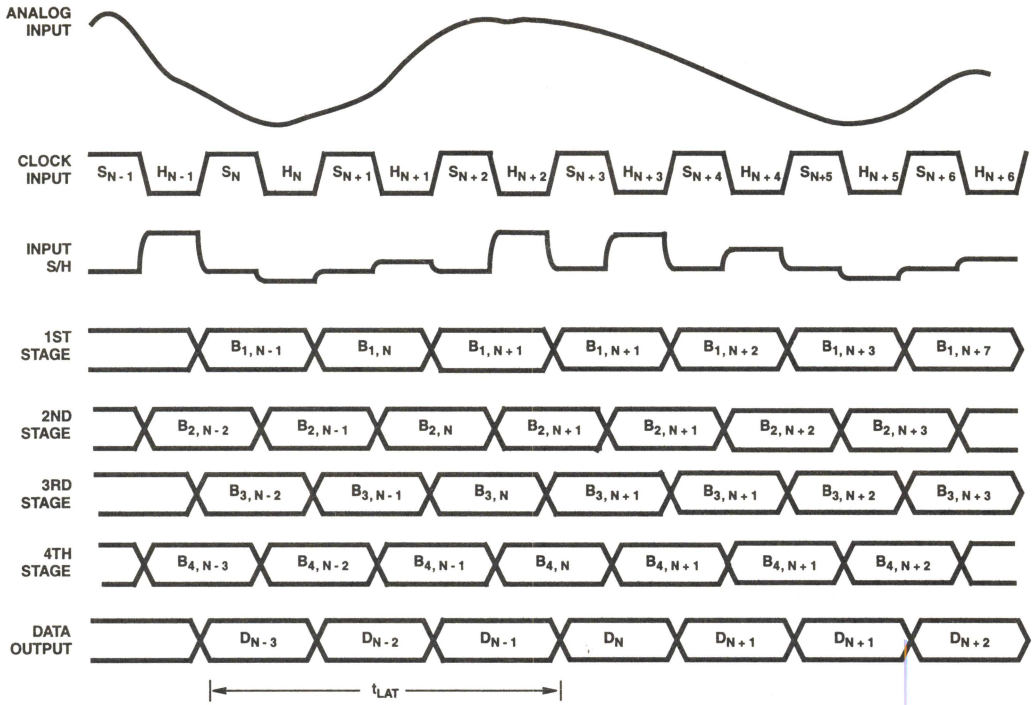
Electrical Specifications $AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$, $f_S = 5$ MSPS at 50% Duty Cycle, $V_{RIN} = 3.5V$, $C_L = 10pF$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL VOLTAGE REFERENCE					
Reference Output Voltage, V_{ROUT}		-	3.5	-	V
Reference Output Current		-	-	1	mA
REFERENCE INPUT					
Total Reference Resistance, R_L		-	7.8	-	kΩ
Reference Current		-	450	-	µA
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	2.3	-	V
Max Output Current (Not to Exceed)		-	-	1	mA
DIGITAL INPUT, CLK					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	$V_{CLK} = 5V$	-	-	10.0	µA
Input Logic Low Current, I_{IL}	$V_{CLK} = 0V$	-	-	10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS, D0-D11					
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$ (Note 2)	1.6	-	-	mA
	$DV_{CC2} = 3.0V$, $V_O = 0.4V$	-	1.6	-	mA
Output Logic Source Current, I_{OH}	$V_O = 2.4V$ (Note 2)	-0.2	-	-	mA
	$DV_{CC2} = 3.0V$, $V_O = 2.4V$	-	-0.2	-	mA
Output Capacitance, C_{OUT}		-	5	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps_{RMS}
Data Output Delay, t_{OD}		-	8	-	ns
Data Output Hold, t_H		-	8	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	3	Cycle
Clock Pulse Width (Low)	5MHz Clock	90	100	110	ns
Clock Pulse width (High)	5MHz Clock	90	100	110	ns
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, AV_{CC}		4.75	5.0	5.25	V
Digital Supply Voltage, DV_{CC1}		4.75	5.0	5.25	V
Digital Output Supply Voltage, DV_{CC2}		2.85	-	5.25	V
Total Supply Current, I_{CC}	$V_{IN}+ - V_{IN}- = 2V$	-	60	-	mA
Analog Supply Current, AI_{CC}	$V_{IN}+ - V_{IN}- = 2V$	-	46	-	mA
Digital Supply Current, DI_{CC1}	$V_{IN}+ - V_{IN}- = 2V$	-	13	-	mA
Digital Output Supply Current, DI_{CC2}	$V_{IN}+ - V_{IN}- = 2V$	-	1	-	mA
Power Dissipation	$V_{IN}+ - V_{IN}- = 2V$	-	300	-	mW
Offset Error Sensitivity, ΔV_{OS}	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±16	-	LSB
Gain Error Sensitivity, ΔFSE	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±16	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock off (clock low, hold mode).

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M,N}$: M-th stage digital output corresponding to N-th sampled input. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5804 INTERNAL CIRCUIT TIMING

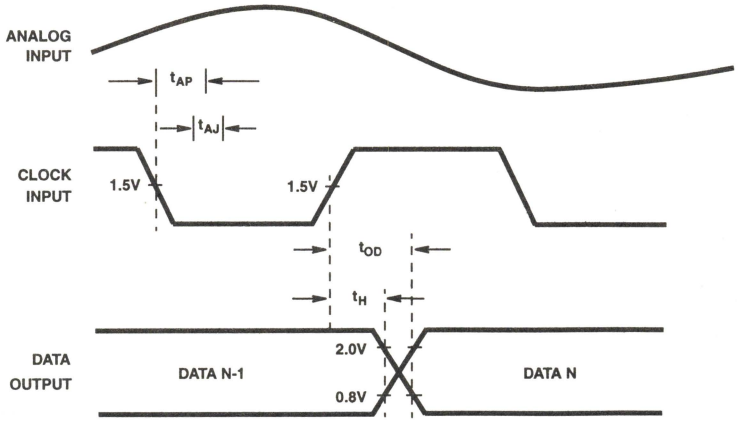


FIGURE 2. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

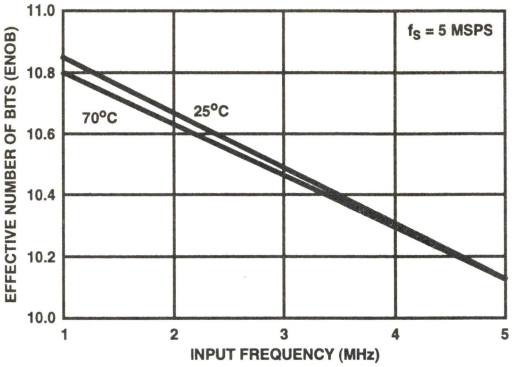


FIGURE 3. TYPICAL ENOB vs INPUT FREQUENCY

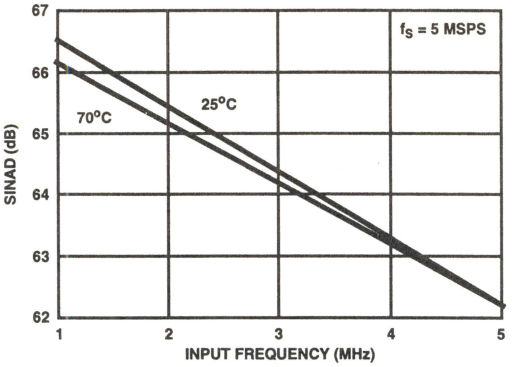


FIGURE 4. TYPICAL SINAD vs INPUT FREQUENCY

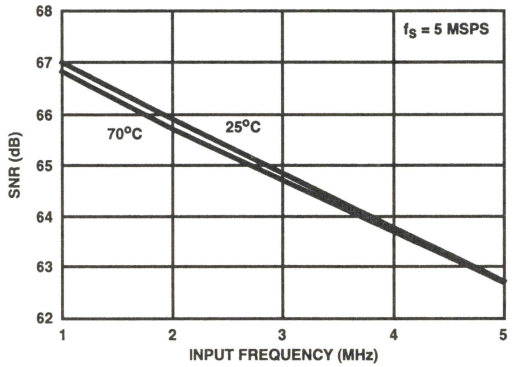


FIGURE 5. TYPICAL SNR vs INPUT FREQUENCY

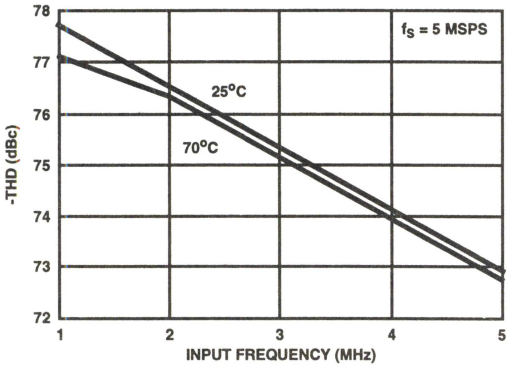


FIGURE 6. TYPICAL -THD vs INPUT FREQUENCY

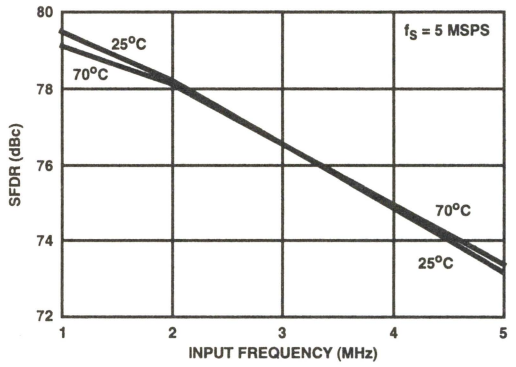


FIGURE 7. TYPICAL SFDR vs INPUT FREQUENCY

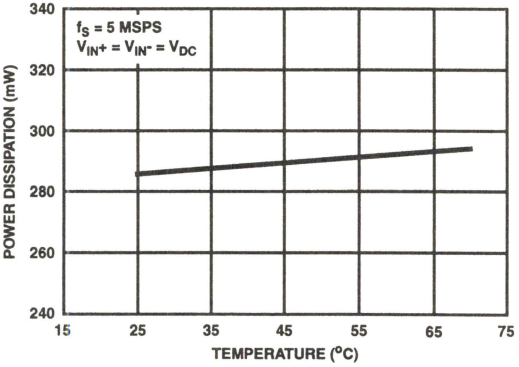


FIGURE 8. TYPICAL POWER DISSIPATION vs TEMPERATURE

Pin Descriptions

PIN #	NAME	DESCRIPTION
1	CLK	Sample Clock Input.
2	DV_{CC1}	Digital Supply (+5.0V).
3	DGND1	Digital Ground.
4	DV_{CC1}	Digital Supply (+5.0V).
5	DGND1	Digital Ground.
6	AV_{CC}	Analog Supply (+5.0V).
7	AGND	Analog Ground.
8	$V_{IN}+$	Positive Analog Input.
9	$V_{IN}-$	Negative Analog Input.
10	V_{DC}	DC Bias Voltage Output.
11	V_{ROUT}	Reference Voltage Output.
12	V_{RIN}	Reference Voltage Input.
13	AGND	Analog Ground.
14	AV_{CC}	Analog Supply (+5.0V).
15	D11	Data Bit 11 Output (MSB).
16	D10	Data Bit 10 Output.
17	D9	Data Bit 9 Output.
18	D8	Data Bit 8 Output.
19	D7	Data Bit 7 Output.
20	D6	Data Bit 6 Output.
21	DGND2	Digital Output Ground.
22	DV_{CC2}	Digital Output Supply (+3.0V to +5.0V).
23	D5	Data Bit 5 Output.
24	D4	Data Bit 4 Output.
25	D3	Data Bit 3 Output.
26	D2	Data Bit 2 Output.
27	D1	Data Bit 1 Output.
28	D0	Data Bit 0 Output (LSB).

Detailed Description

Theory of Operation

The HI5804 is a 12-bit, fully-differential, sampling pipeline A/D converter with digital error correction. Figure 9 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 100MHz for the converter.

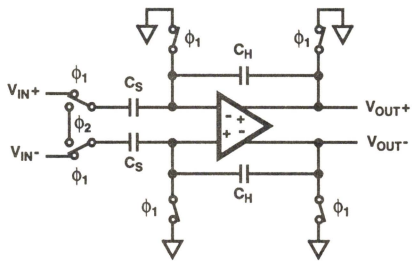


FIGURE 9. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, three identical pipeline subconverter stages, each containing a four-bit flash converter, a four-bit digital-to-analog converter and an amplifier with a voltage gain of 8, follow the S/H circuit with the fourth stage being only a four bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual sub-converter clock signal is offset by 180 degrees from the previous stage clock signal with the result that alternate stages in the pipeline will perform the same operation.

The 4-bit digital output of each stage is fed to a digital delay line controlled by the internal clock. The purpose of the delay line is to align the digital output data to the corresponding sampled analog input signal. This delayed data is fed to the digital error correction circuit which corrects the error in the output data with the information contained in the redundant bits to form the final twelve bit output for the converter.

Because of the pipeline nature of this converter, the data on the bus is output at the 3rd cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The output data is synchronized to the external clock by a latch. The digital outputs are in offset binary format (See Table 1).

Internal Reference Generator, V_{ROUT} and V_{RIN}

The HI5804 has an internal reference voltage generator, therefore no external reference voltage is required. V_{ROUT} must be connected to V_{RIN} when using the internal reference voltage.

The HI5804 can be used with an external reference voltage. The converter requires only one external reference voltage connected to the V_{RIN} pin with V_{ROUT} left open.

The HI5804 is tested with V_{RIN} equal to 3.5V. Internal to the converter two reference voltages of 1.3V and 3.3V are generated for a fully differential input signal range of ±2V.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference voltage input pin, V_{RIN}.

Analog Input, Differential Connection

The analog input to the HI5804 can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 10) will give the best performance for the converter.

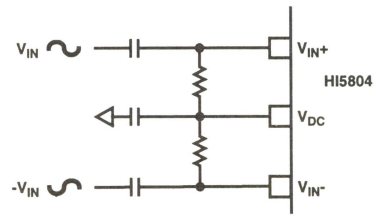


FIGURE 10. AC COUPLED DIFFERENTIAL INPUT

Since the HI5804 is powered off a single +5V supply, the analog input must be biased so it lies within the analog input common mode voltage range of 1.0V to 4.0V. The performance of the ADC does not change significantly with the value of the common mode voltage.

A 2.3V DC bias voltage source, V_{DC}, half way between the top and bottom internal reference voltages, is made available to the user to help simplify circuit design when using a differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the analog input common mode voltage range over temperature.

The difference between the converter's two internal voltage references is 2V. For the AC coupled differential input, (Figure 10), if V_{IN} is a $2V_{P-P}$ sinewave with $-V_{IN}$ being 180 degrees out of phase with V_{IN}, the converter will be at positive full scale when the $V_{IN}+$ input is at V_{DC} + 1V and the $V_{IN}-$ input is at V_{DC} - 1V ($V_{IN}+ - V_{IN}- = 2V$). Conversely, the ADC will be at negative full scale when the $V_{IN}+$ input is equal to V_{DC} - 1V and $V_{IN}-$ is at V_{DC} + 1V ($V_{IN}+ - V_{IN}- = -2V$).

Analog Input, Single-Ended Connection

The configuration shown in Figure 11 may be used with a single ended AC coupled input. Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND.

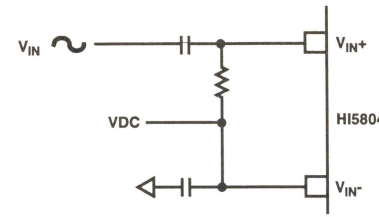


FIGURE 11. AC COUPLED SINGLE ENDED INPUT

Again, the difference between the two internal voltage references is 2V. If V_{IN} is a $4V_{P-P}$ sinewave, then $V_{IN}+$ is a $4V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive full scale when $V_{IN}+$ is at VDC + 2V ($V_{IN}+ - V_{IN}- = 2V$) and will be at negative full scale when $V_{IN}+$ is equal to VDC - 2V ($V_{IN}+ - V_{IN}- = -2V$). In this case, VDC could range between 2V and 3V without a significant change in ADC performance. The simplest way to produce VDC is to use the V_{DC} bias voltage output of the HI5804.

A single ended source will give better overall system performance if it is first converted to differential before driving the analog input of the HI5804.

Digital I/O and Clock Requirements

The HI5804 provides a standard high-speed interface to external TTL/CMOS logic families. The digital CMOS clock input has TTL level thresholds. The low input bias current allows the HI5804 to be driven by CMOS logic.

The digital CMOS outputs have a separate digital supply. This allows the digital outputs to operate from a 3.0V to 5.0V supply. When driving CMOS logic, the digital outputs will swing to the rails. When driving standard TTL loads, the digital outputs will meet standard TTL level requirements even with a 3.0V supply.

In order to ensure rated performance of the HI5804, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5804 will only be guaranteed at conversion rates above 0.5 MSPS. This ensures proper performance of the internal dynamic circuits.

Supply and Ground Considerations

The HI5804 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5804 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to Application Note AN9214, "Using Harris High Speed A/D Converters" for additional considerations when using high speed converters.

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE† (USING INTERNAL REFERENCE)	OFFSET BINARY OUTPUT CODE											
		MSB											LSB
		D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) - $^1/_4$ LSB	+1.99976V	1	1	1	1	1	1	1	1	1	1	1	1
+FS - $1^1/_4$ LSB	1.99878V	1	1	1	1	1	1	1	1	1	1	1	0
+ $^3/_4$ LSB	732.4µV	1	0	0	0	0	0	0	0	0	0	0	0
- $^1/_4$ LSB	-244.1µV	0	1	1	1	1	1	1	1	1	1	1	1
-FS + $1^3/_4$ LSB	-1.99829V	0	0	0	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + $^3/_4$ LSB	-1.99927V	0	0	0	0	0	0	0	0	0	0	0	0

† The voltages listed above represent the ideal center of each offset binary output code.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$ LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is $^3/_4$ LSB below positive full-scale with the offset error removed. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Sensitivity

Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5804. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests. SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency, excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by:

$$ENOB = (SINAD + V_{CORR} - 1.76)/6.02$$

where: $V_{CORR} = 0.5dB$

V_{CORR} adjusts the ENOB for the amount the input is below fullscale.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present on the inputs. The ratio of the measured distortion terms to the signal is calculated. The terms included in the calculation are $(f_1 + f_2)$, $(f_1 - f_2)$, $(2f_1)$, $(2f_2)$, $(2f_1 + f_2)$, $(2f_1 - f_2)$, $(f_1 + 2f_2)$, $(f_1 - 2f_2)$. The ADC is tested with each tone 6dB below full scale.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component in the spectrum below $f_S/2$.

Transient Response

Transient response is measured by providing a full scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 12-bit accuracy.

Overvoltage Recovery

Overvoltage Recovery is measured by providing a full scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 12-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the difference between the two internal voltage references. The bandwidth given is measured at the specified sampling frequency.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture Jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the digital data is output on the bus after the third cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input sample by 3 clock cycles.

HARRIS SEMICONDUCTOR

HI5805

August 1997

12-Bit, 5 MSPS A/D Converter

Features

- Sampling Rate ..... 5 MSPS
- Low Power
- Internal Sample and Hold
- Fully Differential Architecture
- Full Power Input Bandwidth 100MHz
- Low Distortion
- Internal Voltage Reference
- TTL/CMOS Compatible Digital I/O
- Digital Outputs ..... 5V to 3.0V

Applications

- Digital Communication Systems
- Undersampling Digital IF
- Document Scanners
- Additional Reference Documents
  - AN9214 Using Harris High Speed A/D Converters
  - AN9707 Using the HI5805EVAL1 Evaluation Board

Description

The HI5805 is a monolithic, 12-bit, Analog-to-Digital Converter fabricated in Harris' HBC10 BiCMOS process. It is designed for high speed, high resolution applications where wide bandwidth and low power consumption are essential.

The HI5805 is designed in a fully differential pipelined architecture with a front end differential-in-differential-out sample-and-hold (S/H). The HI5805 has excellent dynamic performance while consuming 300mW power at 5 MSPS.

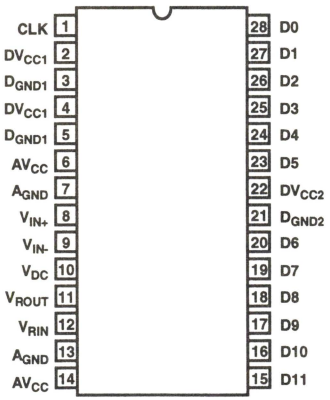
The 100MHz full power input bandwidth is ideal for communication systems and document scanner applications. Data output latches are provided which present valid data to the output bus with a latency of 3 clock cycles. The digital outputs have a separate supply pin which can be powered from a 3.0V to 5.0V supply.

Ordering Information

PART NUMBER	SAMPLE RATE	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5805BIB	5 MSPS	-40 to 85	28 Ld SOIC (W)	M28.3
HI5805EVAL1		25	Evaluation Board	

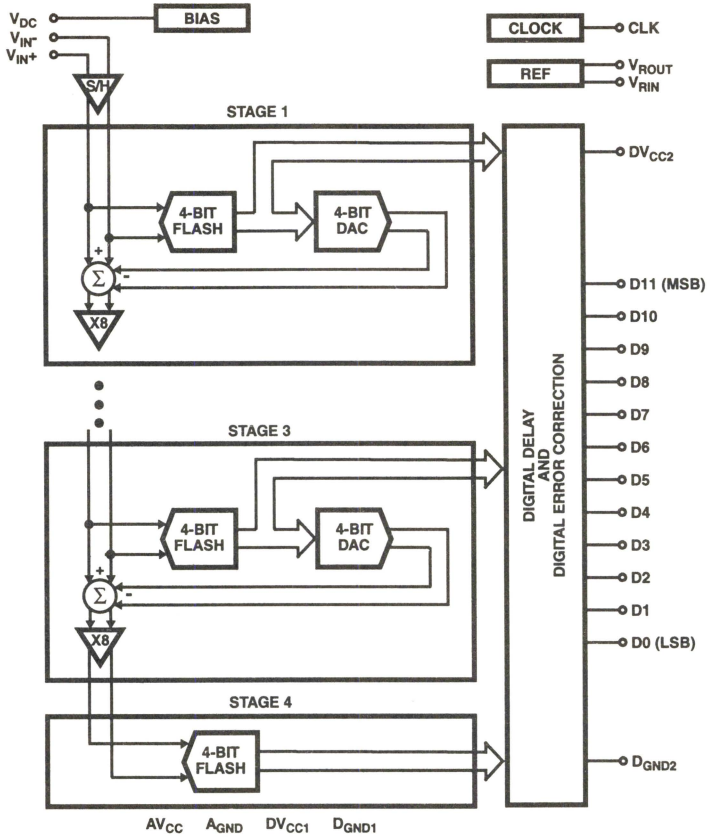
Pinout

HI5805 (SOIC)
TOP VIEW

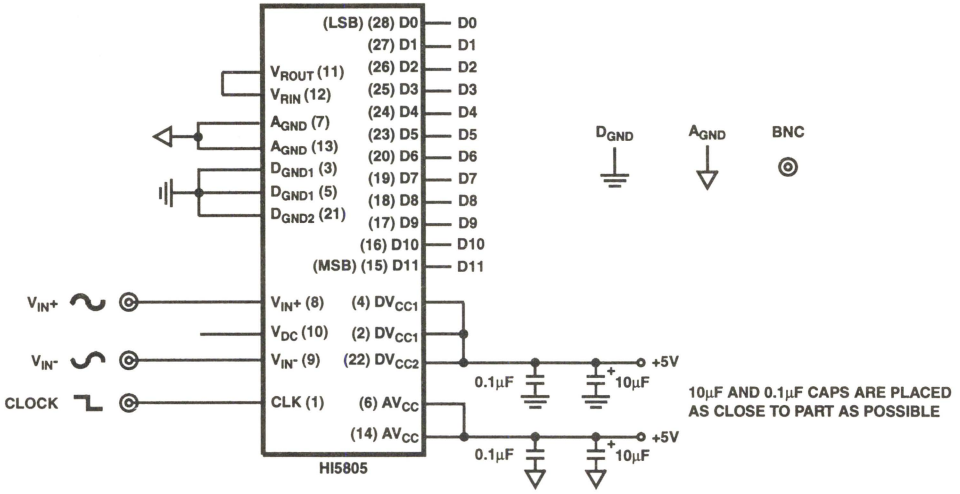


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage, AV_{CC} or DV_{CC} to A_{GND} or D_{GND} . . . . . +6.0V
D_{GND} to A_{GND} 0.3V
Digital I/O Pins . . . . . D_{GND} to DV_{CC}
Analog I/O Pins. . . . . A_{GND} to AV_{CC}

Operating Conditions

Temperature Range, HI5805BIB . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = DV_{CC2} = DV_{CC3} = +5.0V$, $f_S = 5$ MSPS at 50% Duty Cycle, $V_{RIN} = 3.5V$, $C_L = 10pF$, $T_A = -40°C$ to 85°C, Differential Analog Input, Typical Values are Test Results at 25°C, Unless Otherwise Specified

PARAMETER	TEST CONDITION	HI5805BIB (-40°C TO 85°C)			UNITS
		MIN	TYP	MAX	
ACCURACY					
Resolution		12	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±1	±2	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1	LSB
Offset Error, V_{OS}	f_{IN} = DC	-	19	-	LSB
Full Scale Error, FSE	f_{IN} = DC	-	32	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	-	MSPS
Maximum Conversion Rate	No Missing Codes	5	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	10.0	11	-	Bits
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	68	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	-	68	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-	-80	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-86		dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-83	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz	-	83	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	-68	-	dBc
Transient Response		-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive	-	2	-	Cycle
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range ($V_{IN}+ - V_{IN}-$)		-	±2.0	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	4.0	-	V
Analog Input Resistance, R_{IN}	(Notes 2, 3)	1	-	-	MΩ
Analog Input Capacitance, C_{IN}		-	10	-	pF
Analog Input Bias Current, I_B+ or I_B-	(Note 3)	-10	-	+10	µA
Differential Analog Input Bias Current $I_{B\,DIFF} = (I_B+ - I_B-)$		-	±0.5	-	µA
Full Power Input Bandwidth, FPBW		-	100	-	MHz
Analog Input Common Mode Voltage Range ($V_{IN}+ + V_{IN}-$)/2	Differential Mode (Note 2)	1	2.3	4	V

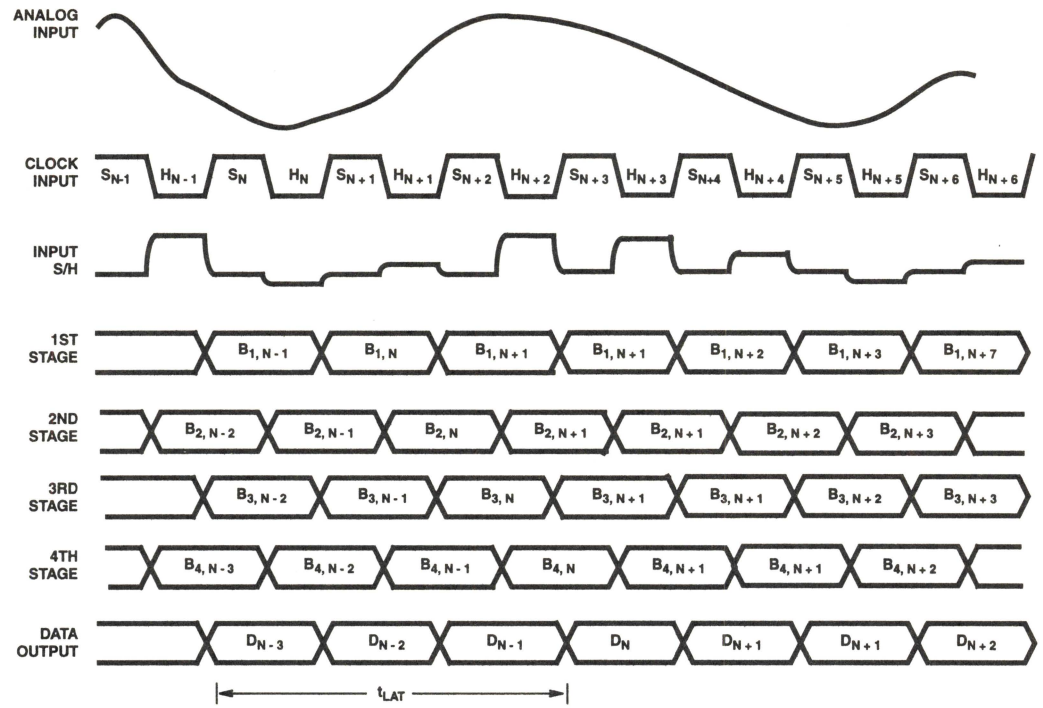
Electrical Specifications $AV_{CC} = DV_{CC1} = DV_{CC2} = DV_{CC3} = +5.0V$, $f_S = 5$ MSPS at 50% Duty Cycle, $V_{RIN} = 3.5V$, $C_L = 10pF$, $T_A = -40^oC$ to 85^oC, Differential Analog Input, Typical Values are Test Results at 25^oC, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	HI5805BIB (-40°C TO 85°C)			UNITS
		MIN	TYP	MAX	
INTERNAL VOLTAGE REFERENCE					
Reference Output Voltage, V_{ROUT} (Loaded)		-	3.5	-	V
Reference Output Current		-	-	1	mA
Reference Temperature Coefficient		-	200	-	ppm/°C
REFERENCE VOLTAGE INPUT					
Reference Voltage Input, V_{RIN}		-	3.5	-	V
Total Reference Resistance, R_L		-	7.8	-	kΩ
Reference Current		-	450	-	µA
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	2.3	-	V
Max Output Current (Not To Exceed)		-	-	1	mA
DIGITAL INPUTS (CLK)					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	$V_{CLK} = 5V$	-	-	10.0	µA
Input Logic Low Current, I_{IL}	$V_{CLK} = 0V$	-	-	10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS (D0-D11)					
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$ (Note 2)	1.6	-	-	mA
	$DV_{CC3} = 3.0V$, $V_O = 0.4V$	-	1.6	-	mA
Output Logic Source Current, I_{OH}	$V_O = 2.4V$ (Note 2)	-0.2	-	-	mA
	$DV_{CC3} = 3.0V$, $V_O = 2.4V$	-	-0.2	-	mA
Output Capacitance, C_{OUT}		-	5	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps (RMS)
Data Output Delay, t_{OD}		-	8	-	ns
Data Output Hold, t_H		-	8	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	3	Cycles
Clock Pulse Width (Low)	5MHz Clock	90	100	110	ns
Clock Pulse Width (High)	5MHz Clock	90	100	110	ns
POWER SUPPLY CHARACTERISTICS					
Total Supply Current, I_{CC}	$V_{IN}+ - V_{IN}- = 2V$	-	60	70	mA
Analog Supply Current, AI_{CC}	$V_{IN}+ - V_{IN}- = 2V$	-	46	-	mA
Digital Supply Current, DI_{CC}	$V_{IN}+ - V_{IN}- = 2V$	-	13	-	mA
Output Supply Current, DI_{CC1}	$V_{IN}+ - V_{IN}- = 2V$	-	1	-	mA
Power Dissipation	$V_{IN}+ - V_{IN}- = 2V$	-	300	350	mW
Offset Error PSRR, ΔV_{OS}	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	2	-	LSB
Gain Error PSRR, ΔFSE	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	30	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock off (clock low, hold mode).

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M,N}$: M-th stage digital output corresponding to N-th sampled input.
7. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. INTERNAL CIRCUIT TIMING

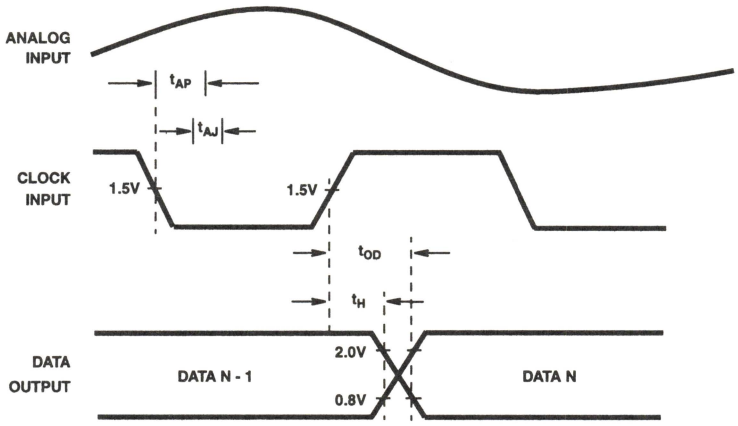


FIGURE 2. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

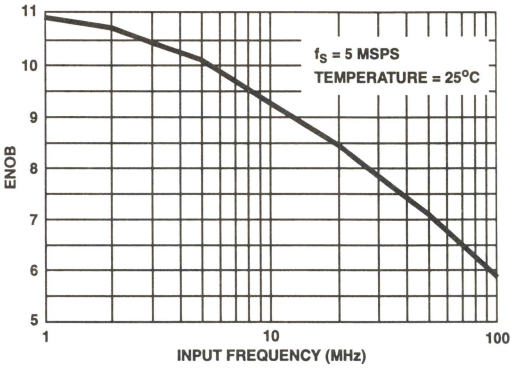


FIGURE 3. EFFECTIVE NUMBER OF BITS (ENOB) vs INPUT FREQUENCY

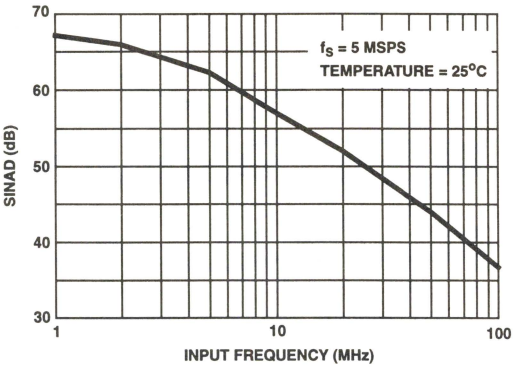


FIGURE 4. SIGNAL TO NOISE AND DISTORTION (SINAD) vs INPUT FREQUENCY

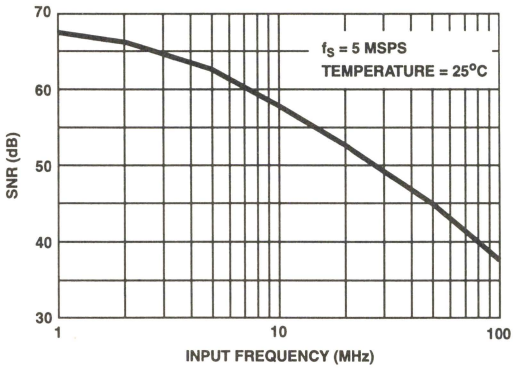


FIGURE 5. SIGNAL TO NOISE RATIO (SNR) vs INPUT FREQUENCY

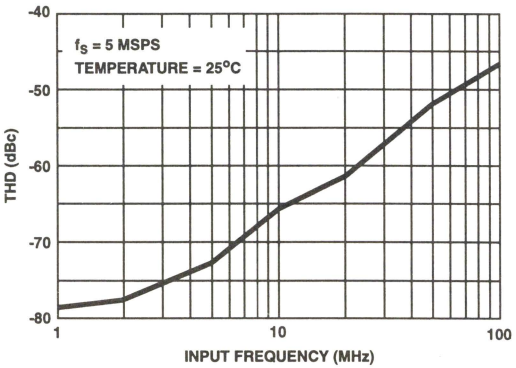


FIGURE 6. TOTAL HARMONIC DISTORTION (THD) vs INPUT FREQUENCY

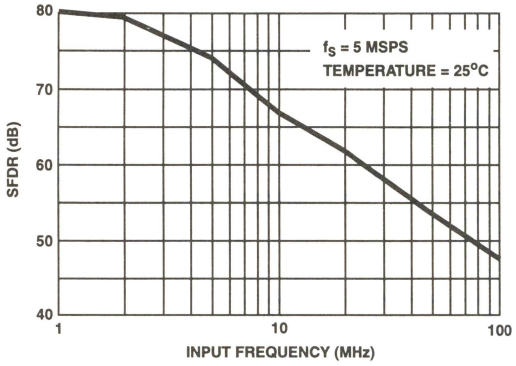


FIGURE 7. SPURIOUS FREE DYNAMIC RANGE (SFDR) vs INPUT FREQUENCY

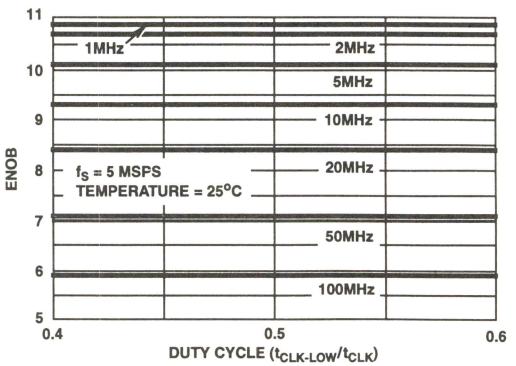


FIGURE 8. EFFECTIVE NUMBER OF BITS (ENOB) vs CLOCK DUTY CYCLE AND INPUT FREQUENCY

Typical Performance Curves (Continued)

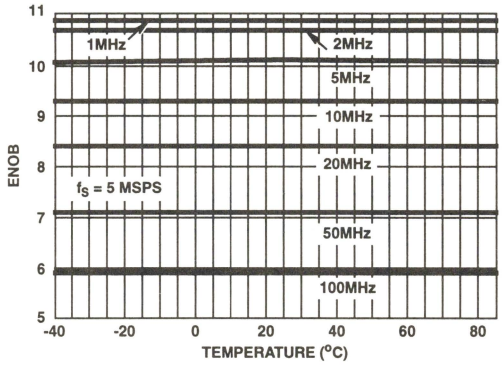


FIGURE 9. EFFECTIVE NUMBER OF BITS (ENOB) vs TEMPERATURE AND INPUT FREQUENCY

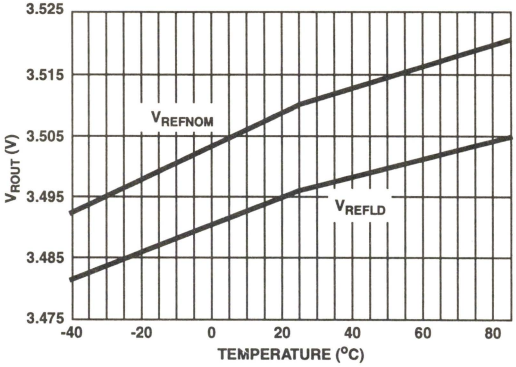


FIGURE 10. INTERNAL VOLTAGE REFERENCE OUTPUT (V_{ROUT}) vs TEMPERATURE AND LOAD

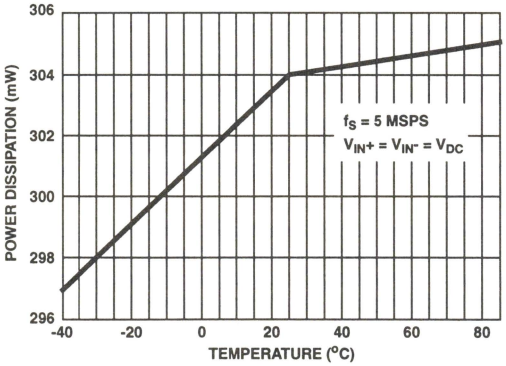


FIGURE 11. POWER DISSIPATION vs TEMPERATURE

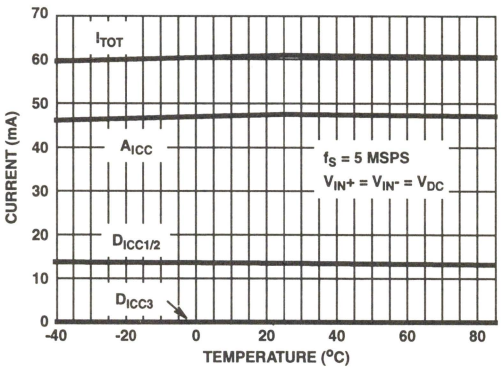


FIGURE 12. POWER SUPPLY CURRENT vs TEMPERATURE

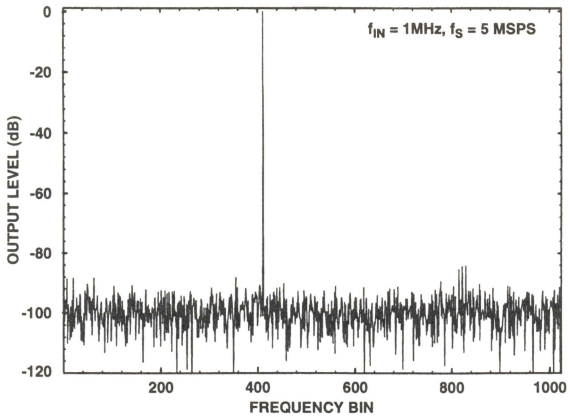


FIGURE 13. 2048 POINT FFT SPECTRAL PLOT

Pin Descriptions

PIN NO.	NAME	DESCRIPTION
1	CLK	Input Clock.
2	DV_{CC1}	Digital Supply (5.0V).
3	D_{GND1}	Digital Ground.
4	DV_{CC1}	Digital Supply (5.0V).
5	D_{GND1}	Digital Ground
6	AV_{CC}	Analog Supply (5.0V).
7	A_{GND}	Analog Ground.
8	$V_{IN}+$	Positive Analog Input.
9	$V_{IN}-$	Negative Analog Input.
10	V_{DC}	DC Bias Voltage Output.
11	V_{ROUT}	Reference Voltage Output.
12	V_{RIN}	Reference Voltage Input.
13	A_{GND}	Analog Ground.
14	AV_{CC}	Analog Supply (5.0V).
15	D11	Data Bit 11 Output (MSB).
16	D10	Data Bit 10 Output.
17	D9	Data Bit 9 Output.
18	D8	Data Bit 8 Output.
19	D7	Data Bit 7 Output.
20	D6	Data Bit 6 Output.
21	D_{GND2}	Digital Output Ground.
22	DV_{CC2}	Digital Output Supply (3.0V to 5.0V).
23	D5	Data Bit 5 Output.
24	D4	Data Bit 4 Output.
25	D3	Data Bit 3 Output.
26	D2	Data Bit 2 Output.
27	D1	Data Bit 1 Output.
28	D0	Data Bit 0 Output (LSB).

Detailed Description

Theory of Operation

The HI5805 is a 12-bit, fully-differential, sampling pipeline A/D converter with digital error correction. Figure 14 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, f_1 and f_2, derived from the master clock. During the sampling phase, f_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of f_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, f_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 100MHz for the converter.

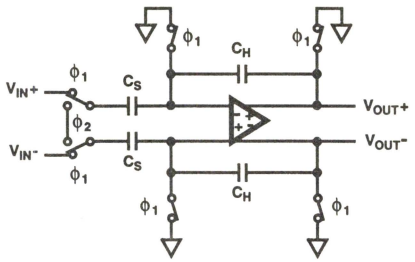


FIGURE 14. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, three identical pipeline subconverter stages, each containing a four-bit flash converter, a four-bit digital-to-analog converter and an amplifier with a voltage gain of 8, follow the S/H circuit with the fourth stage being only a 4-bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual sub-converter clock signal is offset by 180 degrees from the previous stage clock signal, with the result that alternate stages in the pipeline will perform the same operation.

The 4-bit digital output of each stage is fed to a digital delay line controlled by the internal clock. The purpose of the delay line is to align the digital output data to the corresponding sampled analog input signal. This delayed data is fed to the digital error correction circuit which corrects the error in the output data with the information contained in the redundant bits to form the final 12-bit output for the converter.

Because of the pipeline nature of this converter, the data on the bus is output at the 3rd cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The output data is synchronized to the external clock by a latch. The digital outputs are in offset binary format (See Table 1).

Internal Reference Generator, V_{ROUT} and V_{RIN}

The HI5805 has an internal reference generator, therefore, no external reference voltage is required. V_{ROUT} must be connected to V_{RIN} when using the internal reference voltage.

The HI5805 can be used with an external reference. The converter requires only one external reference voltage connected to the V_{RIN} pin with V_{ROUT} left open.

The HI5805 is tested with V_{RIN} equal to 3.5V. Internal to the converter, two reference voltages of 1.3V and 3.3V are generated for a fully differential input signal range of ±2V.

In order to minimize overall converter noise, it is recommended that adequate high frequency decoupling be provided at the reference voltage input pin, V_{RIN}.

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE† (USING INTERNAL REFERENCE)	OFFSET BINARY OUTPUT CODE											
		MSB											LSB
		D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) - $^1/_4$ LSB	+1.99976V	1	1	1	1	1	1	1	1	1	1	1	1
+FS - $1^1/_4$ LSB	1.99878V	1	1	1	1	1	1	1	1	1	1	1	0
+ $^3/_4$ LSB	732.4µV	1	0	0	0	0	0	0	0	0	0	0	0
- $^1/_4$ LSB	-244.1µV	0	1	1	1	1	1	1	1	1	1	1	1
-FS + $1^3/_4$ LSB	-1.99829V	0	0	0	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + $^3/_4$ LSB	-1.99927V	0	0	0	0	0	0	0	0	0	0	0	0

† The voltages listed above represent the ideal center of each offset binary output code shown.

Analog Input, Differential Connection

The analog input to the HI5805 can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 15) will give the best performance for the converter.

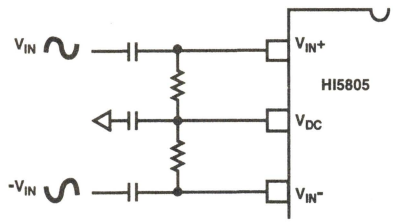


FIGURE 15. AC COUPLED DIFFERENTIAL INPUT

Since the HI5805 is powered off a single +5V supply, the analog input must be biased so it lies within the analog input common mode voltage range of 1.0V to 4.0V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A 2.3V DC bias voltage source, V_{DC}, half way between the top and bottom internal reference voltages, is made available to the user to help simplify circuit design when using a differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the analog input common mode voltage range over temperature.

The difference between the converter's two internal voltage references is 2V. For the AC coupled differential input, (Figure 15), if V_{IN} is a $2V_{P-P}$ sinewave with -V_{IN} being 180 degrees out of phase with V_{IN}, then V_{IN}+ is a $2V_{P-P}$ sinewave riding on a DC bias voltage equal to V_{DC} and V_{IN}- is a $2V_{P-P}$ sinewave riding on a DC bias voltage equal to V_{DC}. Consequently, the converter will be at positive full scale, all 1s digital data output code, when the V_{IN}+ input is at V_{DC} +1V and the V_{IN}- input is at V_{DC} -1V (V_{IN}+-V_{IN}- = 2V). Conversely, the ADC will be at negative full scale, all 0s digital data output code, when the V_{IN}+ input is equal to V_{DC}- 1V and V_{IN}- is at V_{DC}+1V (V_{IN}+-V_{IN}- = -2V). From this, the converter is seen to have a peak-to-peak differential analog input voltage range of ±2V.

The analog input can be DC coupled (Figure 16) as long as the inputs are within the analog input common mode voltage range (1.0V ≤ VDC ≤ 4.0V).

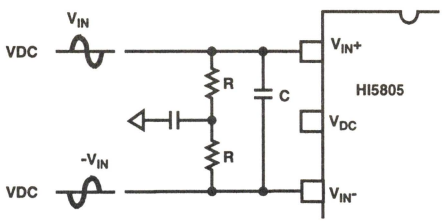


FIGURE 16. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 16 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from V_{IN}+ to V_{IN}- will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

Analog Input, Single-Ended Connection

The configuration shown in Figure 17 may be used with a single ended AC coupled input. Sufficient headroom must be provided such that the input voltage never goes above +5V or below A_{GND}.

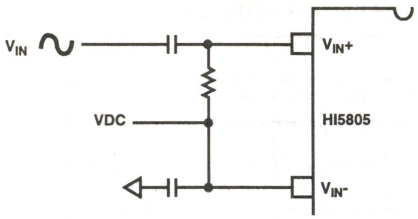


FIGURE 17. AC COUPLED SINGLE ENDED INPUT

Again, the difference between the two internal voltage references is 2V. If V_{IN} is a $4V_{P-P}$ sinewave, then V_{IN}+ is a $4V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive full scale when V_{IN}+ is at VDC + 2V (V_{IN}+ - V_{IN}- = 2V) and will be at negative full scale when V_{IN}+ is equal to VDC - 2V (V_{IN}+ - V_{IN}- = -2V). In this case, V_{DC} could range between 2V and 3V without a significant change in ADC performance. The simplest way to produce VDC is to use the V_{DC} bias voltage output of the HI5805.

The single ended analog input can be DC coupled (Figure 18) as long as the input is within the analog input common mode voltage range.

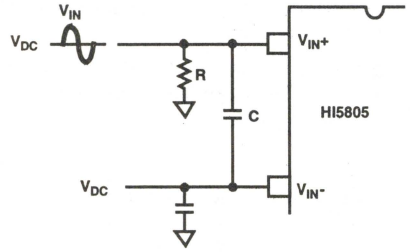


FIGURE 18. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 18 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from V_{IN}+ to V_{IN}- will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

A single ended source will give better overall system performance if it is first converted to differential before driving the HI5805.

Digital I/O and Clock Requirements

The HI5805 provides a standard high-speed interface to external TTL/CMOS logic families. The digital CMOS clock input has TTL level thresholds. The low input bias current allows the HI5805 to be driven by CMOS logic.

The digital CMOS outputs have a separate digital supply. This allows the digital outputs to operate from a 3.0V to 5.0V supply. When driving CMOS logic, the digital outputs will swing to the rails. When driving standard TTL loads, the digital outputs will meet standard TTL level requirements even with a 3.0V supply.

In order to ensure rated performance of the HI5805, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5805 will only be guaranteed at conversion rates above 0.5 MSPS. This ensures proper performance of the internal dynamic circuits.

Supply and Ground Considerations

The HI5805 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5805 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the Application Note AN9214, "Using Harris High Speed A/D Converters" for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$ LSB above half scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is $^3/_4$ LSB below positive full scale with the offset error removed. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection Ratio (PSRR)

Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5805. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and

analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests. SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency, $f_S/2$, excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by:

$$ENOB = (SINAD + V_{CORR} - 1.76)/6.02,$$

where: $V_{CORR} = 0.5dB$.

V_{CORR} adjusts the ENOB for the amount the input is below fullscale.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component in the spectrum below $f_S/2$.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present at the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are $(f_1 + f_2)$, $(f_1 - f_2)$, $(2f_1)$, $(2f_2)$, $(2f_1 + f_2)$, $(2f_1 - f_2)$, $(f_1 + 2f_2)$, $(f_1 - 2f_2)$. The ADC is tested with each tone 6dB below full scale.

Transient Response

Transient response is measured by providing a full-scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 12-bit accuracy.

Over-Voltage Recovery

Over-voltage Recovery is measured by providing a full-scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 12-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the analog input frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sinewave. The input sinewave has an amplitude which swings from $-f_S$ to $+f_S$. The bandwidth given is measured at the specified sampling frequency.

Timing Definitions

Refer to Figure 1, Internal Circuit Timing, and Figure 2, Input-To-Output Timing, for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture Jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the digital data is output on the bus at the third cycle of the clock. This is due to the pipe-line nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input sample by 3 clock cycles.

HARRIS SEMICONDUCTOR

HI5808

August 1997

12-Bit, 10 MSPS A/D Converter

Features

- Sampling Rate ..... 10 MSPS
- Low Power
- Internal Sample and Hold
- Fully Differential Architecture
- Full Power Input Bandwidth 100MHz
- Low Distortion
- Internal Voltage Reference
- TTL/CMOS Compatible Digital I/O
- Digital Outputs ..... 5V to 3.0V

Applications

- Digital Communication Systems
- Undersampling Digital IF
- Document Scanners
- Additional Reference Documents
  - AN9214 Using Harris High Speed A/D Converters
  - AN9724 Using the HI5808EVAL1 Evaluation Board

Description

The HI5808 is a monolithic, 12-bit, Analog-to-Digital Converter fabricated in Harris' HBC10 BiCMOS process. It is designed for high speed, high resolution applications where wide bandwidth and low power consumption are essential.

The HI5808 is designed in a fully differential pipelined architecture with a front end differential-in-differential-out sample-and-hold (S/H). The HI5808 has excellent dynamic performance while consuming 325mW power at 10 MSPS.

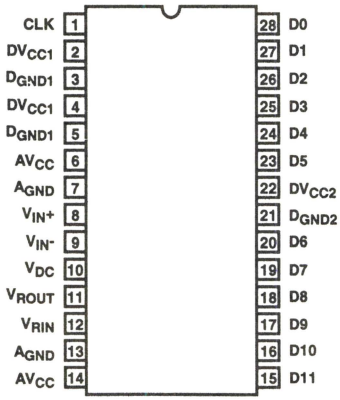
The 100MHz full power input bandwidth is ideal for communication systems and document scanner applications. Data output latches are provided which present valid data to the output bus with a latency of 3 clock cycles. The digital outputs have a separate supply pin which can be powered from a 3V to 5V supply.

Ordering Information

PART NUMBER	SAMPLE RATE	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5808BIB	10 MSPS	-40 to 85	28 Ld SOIC	M28.3
HI5808EVAL1		25	Evaluation Board	

Pinout

HI5808
(SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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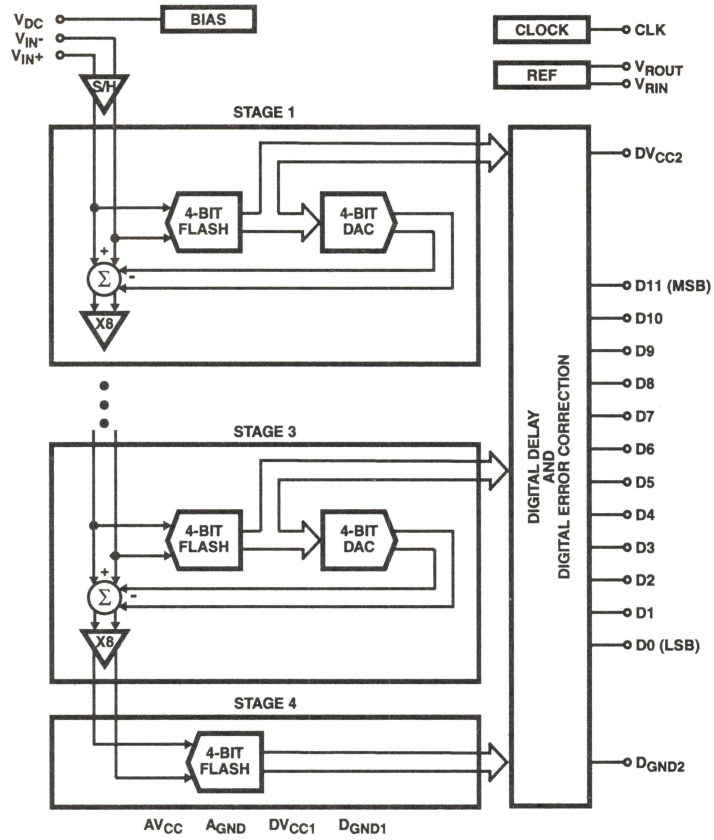
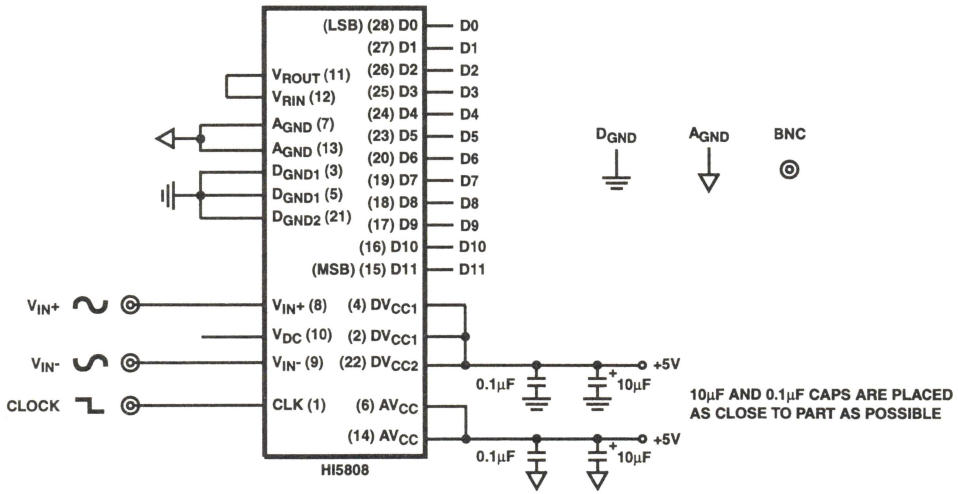
File Number 4233.2

Functional Block Diagram



Typical Applications Schematic



Absolute Maximum Ratings

Supply Voltage, AV_{CC} or DV_{CC} to A_{GND} or D_{GND} . . . . . +6.0V
D_{GND} to A_{GND} 0.3V
Digital I/O Pins . . . . . D_{GND} to DV_{CC}
Analog I/O Pins. . . . . A_{GND} to AV_{CC}

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
SOIC Package 70
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Lead Temperature (Soldering, 10s). . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = DV_{CC2} = +5V$, $f_S = 10$ MSPS at 50% Duty Cycle, $V_{RIN} = 3.5V$, $C_L = 10pF$, $T_A = -40°C$ to $85°C$, Differential Analog Input, Typical Values are Test Results at 25°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	HI5808BIB -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
ACCURACY					
Resolution		12	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±1	±2	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1	LSB
Offset Error, V_{OS}	f_{IN} = DC	-	19	-	LSB
Full Scale Error, FSE	f_{IN} = DC	-	32	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	-	MSPS
Maximum Conversion Rate	No Missing Codes	10	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	10.0	10.8	-	Bits
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	66.5	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	-	67.3	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-	-75	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-80		dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-77	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz	-	77	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	-65	-	dBc
Transient Response		-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive	-	2	-	Cycle
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range ($V_{IN}+ - V_{IN}-$)		-	±2.0	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	4.0	-	V
Analog Input Resistance, R_{IN}	(Notes 2, 3)	1	-	-	MΩ
Analog Input Capacitance, C_{IN}		-	10	-	pF
Analog Input Bias Current, $I_{B}+$ or $I_{B}-$	(Note 3)	-10	-	+10	µA
Differential Analog Input Bias Current $I_{B\ DIFF} = (I_{B}+ - I_{B}-)$		-	±0.5	-	µA
Full Power Input Bandwidth, FPBW		-	100	-	MHz

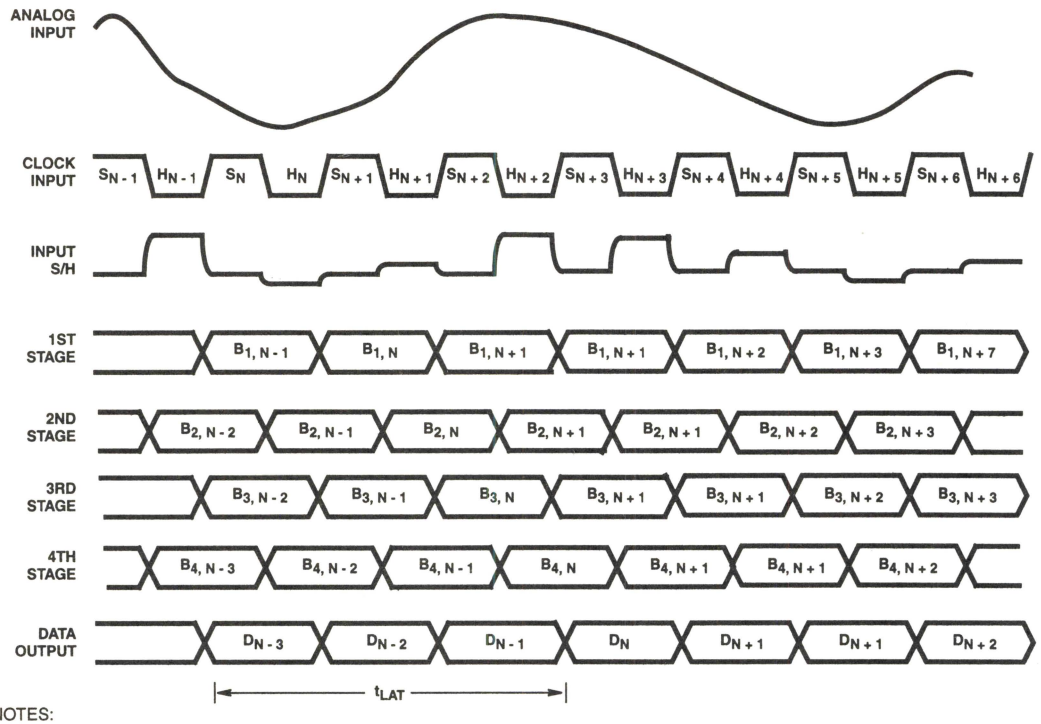
Electrical Specifications $AV_{CC} = DV_{CC1} = DV_{CC2} = +5V$, $f_S = 10$ MSPS at 50% Duty Cycle, $V_{RIN} = 3.5V$, $C_L = 10pF$, $T_A = -40^oC$ to 85^oC, Differential Analog Input, Typical Values are Test Results at 25^oC, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	HI5808BIB -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
Analog Input Common Mode Voltage Range $(V_{IN}+ + V_{IN}-)/2$	Differential Mode (Note 2)	1	2.3	4	V
INTERNAL VOLTAGE REFERENCE					
Reference Output Voltage, V_{ROUT} (Loaded)		-	3.5	-	V
Reference Output Current		-	-	1	mA
Reference Temperature Coefficient		-	50	-	ppm/°C
REFERENCE VOLTAGE INPUT					
Reference Voltage Input, V_{RIN}		-	3.5	-	V
Total Reference Resistance, R_L		-	7.8	-	kΩ
Reference Current		-	450	-	µA
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	2.3	-	V
Max Output Current (Not To Exceed)		-	-	1	mA
DIGITAL INPUTS (CLK)					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	$V_{CLK} = 5V$	-	-	10.0	µA
Input Logic Low Current, I_{IL}	$V_{CLK} = 0V$	-	-	10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS (D0-D11)					
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$ (Note 2)	1.6	-	-	mA
	$DV_{CC3} = 3.0V$, $V_O = 0.4V$	-	1.6	-	mA
Output Logic Source Current, I_{OH}	$V_O = 2.4V$ (Note 2)	-0.2	-	-	mA
	$DV_{CC3} = 3.0V$, $V_O = 2.4V$	-	-0.2	-	mA
Output Capacitance, C_{OUT}		-	5	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps (RMS)
Data Output Delay, t_{OD}		-	8	-	ns
Data Output Hold, t_H		-	8	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	3	Cycles
Clock Pulse Width (Low)	10MHz Clock	45	50	55	ns
Clock Pulse Width (High)	10MHz Clock	45	50	55	ns
POWER SUPPLY CHARACTERISTICS					
Total Supply Current, I_{CC}	$V_{IN}+ - V_{IN}- = 2V$	-	65	73	mA
Analog Supply Current, AI_{CC}	$V_{IN}+ - V_{IN}- = 2V$	-	46	-	mA
Digital Supply Current, DI_{CC1}	$V_{IN}+ - V_{IN}- = 2V$	-	17	-	mA
Output Supply Current, DI_{CC2}	$V_{IN}+ - V_{IN}- = 2V$	-	2	-	mA
Power Dissipation	$V_{IN}+ - V_{IN}- = 2V$	-	325	365	mW
Offset Error PSRR, ΔV_{OS}	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	2	-	LSB
Gain Error PSRR, ΔFSE	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	30	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock off (clock low, hold mode).

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M, N}$: M-th stage digital output corresponding to N-th sampled input.
7. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. INTERNAL CIRCUIT TIMING

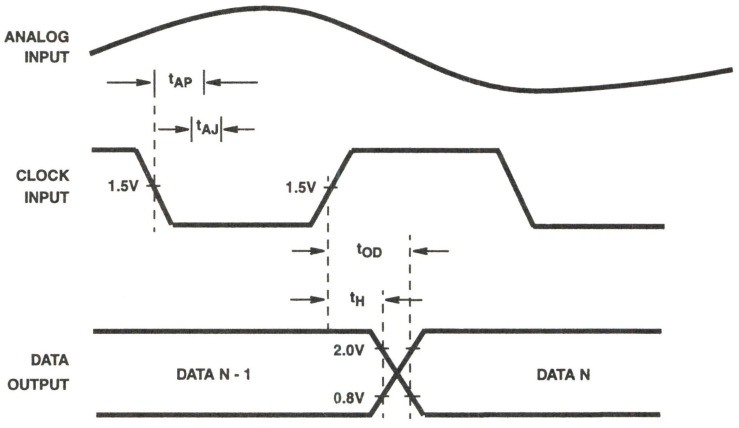


FIGURE 2. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

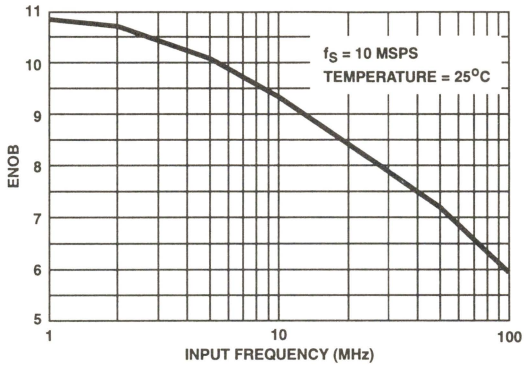


FIGURE 3. EFFECTIVE NUMBER OF BITS (ENOB) vs INPUT FREQUENCY

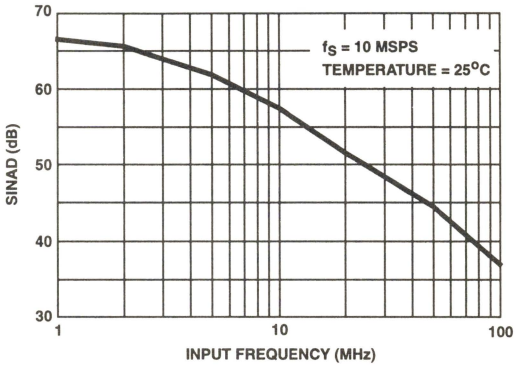


FIGURE 4. SIGNAL TO NOISE AND DISTORTION (SINAD) vs INPUT FREQUENCY

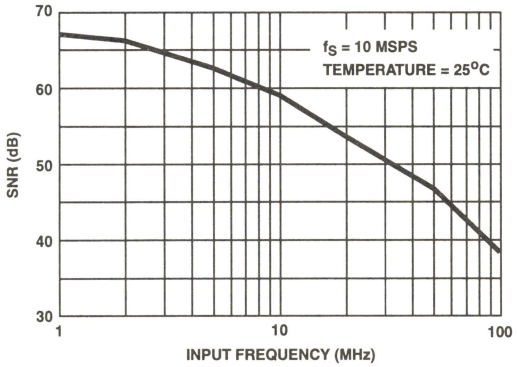


FIGURE 5. SIGNAL TO NOISE RATIO (SNR) vs INPUT FREQUENCY

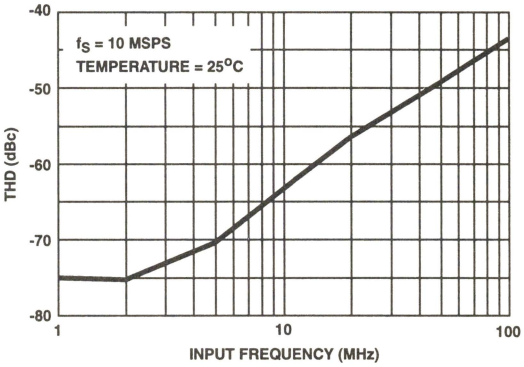


FIGURE 6. TOTAL HARMONIC DISTORTION (THD) vs INPUT FREQUENCY

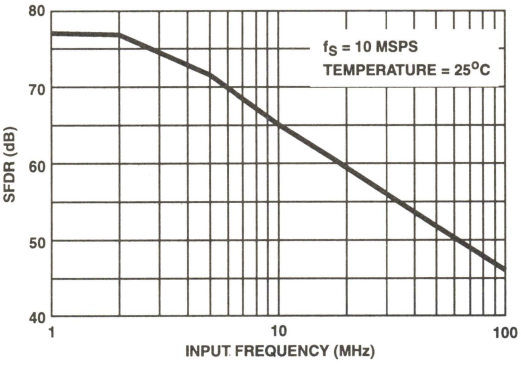


FIGURE 7. SPURIOUS FREE DYNAMIC RANGE (SFDR) vs INPUT FREQUENCY

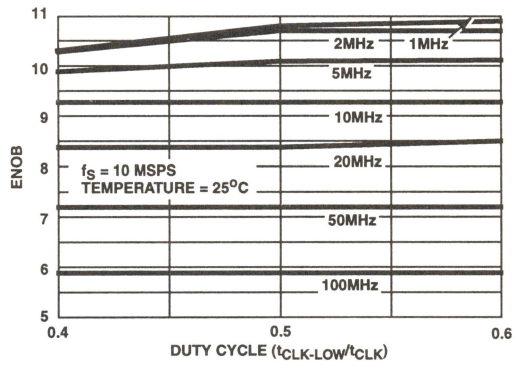


FIGURE 8. EFFECTIVE NUMBER OF BITS (ENOB) vs CLOCK DUTY CYCLE AND INPUT FREQUENCY

Typical Performance Curves (Continued)

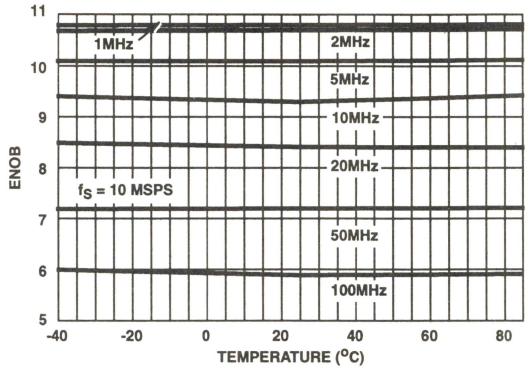


FIGURE 9. EFFECTIVE NUMBER OF BITS (ENOB) vs TEMPERATURE AND INPUT FREQUENCY

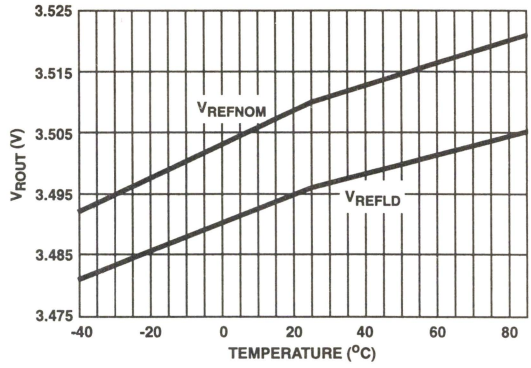


FIGURE 10. INTERNAL VOLTAGE REFERENCE OUTPUT (V_{ROUT}) vs TEMPERATURE AND LOAD

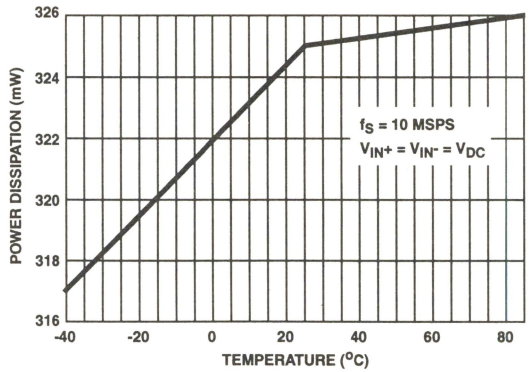


FIGURE 11. POWER DISSIPATION vs TEMPERATURE

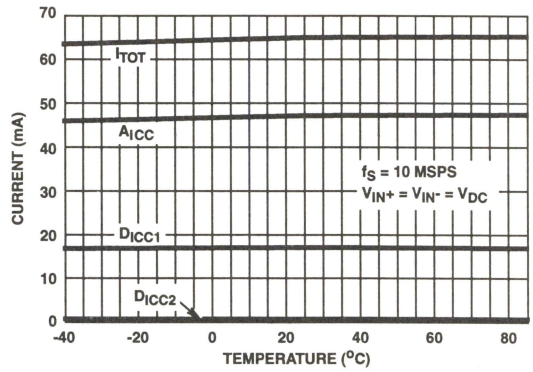


FIGURE 12. POWER SUPPLY CURRENT vs TEMPERATURE

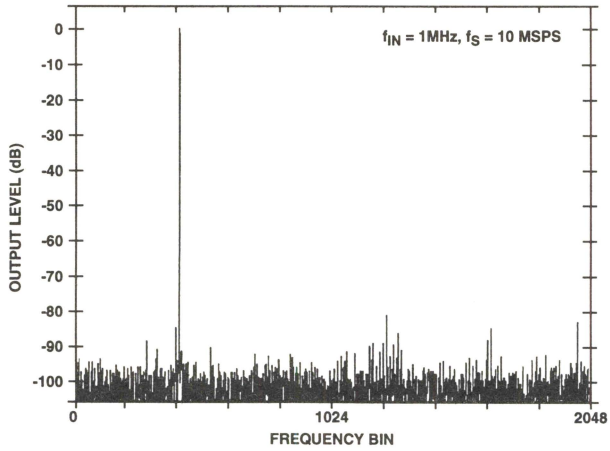


FIGURE 13. 4096 POINT FFT SPECTRAL PLOT

Pin Descriptions

PIN NO.	NAME	DESCRIPTION
1	CLK	Sample Clock Input.
2	DV_{CC1}	Digital Supply (5.0V).
3	D_{GND1}	Digital Ground.
4	DV_{CC1}	Digital Supply (5.0V).
5	D_{GND1}	Digital Ground.
6	AV_{CC}	Analog Supply (5.0V).
7	A_{GND}	Analog Ground.
8	V_{IN+}	Positive Analog Input.
9	V_{IN-}	Negative Analog Input.
10	V_{DC}	DC Bias Voltage Output.
11	V_{ROUT}	Reference Voltage Output.
12	V_{RIN}	Reference Voltage Input.
13	A_{GND}	Analog Ground.
14	AV_{CC}	Analog Supply (5.0V).
15	D11	Data Bit 11 Output (MSB).
16	D10	Data Bit 10 Output.
17	D9	Data Bit 9 Output.
18	D8	Data Bit 8 Output.
19	D7	Data Bit 7 Output.
20	D6	Data Bit 6 Output.
21	D_{GND2}	Digital Output Ground.
22	DV_{CC2}	Digital Output Supply (3.0V to 5.0V).
23	D5	Data Bit 5 Output.
24	D4	Data Bit 4 Output.
25	D3	Data Bit 3 Output.
26	D2	Data Bit 2 Output.
27	D1	Data Bit 1 Output.
28	D0	Data Bit 0 Output (LSB).

Detailed Description

Theory of Operation

The HI5808 is a 12-bit fully differential sampling pipeline A/D converter with digital error correction. Figure 14 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 100MHz for the converter.

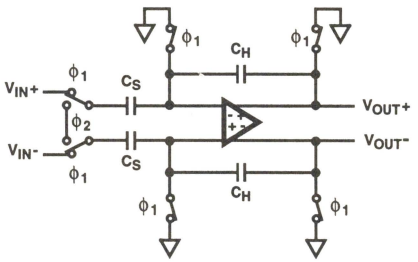


FIGURE 14. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, three identical pipeline subconverter stages, each containing a four-bit flash converter, a four-bit digital-to-analog converter and an amplifier with a voltage gain of 8, follow the S/H circuit with the fourth stage being only a 4-bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual sub-converter clock signal is offset by 180 degrees from the previous stage clock signal, with the result that alternate stages in the pipeline will perform the same operation.

The digital output of each of the three identical 4-bit subconverter stages is a four-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the three identical four-bit subconverter stages with the corresponding output of the fourth stage flash converter before applying the sixteen bit result to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final twelve bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus on the 3rd cycle of the clock after the analog sample is taken. This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output on the following clock pulse. The digital output data is synchronized to the external sampling clock with an output latch. The output of the digital error correction circuit is available in offset binary format (see Table 1, A/D Code Table).

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE † (USING INTERNAL REFERENCE)	OFFSET BINARY OUTPUT CODE											
		MSB											LSB
		D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) - 1/4 LSB	+1.99976V	1	1	1	1	1	1	1	1	1	1	1	1
+FS - 1 1/4 LSB	1.99878V	1	1	1	1	1	1	1	1	1	1	1	0
+ 3/4 LSB	732.4µV	1	0	0	0	0	0	0	0	0	0	0	0
- 1/4 LSB	-244.1µV	0	1	1	1	1	1	1	1	1	1	1	1
-FS + 1 3/4 LSB	-1.99829V	0	0	0	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + 3/4 LSB	-1.99927V	0	0	0	0	0	0	0	0	0	0	0	0

† The voltages listed above represent the ideal center of each offset binary output code shown.

Internal Reference Generator, V_{ROUT} and V_{RIN}

The HI5808 has an internal reference generator, therefore, no external reference voltage is required. V_{ROUT} must be connected to V_{RIN} when using the internal reference voltage.

The HI5808 can be used with an external reference. The converter requires only one external reference voltage connected to the V_{RIN} pin with V_{ROUT} left open.

The HI5808 is tested with V_{RIN} equal to 3.5V. Internal to the converter, two reference voltages of 1.3V and 3.3V are generated for a fully differential input signal range of ±2V.

In order to minimize overall converter noise, it is recommended that adequate high frequency decoupling be provided at the reference voltage input pin, V_{RIN}.

Analog Input, Differential Connection

The analog input to the HI5808 can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 15) will give the best performance for the converter.

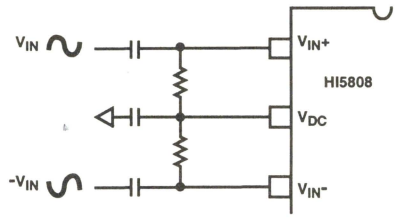


FIGURE 15. AC COUPLED DIFFERENTIAL INPUT

Since the HI5808 is powered off a single +5V supply, the analog input must be biased so it lies within the analog input common mode voltage range of 1.0V to 4.0V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A 2.3V DC bias voltage source, V_{DC}, half way between the top and bottom internal reference voltages, is made available to the user to help simplify circuit design when using a differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the analog input common mode voltage range over temperature.

The difference between the converter's two internal voltage references is 2V. For the AC coupled differential input, (Figure 15), if V_{IN} is a $2V_{P-P}$ sinewave with $-V_{IN}$ being 180 degrees out of phase with V_{IN}, then $V_{IN}+$ is a $2V_{P-P}$ sinewave riding on a DC bias voltage equal to V_{DC} and $V_{IN}-$ is a $2V_{P-P}$ sinewave riding on a DC bias voltage equal to V_{DC}. Consequently, the converter will be at positive full scale, all 1s digital data output code, when the $V_{IN}+$ input is at V_{DC} +1V and the $V_{IN}-$ input is at V_{DC} -1V ($V_{IN}+ - V_{IN}- = 2V$). Conversely, the ADC will be at negative full scale, all 0s digital data output code, when the $V_{IN}+$ input is equal to V_{DC} -1V and $V_{IN}-$ is at V_{DC}+1V ($V_{IN}+ - V_{IN}- = -2V$). From this, the converter is seen to have a peak-to-peak differential analog input voltage range of ±2V.

The analog input can be DC coupled (Figure 16) as long as the inputs are within the analog input common mode voltage range ($1.0V \leq VDC \leq 4.0V$).

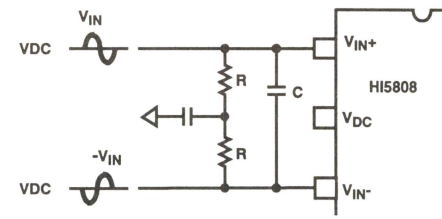


FIGURE 16. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 16 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high

frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

Analog Input, Single-Ended Connection

The configuration shown in Figure 17 may be used with a single ended AC coupled input. Sufficient headroom must be provided such that the input voltage never goes above +5V or below A_{GND}.

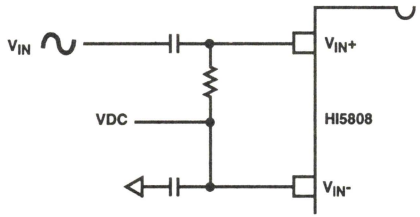


FIGURE 17. AC COUPLED SINGLE ENDED INPUT

Again, the difference between the two internal voltage references is 2V. If V_{IN} is a $4V_{P-P}$ sinewave, then $V_{IN}+$ is a $4V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive full scale when $V_{IN}+$ is at VDC + 2V ($V_{IN}+ - V_{IN}- = 2V$) and will be at negative full scale when $V_{IN}+$ is equal to VDC - 2V ($V_{IN}+ - V_{IN}- = -2V$). In this case, VDC could range between 2V and 3V without a significant change in ADC performance. The simplest way to produce VDC is to use the V_{DC} bias voltage output of the HI5808.

The single ended analog input can be DC coupled (Figure 18) as long as the input is within the analog input common mode voltage range.

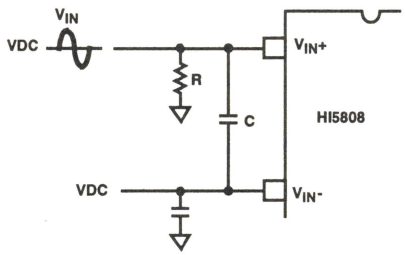


FIGURE 18. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 18 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

A single ended source will give better overall system performance if it is first converted to differential before driving the HI5808.

Digital I/O and Clock Requirements

The HI5808 provides a standard high-speed interface to external TTL/CMOS logic families. The digital CMOS clock input has TTL level thresholds. The low input bias current allows the HI5808 to be driven by CMOS logic.

The digital CMOS outputs have a separate digital supply. This allows the digital outputs to operate from a 3.0V to 5.0V supply. When driving CMOS logic, the digital outputs will swing to the rails. When driving standard TTL loads, the digital outputs will meet standard TTL level requirements even with a 3.0V supply.

In order to ensure rated performance of the HI5808, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5808 will only be guaranteed at conversion rates above 0.5 MSPS. This ensures proper performance of the internal dynamic circuits.

Supply and Ground Considerations

The HI5808 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5808 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the Application Note AN9214, "Using Harris High Speed A/D Converters" for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$ LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is $^3/_4$ LSB below positive full scale with the offset error removed. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection Ratio (PSRR)

Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5808. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests. SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency, $f_S/2$, excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by:

$$ENOB = (SINAD + V_{CORR} - 1.76)/6.02,$$

where: $V_{CORR} = 0.5dB$.

V_{CORR} adjusts the ENOB for the amount the input is below full scale.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component in the spectrum below $f_S/2$.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present at the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are $(f_1 + f_2)$, $(f_1 - f_2)$, $(2f_1)$, $(2f_2)$, $(2f_1 + f_2)$, $(2f_1 - f_2)$, $(f_1 + 2f_2)$, $(f_1 - 2f_2)$. The ADC is tested with each tone 6dB below full scale.

Transient Response

Transient response is measured by providing a full-scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 12-bit accuracy.

Over-Voltage Recovery

Over-voltage Recovery is measured by providing a full-scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 12-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the analog input frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sinewave. The input sinewave has an amplitude which swings from $-f_S$ to $+f_S$. The bandwidth given is measured at the specified sampling frequency.

Timing Definitions

Refer to Figure 1, Internal Circuit Timing, and Figure 2, Input-To-Output Timing, for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture Jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the digital data is output on the bus at the third cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input sample by 3 clock cycles.

HARRIS SEMICONDUCTOR

HI5905

PRELIMINARY

August 1997

14-Bit, 5 MSPS A/D Converter

Features

- Sampling Rate ..... 5 MSPS
- Low Power at 5 MSPS 350mW
- Internal Sample and Hold
- Fully Differential Architecture
- Full Power Input Bandwidth 100MHz
- Typical SINAD at 1MHz ..... >70dB
- Low Latency
- Internal Voltage Reference
- TTL Compatible Clock Input
- CMOS Compatible Digital Data Outputs

Applications

- Asymmetric Digital Subscriber Line (ADSL)
- Digital Communication Systems
- Undersampling Digital IF
- Document Scanners
- Reference Literature
  - AN9214 Using Harris High Speed A/D Converters

Description

The HI5905 is a monolithic, 14-bit, Analog-to-Digital Converter fabricated in Harris' HBC10 BiCMOS process. It is designed for high speed, high resolution applications where wide bandwidth, low power consumption and excellent SINAD performance are essential. With a 100MHz full power input bandwidth the converter is ideal for many types of communication systems and document scanner applications.

The HI5905 is designed in a fully differential pipelined architecture with a front end differential-in-differential-out sample-and-hold (S/H). The HI5905 has excellent dynamic performance while consuming 350mW power at 5 MSPS.

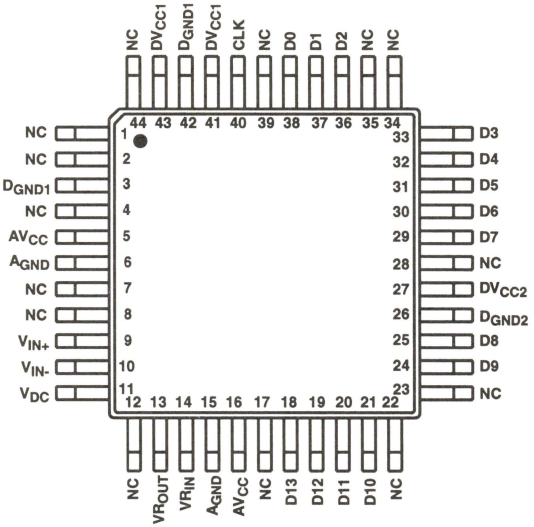
Data output latches are provided which present valid data to the output bus with a latency of 4 clock cycles.

Ordering Information

PART NUMBER	SAMPLE RATE	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5905IN	5 MSPS	-40 to 85	44 Ld MQFP	Q44.10x10

Pinout

HI5905 (MQFP)
TOP VIEW



4 A/D CONVERTERS HIGH SPEED

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

File Number 4259

DATA ACQUISITION 5

A/D CONVERTERS - INTEGRATING

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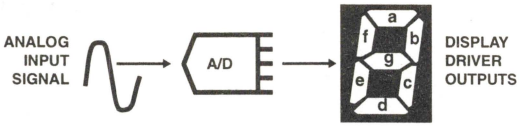
ICL7135	$4\frac{1}{2}$ Digit, BCD Output, A/D Converter	5-5
ICL8052/ICL7104, ICL8068/ICL7104	14-Bit/16-Bit, Microprocessor-Compatible, 2-Chip, A/D Converter	5-6

Selection Guide

ANALOG TO DIGITAL CONVERTERS WITH DISPLAY OUTPUTS (2 Chip Sets)

PART NUMBER	OUTPUT TYPE	RESOLUTION	CONVERSION TIME (SAMPLE RATE)	PACKAGE TYPES	FEATURES
ICL7135	MUXED BCD	$4^1/_2$ Digits	250ms (4SPS)	28 Lead Plastic DIP	2 Chip Set 100μV Resolution, Differential Inputs

NOTE: Sorted by ascending resolution (Digits) and conversion time.



HARRIS SEMICONDUCTOR

HI-7159A

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

Microprocessor-Compatible, $5^1/_2$ Digit A/D Converter

Features

- ±200,000 Count A/D Converter
- 2V Full Scale Reading With 10μV Resolution
- 15 Conversions Per Second in $5^1/_2$ Digit Mode
- 60 Conversions Per Second in $4^1/_2$ Digit Mode
- Serial or Parallel Interface Modes
- Four Selectable Baud Rates
- Differential Analog Input
- Differential Reference Input
- Digital Autozero

Applications

- Weigh Scales
- Part Counting Scales
- Laboratory Instruments
- Process Control/Monitoring
- Energy Management
- Seismic Monitoring

NOT RECOMMENDED FOR NEW DESIGNS

Description

The Harris HI-7159A is a monolithic A/D converter that uses a unique dual slope technique which allows it to resolve input changes as small as 1 part in 200,000 (10μV) without the use of critical external components. Its digital autozeroing feature virtually eliminates zero drift over temperature. The device is fabricated in Harris' proprietary low noise BiMOS process, resulting in exceptional linearity and noise performance. The HI-7159A's resolution can be switched between a high resolution 200,000 count ($5^1/_2$ digit) mode, and a high speed 20,000 count ($4^1/_2$ digit) mode without any hardware modifications. In the $4^1/_2$ digit uncompensated mode, speeds of 60 conversions per second can be achieved. The HI-7159A is designed to be easily interfaced with most microprocessors through either of its three serial and one parallel interface modes. In the serial modes, any one of four common baud rates is available.

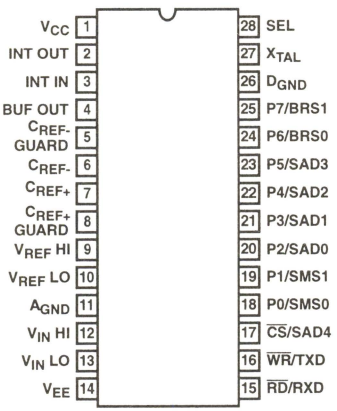
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3-7159A-5	0 to 75	28 Ld PDIP	E28.6

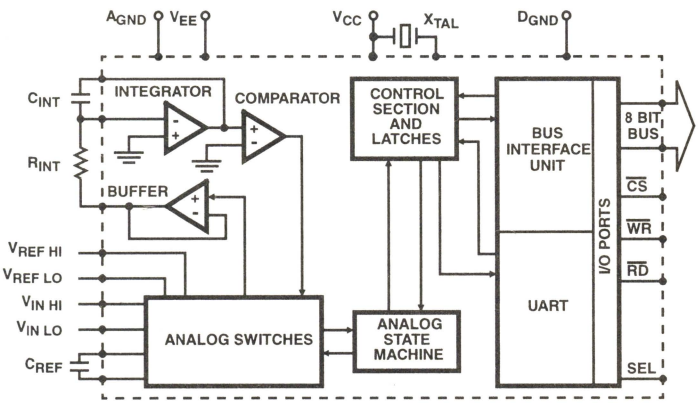
5 A/D CONVERTERS INTEGRATING

Pinout

HI-7159A
(PDIP)
TOP VIEW



Functional Block Diagram



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File Number **2936.2**

HARRIS SEMICONDUCTOR

ICL7109

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

12-Bit, Microprocessor-Compatible A/D Converter

Features

- **12-Bit Binary (Plus Polarity and Over-Range) Dual Slope Integrating Analog-to-Digital Converter**
- **Byte-Organized, TTL Compatible Three-State Outputs and UART Handshake Mode for Simple Parallel or Serial Interfacing to Microprocessor Systems**
- **RUN/$\overline{\text{HOLD}}$ Input and STATUS Output Can Be Used to Monitor and Control Conversion Timing**
- **True Differential Input and Differential Reference**
- **Low Noise (Typ) ..... $15\mu V_{P-P}$**
- **Input Current (Typ) 1pA**
- **Operates At Up to 30 Conversions/s**
- **On-Chip Oscillator Operates with Inexpensive 3.58MHz TV Crystal Giving 7.5 Conversions/s for 60Hz Rejection. May Also Be Used with An RC Network Oscillator for Other Clock Frequencies**

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICL7109MDL	-55 to 125	40 Ld SBDIP	D40.6
ICL7109IDL	-25 to 85	40 Ld SBDIP	D40.6
ICL7109IJL	-25 to 85	40 Ld CERDIP	F40.6
ICL7109CPL	0 to 70	40 Ld PDIP	E40.6
ICL7109MDL/883B	-55 to 125	40 Ld SBDIP	D40.6
ICL7109IPL	-25 to 85	40 Ld PDIP	E40.6

Description

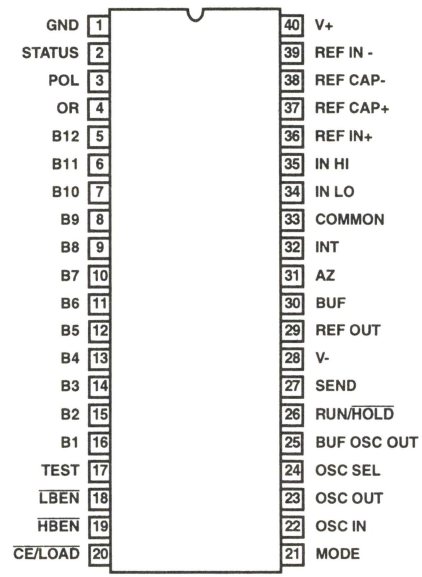
The ICL7109 is a high performance, CMOS, low power integrating A/D converter designed to easily interface with microprocessors.

The output data (12 bits, polarity and over-range) may be directly accessed under control of two byte enable inputs and a chip select input for a single parallel bus interface. A UART handshake mode is provided to allow the ICL7109 to work with industry-standard UARTs in providing serial data transmission. The RUN/$\overline{\text{HOLD}}$ input and STATUS output allow monitoring and control of conversion timing.

The ICL7109 provides the user with the high accuracy, low noise, low drift versatility and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, drift of less than $1\mu V/^{o}C$, maximum input bias current of 10pA, and typical power consumption of 20mW make the ICL7109 an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

Pinout

ICL7109
(CERDIP, PDIP, SBDIP)
TOP VIEW



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File Number **3092.1**

HARRIS SEMICONDUCTOR

ICL7135

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

$4\frac{1}{2}$ Digit, BCD Output, A/D Converter

Features

- Accuracy Guaranteed to ±1 Count Over Entire ±20000 Counts (2.0000V Full Scale)
- Guaranteed Zero Reading for 0V Input
- 1pA Typical Input Leakage Current
- True Differential Input
- True Polarity at Zero Count for Precise Null Detection
- Single Reference Voltage Required
- Overrange and Underrange Signals Available for Auto-Range Capability
- All Outputs TTL Compatible
- Blinking Outputs Gives Visual Indication of Overrange
- Six Auxiliary Inputs/Outputs are Available for Interfacing to UARTs, Microprocessors, or Other Circuitry
- Multiplexed BCD Outputs

Description

The Harris ICL7135 precision A/D converter, with its multiplexed BCD output and digit drivers, combines dual-slope conversion reliability with ±1 in 20,000 count accuracy and is ideally suited for the visual display DVM/DPM market. The 2.0000V full scale capability, auto-zero, and auto-polarity are combined with true ratiometric operation, almost ideal differential linearity and true differential input. All necessary active devices are contained on a single CMOS IC, with the exception of display drivers, reference, and a clock.

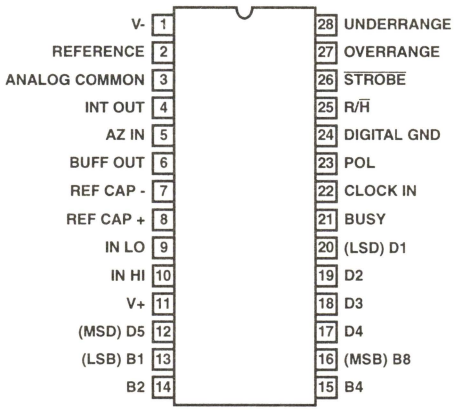
The ICL7135 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10µV, zero drift of less than 1µV/°C, input bias current of 10pA (Max), and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins which allow it to operate in more sophisticated systems. These include $\overline{\text{STROBE}}$, OVERRANGE, UNDERRANGE, RUN/$\overline{\text{HOLD}}$ and BUSY lines, making it possible to interface the circuit to a microprocessor or UART.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL7135CPI	0 to 70	28 Ld PDIP	E28.6

Pinout

ICL7135
(PDIP)
TOP VIEW



5 A/D CONVERTERS INTEGRATING

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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HARRIS SEMICONDUCTOR

ICL8052/ICL7104, ICL8068/ICL7104

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

14-Bit/16-Bit, Microprocessor-Compatible, 2-Chip, A/D Converter

Features

- 16-Bit/14-Bit Binary Three-State Latched Outputs Plus Polarity and Overrange
- Ideally Suited for Interface to UARTs and Microprocessors
- Conversion on Demand or Continuously
- Guaranteed Zero Reading for 0V Input
- True Polarity at Zero Count for Precise Null Detection
- Single Reference Voltage for True Ratiometric Operation
- Onboard Clock and Reference
- Auto-Zero, Auto-Polarity
- Accuracy Guaranteed to 1 Count
- All Outputs TTL Compatible
- ±4V Analog Input Range
- Status Signal Available for External Sync, A/Z in Preamp, Etc.

Description

The ICL7104, combined with the ICL8052 or ICL8068, forms a member of Harris' high performance A/D converter family. The ICL7104-16, performs the analog switching and digital function for a 16-bit binary A/D converter, with full three-state output, UART handshake capability, and other outputs for easy interfacing. The ICL7014-14 is a 14-bit version. The analog section, as with all Harris' integrating converters, provides fully precise Auto-Zero, Auto-Polarity (including ±0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully rationmetric operation, over-range indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external Auto-Zero capability in preconditioning circuitry, synchronizing external multiplexers, etc.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL8052CPD	0 to 70	14 Ld PDIP	E14.3
ICL8052CDD	0 to 70	14 Ld CERDIP	F14.3
ICL8052ACPD	0 to 70	14 Ld PDIP	E14.3
ICL8052ACDD	0 to 70	14 Ld CERDIP	F14.3
ICL8068CDD	0 to 70	14 Ld CERDIP	F14.3
ICL8068ACDD	0 to 70	14 Ld CERDIP	F14.3
ICL8068ACJD	0 to 70	14 Ld CERDIP	F14.3
ICL7104-14CPL	0 to 70	40 Ld PDIP	E40.6
ICL7104-16CPL	0 to 70	40 Ld PDIP	E40.6

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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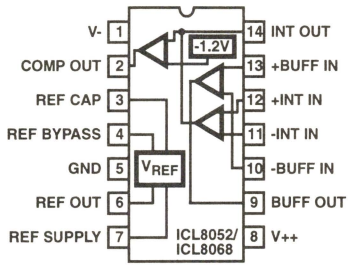
File Number **3091.1**

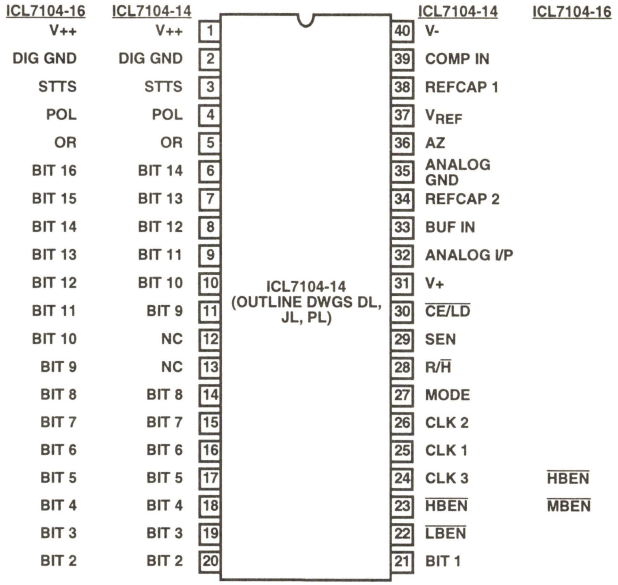
Pinouts

ICL8052/ICL8068
(CERDIP, PDIP)
TOP VIEW



(OUTLINE DWGS DD, JD, PD)

ICL7104
(PDIP)
TOP VIEW



Functional Block Diagram

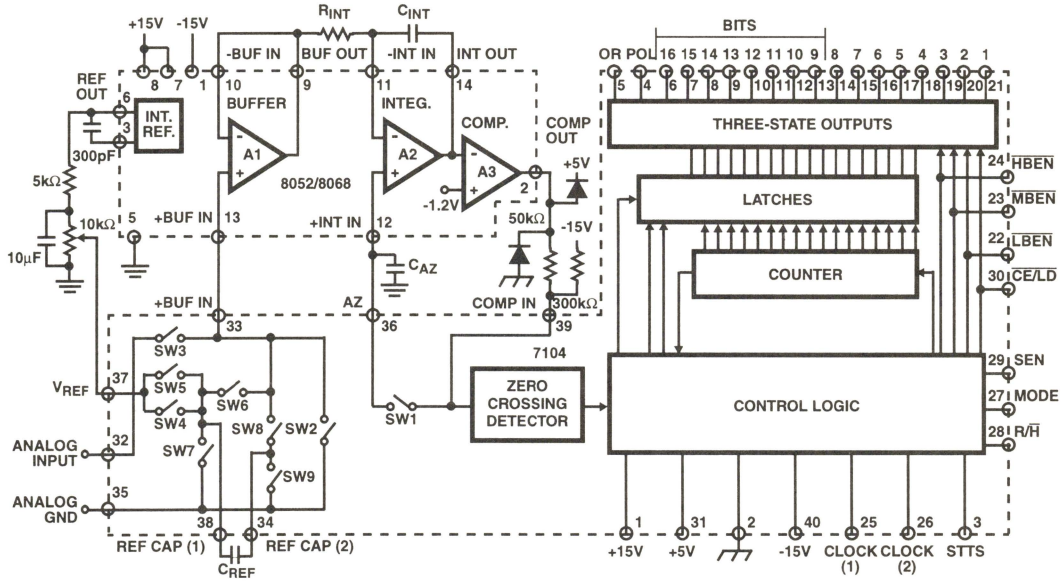


FIGURE 1. ICL8052A (8068A)/ICL7104 16-BIT/14-BIT A/D CONVERTER FUNCTIONAL DIAGRAM

DATA ACQUISITION 6

A/D CONVERTERS - SAR

		PAGE
Selection Guide		6-2
A/D Converter - SAR Data Sheets		
ADC0802, ADC0803 ADC0804	8-Bit, Microprocessor-Compatible, A/D Converters	6-5
CA3310, CA3310A	CMOS, 10-Bit, A/D Converters with Internal Track and Hold	6-6
HI-574A, HI-674A, HI-774	Complete, 12-Bit A/D Converters with Microprocessor Interface	6-7
HI5810	CMOS 10 Microsecond, 12-Bit, Sampling A/D Converter with Internal Track and Hold	6-24
HI5812	CMOS 20 Microsecond, 12-Bit, Sampling A/D Converter with Internal Track and Hold	6-36
HI5813	CMOS 3.3V, 25 Microsecond, 12-Bit, Sampling A/D Converter with Internal Track and Hold	6-49

8-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER

DEVICE	SUFFIX CODE	OUTPUTS	CONV. TYPE	CONV. RATE (KSPS)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
ADC0802	LCN	8-Bit Three-State	Successive Approximation	10	CMOS	+5	5	$\pm 1/2$	COM	EXT	80C48 and 80C80/85 Bus Compatible - No Interfacing Logic Required, Conversion Time <100µs, Easy Interface to Most Microprocessors, Will Operate in a "Stand Alone" Mode, Differential Analog Voltage Inputs, Works with Bandgap Voltage References, TTL Compatible Inputs and Outputs, On-Chip Clock Generator, 0V to 5V Analog Voltage Input Range (Single +5V Supply), No Zero-Adjust Required
ADC0802	LCD							$\pm 3/4$	IND		
ADC0802	LD							±1	MIL		
ADC0803	LCN							$\pm 1/2$	COM		
ADC0803	LCD							$\pm 3/4$	IND		
ADC0802	LCWM							±1	IND		
ADC0803	LD							±1	MIL		
ADC0804	LCN							±1	COM		
ADC0804	LCD							±1	IND		

10-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER

DEVICE	SUFFIX CODE	OUTPUTS	CONV. TYPE	CONV. RATE (KSPS)	INPUT FPBW (MHz)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	DNL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
CA3310	E	10-Bit Microprocessor Compatible	Successive Approximation	77	1.5	CMOS	+3 to +6	ADJ	±0.75	±0.75	IND		CMOS Low Power (15mW Typ), Single Supply Voltage (3V to 6V), 13µs Conversion Time, Built-In Track and Hold, Rail-to-Rail Input Range, Latched Three-State Output Drivers, Microprocessor-Compatible Control Lines, Internal or External Clock
CA3310	AE								±0.5	±0.5	IND		
CA3310	M								±0.75	±0.75	IND		
CA3310	AM								±0.5	±0.5	IND		
CA3310	D								±0.75	±0.75	MIL		
CA3310	AD								±0.5	±0.5	MIL		

12-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER

DEVICE	SUF-FIX CODE	MIL SPEC	OUTPUTS	CONV. TYPE	CONV. RATE (KSPS)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	DNL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI5813	JIP, JIB, JIJ		12-Bit Latched Three-State	Successive Approximation	40	CMOS	+3.3	5	±4.0	±4.0	IND	EXT	3.3V Supply, 25µs Conversion, Same as HI5812
	KIP, KIB, KIJ								±2.5	±2.5	IND	EXT	

12-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER (Continued)

DEVICE	SUF-FIX CODE	MIL SPEC	OUTPUTS	CONV. TYPE	CONV. RATE (KSPS)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	DNL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI3-574AJN	-5		8, 12, or 16-Bit Three-State Digital Interface for Microprocessor Control	Successive Approximation	40	Bipolar	±12 or ±15	12	±1.0		COM	10	Complete 12-Bit A/D Converter with Reference and Clock, Full 8-, 12- or 16-Bit Microprocessor Bus Interface 150ns Bus Access Time, No Missing Codes Over Temperature, Minimal Setup Time for Control Signals, 25µs Max Conversion Times, Low Noise, via Current-Mode Signal Transmission Between Chips, Byte Enable/Short Cycle (A_O Input), Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by Start Convert Input (To Set the Conversion Length), ±12V to ±15V Operation
HI3-574AKN	-5								±0.5		COM		
HI3-574ALN	-5								±0.5		COM		
HI1-574AJD	-5								±1.0		COM		
HI1-574AKD	-5								±0.5		COM		
HI1-574ALD	-5								±0.5		COM		
HI1-574ASD	-2	Y							±1.0		MIL		
HI1-574ATD	-2	Y							±0.5		MIL		
HI1-574AUD	-2	Y							±0.5		MIL		
HI5812	JIP, JIB, JIJ		12-Bit Latched Three-State	Successive Approximation	50	CMOS	+5	5	±1.5	±2.0	IND	EXT	20µs Conversion Time, 50 KSPS Throughput Rate, Built-In Track and Hold, Single +5V Supply Voltage, 25mW Maximum Power Consumption, Internal or External Clock
	KIP, KIB, KIJ								±1.0	±2.0	IND	EXT	
HI3-674AJN	-5		8, 12, or 16-Bit Three-State Digital Interface for Microprocessor Control	Successive Approximation	67	Bipolar	±12 or ±15	12	±1.0		COM	10	Complete 12-Bit A/D Converter with Reference and Clock, Full 8-, 12- or 16-Bit Microprocessor Bus Interface, 150ns Bus Access Time, No Missing Codes Over Temperature, Minimal Setup Time for Control Signals, 15µs Max Conversion Times, Low Noise, via Current-Mode Signal Transmission Between Chips, Byte Enable/Short Cycle (A_O Input), Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by Start Convert Input (To Set the Conversion Length), ±12V to ±15V Operation
HI3-674AKN	-5								±0.5		COM		
HI3-674ALN	-5								±0.5		COM		
HI1-674AJD	-5								±1.0		COM		
HI1-674AKD	-5								±0.5		COM		
HI1-674ALD	-5								±0.5		COM		
HI1-674ASD	-2	Y							±1.0		MIL		
HI1-674ATD	-2	Y							±0.5		MIL		
HI1-674AUD	-2	Y							±0.5		MIL		
HI5810	JIP, JIB, JIJ		12-Bit Latched Three-State	Successive Approximation	100	CMOS	+5	5	±2.5	±2.0	IND	EXT	10µs Conversion Time, 100 KSPS Throughput Rate, Built-In Track and Hold, Single +5V Supply Voltage, 40mW Maximum Power Consumption, Internal or External Clock, 1MHz Input Bandwidth -3dB
	KIP, KIB, KIJ								±2.0	±2.0	IND	EXT	

12-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER (Continued)

DEVICE	SUF-FIX CODE	MIL SPEC	OUTPUTS	CONV. TYPE	CONV. RATE (KSPS)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	DNL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI3-774J	-5		8, 12, or 16-Bit Three-State Digital Interface for Microprocessor Control	Successive Approximation	111	Bipolar	±12 or ±15	12	±1.0		COM	10	Complete 12-Bit A/D Converter with Reference and Clock, Full 8-, 12- or 16-Bit Microprocessor Bus Interface 150ns Bus Access Time, No Missing Codes Over Temperature, Minimal Setup Time for Control Signals, 9µs Max Conversion Times, Digital Error Correction (HI-774), Low Noise, via Current-Mode Signal Transmission Between Chips, Byte Enable/Short Cycle (A_0 Input), Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by Start Convert Input (To Set the Conversion Length), ±12V to ±15V Operation
HI3-774K									±0.5		COM		
HI1-774J									±1.0		COM		
HI1-774K									±0.5		COM		
HI1-774L									±0.5		COM		
HI1-774S	-2	Y							±1.0		MIL		
HI1-774T		Y							±0.5		MIL		
HI1-774U		Y							±0.5		MIL		

HARRIS SEMICONDUCTOR

ADC0802, ADC0803 ADC0804

8-Bit, Microprocessor-Compatible, A/D Converters

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

Features

- 80C48 and 80C80/85 Bus Compatible - No Interfacing Logic Required
- Conversion Time < 100μs
- Easy Interface to Most Microprocessors
- Will Operate in a "Stand Alone" Mode
- Differential Analog Voltage Inputs
- Works with Bandgap Voltage References
- TTL Compatible Inputs and Outputs
- On-Chip Clock Generator
- 0V to 5V Analog Voltage Input Range (Single + 5V Supply)
- No Zero-Adjust Required

Description

The ADC0802 family are CMOS 8-Bit, successive-approximation A/D converters which use a modified potentiometric ladder and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, and hence no interfacing logic is required.

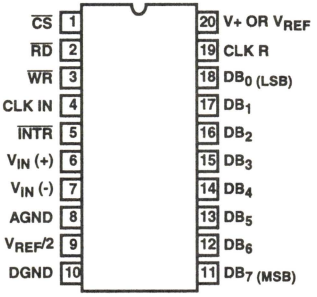
The differential analog voltage input has good common-mode-rejection and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Ordering Information

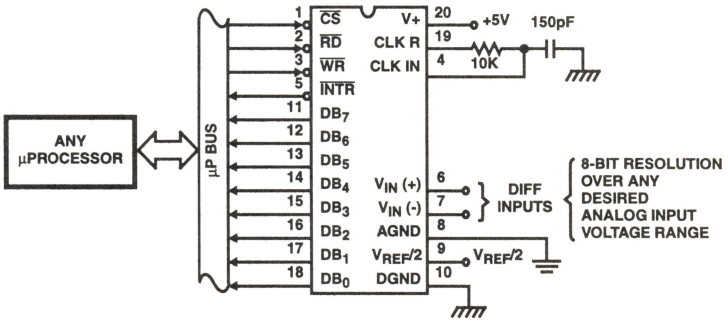
PART NUMBER	ERROR	EXTERNAL CONDITIONS	TEMP. RANGE (°C)	PACKAGE	PKG. NO
ADC0802LCN	$\pm 1/2$ LSB	$V_{REF}/2 = 2.500V_{DC}$ (No Adjustments)	0 to 70	20 Ld PDIP	E20.3
ADC0802LCD	$\pm 3/4$ LSB		-40 to 85	20 Ld CERDIP	F20.3
ADC0802LD	±1 LSB		-55 to 125	20 Ld CERDIP	F20.3
ADC0803LCN	$\pm 1/2$ LSB	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	0 to 70	20 Ld PDIP	E20.3
ADC0803LCD	$\pm 3/4$ LSB		-40 to 85	20 Ld CERDIP	F20.3
ADC0803LCWM	±1 LSB		-40 to 85	20 Ld SOIC	M20.3
ADC0803LD	±1 LSB		-55 to 125	20 Ld CERDIP	F20.3
ADC0804LCN	±1 LSB	$V_{REF}/2 = 2.500V_{DC}$ (No Adjustments)	0 to 70	20 Ld PDIP	E20.3
ADC0804LCD	±1 LSB		-40 to 85	20 Ld CERDIP	F20.3
ADC0804LCWM	±1 LSB		-40 to 85	20 Ld SOIC	M20.3

Pinout

ADC0802, ADC0803, ADC0804
(PDIP, CERDIP)
TOP VIEW



Typical Application Schematic



6 A/D CONVERTERS SAR

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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HARRIS SEMICONDUCTOR

CA3310, CA3310A

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

CMOS, 10-Bit, A/D Converters with Internal Track and Hold

Features

- CMOS Low Power (Typ) 15mW
- Single Supply Voltage . . . . . 3V to 6V
- Conversion Time 13µs
- Built-In Track and Hold
- Rail-to-Rail Input Range
- Latched Three-state Output Drivers
- Microprocessor-Compatible Control Lines
- Internal or External Clock

Applications

- Fast, No-Droop, Sample and Hold
- Voice Grade Digital Audio
- DSP Modems
- Remote Low Power Data Acquisition Systems
- µP Controlled Systems

Description

The Harris CA3310 is a fast, low power, 10-bit successive approximation analog-to-digital converter, with microprocessor-compatible outputs. It uses only a single 3V to 6V supply and typically draws just 3mA when operating at 5V. It can accept full rail-to-rail input signals, and features a built-in track and hold. The track and hold will follow high bandwidth input signals, as it has only a 100ns (typical) input time constant.

The ten data outputs feature full high-speed CMOS three-state bus driver capability, and are latched and held through a full conversion cycle. Separate 8 MSB and 2 LSB enables, a data ready flag, and conversion start and ready reset inputs complete the microprocessor interface.

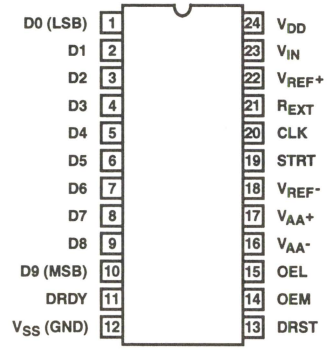
An internal, adjustable clock is provided and is available as an output. The clock may also be driven from an external source.

Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3310E	±0.75 LSB	-40 to 85	24 Ld PDIP	E24.6
CA3310AE	±0.5 LSB	-40 to 85	24 Ld PDIP	E24.6
CA3310M	±0.75 LSB	-40 to 85	24 Ld SOIC	M24.3
CA3310AM	±0.5 LSB	-40 to 85	24 Ld SOIC	M24.3
CA3310D	±0.75 LSB	-55 to 125	24 Ld SBDIP	D24.6
CA3310AD	±0.5 LSB	-55 to 125	24 Ld SBDIP	D24.6

Pinout

CA3310, CA3310A
(PDIP, SBDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3095.1**

HARRIS SEMICONDUCTOR

HI-574A, HI-674A, HI-774

Complete, 12-Bit A/D Converters with Microprocessor Interface

August 1997

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-Bit, 12-Bit or 16-Bit Microprocessor Bus Interface
- Bus Access Time 150ns
- No Missing Codes Over Temperature
- Minimal Setup Time for Control Signals
- Fast Conversion Times
  - HI-574A (Max) 25µs
  - HI-674A (Max) 15µs
  - HI-774 (Max) 9µs
- Digital Error Correction (HI-774)
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by Start Convert Input (To Set the Conversion Length)
- Supply Voltage . . . . . ±12V to ±15V

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-X74(A) is a complete 12-bit, Analog-to-Digital Converter, including a +10V reference clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 lead package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

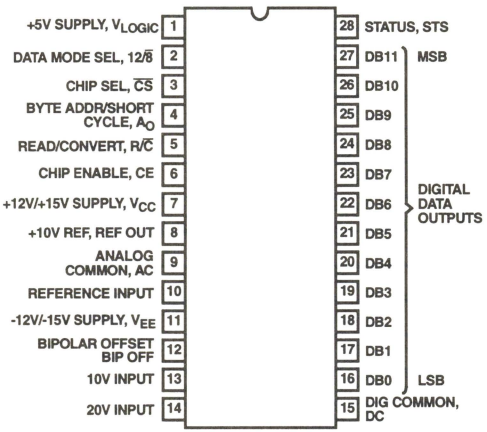
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital ICs. Also, the clock oscillator is current controlled for excellent stability over temperature.

The HI-X74(A) offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The low noise buried zener reference circuit is trimmed for minimum temperature coefficient.

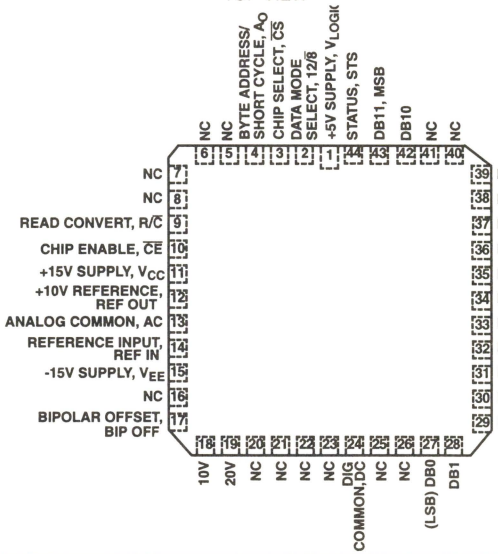
Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW (HI-574A/674A) and 390mW (HI-774) at 12V. All models are available in sidebrazed DIP, PDIP, and CLCC. For additional HI-Rel screening including 160 hour burn-in, specify "-8" suffix. For MIL-STD-883 compliant parts, request HI-574A/883, HI-674A/883, and HI-774/883 data sheets.

Pinouts

(PDIP, SBDIP)
TOP VIEW



(CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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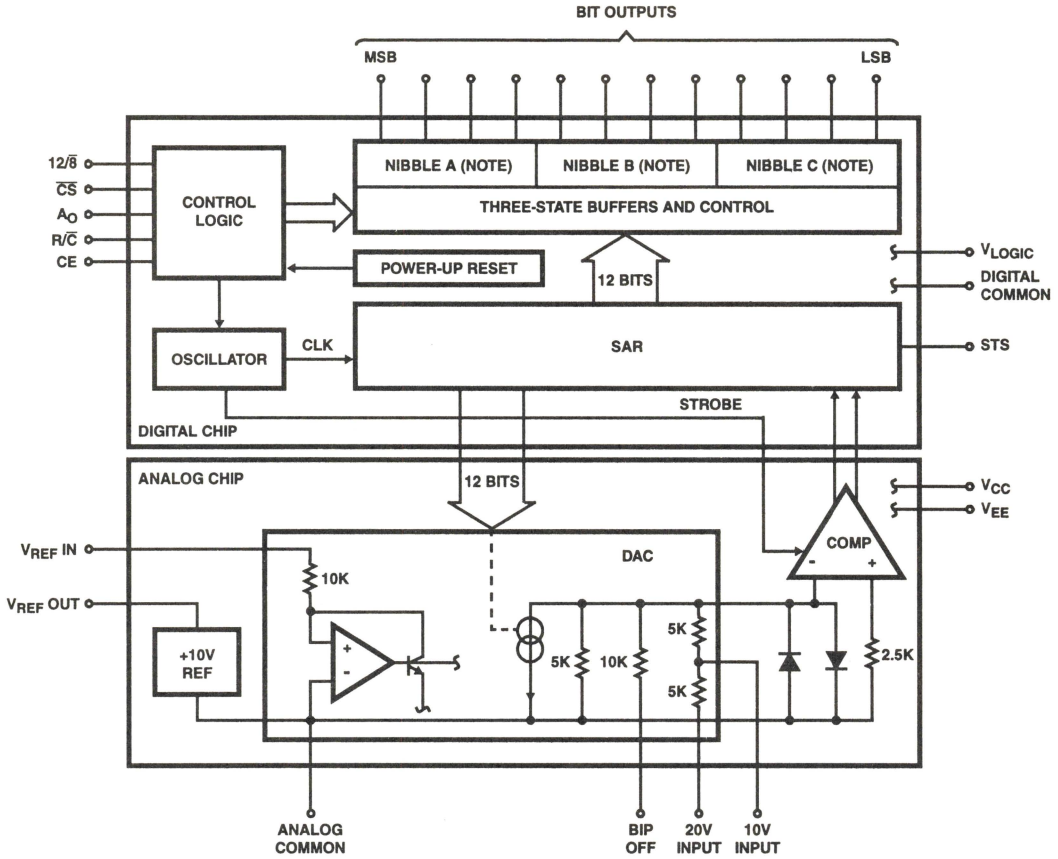
File Number 3096.4

Ordering Information

PART NUMBER	INL	TEMPERATURE RANGE (°C)	PACKAGE	PKG. NO.
HI3-574AJN-5	±1.0 LSB	0 to 75	28 Ld PDIP	E28.6
HI3-574AKN-5	±0.5 LSB	0 to 75	28 Ld PDIP	E28.6
HI3-574ALN-5	±0.5 LSB	0 to 70	28 Ld PDIP	E28.6
HI1-574AJD-5	±1.0 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-574AKD-5	±0.5 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-574ALD-5	±0.5 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-574ASD-2	±1.0 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-574ATD-2	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-574AUD-2	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-574ASD/883	±1.0 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-574ATD/883	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-574AUD/883	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI4-574ASE/883	±1.0 LSB	-55 to 125	44 Ld CLCC	J44.A
HI4-574ATE/883	±0.5 LSB	-55 to 125	44 Ld CLCC	J44.A
HI4-574AUE/883	±0.5 LSB	-55 to 125	44 Ld CLCC	J44.A
HI3-674AJN-5	±1.0 LSB	0 to 75	28 Ld PDIP	E28.6
HI3-674AKN-5	±0.5 LSB	0 to 75	28 Ld PDIP	E28.6
HI3-674ALN-5	±0.5 LSB	0 to 75	28 Ld PDIP	E28.6
HI1-674AJD-5	±1.0 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-674AKD-5	±0.5 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-674ALD-5	±0.5 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-674ASD-2	±1.0 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-674ATD-2	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-674AUD-2	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-674ASD/883	±1.0 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-674ATD/883	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-674AUD/883	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI4-674ASE/883	±1.0 LSB	-55 to 125	44 Ld CLCC	J44.A
HI4-674ATE/883	±0.5 LSB	-55 to 125	44 Ld CLCC	J44.A
HI4-674AUE/883	±0.5 LSB	-55 to 125	44 Ld CLCC	J44.A
HI3-774J-5	±1.0 LSB	0 to 75	28 Ld PDIP	E28.6
HI3-774K-5	±0.5 LSB	0 to 75	28 Ld PDIP	E28.6
HI1-774J-5	±1.0 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-774K-5	±0.5 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-774U-2	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-774T/883	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI4-774S/883	±1.0 LSB	-55 to 125	44 Ld CLCC	J44.A
HI4-774T/883	±0.5 LSB	-55 to 125	44 Ld CLCC	J44.A
HI4-774U/883	±0.5 LSB	-55 to 125	44 Ld CLCC	J44.A

Functional Block Diagram



NOTE: "Nibble" is a 4-bit digital word.

Absolute Maximum Ratings

Supply Voltage
- V_{CC} to Digital Common . . . . . 0V to +16.5V
- V_{EE} to Digital Common. . . . . 0V to -16.5V
- V_{LOGIC} to Digital Common. . . . . 0V to +7V
- Analog Common to Digital Common±1V

Control Inputs
- (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common . . -0.5V to V_{LOGIC} +0.5V

Analog Inputs
- (REFIN, BIPOFF, 10VIN) to Analog Common. . . . . ±16.5V
- 20VIN to Analog Common . . . . . ±24V

REFOUT . . . . Indefinite Short To Common, Momentary Short To V_{CC}

Operating Conditions

Temperature Range
- HI3-574AxN-5, HI1-574AxD-5 . . . . . .0°C to 75°C
- HI3-674AxN-5, HI1-674AxD-5 . . . . . .0°C to 75°C
- HI3-774xN-5, HI1-774xD-5 . . . . . .0°C to 75°C
- HI1-574AxD-2, HI1-674AxD-2, HI1-774xD-2 . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CLCC Package	65	14
SBDIP Package	60	18
HI3-574AxN-5, HI3-674AxN-5, HI3-774xN-5	65	N/A

Maximum Junction Temperature
- HI3-574AxN-5, HI3-674AxN-5, HI3-774xN-5. . . . . 150°C
- HI1-574AxD-2, HI1-574AxD-5. . . . . 175°C
- HI1-674AxD-2, HI1-674AxD-5. . . . . 175°C
- HI1-774xD-2, HI1-774xD-5 . . . . . 175°C

Maximum Storage Temperature Range
- HI3-574AxN-5, HI3-674AxN-5, HI3-774xN-5. . . . . -40°C to 85°C
- HI1-574AxD-2, HI1-574AxD-5. . . . . -65°C to 150°C
- HI1-674AxD-2, HI1-674AxD-5. . . . . -65°C to 150°C
- HI1-774xD-2, HI1-774xD-5 . . . . . -65°C to 150°C

Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C

Die Characteristics

Transistor Count
- HI-574A, HI-674A 1117
- HI-774 2117

DC and Transfer Accuracy Specifications

Typical at 25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified

PARAMETER		TEMPERATURE RANGE -5 (0°C to 75°C) J SUFFIX	K SUFFIX	L SUFFIX	UNITS
DYNAMIC CHARACTERISTICS					
Resolution (Max)		12	12	12	Bits
Linearity Error					
25°C (Max)		±1	±1/2	±1/2	LSB
0°C to 75°C (Max)		±1	±1/2	±1/2	LSB
Max Resolution For Which No Missing Codes Is Guaranteed					
25°C	HI-574A, HI-674A	12	12	12	Bits
	HI-774	11	12	12	Bits
T_{MIN} to T_{MAX}	HI-574A, HI-674A	11	12	12	Bits
	HI-774	11	12	12	Bits
Unipolar Offset (Max)					
Adjustable to Zero		±2	±1.5	±1	LSB
Bipolar Offset (Max)					
V_{IN} = 0V (Adjustable to Zero)		±4	±4	±3	LSB
V_{IN} = -10V		±0.15	±0.1	±0.1	% of FS
Full Scale Calibration Error					
25°C (Max), With Fixed 50Ω Resistor From REF OUT To REF IN (Adjustable to Zero)		±0.25	±0.25	±0.15	% of FS
T_{MIN} to T_{MAX} (No Adjustment At 25°C)		±0.475	±0.375	±0.20	% of FS
T_{MIN} to T_{MAX} (With Adjustment To Zero 25°C)		±0.22	±0.12	±0.05	% of FS

DC and Transfer Accuracy Specifications Typical at 25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMPERATURE RANGE -5 (0°C to 75°C) J SUFFIX	K SUFFIX	L SUFFIX	UNITS
Temperature Coefficients Guaranteed Max Change, T_{MIN} to T_{MAX} (Using Internal Reference)					
Unipolar Offset	HI-574A, HI-674A	±2	±1	±1	LSB
	HI-774	±2	±1	±1	LSB
Bipolar Offset	HI-574A, HI-674A	±2	±1	±1	LSB
	HI-774	±2	±2	±1	LSB
Full Scale Calibration	HI-574A, HI-674A	±9	±2	±2	LSB
	HI-774	±9	±5	±2	LSB
Power Supply Rejection Max Change In Full Scale Calibration					
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V		±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V		±1/2	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V		±2	±1	±1	LSB
ANALOG INPUTS					
Input Ranges					
Bipolar		-5 to +5			V
		-10 to +10			V
Unipolar		0 to +10			V
		0 to +20			V
Input Impedance					
10V Span		5K, ±25%			Ω
20V Span		10K, ±25%			Ω
POWER SUPPLIES					
Operating Voltage Range					
V_{LOGIC}		+4.5 to +5.5			V
V_{CC}		+11.4 to +16.5			V
V_{EE}		-11.4 to -16.5			V
Operating Current					
I_{LOGIC}		7 Typ, 15 Max			mA
I_{CC} +15V Supply		11 Typ, 15 Max			mA
I_{EE} -15V Supply		21 Typ, 28 Max			mA
Power Dissipation					
±15V, +15V		515 Typ, 720 Max			mW
±12V, +5V		385 Typ			mW
Internal Reference Voltage					
T_{MIN} to T_{MAX}		+10.00 ±0.05 Max			V
Output Current, Available For External Loads (External Load Should Not Change During Conversion).		2.0 Max			mA

DC and Transfer Accuracy Specifications Typical at 25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified

PARAMETER		TEMPERATURE RANGE -2 (-55°C to 125°C) S SUFFIX	T SUFFIX	U SUFFIX	UNITS
DYNAMIC CHARACTERISTICS					
Resolution (Max)		12	12	12	Bits
Linearity Error					
25°C		±1	±1/2	±1/2	LSB
-55°C to 125°C (Max)		±1	±1	±1	LSB
Max Resolution For Which No Missing Codes Is Guaranteed					
25°C	HI-574A, HI-674A	12	12	12	Bits
	HI-774	11	12	12	Bits
T_{MIN} to T_{MAX}	HI-574A, HI-674A	11	12	12	Bits
	HI-774	11	12	12	Bits
Unipolar Offset (Max)					
Adjustable to Zero	HI-574A, HI-674A	±2	±1.5	±1	LSB
	HI-774	±2	±2	±1	LSB
Bipolar Offset (Max)					
V_{IN} = 0V (Adjustable to Zero)		±4	±4	±3	LSB
V_{IN} = -10V		±0.15	±0.1	±0.1	% of FS
Full Scale Calibration Error					
25°C (Max), With Fixed 50Ω Resistor From REF OUT To REF IN (Adjustable To Zero)		±0.25	±0.25	±0.15	% of FS
T_{MIN} to T_{MAX} (No Adjustment At 25°C)		±0.75	±0.50	±0.275	% of FS
T_{MIN} to T_{MAX} (With Adjustment To Zero At 25°C)		±0.50	±0.25	±0.125	% of FS
Temperature Coefficients Guaranteed Max Change, T_{MIN} to T_{MAX} (Using Internal Reference)					
Unipolar Offset		±2	±1	±1	LSB
Bipolar Offset		±2	±2	±1	LSB
Full Scale Calibration		±20	±10	±5	LSB
Power Supply Rejection Max Change In Full Scale Calibration					
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V		±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V		±1/2	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V		±2	±1	±1	LSB
ANALOG INPUTS					
Input Ranges					
Bipolar		-5 to +5			V
		-10 to +10			V
Unipolar		0 to +10			V
		0 to +20			V

DC and Transfer Accuracy Specifications Typical at 25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMPERATURE RANGE -2 (-55°C to 125°C) S SUFFIX	T SUFFIX	U SUFFIX	UNITS
Input Impedance				
10V Span	5K, ±25%			Ω
20V Span	10K, ±25%			Ω
POWER SUPPLIES				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			V
V_{CC}	+11.4 to +16.5			V
V_{EE}	-11.4 to -16.5			V
Operating Current				
I_{LOGIC}	7 Typ, 15 Max			mA
I_{CC} +15V Supply	11 Typ, 15 Max			mA
I_{EE} -15V Supply	21 Typ, 28 Max			mA
Power Dissipation				
±15V, +15V	515 Typ, 720 Max			mW
±12V, +5V	385 Typ			mW
Internal Reference Voltage				
T_{MIN} to T_{MAX}	+10.00 ±0.05 Max			V
Output current, available for external loads (External load should not change during conversion).	2.0 Max			mA

Digital Specifications All Models, Over Full Temperature Range

PARAMETER	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 412/$\overline{8}$)			
Logic "1"	+2.4V	-	+5.5V
Logic "0"	-0.5V	-	+0.8V
Current	-	±0.1µA	±5µA
Capacitance	-	5pF	-
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} - 1.6mA)	-	-	+0.4V
Logic "1" (I_{SOURCE} - 500µA)	+2.4V	-	-
Logic "1" (I_{SOURCE} - 10µA)	+4.5V	-	-
Leakage (High-Z State, DB11-DB0 Only)	-	±0.1µA	±5µA
Capacitance	-	5pF	-

Timing Specifications (HI-574A) 25°C, Note 2, Unless Otherwise Specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
t_{DSC}	STS Delay from CE	-	-	200	ns

Timing Specifications (HI-574A) 25°C, Note 2, Unless Otherwise Specified **(Continued)**

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
t_{HEC}	CE Pulse Width		50	-	-	ns
t_{SSC}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{HSC}	$\overline{CS}$ Low During CE High		50	-	-	ns
t_{SRC}	R/$\overline{C}$ to CE Setup		50	-	-	ns
t_{HRC}	R/$\overline{C}$ Low During CE High		50	-	-	ns
t_{SAC}	A_0 to CE Setup		0	-	-	ns
t_{HAC}	A_0 Valid During CE High		50	-	-	ns
t_C	Conversion Time	12-Bit Cycle T_{MIN} to T_{MAX}	15	20	25	µs
		8-Bit Cycle T_{MIN} to T_{MAX}	10	13	17	µs
READ MODE						
t_{DD}	Access Time from CE		-	75	150	ns
t_{HD}	Data Valid After CE Low		25	-	-	ns
t_{HL}	Output Float Delay		-	100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{SRR}	R/$\overline{C}$ to CE Setup		0	-	-	ns
t_{SAR}	A_0 to CE Setup		50	-	-	ns
t_{HSR}	$\overline{CS}$ Valid After CE Low		0	-	-	ns
t_{HRR}	R/$\overline{C}$ High After CE Low		0	-	-	ns
t_{HAR}	A_0 Valid After CE Low		50	-	-	ns
t_{HS}	STS Delay After Data Valid		300	-	1200	ns

Timing Specifications (HI-674A) 25°C, Note 2, Unless Otherwise Specified

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
CONVERT MODE						
t_{DSC}	STS Delay from CE		-	-	200	ns
t_{HEC}	CE Pulse Width		50	-	-	ns
t_{SSC}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{HSC}	$\overline{CS}$ Low During CE High		50	-	-	ns
t_{SRC}	R/$\overline{C}$ to CE Setup		50	-	-	ns
t_{HRC}	R/$\overline{C}$ Low During CE High		50	-	-	ns
t_{SAC}	A_0 to CE Setup		0	-	-	ns
t_{HAC}	A_0 Valid During CE High		50	-	-	ns
t_C	Conversion Time	12-Bit Cycle T_{MIN} to T_{MAX}	9	12	15	µs
		8-Bit Cycle T_{MIN} to T_{MAX}	6	8	10	µs
READ MODE						
t_{DD}	Access Time from CE		-	75	150	ns
t_{HD}	Data Valid After CE Low		25	-	-	ns
t_{HL}	Output Float Delay		-	100	150	ns

Timing Specifications (HI-674A) 25°C, Note 2, Unless Otherwise Specified **(Continued)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{SSR}	$\overline{CS}$ to CE Setup	50	-	-	ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	-	-	ns
t_{SAR}	A_O to CE Setup	50	-	-	ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0	-	-	ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0	-	-	ns
t_{HAR}	A_O Valid After CE Low	50	-	-	ns
t_{HS}	STS Delay After Data Valid	25	-	850	ns

Timing Specifications (HI-774) 25°C, Into a load with R_L = 3kΩ and C_L = 50pF, Note 2, Unless Otherwise Specified

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
CONVERT MODE						
t_{DSC}	STS Delay from CE		-	100	200	ns
t_{HEC}	CE Pulse Width		50	30	-	ns
t_{SSC}	$\overline{CS}$ to CE Setup		50	20	-	ns
t_{HSC}	$\overline{CS}$ Low During CE High		50	20	-	ns
t_{SRC}	R/$\overline{C}$ to CE Setup		50	0	-	ns
t_{HRC}	R/$\overline{C}$ Low During CE High		50	20	-	ns
t_{SAC}	A_O to CE Setup		0	0	-	ns
t_{HAC}	A_O Valid During CE High		50	30	-	ns
t_C	Conversion Time	12-Bit Cycle T_{MIN} to T_{MAX} (-5)	-	8.0	9	µs
		8-Bit Cycle T_{MIN} to T_{MAX} (-5)	-	6.4	6.8	µs
		12-Bit Cycle T_{MIN} to T_{MAX} (-2)	-	9	11	µs
		8-Bit Cycle T_{MIN} to T_{MAX} (-2)	-	6.8	8.3	µs
READ MODE						
t_{DD}	Access Time from CE		-	75	150	ns
t_{HD}	Data Valid After CE Low		25	35	-	ns
t_{HL}	Output Float Delay		-	70	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup		50	0	-	ns
t_{SRR}	R/$\overline{C}$ to CE Setup		0	0	-	ns
t_{SAR}	A_O to CE Setup		50	25	-	ns
t_{HSR}	CS Valid After CE Low		0	0	-	ns
t_{HRR}	R/$\overline{C}$ High After CE Low		0	0	-	ns
t_{HAR}	A_O Valid After CE Low		50	25	-	ns
t_{HS}	STS Delay After Data Valid		-	90	300	ns

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	V_{LOGIC}	Logic supply pin (+5V)
2	12/$\overline{8}$	Data Mode Select - Selects between 12-bit and 8-bit output modes.
3	$\overline{CS}$	Chip Select - Chip Select high disables the device.
4	A_0	Byte Address/Short Cycle - See Table 1 for operation.
5	R/$\overline{C}$	Read/Convert - See Table 1 for operation.
6	CE	Chip Enable - Chip Enable low disables the device.
7	V_{CC}	Positive Supply (+12V/+15V)
8	REF OUT	+10V Reference
9	AC	Analog Common
10	REF IN	Reference Input
11	V_{EE}	Negative Supply (-12V/-15V).
12	BIP OFF	Bipolar Offset
13	10V Input	10V Input - Used for 0V to 10V and -5V to +5V input ranges.
14	20V Input	20V Input - Used for 0V to 20V and -10V to +10V input ranges.
15	DC	Digital Common
16	DB0	Data Bit 0 (LSB)
17	DB1	Data Bit 1
18	DB2	Data Bit 2
19	DB3	Data Bit 3
20	DB4	Data Bit 4
21	DB5	Data Bit 5
22	DB6	Data Bit 6
23	DB7	Data Bit 7
24	DB8	Data Bit 8
25	DB9	Data Bit 9
26	DB10	Data Bit 10
27	DB11	Data Bit 11 (MSB)
28	STS	Status Bit - Status high implies a conversion is in progress.

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs $^1/_2$ LSB (1.22mV for 10V span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level $1^1/_2$ LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-X74(A)K and L grades are guaranteed for maximum nonlinearity of $\pm^1/_2$ LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-X74(A)J is guaranteed to ±1 LSB max error. For this grade, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-X74(A)K and L grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-X74(A)J grade guarantees no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

The first transition should occur at a level $^1/_2$ LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value $^1/_2$ LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value $1^1/_2$ LSB below the nominal full scale (9.9963V for 10.000V full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10V reference.

Temperature Coefficients

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection

The standard specifications for the HI-X74A assume use of +5.00V and ±15.00V or ±12.00V supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10V for a 12-bit ADC.

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of $\pm^1/_2$ LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-justified Data

The data format used in the HI-X74(A) is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-X74(A)

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

Physical Mounting and Layout Considerations

Layout

Unwanted, parasitic circuit components, (L, R, and C) can make 12-bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vector board, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-X74(A) (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSBs to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10µF tantalum type in parallel with a 0.1µF ceramic type is recommended.

Ground Connections

Pins 9 and 15 should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) +15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-X74(A)'s Analog Common or Digital Common).

Analog Signal Source

HI-574A and HI-674A

The device chosen to drive the HI-X74A analog input will see a nominal load of 5kΩ (10V range) or 10kΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 1.6µs and 950ns intervals for the HI-574A and HI-674A, respectively. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 600KHz for use with the HI-X74A. To check whether the output properties of a signal source are suitable, monitor the HI-X74A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in 1µs or less for the HI-574A and 500ns or less for the HI-674A. (The comparator decision is made about 1.5µs and 850ns after each code change from the SAR for the HI-574A and HI-674A, respectively.)

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-574A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-574A.

HI-774

The device driving the HI-774 analog input will see a nominal load of 5kΩ (10V range) or 10kΩ (20V range). However, the other end of these input resistors may change as much as ±400mV with each bit decision. These input disturbances are caused by the internal DAC changing codes which causes a glitch on the summing junction. This creates abrupt changes in current at the analog input causing a "kick back" glitch from the input. Because the algorithm starts with the MSB, the first glitches will be the largest and get smaller as the conversion proceeds. These glitches can occur at 350ns intervals so an op amp with a low output impedance and fast settling is desirable. Ultimately the input must settle to within the window of Figure 1 at the bit decision points in order to achieve 12-bit accuracy.

The HI-774 differs from the most high-speed successive approximation type ADC's in that it does not require a high performance buffer or sample and hold. With error correction the input can settle while the conversion is underway, but only during the first 4.8µs. The input must be within 10.76% of the final value when the MSB decision is made. This occurs approximately 650ns after the conversion has been initiated. Digital error correction also loosens the bandwidth requirements of the buffer or sample and hold. As long as the input "kick back" disturbances settle within the window of Figure 1 the device will remain accurate. The combined effect of settling and the "kick back" disturbances must remain in the Figure 1 window.

If the design is being optimized for speed, the input device should have closed loop bandwidth to 3MHz, and a low output impedance (calculated by dividing the open loop output resistance by the open loop gain). If the application requires a high speed sample and hold the Harris HA-5330 or HA-5320 are recommended.

In any design the input (pin 13 or 14) should be checked during a conversion to make sure that the input stays within the correctable window of Figure 1.

Digital Error Correction

HI-774

The HI-774 features the smart successive approximation register (SSAR) which includes digital error correction. This has the advantage of allowing the initial input to vary within a +31 to -32 LSB window about the final value. The input can move during the first 4.8µs, after which it must remain stable within $\pm^1/_2$ LSB. With this feature a conversion can start before the input has settled completely; however, it must be within the window as described in Figure 1.

The conversion cycle starts by making the first 8-bit decisions very quickly, allowing the internal DAC to settle only to 8-bit accuracy. Then the converter goes through two error correction cycles. At this point the input must be stable within $\pm^1/_2$ LSB. These cycles correct the 8-bit word to 12-bit accuracy for any errors made (up to +16 or -32 LSBs). This is up one count or down two counts at 8-bit resolution. The converter then continues to make the 4 LSB decisions, settling out to 12-bit accuracy. The last four bits can adjust the code in the positive direction by up to 15 LSBs. This results in a total correction range of +31 to -32 LSBs. When an 8-bit conversion is performed, the input must settle to within $\pm^1/_2$ LSB at 8-bit resolution (which equals ±8 LSBs at 12-bit resolution).

With the HI-774 a conversion can be initiated before the input has completely settled, as long as it meets the constraints of the Figure 1 window. This allows the user to start conversion up to 4.8µs earlier than with a typical analog to digital converter. A typical successive approximation type ADC must have a constant input during a conversion because once a bit decision is made it is locked in and cannot change.

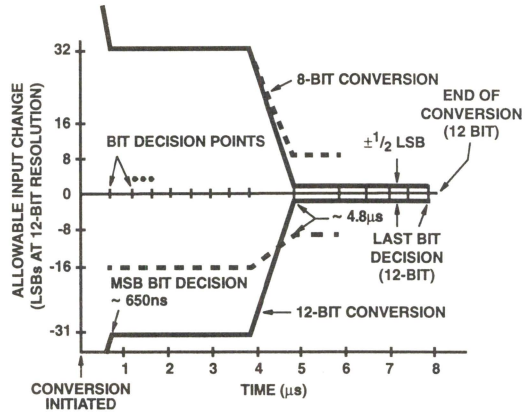
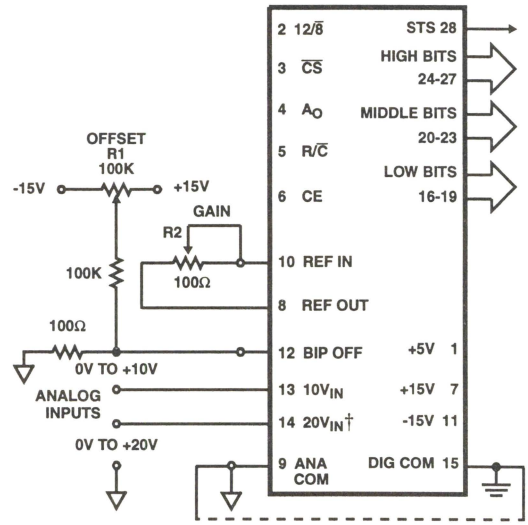
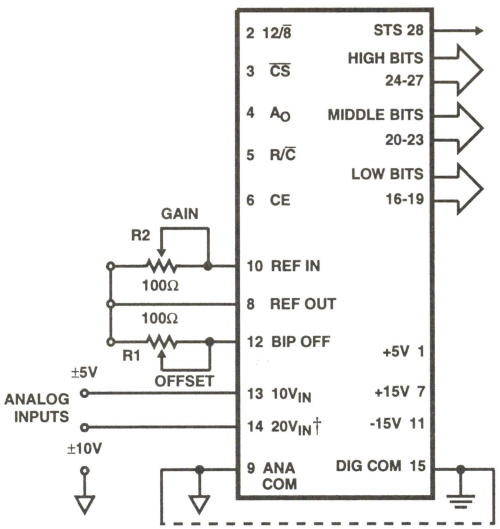


FIGURE 1. HI-774 ERROR CORRECTION WINDOW vs TIME



†When driving the 20V (pin 14) input, minimize capacitance on pin 13.

FIGURE 2. UNIPOLAR CONNECTIONS



†When driving the 20V (pin 14) input, minimize capacitance on pin 13.

FIGURE 3. BIPOLAR CONNECTIONS

Range Connections and Calibration Procedures

The HI-X74(A) is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figure 2 and Figure 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-X74(A) offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration

Refer to Figure 2. The resistors shown (see Note) are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem - the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of $+^1/_2$ LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is $1^1/_2$ LSBs below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2 (see Note). If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage $^1/_2$ LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage $1^1/_2$ LSBs below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

NOTE: The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

Controlling the HI-X74(A)

The HI-X74(A) includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8-bit or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready-choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 7.

"Stand-Alone Operation"

The simplest control interface calls for a singe control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 8 and 9. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing".

HI-574A STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	-	-	ns
t_{DS}	STS Delay from R/$\overline{C}$	-	-	200	ns
t_{HDR}	Data Valid after R/$\overline{C}$ Low	25	-	-	ns
t_{HS}	STS Delay after Data Valid	300	-	1200	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	-	-	ns
t_{DDR}	Data Access Time	-	-	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

HI-674A STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	-	-	ns
t_{DS}	STS Delay from R/$\overline{C}$	-	-	200	ns
t_{HDR}	Data Valid after R/$\overline{C}$ Low	25	-	-	ns
t_{HS}	STS Delay after Data Valid	25	-	850	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	-	-	ns
t_{DDR}	Data Access Time	-	-	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

HI-774 STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	-	-	ns
t_{DS}	STS Delay from R/$\overline{C}$	-	-	200	ns
t_{HDR}	Data Valid after R/$\overline{C}$ Low	20	-	-	ns
t_{HS}	STS Delay after Data Valid	-	-	850	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	-	-	ns
t_{DDR}	Data Access Time	-	-	150	ns

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8-bit conversion, the last three LSBs will read ZERO and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

TABLE 1. TRUTH TABLE FOR HI-X74(A) CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit Output
1	0	1	0	0	Enable 8 MSBs Only
1	0	1	0	1	Enable 4 LSBs Plus 4 Trailing Zeroes

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. However, to ensure that a particular input controls the start of conversion, the other two should be set up at least 50ns earlier. See the HI-774 Timing Specifications, Convert Mode.

This variety of HI-X74(A) control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 4.

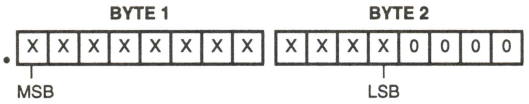
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high.

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 5.

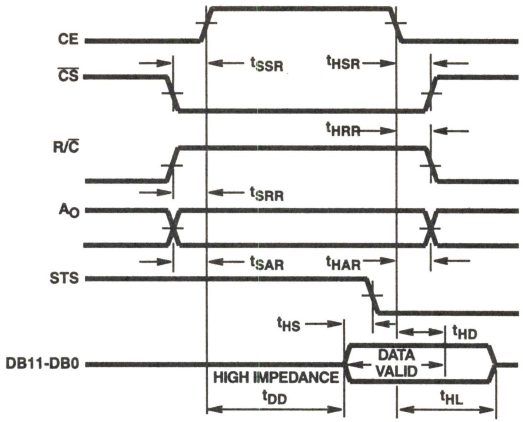
The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12-bit or 16-bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8-bit bytes, selected one at a time by A_0. This allows an 8-bit data bus to be connected as shown in Figure 6. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-X74(A) output in two consecutive memory locations. (With A_0 low, the 8 MSBs only are enabled. With A_0 high, 4 MSBs are disabled, bits 4 through 7 are forced low, and the 4 LSBs are enabled). This two byte format is considered "left justified data," for which a decimal (or binary!) point is assumed to the left of byte 1:



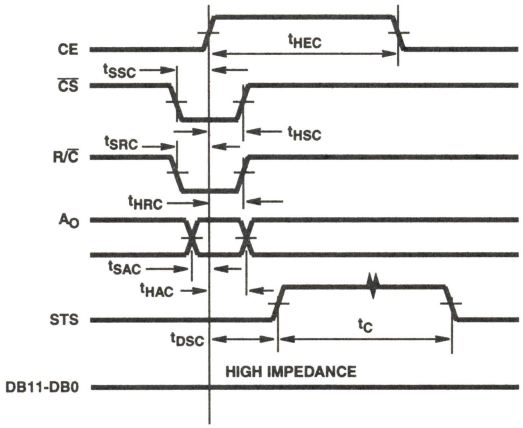
Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 6 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data, however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. See Figure 5.



See HI-774 Timing Specifications for more information.

FIGURE 5. READ CYCLE TIMING



See HI-774 Timing Specifications for more information.

FIGURE 4. CONVERT START TIMING

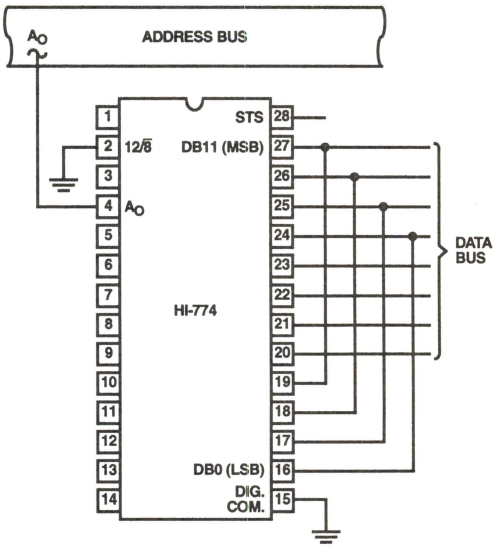


FIGURE 6. INTERFACE TO AN 8-BIT DATA BUS

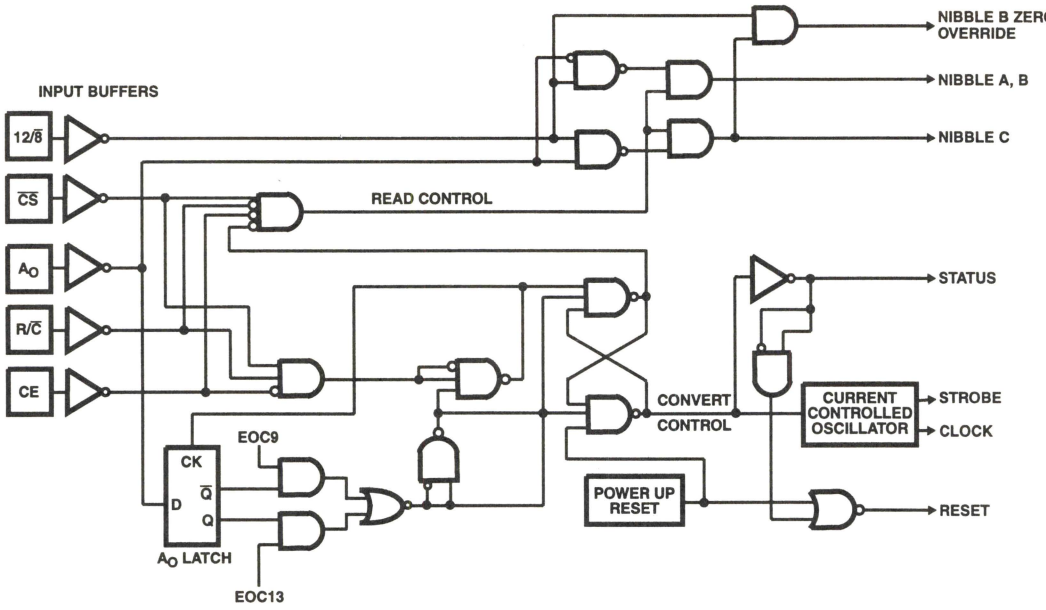


FIGURE 7. HI-774 CONTROL LOGIC

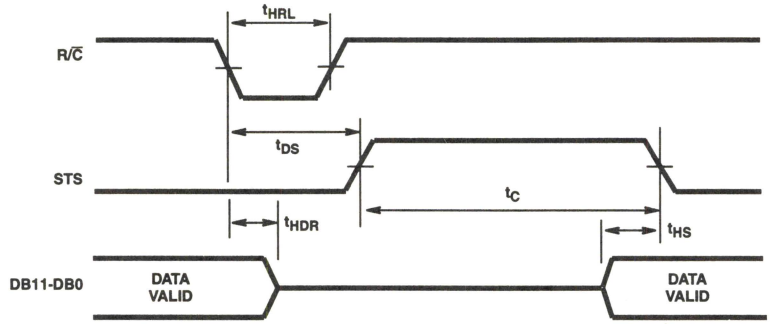


FIGURE 8. LOW PULSE FOR R/C - OUTPUTS ENABLED AFTER CONVERSION

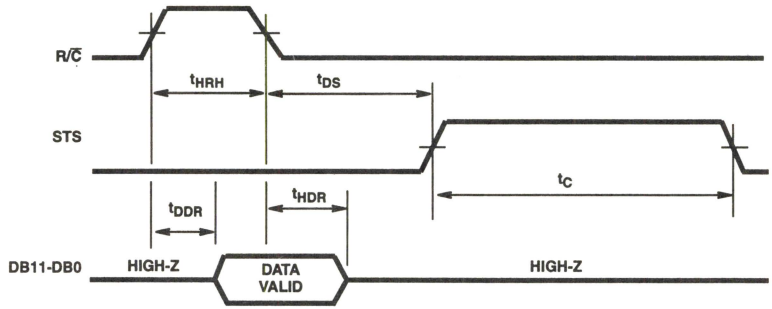


FIGURE 9. HIGH PULSE FOR R/C - OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

Die Characteristics

DIE DIMENSIONS:

Analog: 3070mm x 4610mm
Digital: 1900mm x 4510mm

METALLIZATION:

Digital Type: Nitrox
Thickness: 10kÅ ±2kÅ

Metal 1: AlSiCu
Thickness: 8kÅ ±1kÅ

Metal 2: AlSiCu
Thickness: 16kÅ ±2kÅ

Analog Type: Al
Thickness: 16kÅ ±2kÅ

PASSIVATION:

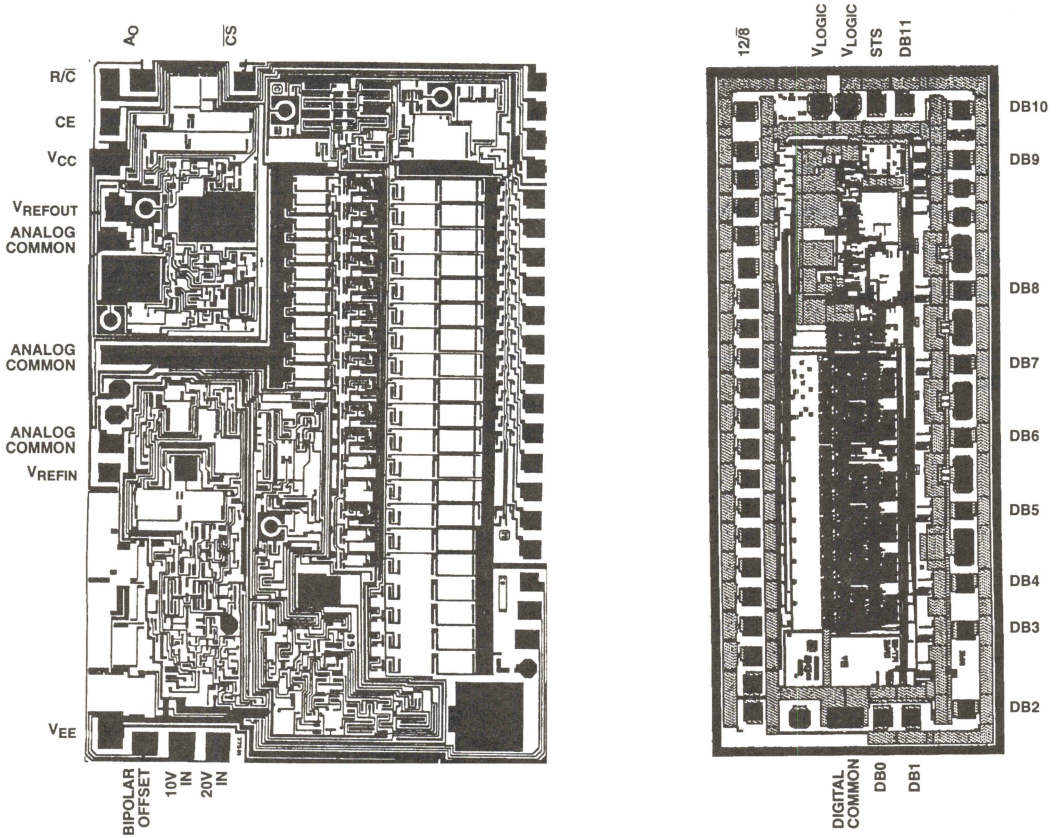
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±0.5kÅ
Silox Thickness: 12kÅ ±1.5kÅ

WORST CASE CURRENT DENSITY:

1.3×10^5 A/cm^2

Metallization Mask Layout

HI-574A, HI-674A, HI-774



HARRIS SEMICONDUCTOR

HI5810

CMOS 10 Microsecond, 12-Bit, Sampling A/D Converter with Internal Track and Hold

August 1997

Features

- Conversion Time 10µs
- Throughput Rate . . . . . 100 KSPS
- Built-In Track and Hold
- Single Supply Voltage . . . . . +5V
- Maximum Power Consumption. 40mW
- Internal or External Clock
- 1MHz Input Bandwidth . . . . . -3dB

Applications

- Remote Low Power Data Acquisition Systems
- Digital Audio
- DSP Modems
- General Purpose DSP Front End
- µP Controlled Measurement Systems
- Process Controls
- Industrial Controls

Description

The HI5810 is a fast, low power, 12-bit, successive-approximation, analog-to-digital converter. It can operate from a single 3V to 6V supply and typically draws just 1.9mA when operating at 5V. The HI5810 features a built-in track and hold. The conversion time is as low as 10µs with a 5V supply.

The twelve data outputs feature full high speed CMOS three-state bus driver capability, and are latched and held through a full conversion cycle. The output is user selectable: [i.e., 12-bit, 8-bit (MSBs), and/or 4-bit (LSBs)]. A data ready flag, and conversion-start input complete the digital interface.

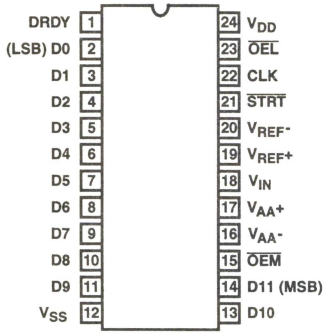
An internal clock is provided and is available as an output. The clock may also be over-driven by an external source.

Ordering Information

PART NUMBER	INL (LSB) (MAX OVER TEMP.)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5810JIP	±2.5	-40 to 85	24 Ld PDIP	E24.3
HI5810KIP	±2.0	-40 to 85	24 Ld PDIP	E24.3
HI5810JIB	±2.5	-40 to 85	24 Ld SOIC	M24.3
HI5810KIB	±2.0	-40 to 85	24 Ld SOIC	M24.3
HI5810JIJ	±2.5	-40 to 85	24 Ld CERDIP	F24.3
HI5810KIJ	±2.0	-40 to 85	24 Ld CERDIP	F24.3

Pinout

HI5810
(PDIP, CERDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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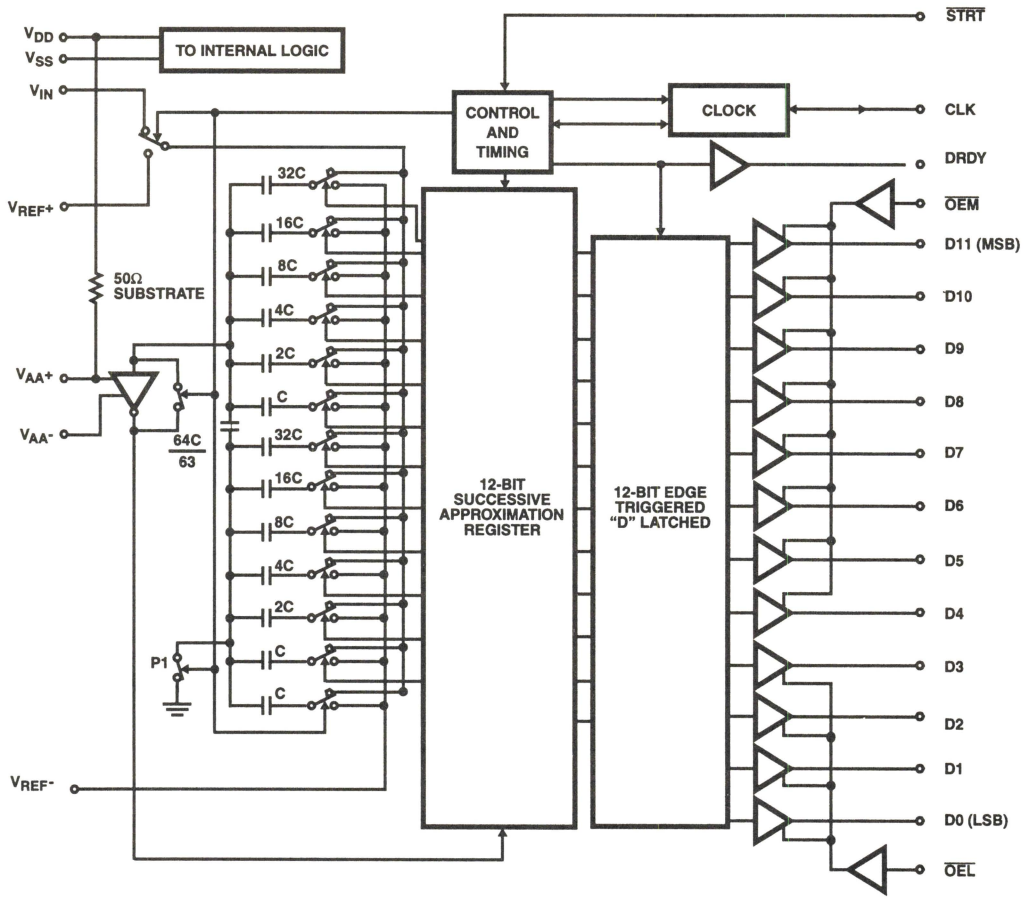
File Number 3633.1

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage
- V_{DD} to V_{SS} ..... (V_{SS} -0.5V) < V_{DD} < +6.5V
- V_{AA}+ to V_{AA}- ..... (V_{SS} -0.5V) to (V_{SS} +6.5V)
- V_{AA}+ to V_{DD} ..... ±0.3V

Analog and Reference Inputs
- V_{IN}, V_{REF}+, V_{REF}- ..... (V_{SS} -0.3V) < V_{INA} < (V_{DD} +0.3V)

Digital I/O Pins ..... (V_{SS} -0.3V) < VI/O < (V_{DD} +0.3V)

Operating Conditions

Temperature Range
- PDIP, SOIC, and CERDIP Packages ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	60	12
PDIP Package	80	N/A
SOIC Package	75	N/A

Maximum Junction Temperature
- Plastic Packages ..... 150°C
- Hermetic Package ..... 175°C

Maximum Storage Temperature Range ..... -65°C to 150°C

Maximum Lead Temperature (Soldering, 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{DD} = V_{AA}+ = 5V, V_{REF}+ = +4.608V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = External 1.5MHz, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	UNITS
ACCURACY								
Resolution			12	-	-	12	-	Bits
Integral Linearity Error, INL (End Point)	J		-	-	±2.5	-	±2.5	LSB
	K		-	-	±2.0	-	±2.0	LSB
Differential Linearity Error, DNL	J		-	-	±2.0	-	±2.0	LSB
	K		-	-	±2.0	-	±2.0	LSB
Gain Error, FSE (Adjustable to Zero)	J		-	-	±3.5	-	±3.5	LSB
	K		-	-	±2.5	-	±2.5	LSB
Offset Error, V_{OS} (Adjustable to Zero)	J		-	-	±2.5	-	±2.5	LSB
	K		-	-	±1.5	-	±1.5	LSB
DYNAMIC CHARACTERISTICS								
Signal to Noise Ratio, SINAD = RMS Signal / RMS Noise + Distortion	J	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	68.8 62.1	-	-	-	dB dB
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	71.0 63.6	-	-	-	dB dB
Signal to Noise Ratio, SNR = RMS Signal / RMS Noise	J	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	70.5 63.2	-	-	-	dB dB
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	71.5 65.0	-	-	-	dB dB
Total Harmonic Distortion, THD	J	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	-73.9 -68.4	-	-	-	dBc dBc
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	-80.3 69.7	-	-	-	dBc dBc
Spurious Free Dynamic Range, SFDR	J	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	75.4 69.2	-	-	-	dB dB
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	80.9 70.7	-	-	-	dB dB
ANALOG INPUT								
Input Current, Dynamic		At V_{IN} = V_{REF}+, 0V	-	±125	±150	-	±150	µA

Electrical Specifications $V_{DD} = V_{AA}+ = 5V$, $V_{REF}+ = +4.608V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = External 1.5MHz, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	25°C			-40°C TO 85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
Input Current, Static	Conversion Stopped	-	±0.6	±10	-	±10	µA
Input Bandwidth -3dB		-	1	-	-	-	MHz
Reference Input Current		-	160	-	-	-	µA
Input Series Resistance, R_S	In Series with Input C_{SAMPLE}	-	420	-	-	-	Ω
Input Capacitance, C_{SAMPLE}	During Sample State	-	380	-	-	-	pF
Input Capacitance, C_{HOLD}	During Hold State	-	20	-	-	-	pF
DIGITAL INPUTS $\overline{OEL}$, $\overline{OEM}$, $\overline{STRT}$							
High-Level Input Voltage, V_{IH}		2.4	-	-	2.4	-	V
Low-Level Input Voltage, V_{IL}		-	-	0.8	-	0.8	V
Input Leakage Current, I_{IL}	Except CLK, V_{IN} = 0V, 5V	-	-	±10	-	±10	µA
Input Capacitance, C_{IN}		-	10	-	-	-	pF
DIGITAL OUTPUTS							
High-Level Output Voltage, V_{OH}	I_{SOURCE} = -400µA	4.6	-	-	4.6	-	V
Low-Level Output Voltage, V_{OL}	I_{SINK} = 1.6mA	-	-	0.4	-	0.4	V
Three-State Leakage, I_{OZ}	Except DRDY, V_{OUT} = 0V, 5V	-	-	±10	-	±10	µA
Output Capacitance, C_{OUT}	Except DRDY	-	20	-	-	-	pF
CLOCK							
High-Level Output Voltage, V_{OH}	I_{SOURCE} = -100µA (Note 2)	4	-	-	4	-	V
Low-Level Output Voltage, V_{OL}	I_{SINK} = 100µA (Note 2)	-	-	1	-	1	V
Input Current	CLK Only, V_{IN} = 0V, 5V	-	-	±5	-	±5	mA
TIMING							
Conversion Time (t_{CONV} + t_{ACQ}) (Includes Acquisition Time)		10	-	-	10	-	µs
Clock Frequency	Internal Clock, (CLK = Open)	200	300	400	150	500	kHz
	External CLK (Note 2)	0.05	-	2.0	-	-	MHz
Clock Pulse Width, t_{LOW}, t_{HIGH}	External CLK (Note 2)	100	-	-	100	-	ns
Aperture Delay, t_DAPR	(Note 2)	-	35	50	-	70	ns
Clock to Data Ready Delay, t_{D1}DRDY	(Note 2)	-	105	150	-	180	ns
Clock to Data Ready Delay, t_{D2}DRDY	(Note 2)	-	100	160	-	195	ns
Start Removal Time, $t_R\overline{STRT}$	(Note 2)	75	30	-	75	-	ns
Start Setup Time, $t_{SU}\overline{STRT}$	(Note 2)	85	60	-	100	-	ns
Start Pulse Width, $t_W\overline{STRT}$	(Note 2)	10	4	-	15	-	ns
Start to Data Ready Delay, t_{D3} DRDY	(Note 2)	-	65	105	-	120	ns
Clock Delay from Start, $t_D\overline{STRT}$	(Note 2)	-	60	-	-	-	ns
Output Enable Delay, t_{EN}	(Note 2)	-	20	30	-	50	ns
Output Disabled Delay, t_{DIS}	(Note 2)	-	80	95	-	120	ns
POWER SUPPLY CHARACTERISTICS							
Supply Current, I_{DD} + I_{AA}		-	2.6	8	-	8.5	mA

NOTE:

2. Parameter guaranteed by design or characterization, not production tested.

Timing Diagrams

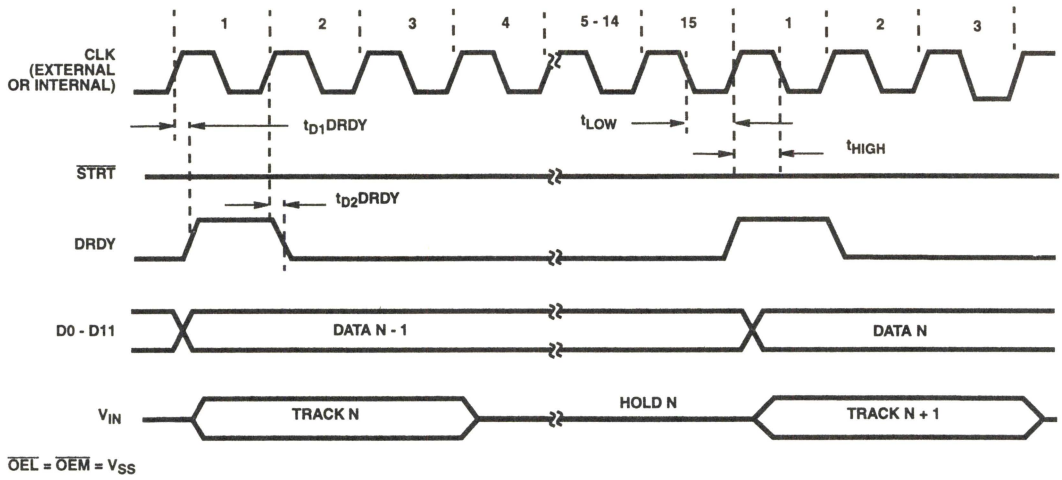


FIGURE 1. CONTINUOUS CONVERSION MODE

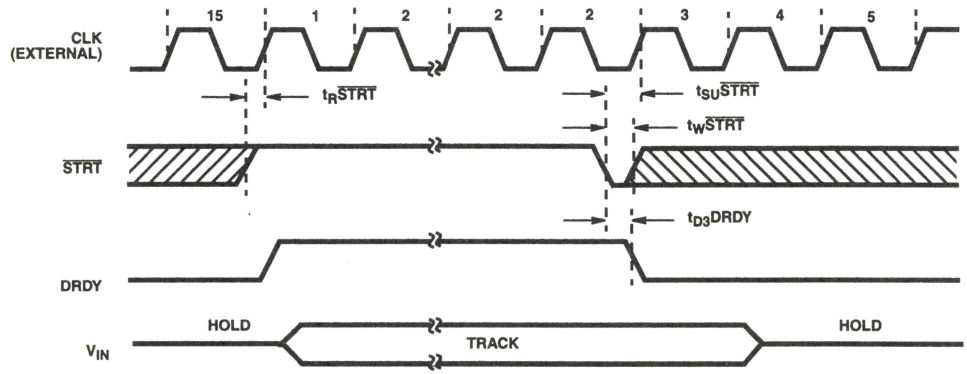


FIGURE 2. SINGLE SHOT MODE EXTERNAL CLOCK

Timing Diagrams (Continued)

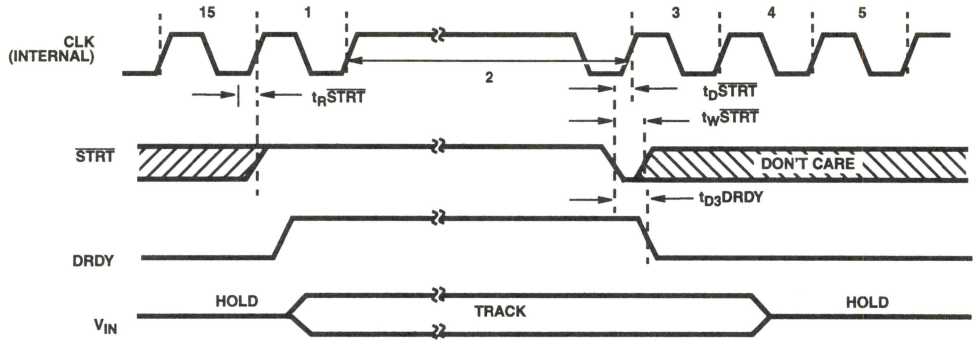


FIGURE 3. SINGLE SHOT MODE INTERNAL CLOCK

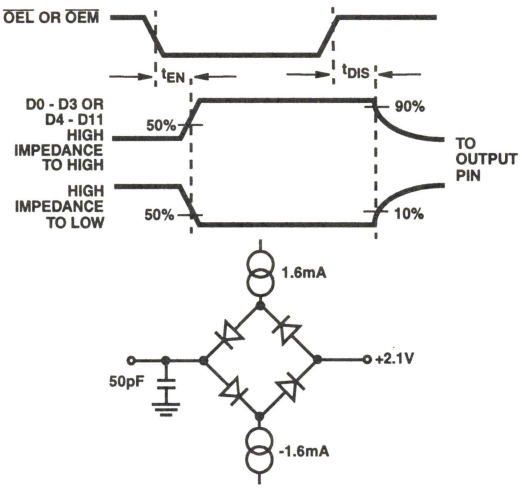


FIGURE 4. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

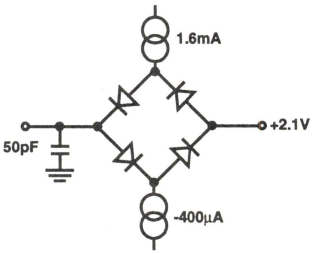


FIGURE 5. TIMING LOAD CIRCUIT

Typical Performance Curves

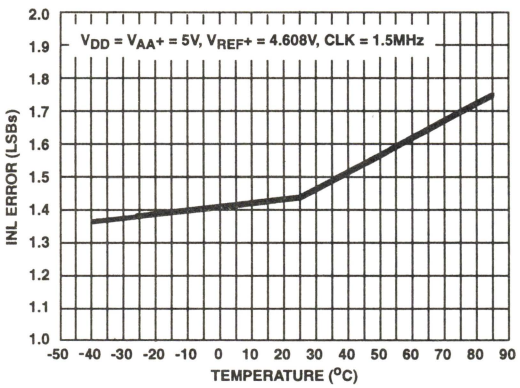


FIGURE 6. NL vs TEMPERATUREI

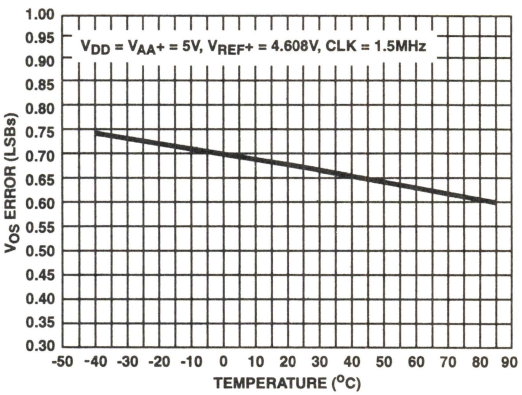


FIGURE 7. OFFSET ERROR vs TEMPERATURE

Typical Performance Curves (Continued)

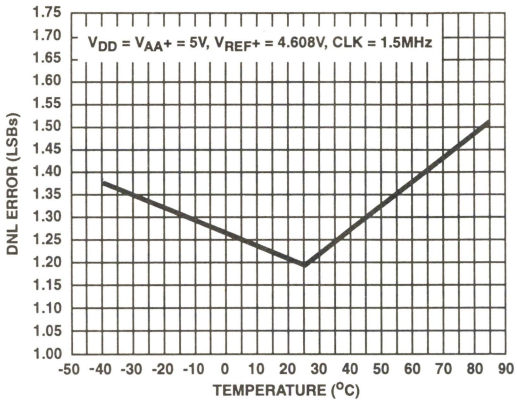


FIGURE 8. DNL vs TEMPERATURE

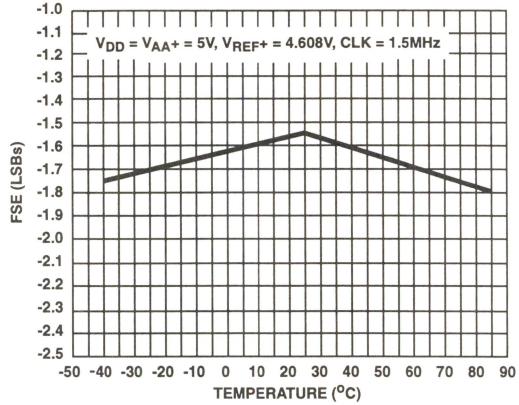


FIGURE 9. FULL SCALE ERROR vs TEMPERATURE

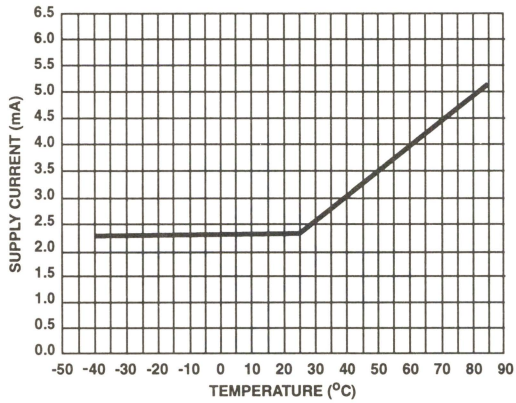


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

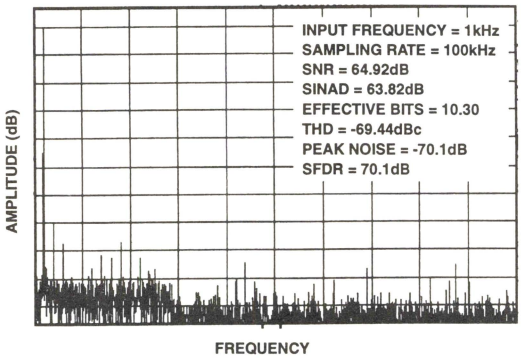


FIGURE 11. FFT SPECTRUM

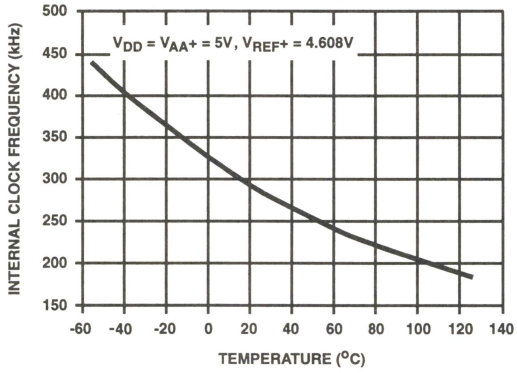


FIGURE 12. INTERNAL CLOCK FREQUENCY vs TEMPERATURE

TABLE 1. PIN DESCRIPTIONS

PIN NO.	NAME	DESCRIPTION
1	DRDY	Output flag signifying new data is available. Goes high at end of clock period 15. Goes low when new conversion is started.
2	D0	Bit-0 (Least Significant Bit, LSB).
3	D1	Bit 1.
4	D2	Bit 2.
5	D3	Bit 3.
6	D4	Bit 4.
7	D5	Bit 5.
8	D6	Bit 6.
9	D7	Bit 7.
10	D8	Bit 8.
11	D9	Bit 9.
12	V_{SS}	Digital Ground, (0V).
13	D10	Bit 10.
14	D11	Bit 11 (Most Significant Bit, MSB)
15	$\overline{OEM}$	Three-State Enable for D4-D11. Active low input.
16	V_{AA}-	Analog Ground, (0V).
17	V_{AA}+	Analog Positive Supply. (+5V) (See text.)
18	V_{IN}	Analog Input.
19	V_{REF}+	Reference Voltage Positive Input, sets 4095 code end of input range.
20	V_{REF}-	Reference Voltage Negative Input, sets 0 code end of input range.
21	$\overline{STRT}$	Start Conversion Input active low, recognized after end of clock period 15.
22	CLK	CLK Input or Output. Conversion functions are synchronized to positive going edge (see text).
23	$\overline{OEL}$	Three-State Enable for D0 D3. Active low input.
24	V_{DD}	Digital Positive Supply (+5V).

Theory of Operation

The HI5810 is a CMOS 12-bit, Analog-to-Digital Converter that uses capacitor charge balancing to successively approximate the analog input. A binarily weighted capacitor network forms the A/D heart of the device. See the block diagram for the HI5810.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, V_{REF}+ or V_{REF}-.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input and the comparator is being auto balanced at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input; the one representing the MSB (D11) is connected to the V_{REF}+ terminal; and the remaining capacitors to V_{REF}-. The capacitor common node, after the charges balance out, will indicate whether the input was above $^1/_2$ of (V_{REF}+ - V_{REF}-). At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to V_{REF}+ (if the comparator was high) or returned to V_{REF}-. This allows the next comparison to be at either $^3/_4$ or $^1/_4$ of (V_{REF}+ - V_{REF}-).

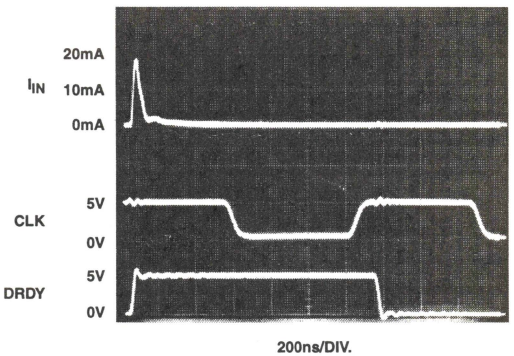
At the end of periods 5 through 14, capacitors representing D10 through D1 are tested, the result stored, and each capacitor either left at V_{REF}+ or at V_{REF}-.

At the end of the 15th period, when the LSB (D0) capacitor is tested, (D0) and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data ready output goes active. The conversion cycle is now complete.

Analog Input

The analog input pin is a predominately capacitive load that changes between the track and hold periods of the conversion cycle. During hold, clock period 4 through 15, the input loading is leakage and stray capacitance, typically less than 5µA and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the current spike by the end of the tracking period as shown in Figure 13. The amount of charge is dependent on supply and input voltages. The average current is also proportional to clock frequency.



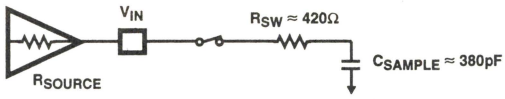
CONDITIONS: V_{DD} = V_{AA}+ = 5.0V, V_{REF}+ = 4.608V, V_{IN} = 4.608V, CLK = 750kHz, T_A = 25°C

FIGURE 13. TYPICAL ANALOG INPUT CURRENT

As long as these current spikes settle completely by end of the signal acquisition period, converter accuracy will be preserved. The analog input is tracked for 3 clock cycles. With an external clock of 1.5MHz the track period is 2µs.

A simplified analog input model is presented in Figure 14. During tracking, the A/D input (V_{IN}) typically appears as a 380pF capacitor being charged through a 420Ω internal switch resistance. The time constant is 160ns. To charge this capacitor from an external "zero Ω" source to 0.5 LSB (1/8192), the charging time must be at least 9 time constants or 1.4µs. The maximum source impedance (R_{SOURCE} Max) for a 2µs acquisition time settling to within 0.5 LSB is 164Ω.

If the clock frequency was slower, or the converter was not restarted immediately (causing a longer sample time), a higher source impedance could be tolerated.



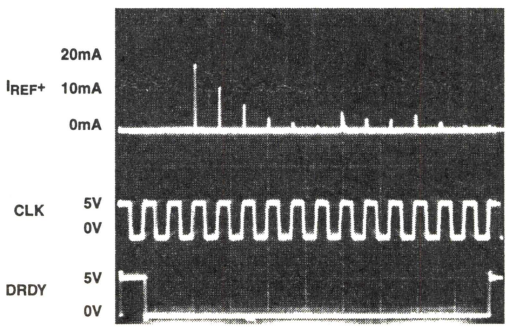
$$R_{SOURCE\ (MAX)} = \frac{-t_{ACQ}}{C_{SAMPLE} \ln [2^{-(N+1)}]} - R_{SW}$$

FIGURE 14. ANALOG INPUT MODEL IN TRACK MODE

Reference Input

The reference input $V_{REF}+$ should be driven from a low impedance source and be well decoupled.

As shown in Figure 15, current spikes are generated on the reference pin during each bit test of the successive approximation part of the conversion cycle as the charge balancing capacitors are switched between $V_{REF}-$ and $V_{REF}+$ (clock periods 5 - 14). These current spikes must settle completely during each bit test of the conversion to not degrade the accuracy of the converter. Therefore $V_{REF}+$ and $V_{REF}-$ should be well bypassed. Reference input $V_{REF}-$ is normally connected directly to the analog ground plane. If $V_{REF}-$ is biased for nulling the converters offset it must be stable during the conversion cycle.



CONDITIONS: $V_{DD} = V_{AA}+ = 5.0V$, $V_{REF}+ = 4.608V$, $V_{IN} = 2.3V$, CLK = 750kHz, $T_A = 25^oC$

FIGURE 15. TYPICAL REFERENCE INPUT CURRENT

The HI5810 is specified with a 4.608V reference, however, it will operate with a reference down to 3V having a slight degradation in performance.

Full Scale and Offset Adjustment

In many applications the accuracy of the HI5810 would be sufficient without any adjustments. In applications where accuracy is of utmost importance full scale and offset errors may be adjusted to zero.

The $V_{REF}+$ and $V_{REF}-$ pins reference the two ends of the analog input range and may be used for offset and full scale adjustments. In a typical system the $V_{REF}-$ might be returned to a clean ground, and the offset adjustment done on an input amplifier. $V_{REF}+$ would then be adjusted to null out the full scale error. When this is not possible, the $V_{REF}-$ input can be adjusted to null the offset error, however, $V_{REF}-$ must be well decoupled.

Full scale and offset error can also be adjusted to zero in the signal conditioning amplifier driving the analog input (V_{IN}).

Control Signal

The HI5810 may be synchronized from an external source by using the $\overline{STRT}$ (Start Conversion) input to initiate conversion, or if $\overline{STRT}$ is tied low, may be allowed to free run. Each conversion cycle takes 15 clock periods.

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by t_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by t_{D1}DRDY) after the start of clock period 1, and returns low (specified by t_{D2}DRDY) after the start of clock period 2.

The 12 data bits are available in parallel on three-state bus driver outputs. When low, the $\overline{OEM}$ input enables the most significant byte (D4 through D11) while the $\overline{OEL}$ input enables the four least significant bits (D0 - D3). t_{EN} and t_{DIS} specify the output enable and disable times.

If the output data is to be latched externally, either the trailing edge of data ready or the next falling edge of the clock after data ready goes high can be used.

When $\overline{STRT}$ input is used to initiate conversions, operation is slightly different depending on whether an internal or external clock is used.

Figure 3 illustrates operation with an internal clock. If the $\overline{STRT}$ signal is removed (at least $t_R\overline{STRT}$) before clock period 1, and is not reapplied during that period, the clock will shut off after entering period 2. The input will continue to track and the DRDY output will remain high during this time.

A low signal applied to $\overline{STRT}$ (at least $t_W\overline{STRT}$ wide) can now initiate a new conversion. The $\overline{STRT}$ signal (after a delay of ($t_D\overline{STRT}$)) causes the clock to restart.

Depending on how long the clock was shut off, the low portion of clock period 2 may be longer than during the remaining cycles.

The input will continue to track until the end of period 3, the same as when free running.

Figure 2 illustrates the same operation as above but with an external clock. If $\overline{STRT}$ is removed (at least $t_R\overline{STRT}$) before clock period 2, a low signal applied to $\overline{STRT}$ will drop the DRDY flag as before, and with the first positive going clock edge that meets the ($t_{SU}\overline{STRT}$) setup time, the converter will continue with clock period 3.

Clock

The HI5810 can operate either from its internal clock or from one externally supplied. The CLK pin functions either as the clock output or input. All converter functions are synchronized with the rising edge of the clock signal.

Figure 16 shows the configuration of the internal clock. The clock output drive is low power: if used as an output, it should not have more than 1 CMOS gate load applied, and stray wiring capacitance should be kept to a minimum.

The internal clock will shut down if the A/D is not restarted after a conversion. The clock could also be shut down with an open collector driver applied to the CLK pin. This should only be done during the sample portion (the first three clock periods) of a conversion cycle, and might be useful for using the device as a digital sample and hold.

If an external clock is supplied to the CLK pin, it must have sufficient drive to overcome the internal clock source. The external clock can be shut off, but again, only during the sample portion of a conversion cycle. At other times, it must be above the minium frequency shown in the specifications. In the above two cases, a further restriction applies in that the clock should not be shut off during the third sample period for more than 1ms. This might cause an internal charge pump voltage to decay.

If the internal or external clock was shut off during the conversion time (clock cycles 4 through 15) of the A/D, the output might be invalid due to balancing capacitor droop.

An external clock must also meet the minimum t_{LOW} and t_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

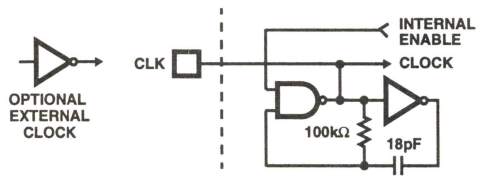


FIGURE 16. INTERNAL CLOCK CIRCUITRY

Power Supplies and Grounding

V_{DD} and V_{SS} are the digital supply pins: they power all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for $V_{AA}+$, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}. Input transients above V_{DD} or below V_{SS} will get steered to the digital supplies.

The $V_{AA}+$ and $V_{AA}-$ terminals supply the charge balancing comparator only. Because the comparator is autobalanced between conversions, it has good low frequency supply rejection. It does not reject well at high frequencies however; $V_{AA}-$ should be returned to a clean analog ground and $V_{AA}+$ should be RC decoupled from the digital supply as shown in Figure 17.

There is approximately 50Ω of substrate impedance between V_{DD} and $V_{AA}+$. This can be used, for example, as part of a low pass RC filter to attenuate switching supply noise. A 10µF capacitor from $V_{AA}+$ to ground would attenuate 30kHz noise by approximately 40dB. Note that back-to-back diodes should be placed from V_{DD} to $V_{AA}+$ to handle supply to capacitor turn-on or turn-off current spikes.

Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the A/D. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is than transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See Typical Performance Characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured RMS signal to RMS sum of noise at a specified input and sampling frequency. The noise is the RMS sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76)dB. For an ideal 12-bit converter the SNR is 74dB. Differential and integral linearity errors will degrade SNR.

$$SNR = 10 \text{ Log} \frac{\text{Sinewave Signal Power}}{\text{Total Noise Power}}$$

Signal-To-Noise + Distortion Ratio

SINAD is the measured RMS signal to RMS sum of noise plus harmonic power and is expressed by the following.

$$SINAD = 10 \text{ Log} \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (2nd - 6th)}}$$

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data;

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of the second through sixth harmonic components to the fundamental RMS signal for a specified input and sampling frequency.

$$THD = 10Log\frac{\text{Total Harmonic Power (2nd - 6th Harmonic)}}{\text{Sinewave Signal Power}}$$

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

$$SFDR = 10Log\frac{\text{Sinewave Signal Power}}{\text{Highest Spurious Signal Power}}$$

TABLE 2. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE† V_{REF+} = 4.608V V_{REF-} = 0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB											LSB
			D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale (FS)	4.6069	4095	1	1	1	1	1	1	1	1	1	1	1	1
FS - 1 LSB	4.6058	4094	1	1	1	1	1	1	1	1	1	1	1	0
3/4 FS	3.4560	3072	1	1	0	0	0	0	0	0	0	0	0	0
1/2 FS	2.3040	2048	1	0	0	0	0	0	0	0	0	0	0	0
1/4 FS	1.1520	1024	0	1	0	0	0	0	0	0	0	0	0	0
1 LSB	0.001125	1	0	0	0	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0	0	0	0

†The voltages listed above represent the ideal lower transition of each output code shown as a function of the reference voltage.

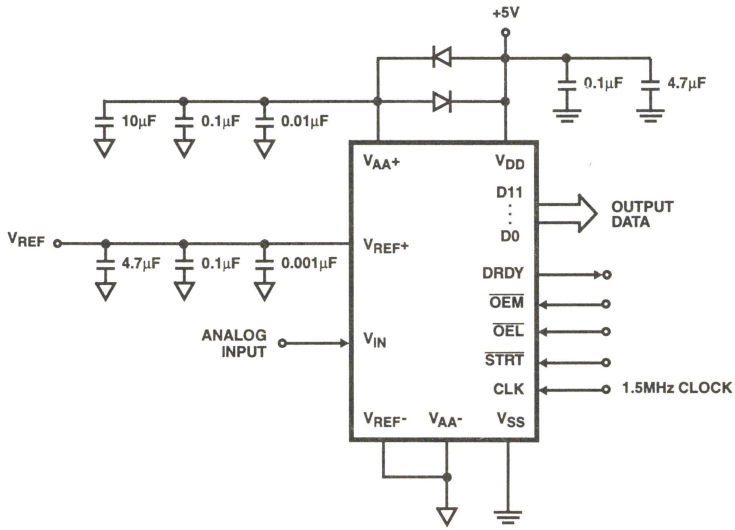


FIGURE 17. GROUND AND SUPPLY DECOUPLING

Die Characteristics

DIE DIMENSIONS:

3200µm x 3940µm

METALLIZATION:

Type: AlSi
Thickness: 11kÅ ±1kÅ

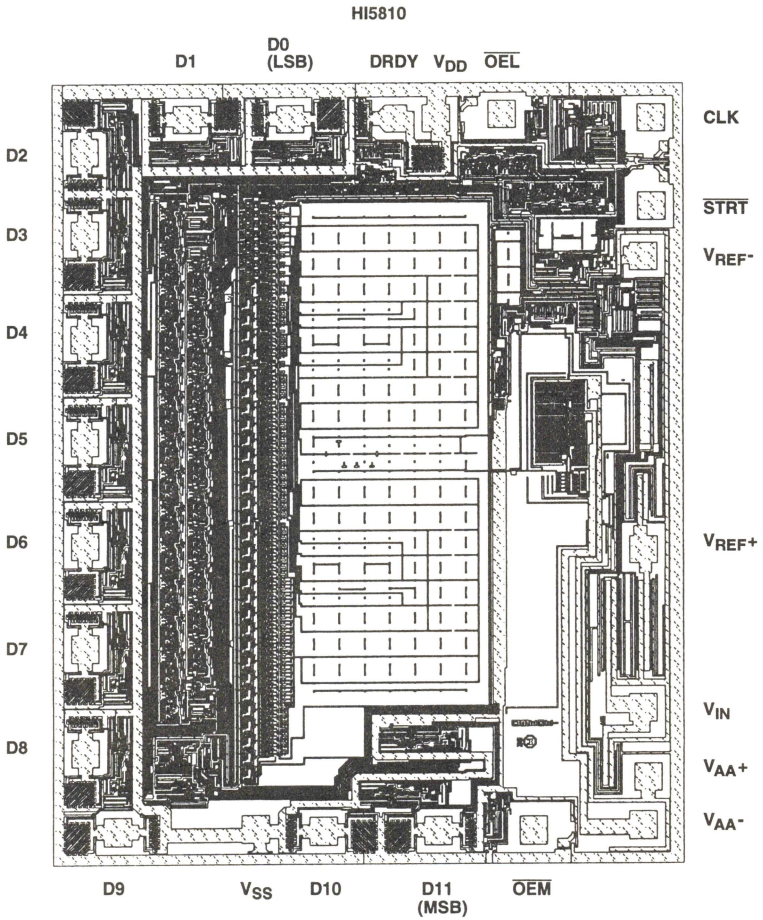
PASSIVATION:

Type: PSG
Thickness: 13kÅ ±2.5kÅ

WORST CASE CURRENT DENSITY:

1.84×10^5 A/cm^2

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HI5812

CMOS 20 Microsecond, 12-Bit, Sampling A/D Converter with Internal Track and Hold

August 1997

Features

- Conversion Time 20µs
- Throughput Rate . . . . . .50 KSPS
- Built-In Track and Hold
- Guaranteed No Missing Codes Over Temperature
- Single Supply Voltage . . . . . +5V
- Maximum Power Consumption. 25mW
- Internal or External Clock

Applications

- Remote Low Power Data Acquisition Systems
- Digital Audio
- DSP Modems
- General Purpose DSP Front End
- µP Controlled Measurement System
- Professional Audio Positioner/Fader

Description

The HI5812 is a fast, low power, 12-bit, successive approximation analog-to-digital converter. It can operate from a single 3V to 6V supply and typically draws just 1.9mA when operating at 5V. The HI5812 features a built-in track and hold. The conversion time is as low as 15µs with a 5V supply.

The twelve data outputs feature full high speed CMOS three-state bus driver capability, and are latched and held through a full conversion cycle. The output is user selectable: (i.e.) 12-bit, 8-bit (MSBs), and/or 4-bit (LSBs). A data ready flag, and conversion-start inputs complete the digital interface.

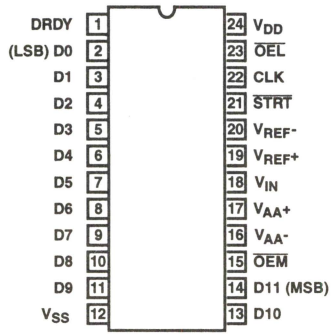
An internal clock is provided and is available as an output. The clock may also be over-driven by an external source.

Ordering Information

PART NUMBER	INL (LSB) (MAX OVER TEMP.)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5812JIP	±1.5	-40 to 85	24 Ld PDIP	E24.3
HI5812KIP	±1.0	-40 to 85	24 Ld PDIP	E24.3
HI5812JIB	±1.5	-40 to 85	24 Ld SOIC	M24.3
HI5812KIB	±1.0	-40 to 85	24 Ld SOIC	M24.3
HI5812JIJ	±1.5	-40 to 85	24 Ld CERDIP	F24.3
HI5812KIJ	±1.0	-40 to 85	24 Ld CERDIP	F24.3

Pinout

HI5812
(PDIP, CERDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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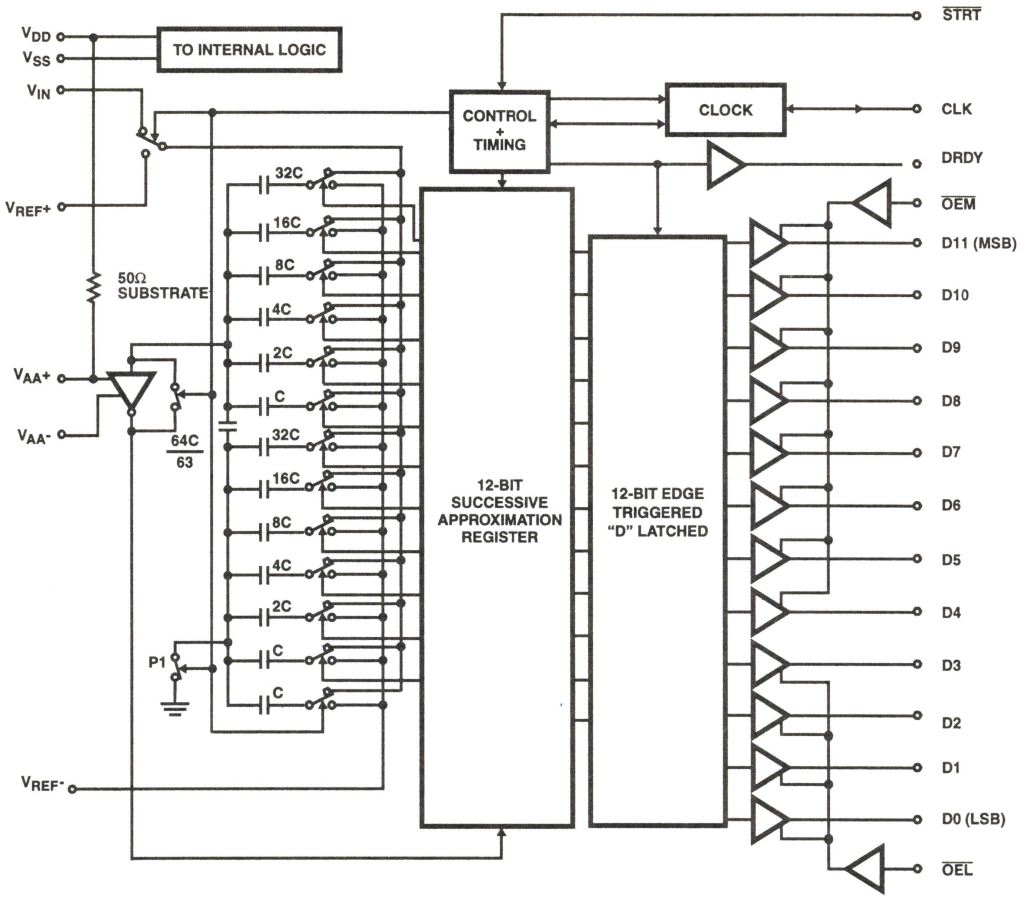
File Number 3214.4

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage
- V_{DD} to V_{SS} ..... $(V_{SS}$ -0.5V) < V_{DD} < +6.5V
- V_{AA}+ to V_{AA}- ..... $(V_{SS}$ -0.5V) to (V_{SS} +6.5V)
- V_{AA}+ to V_{DD} ..... ±0.3V

Analog and Reference Inputs
- V_{IN}, V_{REF}+, V_{REF}- ..... (V_{SS} -0.3V) < V_{INA} < (V_{DD} +0.3V)

Digital I/O Pins ..... (V_{SS} -0.3V) < VI/O < (V_{DD} +0.3V)

Operating Conditions

Temperature Range

PDIP, SOIC, and CERDIP Packages ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	60	12
PDIP Package	80	N/A
SOIC Package	75	N/A

Maximum Junction Temperature
- Plastic Packages ..... 150°C
- Ceramic Package ..... 175°C

Maximum Storage Temperature Range ..... -65°C to 150°C

Maximum Lead Temperature (Soldering, 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{DD} = V_{AA}+ = 5V, V_{REF}+ = +4.608V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = External 750kHz, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	UNITS
ACCURACY								
Resolution			12	-	-	12	-	Bits
Integral Linearity Error, INL (End Point)	J		-	-	±1.5	-	±1.5	LSB
	K		-	-	±1.0	-	±1.0	LSB
Differential Linearity Error, DNL	J		-	-	±2.0	-	±2.0	LSB
	K		-	-	±1.0	-	±1.0	LSB
Gain Error, FSE (Adjustable to Zero)	J		-	-	±3.0	-	±3.0	LSB
	K		-	-	±2.5	-	±2.5	LSB
Offset Error, V_{OS} (Adjustable to Zero)	J		-	-	±2.0	-	±2.0	LSB
	K		-	-	±1.0	-	±1.0	LSB
Power Supply Rejection, PSRR		V_{REF} = 4V						
Offset Error PSRR		V_{DD} = V_{AA}+ = 5V ±5%		0.1	±0.5		±0.5	LSB
Gain Error PSRR		V_{DD} = V_{AA}+ = 5V ±5%		0.1	±0.5		±0.5	LSB
DYNAMIC CHARACTERISTICS								
Signal to Noise Ratio, SINAD = RMS Signal / RMS Noise + Distortion	J	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz	-	68.8 69.2	-	-	-	dB dB
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz	-	71.0 71.5	-	-	-	dB dB
Signal to Noise Ratio, SNR = RMS Signal / RMS Noise	J	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz	-	70.5 71.1	-	-	-	dB dB
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz	-	71.5 72.1	-	-	-	dB dB
Total Harmonic Distortion, THD	J	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz	-	-73.9 -73.8	-	-	-	dBc dBc
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz		-80.3 -79.0	-	-	-	dBc dBc
Spurious Free Dynamic Range, SFDR	J	f_S =Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz	-	-75.4 -75.1	-	-	-	dB dB
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz	-	-80.9 -79.6	-	-	-	dB dB

Electrical Specifications $V_{DD} = V_{AA}+ = 5V$, $V_{REF}+ = +4.608V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = External 750kHz, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	25°C			-40°C TO 85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
ANALOG INPUT							
Input Current, Dynamic	At $V_{IN} = V_{REF}+$, 0V	-	±50	±100	-	±100	µA
Input Current, Static	Conversion Stopped	-	±0.4	±10	-	±10	µA
Input Bandwidth -3dB		-	1	-	-	-	MHz
Reference Input Current		-	160	-	-	-	µA
Input Series Resistance, R_S	In Series with Input C_{SAMPLE}	-	420	-	-	-	Ω
Input Capacitance, C_{SAMPLE}	During Sample State	-	380	-	-	-	pF
Input Capacitance, C_{HOLD}	During Hold State	-	20	-	-	-	pF
DIGITAL INPUTS $\overline{OEL}$, $\overline{OEM}$, $\overline{STRT}$							
High-Level Input Voltage, V_{IH}		2.4	-	-	2.4	-	V
Low-Level Input Voltage, V_{IL}		-	-	0.8	-	0.8	V
Input Leakage Current, I_{IL}	Except CLK, V_{IN} = 0V, 5V	-	-	±10	-	±10	µA
Input Capacitance, C_{IN}		-	10	-	-	-	pF
DIGITAL OUTPUTS							
High-Level Output Voltage, V_{OH}	I_{SOURCE} = -400µA	4.6	-	-	4.6	-	V
Low-Level Output Voltage, V_{OL}	I_{SINK} = 1.6mA	-	-	0.4	-	0.4	V
Three-State Leakage, I_{OZ}	Except DRDY, V_{OUT} = 0V, 5V	-	-	±10	-	±10	µA
Output Capacitance, C_{OUT}	Except DRDY	-	20	-	-	-	pF
CLOCK							
High-Level Output Voltage, V_{OH}	I_{SOURCE} = -100µA (Note 2)	4	-	-	4	-	V
Low-Level Output Voltage, V_{OL}	I_{SINK} = 100µA (Note 2)	-	-	1	-	1	V
Input Current	CLK Only, V_{IN} = 0V, 5V	-	-	±5	-	±5	mA
TIMING							
Conversion Time ($t_{CONV} + t_{ACQ}$) (Includes Acquisition Time)		20	-	-	20	-	µs
Clock Frequency	Internal Clock, (CLK = Open)	200	300	400	150	500	kHz
	External CLK (Note 2)	0.05	2	1.5	0.05	1.5	MHz
Clock Pulse Width, t_{LOW}, t_{HIGH}	External CLK (Note 2)	100	-	-	100	-	ns
Aperture Delay, t_DAPR	(Note 2)	-	35	50	-	70	ns
Clock to Data Ready Delay, t_{D1}DRDY	(Note 2)	-	105	150	-	180	ns
Clock to Data Ready Delay, t_{D2}DRDY	(Note 2)	-	100	160	-	195	ns
Start Removal Time, $t_R\overline{STRT}$	(Note 2)	75	30	-	75	-	ns
Start Setup Time, $t_{SU}\overline{STRT}$	(Note 2)	85	60	-	100	-	ns
Start Pulse Width, $t_W\overline{STRT}$	(Note 2)	10	4	-	15	-	ns
Start to Data Ready Delay, t_{D3} DRDY	(Note 2)	-	65	105	-	120	ns
Clock Delay from Start, $t_D\overline{STRT}$	(Note 2)	-	60	-	-	-	ns
Output Enable Delay, t_{EN}	(Note 2)	-	20	30	-	50	ns
Output Disabled Delay, t_{DIS}	(Note 2)	-	80	95	-	120	ns
POWER SUPPLY CHARACTERISTICS							
Supply Current, $I_{DD} + I_{AA}$		-	1.9	5	-	8	mA

NOTE:

2. Parameter guaranteed by design or characterization, not production tested.

Timing Diagrams

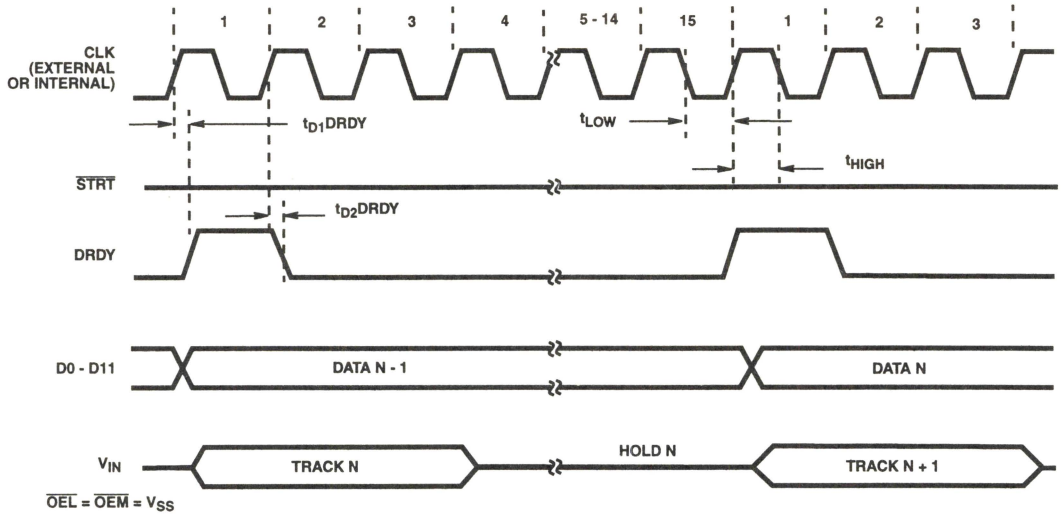


FIGURE 1. CONTINUOUS CONVERSION MODE

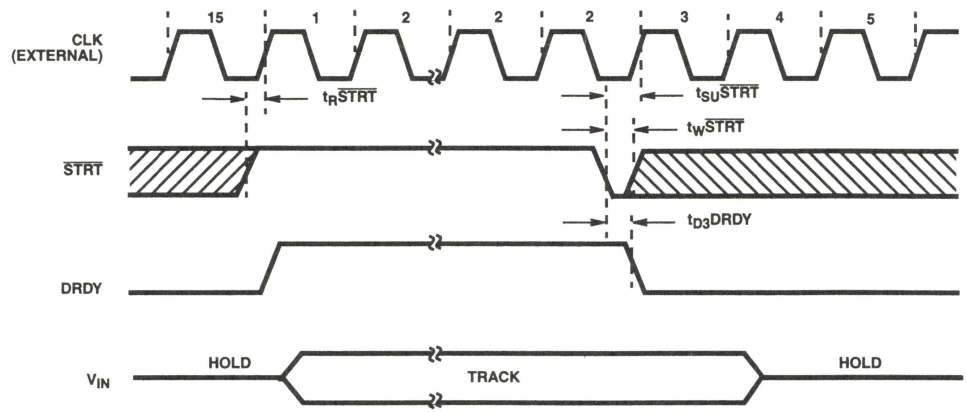


FIGURE 2. SINGLE SHOT MODE EXTERNAL CLOCK

Timing Diagrams (Continued)

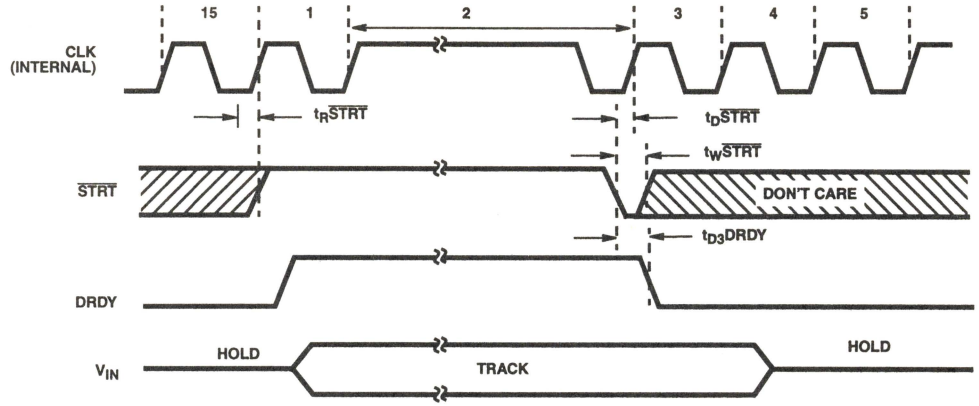


FIGURE 3. SINGLE SHOT MODE INTERNAL CLOCK

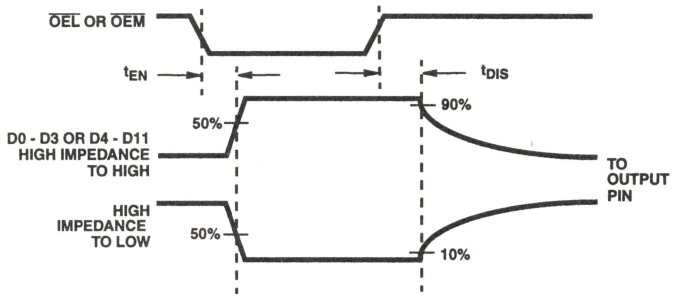


FIGURE 4A.

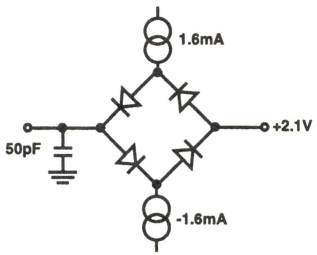


FIGURE 4B.

FIGURE 4. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

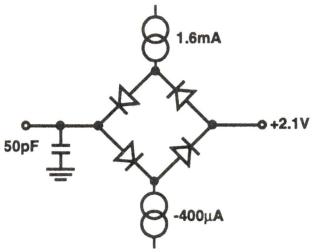


FIGURE 5. GENERAL TIMING LOAD CIRCUIT

Typical Performance Curves

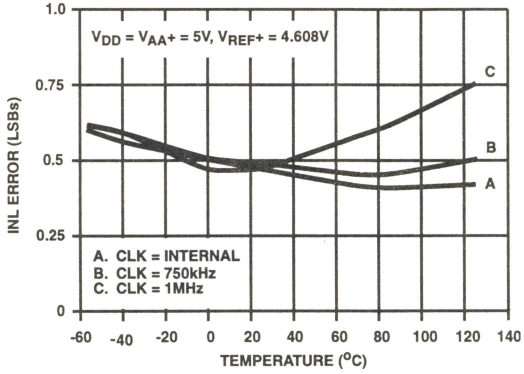


FIGURE 6. INL vs TEMPERATURE

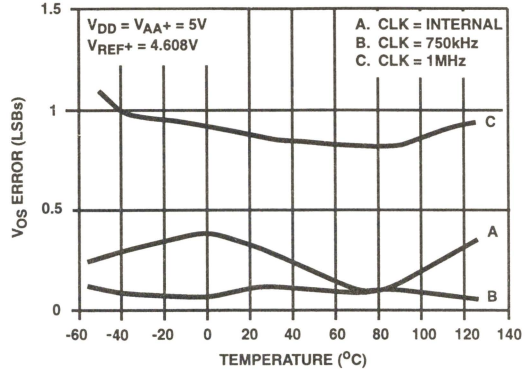


FIGURE 7. OFFSET VOLTAGE vs TEMPERATURE

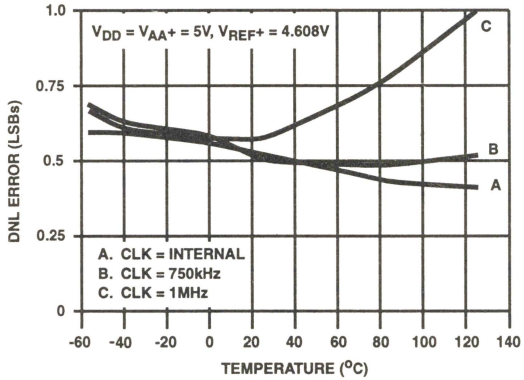


FIGURE 8. DNL vs TEMPERATURE

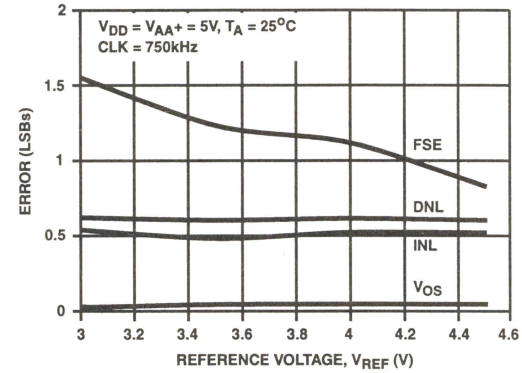


FIGURE 9. ACCURACY vs REFERENCE VOLTAGE

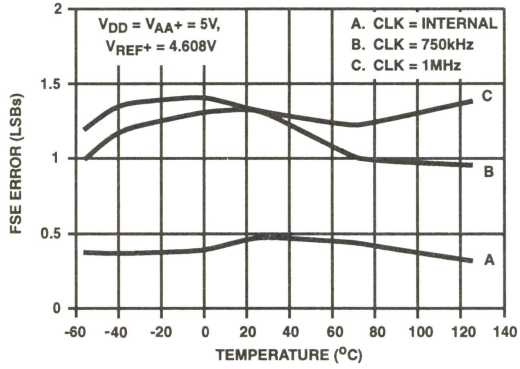


FIGURE 10. FULL SCALE ERROR vs TEMPERATURE

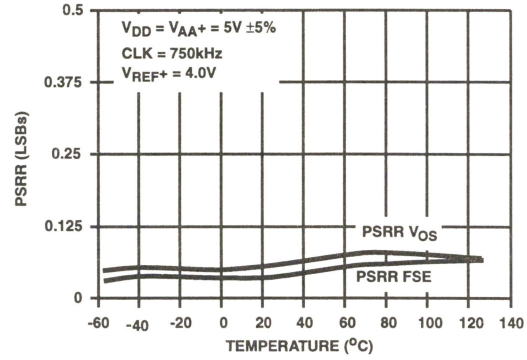


FIGURE 11. POWER SUPPLY REJECTION vs TEMPERATURE

Typical Performance Curves (Continued)

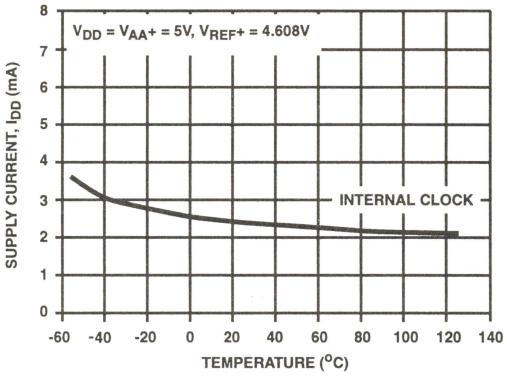


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

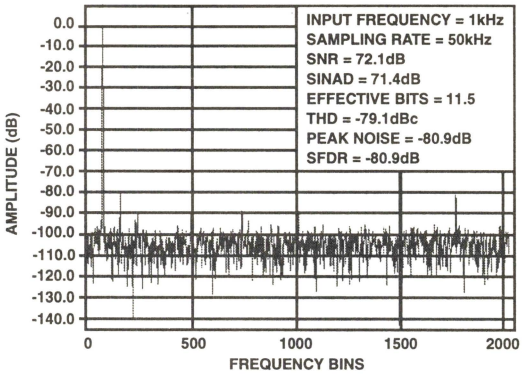


FIGURE 13. FFT SPECTRUM

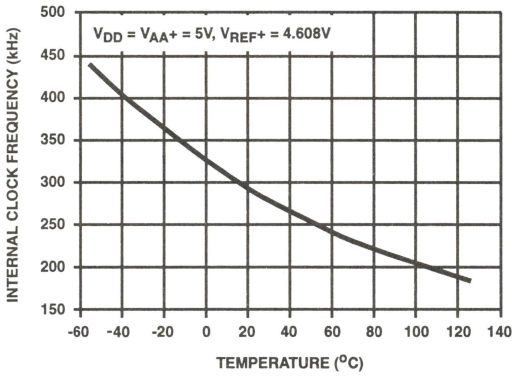


FIGURE 14. INTERNAL CLOCK FREQUENCY vs TEMPERATURE

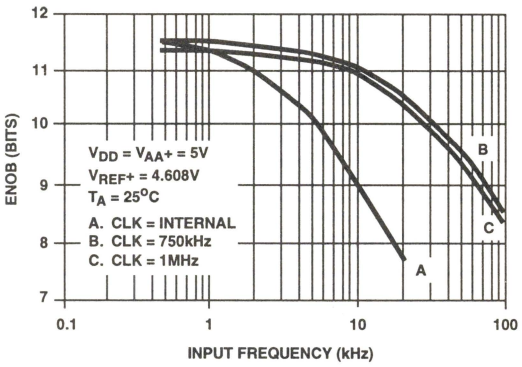


FIGURE 15. EFFECTIVE BITS vs INPUT FREQUENCY

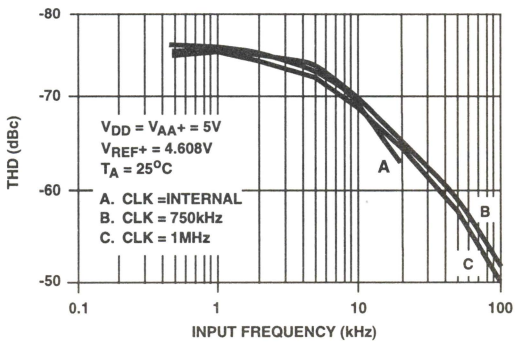


FIGURE 16. TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

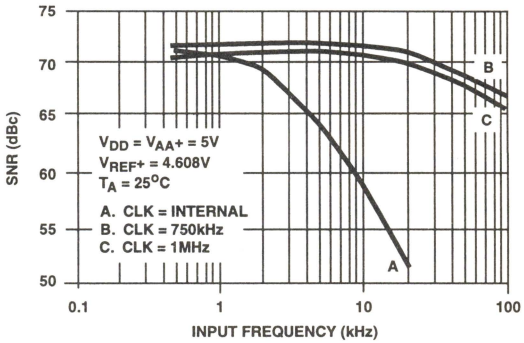


FIGURE 17. SIGNAL NOISE RATIO vs INPUT FREQUENCY

TABLE 1. PIN DESCRIPTIONS

PIN NO.	NAME	DESCRIPTION
1	DRDY	Output flag signifying new data is available. Goes high at end of clock period 15. Goes low when new conversion is started.
2	D0	Bit 0 (Least Significant Bit, LSB).
3	D1	Bit 1.
4	D2	Bit 2.
5	D3	Bit 3.
6	D4	Bit 4.
7	D5	Bit 5.
8	D6	Bit 6.
9	D7	Bit 7.
10	D8	Bit 8.
11	D9	Bit 9.
12	V_{SS}	Digital Ground (0V).
13	D10	Bit 10.
14	D11	Bit 11 (Most Significant Bit, MSB).
15	$\overline{OEM}$	Three-State Enable for D4-D11. Active low input.
16	V_{AA}-	Analog Ground, (0V).
17	V_{AA}+	Analog Positive Supply. (+5V) (See text.)
18	V_{IN}	Analog Input.
19	V_{REF}+	Reference Voltage Positive Input, sets 4095 code end of input range.
20	V_{REF}-	Reference Voltage Negative Input, sets 0 code end of input range.
21	$\overline{STRT}$	Start Conversion Input Active Low, recognized after end of clock period 15.
22	CLK	CLK Input or Output. Conversion functions are synchronized to positive going edge. (See text.)
23	$\overline{OEL}$	Three-State Enable for D0 D3. Active Low Input.
24	V_{DD}	Digital Positive Supply (+5V).

Theory of Operation

HI5812 is a CMOS 12-Bit Analog-to-Digital Converter that uses capacitor-charge balancing to successively approximate the analog input. A binarily weighted capacitor network forms the A/D heart of the device. See the block diagram for the HI5812.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, V_{REF}+ or V_{REF}-.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input and the comparator is being auto-balanced at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input; the one representing the MSB (D11) is connected to the V_{REF}+ terminal; and the remaining capacitors to V_{REF}-. The capacitor-common node, after the charges balance out, will indicate whether the input was above $^1/_2$ of (V_{REF}+ - V_{REF}-). At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to V_{REF}+ (if the comparator was high) or returned to V_{REF}-. This allows the next comparison to be at either $^3/_4$ or $^1/_4$ of (V_{REF}+ - V_{REF}-).

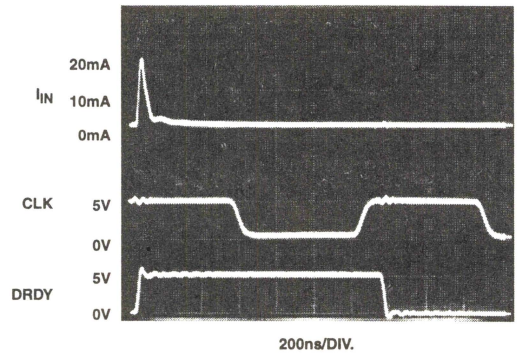
At the end of periods 5 through 14, capacitors representing D10 through D1 are tested, the result stored, and each capacitor either left at V_{REF}+ or at V_{REF}-.

At the end of the 15th period, when the LSB (D0) capacitor is tested, (D0) and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data-ready output goes active. The conversion cycle is now complete.

Analog Input

The analog input pin is a predominately capacitive load that changes between the track and hold periods of the conversion cycle. During hold, clock period 4 through 15, the input loading is leakage and stray capacitance, typically less than 5µA and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the current spike by the end of the tracking period as shown in Figure 18. The amount of charge is dependent on supply and input voltages. The average current is also proportional to clock frequency.



CONDITIONS: V_{DD} = V_{AA}+ = 5.0V, V_{REF}+ = 4.608V, V_{IN} = 4.608V, CLK = 750kHz, T_A = 25°C

FIGURE 18. TYPICAL ANALOG INPUT CURRENT

As long as these current spikes settle completely by end of the signal acquisition period, converter accuracy will be preserved. The analog input is tracked for 3 clock cycles. With an external clock of 750kHz the track period is 4µs.

A simplified analog input model is presented in Figure 19. During tracking, the A/D input (V_{IN}) typically appears as a 380pF capacitor being charged through a 420Ω internal switch resistance. The time constant is 160ns. To charge this capacitor from an external "zero Ω" source to 0.5 LSB (1/8192), the charging time must be at least 9 time constants or 1.4µs. The maximum source impedance (R_{SOURCE} Max) for a 4µs acquisition time settling to within 0.5LSB is 750Ω.

If the clock frequency was slower, or the converter was not restarted immediately (causing a longer sample time), a higher source impedance could be tolerated.

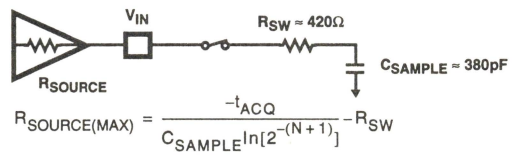
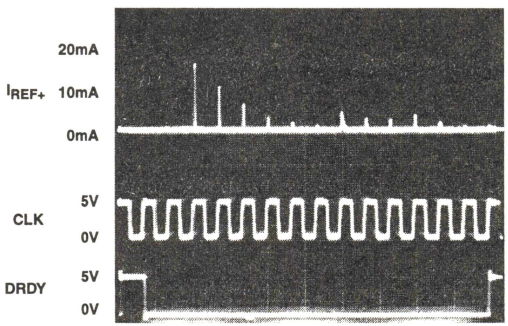


FIGURE 19. ANALOG INPUT MODEL IN TRACK MODE

Reference Input

The reference input $V_{REF}+$ should be driven from a low impedance source and be well decoupled.

As shown in Figure 20, current spikes are generated on the reference pin during each bit test of the successive approximation part of the conversion cycle as the charge-balancing capacitors are switched between $V_{REF}-$ and $V_{REF}+$ (clock periods 5 - 14). These current spikes must settle completely during each bit test of the conversion to not degrade the accuracy of the converter. Therefore $V_{REF}+$ and $V_{REF}-$ should be well bypassed. Reference input $V_{REF}-$ is normally connected directly to the analog ground plane. If $V_{REF}-$ is biased for nulling the converters offset it must be stable during the conversion cycle.



CONDITIONS: $V_{DD} = V_{AA}+ = 5.0V$, $V_{REF}+ = 4.608V$, $V_{IN} = 2.3V$, CLK = 750kHz, $T_A = 25^oC$

FIGURE 20. TYPICAL REFERENCE INPUT CURRENT

The HI5812 is specified with a 4.608V reference, however, it will operate with a reference down to 3V having a slight degradation in performance. A typical graph of accuracy vs reference voltage is presented.

Full Scale and Offset Adjustment

In many applications the accuracy of the HI5812 would be sufficient without any adjustments. In applications where accuracy is of utmost importance full scale and offset errors may be adjusted to zero.

The $V_{REF}+$ and $V_{REF}-$ pins reference the two ends of the analog input range and may be used for offset and full scale adjustments. In a typical system the $V_{REF}-$ might be returned to a clean ground, and the offset adjustment done on an input amplifier. $V_{REF}+$ would then be adjusted to null out the full scale error. When this is not possible, the $V_{REF}-$ input can be adjusted to null the offset error, however, $V_{REF}-$ must be well decoupled.

Full scale and offset error can also be adjusted to zero in the signal conditioning amplifier driving the analog input (V_{IN}).

Control Signal

The HI5812 may be synchronized from an external source by using the $\overline{STRT}$ (Start Conversion) input to initiate conversion, or if $\overline{STRT}$ is tied low, may be allowed to free run. Each conversion cycle takes 15 clock periods.

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by t_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by t_{D1}DRDY) after the start of clock period 1, and returns low (specified by t_{D2}DRDY) after the start of clock period 2.

The 12 data bits are available in parallel on three-state bus driver outputs. When low, the $\overline{OEM}$ input enables the most significant byte (D4 through D11) while the $\overline{OEL}$ input enables the four least significant bits (D0 - D3). t_{EN} and t_{DIS} specify the output enable and disable times.

If the output data is to be latched externally, either the trailing edge of data ready or the next falling edge of the clock after data ready goes high can be used.

When $\overline{STRT}$ input is used to initiate conversions, operation is slightly different depending on whether an internal or external clock is used.

Figure 3 illustrates operation with an internal clock. If the $\overline{STRT}$ signal is removed (at least $t_R\overline{STRT}$) before clock period 1, and is not reapplied during that period, the clock will shut off after entering period 2. The input will continue to track and the DRDY output will remain high during this time.

A low signal applied to $\overline{STRT}$ (at least $t_W\overline{STRT}$ wide) can now initiate a new conversion. The $\overline{STRT}$ signal (after a delay of ($t_D\overline{STRT}$)) causes the clock to restart.

Depending on how long the clock was shut off, the low portion of clock period 2 may be longer than during the remaining cycles.

The input will continue to track until the end of period 3, the same as when free running.

Figure 2 illustrates the same operation as above but with an external clock. If $\overline{STRT}$ is removed (at least $t_R\overline{STRT}$) before clock period 2, a low signal applied to $\overline{STRT}$ will drop the DRDY flag as before, and with the first positive-going clock edge that meets the ($t_{SU}\overline{STRT}$) setup time, the converter will continue with clock period 3.

Clock

The HI5812 can operate either from its internal clock or from one externally supplied. The CLK pin functions either as the clock output or input. All converter functions are synchronized with the rising edge of the clock signal.

Figure 21 shows the configuration of the internal clock. The clock output drive is low power: if used as an output, it should not have more than 1 CMOS gate load applied, and stray wiring capacitance should be kept to a minimum.

The internal clock will shut down if the A/D is not restarted after a conversion. The clock could also be shut down with an open collector driver applied to the CLK pin. This should only be done during the sample portion (the first three clock periods) of a conversion cycle, and might be useful for using the device as a digital sample and hold.

If an external clock is supplied to the CLK pin, it must have sufficient drive to overcome the internal clock source. The external clock can be shut off, but again, only during the sample portion of a conversion cycle. At other times, it must be above the minium frequency shown in the specifications. In the above two cases, a further restriction applies in that the clock should not be shut off during the third sample period for more than 1ms. This might cause an internal charge-pump voltage to decay.

If the internal or external clock was shut off during the conversion time (clock cycles 4 through 15) of the A/D, the output might be invalid due to balancing capacitor droop.

An external clock must also meet the minimum t_{LOW} and t_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

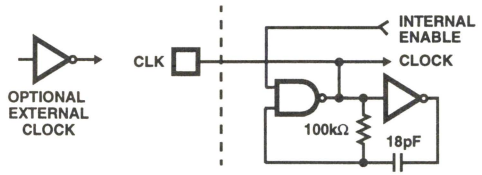


FIGURE 21. INTERNAL CLOCK CIRCUITRY

Power Supplies and Grounding

V_{DD} and V_{SS} are the digital supply pins: they power all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for $V_{AA}+$, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}. Input transients above V_{DD} or below V_{SS} will get steered to the digital supplies.

The $V_{AA}+$ and $V_{AA}-$ terminals supply the charge-balancing comparator only. Because the comparator is autobalanced between conversions, it has good low-frequency supply rejection. It does not reject well at high frequencies however; $V_{AA}-$ should be returned to a clean analog ground and $V_{AA}+$ should be RC decoupled from the digital supply as shown in Figure 22.

There is approximately 50Ω of substrate impedance between V_{DD} and $V_{AA}+$. This can be used, for example, as part of a low-pass RC filter to attenuate switching supply noise. A 10µF capacitor from $V_{AA}+$ to ground would attenuate 30kHz noise by approximately 40dB. Note that back-to-back diodes should be placed from V_{DD} to $V_{AA}+$ to handle supply to capacitor turn-on or turn-off current spikes.

Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the A/D. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is than transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See typical performance characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured RMS signal to RMS sum of noise at a specified input and sampling frequency. The noise is the RMS sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76) dB. For an ideal 12-bit converter the SNR is 74dB. Differential and integral linearity errors will degrade SNR.

$$SNR = 10\ Log \frac{\text{Sinewave Signal Power}}{\text{Total Noise Power}}$$

Signal-To-Noise + Distortion Ratio

SINAD is the measured RMS signal to RMS sum of noise plus harmonic power and is expressed by the following:

$$SINAD = 10\ Log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (2nd - 6th)}}$$

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data;

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of the second through sixth harmonic components to the fundamental RMS signal for a specified input and sampling frequency.

$$THD = 10 \text{ Log} \frac{\text{Total Harmonic Power (2nd - 6th Harmonic)}}{\text{Sinewave Signal Power}}$$

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

$$SFDR = 10 \text{ Log} \frac{\text{Sinewave Signal Power}}{\text{Highest Spurious Signal Power}}$$

TABLE 2. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE† V_{REF+} = 4.608V V_{REF-} = 0.0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB											LSB
			D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale (FS)	4.6069	4095	1	1	1	1	1	1	1	1	1	1	1	1
FS - 1 LSB	4.6058	4094	1	1	1	1	1	1	1	1	1	1	1	0
3/4 FS	3.4560	3072	1	1	0	0	0	0	0	0	0	0	0	0
1/2 FS	2.3040	2048	1	0	0	0	0	0	0	0	0	0	0	0
1/4 FS	1.1520	1024	0	1	0	0	0	0	0	0	0	0	0	0
1 LSB	0.001125	1	0	0	0	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0	0	0	0

†The voltages listed above represent the ideal lower transition of each output code shown as a function of the reference voltage.

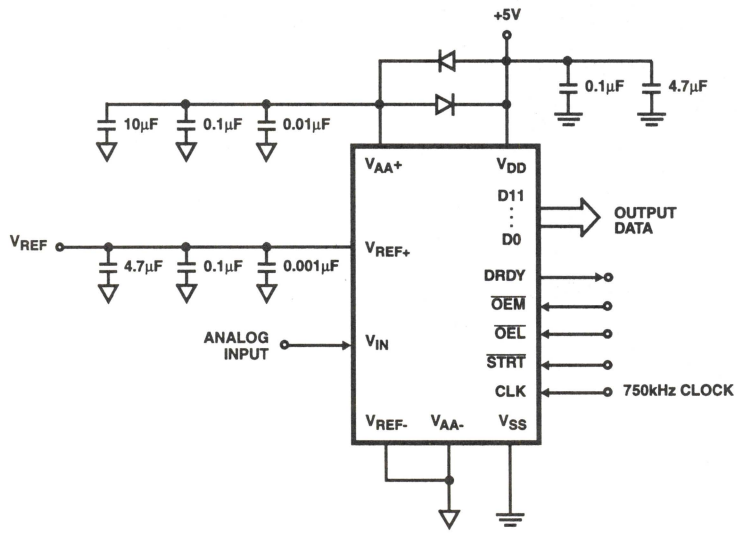


FIGURE 22. GROUND AND SUPPLY DECOUPLING

Die Characteristics

DIE DIMENSIONS:

3200µm x 3940µm

METALLIZATION:

Type: AlSi
Thickness: 11kÅ ±1kÅ

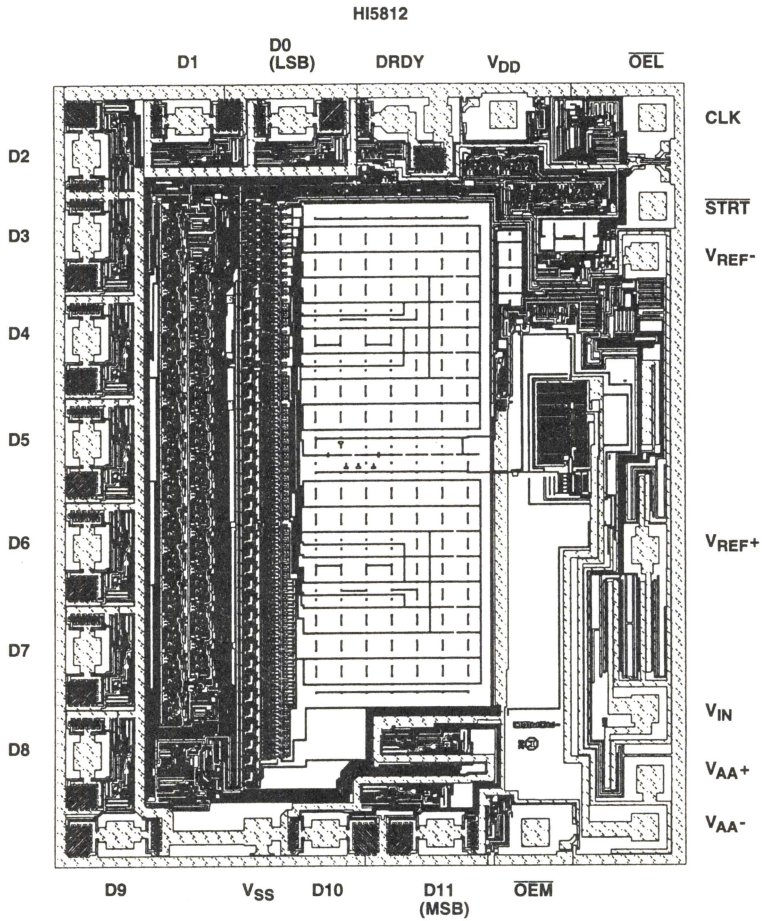
PASSIVATION:

Type: PSG
Thickness: 13kÅ ±2.5kÅ

WORST CASE CURRENT DENSITY:

1.84×10^5 A/cm^2

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HI5813

CMOS 3.3V, 25 Microsecond, 12-Bit, Sampling A/D Converter with Internal Track and Hold

August 1997

Features

- Conversion Time 25µs
- Throughput Rate . . . . . 40 KSPS
- Built-In Track and Hold
- Single Supply Voltage . . . . . +3.3V
- Maximum Power Consumption at 25°C. 3.3mW

Applications

- Remote Low Power Data Acquisition Systems
- Battery Operated Systems
- Pen Based PC Handheld Scanners
- DSP Modems
- General Purpose DSP Front End
- µP Controlled Measurement Systems
- PCMCIA Type II Compliant
- PC Based Industrial Controls/DAQ Systems

Description

The HI5813 is a 3.3V, very low power, 12-bit, successive approximation analog-to-digital converter. It can operate from a single 3V to 6V supply and typically draws a maximum of 1.0mA (at 25°C) when operating at 3.3V. The HI5813 features a built-in track and hold. The conversion time is as low as 25µs with a 3.3V supply.

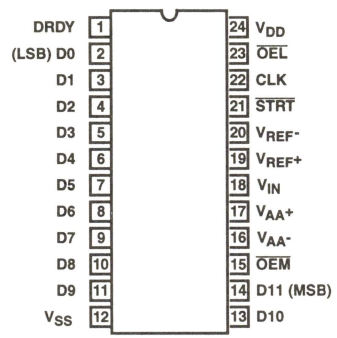
The twelve data outputs feature full high speed CMOS three-state bus driver capability, and are latched and held through a full conversion cycle. The output is user selectable: (i.e.) 12-bit , 8-bit (MSBs), and/or 4-bit (LSBs). A data ready flag and conversion start input complete the digital interface.

Ordering Information

PART NUMBER	INL (LSB) (MAX OVER TEMP.)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5813JIP	±4.0	-40 to 85	24 Ld PDIP	E24.3
HI5813KIP	±2.5	-40 to 85	24 Ld PDIP	E24.3
HI5813JIB	±4.0	-40 to 85	24 Ld SOIC	M24.3
HI5813KIB	±2.5	-40 to 85	24 Ld SOIC	M24.3
HI5813JIJ	±4.0	-40 to 85	24 Ld CERDIP	F24.3
HI5813KIJ	±2.5	-40 to 85	24 Ld CERDIP	F24.3

Pinout

HI5813 (PDIP, CERDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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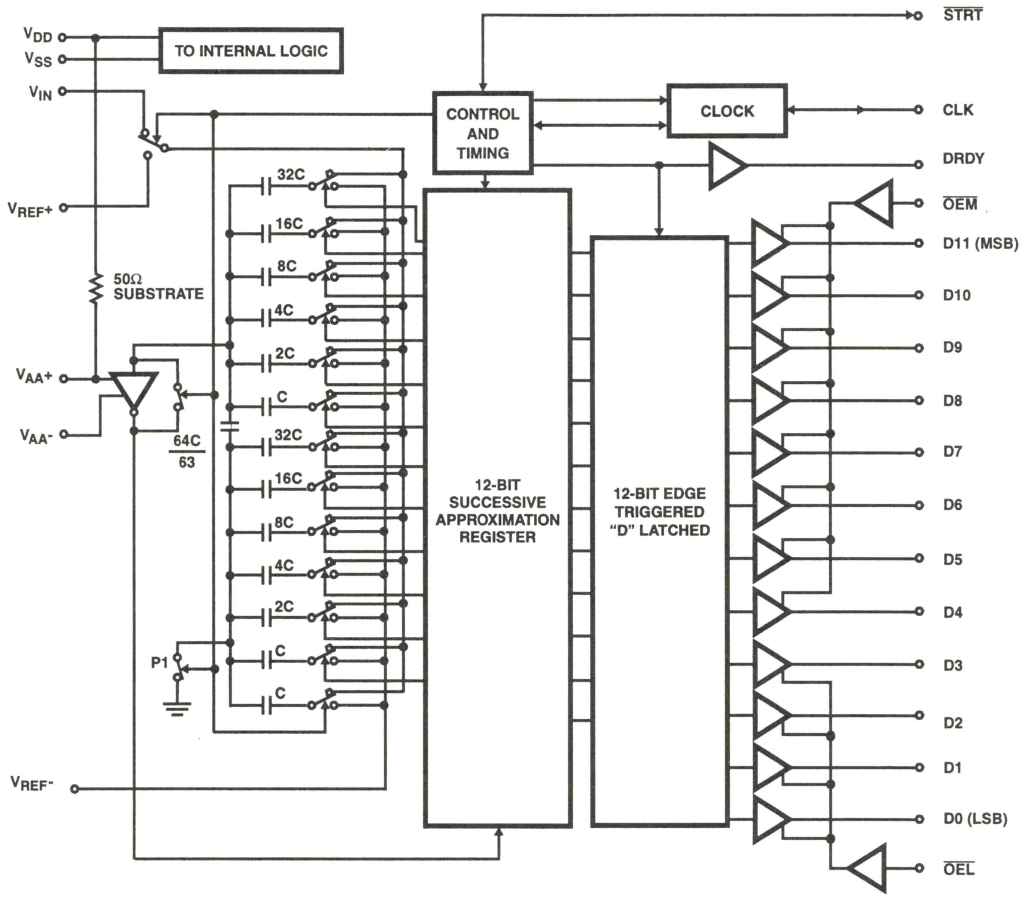
Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage
- V_{DD} to V_{SS} ..... $(V_{SS}$ -0.5V) < V_{DD} < +6.5V
- V_{AA}+ to V_{AA}- ..... $(V_{SS}$ -0.5V) to (V_{SS} +6.5V)
- V_{AA}+ to V_{DD} ..... ±0.3V

Analog and Reference Inputs
- V_{IN}, V_{REF}+, V_{REF}- ..... $(V_{SS}$ -0.3V) < V_{INA} < (V_{DD} +0.3V)

Digital I/O Pins ..... $(V_{SS}$ -0.3V) < VI/O < (V_{DD} +0.3V)

Operating Conditions

Temperature Range
- PDIP, SOIC, and CERDIP Packages ..... -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	80	N/A
SOIC Package	75	N/A
CERDIP Package	60	12

Maximum Junction Temperature
- PDIP and SOIC Packages ..... 150°C
- CERDIP Package ..... 175°C

Maximum Storage Temperature Range ..... -65°C to 150°C

Maximum Lead Temperature (Soldering, 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{DD} = V_{AA}+ = V_{REF}+ = 3.3V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = 600kHz (J suffix), CLK = 500kHz (K suffix), Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	UNITS
ACCURACY								
Resolution			12	-	-	12	-	Bits
Integral Linearity Error, INL (End Point)	J		-	-	±4.0	-	±4.0	LSB
	K		-	-	±2.5	-	±2.5	LSB
Differential Linearity Error, DNL	J		-	-	±4.0	-	±4.0	LSB
	K		-	-	±2.0	-	±2.0	LSB
Gain Error, FSE (Adjustable to Zero)	J		-	-	±2.0	-	±2.0	LSB
	K		-	-	±2.0	-	±2.0	LSB
Offset Error, V_{OS} (Adjustable to Zero)	J		-	-	±3.0	-	±3.0	LSB
	K		-	-	±2.5	-	±2.5	LSB
DYNAMIC CHARACTERISTICS								
Signal to Noise Ratio, SINAD $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	J	f_S = 600kHz, f_{IN} = 1kHz	-	61.5	-	-	-	dB
	K	f_S = 500kHz, f_{IN} = 1kHz	-	63.9	-	-	-	dB
Signal to Noise Ratio, SNR $\frac{\text{RMS Signal}}{\text{RMS Noise}}$	J	f_S = 600kHz, f_{IN} = 1kHz	-	63.2	-	-	-	dB
	K	f_S = 500kHz, f_{IN} = 1kHz	-	65.1	-	-	-	dB
Total Harmonic Distortion, THD	J	f_S = 750kHz, f_{IN} = 1kHz	-	-68.4	-	-	-	dBc
	K	f_S = 750kHz, f_{IN} = 1kHz	-	-70.8	-	-	-	dBc
Spurious Free Dynamic Range, SFDR	J	f_S = 600kHz, f_{IN} = 1kHz	-	69.0	-	-	-	dB
	K	f_S = 500kHz, f_{IN} = 1kHz	-	71.8	-	-	-	dB
ANALOG INPUT								
Input Current, Dynamic		At V_{IN} = V_{REF}+, 0V	-	±50	±100	-	±100	µA
Input Current, Static		Conversion Stopped	-	±0.4	±10	-	±10	µA

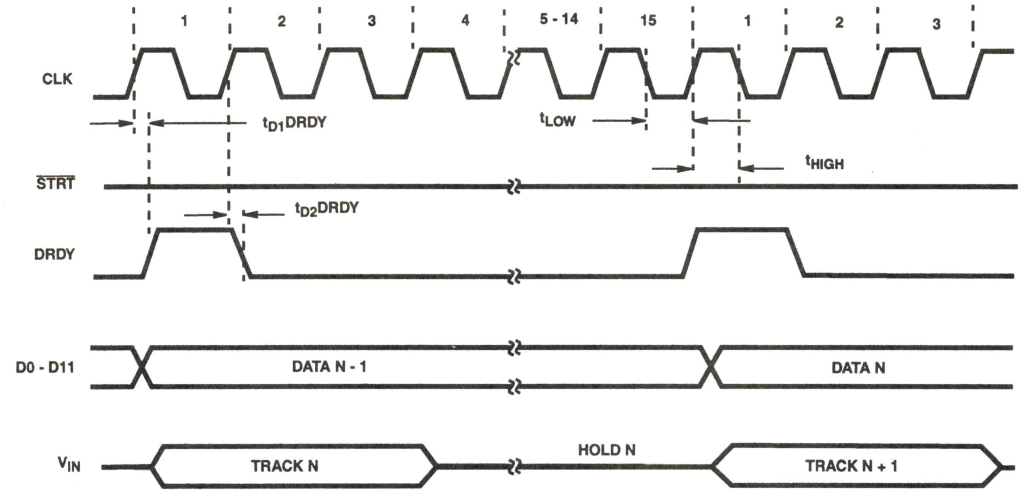
Electrical Specifications $V_{DD} = V_{AA}+ = V_{REF}+ = 3.3V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = 600kHz (J suffix), CLK = 500kHz (K suffix), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	25°C			-40°C TO 85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
Input Bandwidth -3dB		-	1		-	-	MHz
Reference Input Current		-	160	-	-	-	µA
Input Series Resistance, R_S	In Series with Input C_{SAMPLE}	-	420	-	-	-	Ω
Input Capacitance, C_{SAMPLE}	During Sample State	-	380	-	-	-	pF
Input Capacitance, C_{HOLD}	During Hold State	-	20	-	-	-	pF
DIGITAL INPUTS $\overline{OEL}$, $\overline{OEM}$, $\overline{STRT}$							
High-Level Input Voltage, V_{IH}		2.4	-	-	2.4	-	V
Low-Level Input Voltage, V_{IL}		-	-	0.8	-	0.8	V
Input Leakage Current, I_{IL}	Except CLK, V_{IN} = 0V, 5V	-	-	±10	-	±10	µA
Input Capacitance, C_{IN}		-	10		-	-	pF
DIGITAL OUTPUTS							
High-Level Output Voltage, V_{OH}	I_{SOURCE} = -400µA	2.6	-	-	2.6	-	V
Low-Level Output Voltage, V_{OL}	I_{SINK} = 1.6mA	-	-	0.4	-	0.4	V
Three-State Leakage, I_{OZ}	Except DRDY, V_{OUT} = 0V, 3.3V	-	-	±10	-	±10	µA
Output Capacitance, C_{OUT}	Except DRDY	-	20	-	-	-	pF
TIMING							
Conversion Time ($t_{CONV} + t_{ACQ}$) (Includes Acquisition Time) J		25	-	-	25	-	µs
K		30	-	-	30	-	µs
Clock Frequency	(Note 2)	0.05	-	0.75	0.05	0.75	MHz
Clock Pulse Width, t_{LOW}, t_{HIGH}	(Note 2)	100	-	-	100	-	ns
Aperture Delay, t_DAPR	(Note 2)	-	35	50	-	70	ns
Clock to Data Ready Delay, $t_{D1}DRDY$	(Note 2)	-	180	210	-	240	ns
Clock to Data Ready Delay, $t_{D2}DRDY$	(Note 2)	-	180	220	-	250	ns
Start Removal Time, $t_R\overline{STRT}$	(Note 2)	75	30	-	75	-	ns
Start Setup Time, $t_{SU}\overline{STRT}$	(Note 2)	85	60	-	30	-	ns
Start Pulse Width, $t_W\overline{STRT}$	(Note 2)	-	15	25	-	25	ns
Start to Data Ready Delay, t_{D3} DRDY	(Note 2)	-	110	130	-	160	ns
Output Enable Delay, t_{EN}	(Note 2)	-	65	75	-	80	ns
Output Disabled Delay, t_{DIS}	(Note 2)	-	95	110	-	130	ns
POWER SUPPLY CHARACTERISTICS							
Supply Current, $I_{DD} + I_{AA}$		-	0.5	1	-	2.5	mA

NOTE:

2. Parameter guaranteed by design or characterization, not production tested.

Timing Diagrams



$\overline{OEL}$ = $\overline{OEM}$ = V_{SS}

FIGURE 1. CONTINUOUS CONVERSION MODE

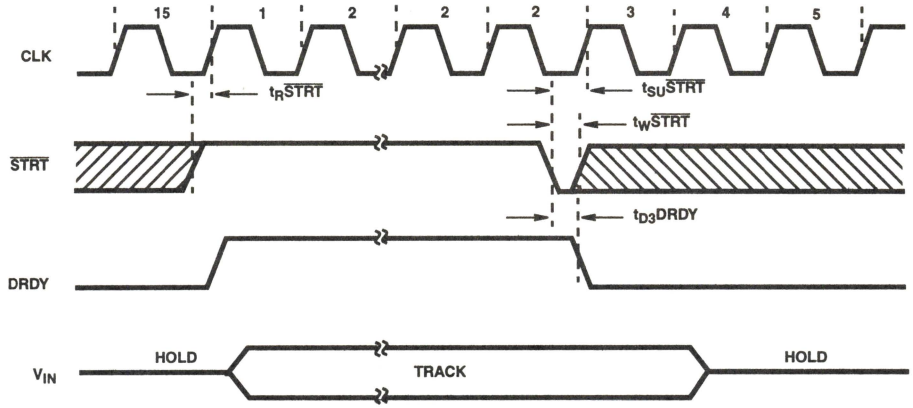


FIGURE 2. SINGLE SHOT MODE

Timing Diagrams (Continued)

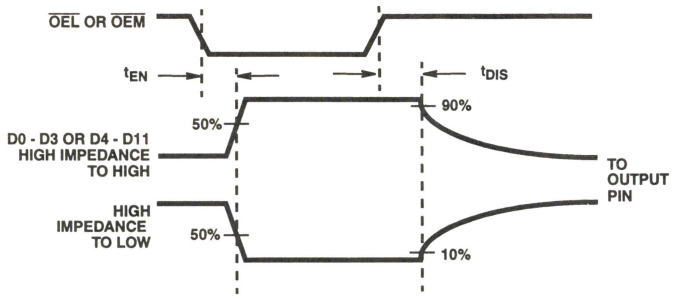


FIGURE 3A.

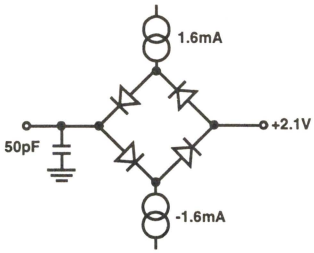


FIGURE 3B.

FIGURE 3. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

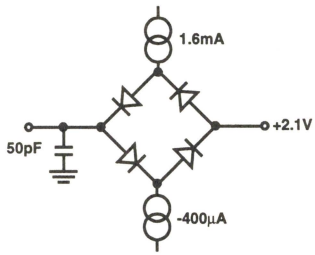


FIGURE 4. GENERAL TIMING LOAD CIRCUIT

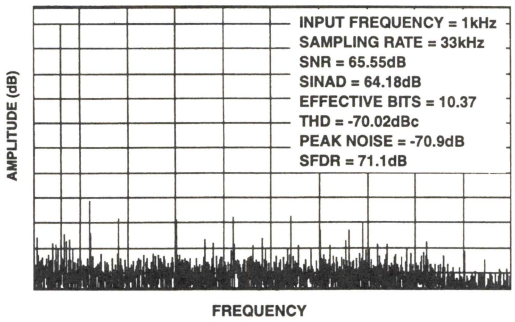


FIGURE 5. FFT SPECTRUM

Typical Performance Curves

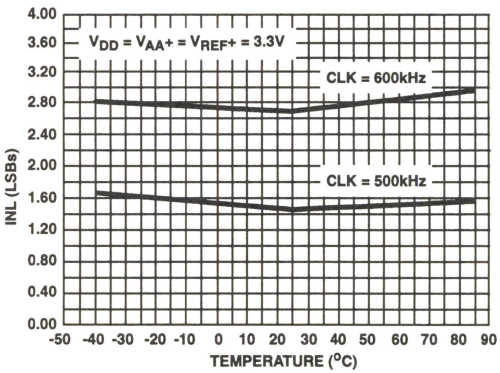


FIGURE 6. INL vs TEMPERATURE

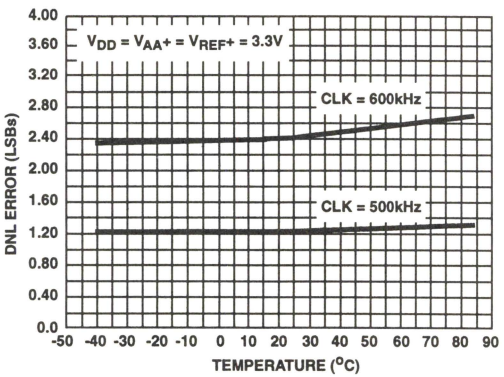


FIGURE 7. DNL vs TEMPERATURE

Typical Performance Curves

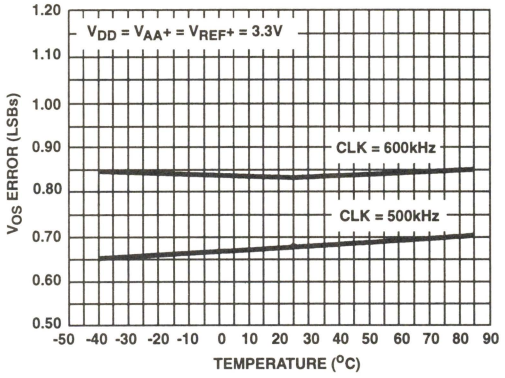


FIGURE 8. OFFSET ERROR vs TEMPERATURE

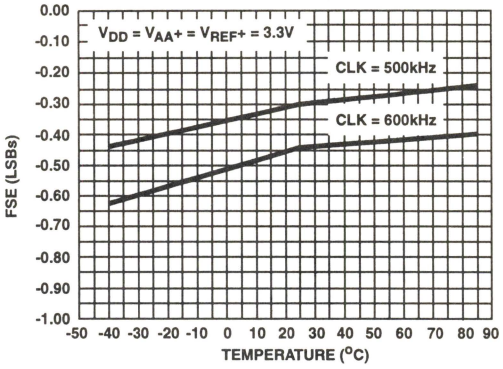


FIGURE 9. FULL SCALE ERROR vs TEMPERATURE

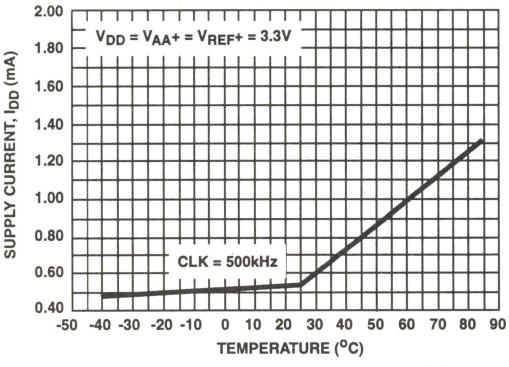


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

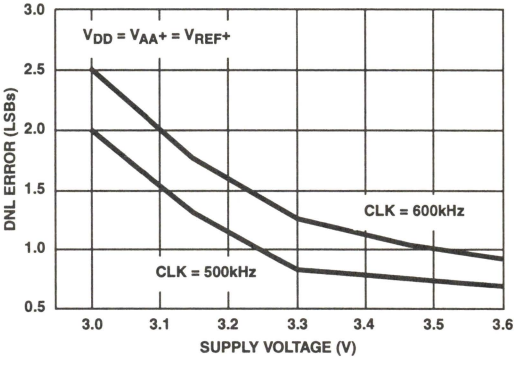


FIGURE 11. DNL vs SUPPLY VOLTAGE

Pin Descriptions

PIN #	NAME	DESCRIPTION
1	DRDY	Output flag signifying new data is available. Goes high at end of clock period 15. Goes low when new conversion is started.
2	D0	Bit 0 (Least Significant Bit, LSB).
3	D1	Bit 1.
4	D2	Bit 2.
5	D3	Bit 3.
6	D4	Bit 4.
7	D5	Bit 5.
8	D6	Bit 6.
9	D7	Bit 7.
10	D8	Bit 8.
11	D9	Bit 9.
12	V_{SS}	Digital Ground, (0V).
13	D10	Bit 10.

PIN #	NAME	DESCRIPTION
14	D11	Bit 11 (Most significant bit, MSB)
15	$\overline{OEM}$	Three-State enable for D4-D11. Active Low Input.
16	V_{AA}-	Analog Ground, (0V).
17	V_{AA}+	Analog Positive Supply. (+3.3V) (See text.)
18	V_{IN}	Analog Input.
19	V_{REF}+	Reference Voltage Positive Input, sets 4095 code end of input range.
20	V_{REF}-	Reference Voltage Negative Input, sets 0 code end of input range.
21	$\overline{STRT}$	Start Conversion Input active low, recognized after end of clock period 15.
22	CLK	CLK Input. Conversion functions are synchronized to positive going edge. (See text)
23	$\overline{OEL}$	Three-State Enable for D0 - D3. Active low input.
24	V_{DD}	Digital Positive Supply (+3.3V).

Theory of Operation

HI5813 is a CMOS 12-Bit, Analog-to-Digital Converter that uses capacitor charge balancing to successively approximate the analog input. A binary weighted capacitor network forms the A/D heart of the device. See the block diagram for the HI5813.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, $V_{REF}+$ or $V_{REF}-$.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input and the comparator is being auto balanced at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input; the one representing the MSB (D11) is connected to the $V_{REF}+$ terminal; and the remaining capacitors to $V_{REF}-$. The capacitor common node, after the charges balance out, will indicate whether the input was above $^1/_2$ of ($V_{REF}+$ - $V_{REF}-$). At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to $V_{REF}+$ (if the comparator was high) or returned to $V_{REF}-$. This allows the next comparison to be at either $^3/_4$ or $^1/_4$ of ($V_{REF}+$ - $V_{REF}-$).

At the end of periods 5 through 14, capacitors representing D10 through D1 are tested, the result stored, and each capacitor either left at $V_{REF}+$ or at $V_{REF}-$.

At the end of the 15th period, when the LSB (D0) capacitor is tested, (D0) and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data ready output goes active. The conversion cycle is now complete.

Analog Input

The analog input pin is a predominately capacitive load that changes between the track and hold periods of the conversion cycle. During hold, clock period 4 through 15, the input loading is leakage and stray capacitance, typically less than 5µA and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the current spike by the end of the tracking period. The amount of charge is dependent on supply and input voltages. The average current is also proportional to clock frequency.

As long as these current spikes settle completely by end of the signal acquisition period, converter accuracy will be preserved. The analog input is tracked for 3 clock cycles. With a clock of 500kHz the track period is 6µs.

A simplified analog input model is presented in Figure 12. During tracking, the A/D input (V_{IN}) typically appears as a 380pF capacitor being charged through a 420Ω internal switch resistance. The time constant is 160ns. To charge this capacitor from an external "zero Ω" source to 0.5 LSB (1/8192), the charging time must be at least 9 time constants or 1.4µs. The maximum source impedance (R_{SOURCE} Max) for a 6µs acquisition time settling to within 0.5 LSB is 1.3kΩ.

If the clock frequency was slower, or the converter was not restarted immediately (causing a longer sample time), a higher source impedance could be tolerated.

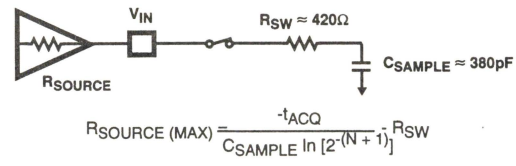


FIGURE 12. ANALOG INPUT MODEL IN TRACK MODE

Reference Input

The reference input $V_{REF}+$ should be driven from a low impedance source and be well decoupled.

Current spikes are generated on the reference pin during each bit test of the successive approximation part of the conversion cycle as the charge balancing capacitors are switched between $V_{REF}-$ and $V_{REF}+$ (clock periods 5 - 14). These current spikes must settle completely during each bit test of the conversion to not degrade the accuracy of the converter. Therefore $V_{REF}+$ and $V_{REF}-$ should be well bypassed. Reference input $V_{REF}-$ is normally connected directly to the analog ground plane. If $V_{REF}-$ is biased for nulling the converters offset it must be stable during the conversion cycle.

Full Scale and Offset Adjustment

In many applications the accuracy of the HI5813 would be sufficient without any adjustments. In applications where accuracy is of utmost importance full scale and offset errors may be adjusted to zero.

The $V_{REF}+$ and $V_{REF}-$ pins reference the two ends of the analog input range and may be used for offset and full scale adjustments. In a typical system the $V_{REF}-$ might be returned to a clean ground, and the offset adjustment done on an input amplifier. $V_{REF}+$ would then be adjusted to null out the full scale error. When this is not possible, the $V_{REF}-$ input can be adjusted to null the offset error, however, $V_{REF}-$ must be well decoupled.

Full scale and offset error can also be adjusted to zero in the signal conditioning amplifier driving the analog input (V_{IN}).

Control Signal

The HI5813 may be synchronized from an external source by using the $\overline{STRT}$ (Start Conversion) input to initiate conversion, or if $\overline{STRT}$ is tied low, may be allowed to free run. Each conversion cycle takes 15 clock periods.

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by t_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by t_{D1}DRDY) after the start of clock period 1, and returns low (specified by t_{D2}DRDY) after the start of clock period 2.

The 12 data bits are available in parallel on three-state bus driver outputs. When low, the $\overline{OEM}$ input enables the most significant byte (D4 through D11) while the $\overline{OEL}$ input enables the four least significant bits (D0 - D3). t_{EN} and t_{DIS} specify the output enable and disable times.

If the output data is to be latched externally, either the trailing edge of data ready or the next falling edge of the clock after data ready goes high can be used.

Figure 2 shows operation of the HI5813 when the $\overline{STRT}$ pin is used to initate a conversion. If $\overline{STRT}$ is taken high at least $t_R\overline{STRT}$ before clock period 1 and is not reapplied during that period, the converter will stay in the track mode and the DRDY output will remain high. A low signal applied to $\overline{STRT}$ will bring the DRDY flag low and the conversion will continue with clock period 3 on the first positive going clock edge that meets the $t_{SU}\overline{STRT}$ setup time.

Clock

The clock used to drive the HI5813 can range in frequency from 50kHz up to 750kHz. All converter functions are synchronized with the rising edge of the clock signal. The clock can be shut off only during the sample (track) portion of the conversion cycle. At other times it must be above the minimum frequency shown in the specifications. In the above two cases, a further restriction applies in that the clock should not be shut off during the third sample period for more than 1ms. This might cause an internal charge pump voltage to decay.

If the clock is shut off during the conversion time (clock cycles 4 through 15) of the A/D, the output might be invalid due to balancing capacitor droop.

The clock must also meet the minimum t_{LOW} and t_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

Power Supplies and Grounding

V_{DD} and V_{SS} are the digital supply pins: they power all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for V_{AA}+, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}. Input transients above V_{DD} or below V_{SS} will get steered to the digital supplies.

The V_{AA}+ and V_{AA}- terminals supply the charge balancing comparator only. Because the comparator is autobalanced between conversions, it has good low frequency supply rejection. It does not reject well at high frequencies however; V_{AA}- should be returned to a clean analog ground and V_{AA}+ should be RC decoupled from the digital supply as shown in Figure 13.

There is approximately 50Ω of substrate impedance between V_{DD} and V_{AA}+. This can be used, for example, as part of a low pass RC filter to attenuate switching supply noise. A 10µF capacitor from V_{AA}+ to ground would attenuate 30kHz noise by approximately 40dB. Note that back to back diodes should be placed from V_{DD} to V_{AA}+ to handle supply to capacitor turn-on or turn-off current spikes.

Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the A/D. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is than transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See typical performance characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured RMS signal to RMS sum of noise at a specified input and sampling frequency. The noise is the RMS sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76)dB. For an ideal 12-bit converter the SNR is 74dB. Differential and integral linearity errors will degrade SNR:

$$SNR = 10\ Log \frac{\text{Sinewave Signal Power}}{\text{Total Noise Power}}$$

Signal-To-Noise + Distortion Ratio

SINAD is the measured RMS signal to RMS sum of noise plus harmonic power and is expressed by the following:

$$SINAD = 10\ Log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (2nd - 6th)}}$$

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of the second through sixth harmonic components to the fundamental RMS signal for a specified input and sampling frequency.

$$THD = 10\ Log \frac{\text{Total Harmonic Power (2nd - 6th Harmonic)}}{\text{Sinewave Signal Power}}$$

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the rms amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

$$SFDR = 10\ Log \frac{\text{Sinewave Signal Power}}{\text{Highest Spurious Signal Power}}$$

TABLE 2. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE† V_{REF+} = 3.3V V_{REF-} = 0.0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB											LSB
			D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale (FS)	3.2992	4095	1	1	1	1	1	1	1	1	1	1	1	1
FS - 1 LSB	3.2984	4094	1	1	1	1	1	1	1	1	1	1	1	0
$^3/_4$ FS	2.4750	3072	1	1	0	0	0	0	0	0	0	0	0	0
$^1/_2$ FS	1.6500	2048	1	0	0	0	0	0	0	0	0	0	0	0
$^1/_4$ FS	0.8250	1024	0	1	0	0	0	0	0	0	0	0	0	0
1 LSB	0.00080566	1	0	0	0	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0	0	0	0

†The voltages listed above represent the ideal lower transition of each output code shown as a function of the reference voltage.

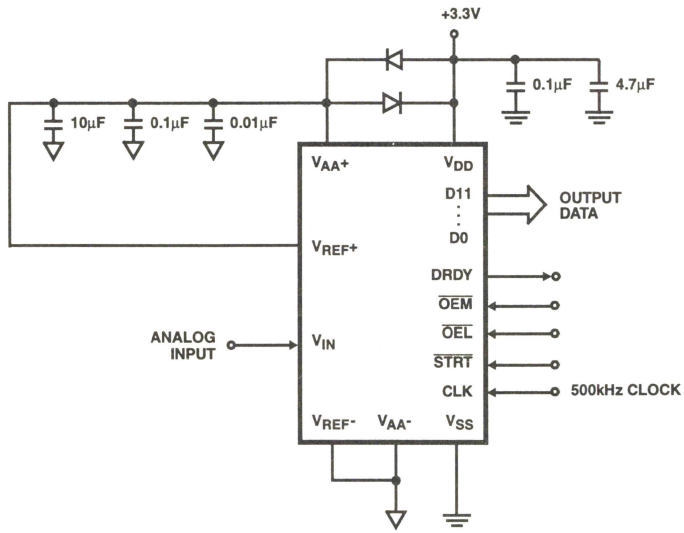


FIGURE 13. GROUND AND SUPPLY DECOUPLING

Die Characteristics

DIE DIMENSIONS:

3200µm x 3940µm

METALLIZATION:

Type: AlSi
Thickness: 11kÅ ±1kÅ

PASSIVATION:

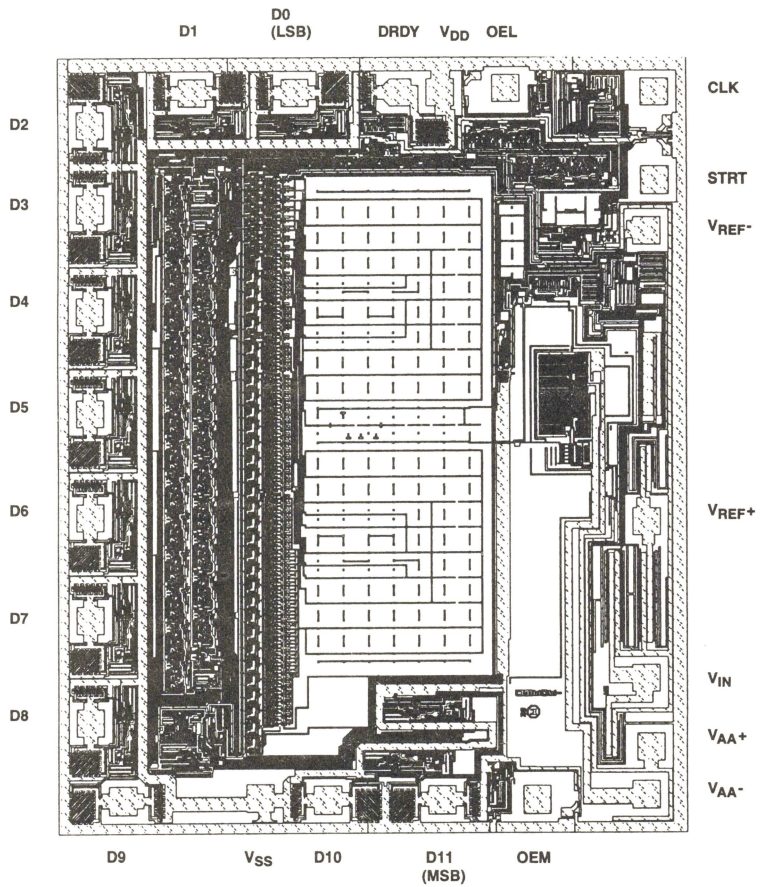
Type: PSG
Thickness: 13kÅ ±2.5kÅ

WORST CASE CURRENT DENSITY:

1.84×10^5 A/cm^2

Metallization Mask Layout

HI5813



DATA ACQUISITION 7

A/D CONVERTERS - SIGMA DELTA

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Selection Guide		7-2
A/D Converters - Sigma Delta Data Sheets		
HI7188	8-Channel, 16-Bit, High Precision, Sigma-Delta A/D Sub-System	7-3
HI7190	24-Bit, High Precision, Sigma Delta A/D Converter.	7-25
HI7191	Low Cost, 24-Bit, High Precision, Sigma Delta A/D Converter	7-46

16-BIT, 8 CHANNEL SIGMA DELTA A/D SUBSYSTEM

DEVICE	SUFFIX CODE	OUTPUTS	CONV. TYPE	CONV. RATE (MSPS)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI7188	IP, IN	Serial QSPI, SP, I, Microwire	Sigma Delta 4th Order Modulator	240/Channel	BiCMOS	+5	±2.5V	(.0015)	IND	+2.5V	High Throughput 8-Channel Sigma Delta A/D On Board Micro-Sequencer

24-BIT SIGMA DELTA A/D CONVERTER

DEVICE	SUFFIX CODE	OUTPUTS	CONV. TYPE	CONV. RATE (MSPS)	TECH-NOLOGY	POWER SUPPLY (V)	INPUT RANGE (V)	INL (LSB)	TEMP. RANGE	V_{REF}	FEATURES
HI7190	IB, IP	Serial QSPI, SP, Microwire	Sigma Delta 2nd Order Modulator	11Hz -2kHz	BiCMOS	+5	±2.5V	(.0007)	IND	+2.5V	Low Noise Sigma Delta 23.5 Bit ENOB at 16 Bits Linear
HI7191											

HARRIS SEMICONDUCTOR

HI7188

8-Channel, 16-Bit, High Precision, Sigma-Delta A/D Sub-System

August 1997

Features

- Fully Differential 8-Channel Multiplexer and Reference
- Automatic Channel Switching with Zero Latency
- 240 Conversions Per Second Per Channel
- 16-Bit Resolution with No Missing Codes
- 0.0015% Integral Non-Linearity
- Fully Software Configurable
  - -120dB Rejection of 60/50Hz Line Noise
  - Channel Conversion Order and Number of Active Channels
  - True Bipolar or Unipolar Input Range Per Channel
  - PGIA Gain Per Channel
  - 2-Wire or 3-Wire Interface
- Chopper Stabilized PGIA with Gains of 1 to 8
- Serial Data I/O Interface, SPI Compatible
- 3 Point System Calibration
- Low Power Dissipation of 30mW (Typ)

Applications

- Multi-Channel Industrial Process Controls
- Weight Scales
- Medical Patient Monitoring
- Laboratory Instrumentation
- Gas Monitoring System
- Reference Literature
  - AN9504 "A Brief Introduction to Sigma Delta Conversion"
  - TB329 "Harris Sigma-Delta Calibration Techniques"
  - AN9518 "Using the HI7188 Evaluation Kit"
  - AN9610 "Interfacing the HI7188 to a Microcontroller"
  - AN9538 "Using the HI7188 Serial Interface"

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI7188IP	-40 to 85	40 Ld PDIP	E40.6
HI7188IN	-40 to 85	44 Ld MQFP	Q44.10x10
HI7188EVAL	25	Evaluation Kit	

Description

The HI7188 is an easy-to-use 8-Channel sigma-delta programmable A/D **subsystem** ideal for low frequency physical and electrical measurements in scientific, medical, and industrial applications. The subsystem has complete on-chip capabilities to support moving the intelligence from the system controller and towards the sensors. This gives the designer faster and more flexible configurability without the traditional drawbacks of low throughput per channel, higher power or cost per channel. Extreme design complexity and excessive software overhead is eliminated.

The HI7188 contains a fully differential 8 channel multiplexer, Programmable Gain Instrumentation Amplifier (PGIA), 4th order sigma-delta ADC, integrating filter, line noise rejection filters, calibration and data RAMs, clock oscillator, and a microsequencer. Communication with the HI7188 is performed via the serial I/O port, and is compatible with most synchronous transfer formats, including both the Motorola/Harris 6805/11 series SPI, QSPI and Intel 8051 series SSR protocols.

The powerful on-board microsequencer provides automatic conversions on the multiplexed input channels (up to 8) by controlling all channel switching, filtering and calibration. The microsequencer supports on-the-fly multiplexer reconfiguration, forty to fifty times faster throughput than the competition and zero step response delay during internal or external multiplexer channel changes. A simple set of commands gives the user control over calibration, PGIA gain, and bipolar/unipolar modes on a per channel basis. Number of channels to convert, data coding, line noise rejection, etc. is programmed at the chip level. The calibration RAMs allow the user to read and write system calibration data while the data RAMs provide a read support of the conversion results for each channel.

This design is effectively eight 16-bit (for 96dB noise-free dynamic range) Sigma-Delta A/D converters combined with a microsequencer and an eight-channel multiplexer in a single package. The HI7188 provides 120dB line-noise rejection at 240 samples/second/channel (in 60Hz line-rejection mode) and 200 samples/second/channel (in 50Hz line-rejection mode) base output data rates. By reusing multiplexer channels for the same input, throughput can increase by integer increments of the base output data rate up to 1920Hz.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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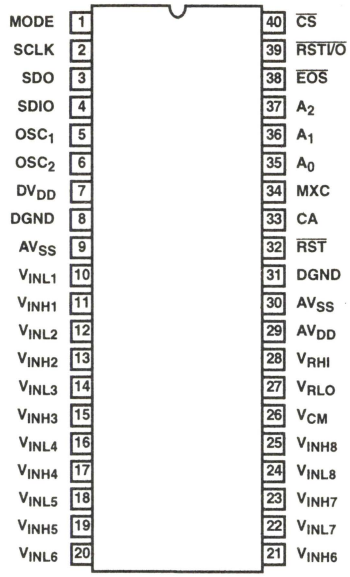
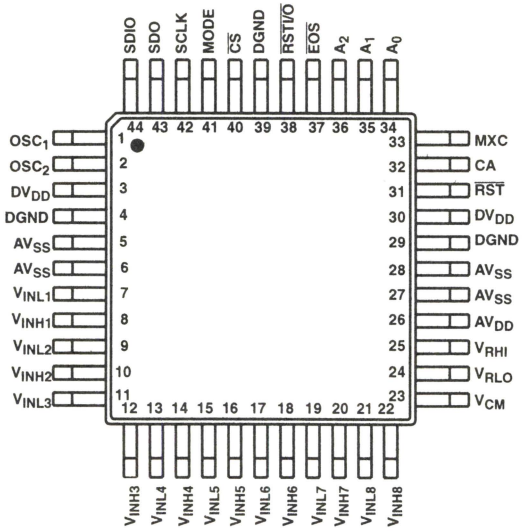
Pinouts

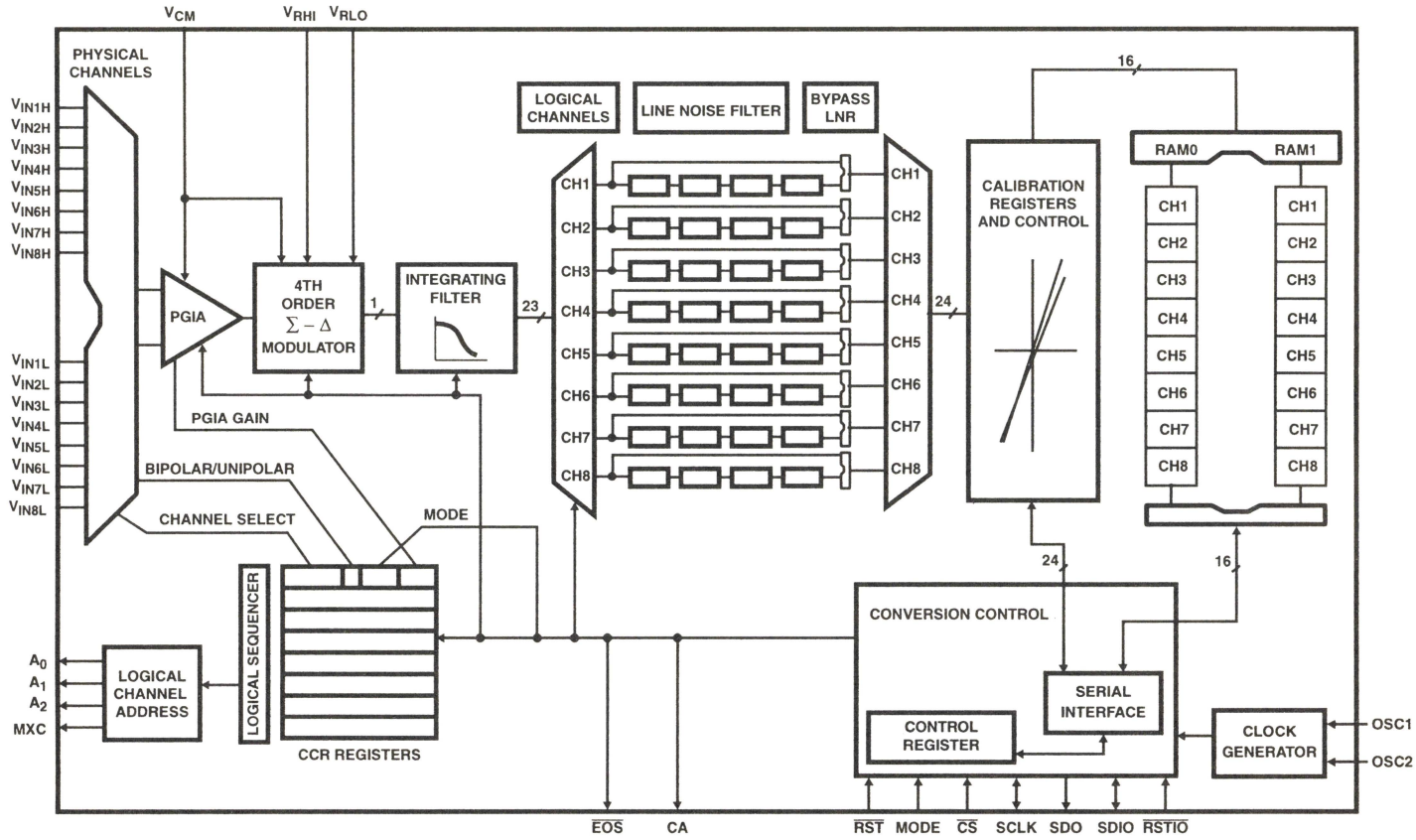
HI7188 (PDIP)
TOP VIEW



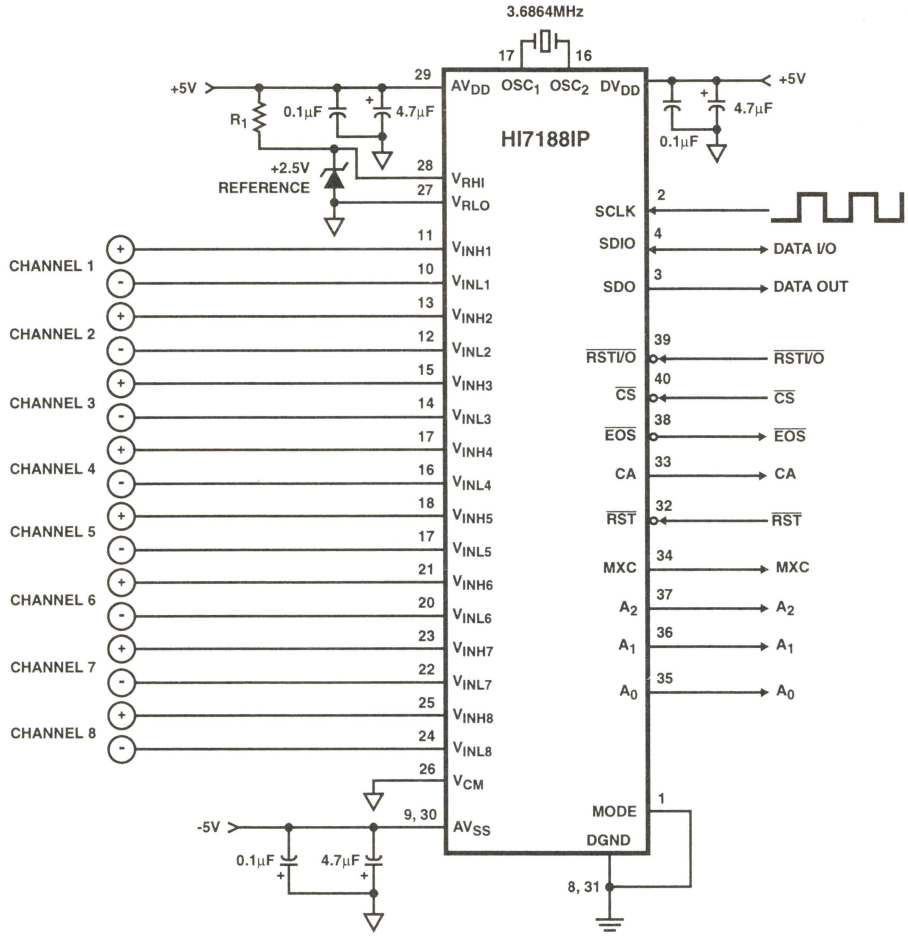
HI7188 (MQFP)
TOP VIEW



Functional Block Diagram



Typical Application Schematic



Pin Descriptions

40 LEAD PDIP	44 LEAD MQFP	PIN NAME	PIN DESCRIPTION
1	41	MODE	Mode input. Used to select between Synchronous Self Clocking (MODE = 1) or Synchronous External Clocking (MODE = 0) for the Serial Port.
2	42	SCLK	Serial interface clock. Synchronizes serial data transfers. Data is input on the rising edge and output on the falling edge.
3	43	SDO	Serial Data Out. Serial data is read from this line when using a 3-wire serial protocol such as the Motorola Serial Peripheral Interface.
4	44	SDIO	Serial Data IN or OUT. This line is bidirectional programmable and interfaces directly to the Intel Standard Serial Interface using a 2-wire serial protocol.
5	1	OSC_1	Oscillator clock input for the device. A crystal connected between OSC_1 and OSC_2 will provide a clock to the device, or an external oscillator can drive OSC_1. The oscillator frequency should be 3.6864MHz to maintain Line Noise Rejection.
6	2	OSC_2	Used to connect a crystal source between OSC_1 and OSC_2. Leave open otherwise.
7	3, 30	DV_{DD}	Positive Digital supply (+5V).
8, 31	4, 29, 39	DGND	Digital supply ground.
9, 30	5, 6, 27, 28	AV_{SS}	Negative analog power supply (-5V).
10	7	V_{INL1}	Analog input low for Channel 1.
11	8	V_{INH1}	Analog input high for Channel 1.
12	9	V_{INL2}	Analog input low for Channel 2.
13	10	V_{INH2}	Analog input high for Channel 2.
14	11	V_{INL3}	Analog input low for Channel 3.
15	12	V_{INH3}	Analog input high for Channel 3.
16	13	V_{INL4}	Analog input low for Channel 4.
17	14	V_{INH4}	Analog input high for Channel 4.
18	15	V_{INL5}	Analog input low for Channel 5.
19	16	V_{INH5}	Analog input high for Channel 5.
20	17	V_{INL6}	Analog input low for Channel 6.
21	18	V_{INH6}	Analog input high for Channel 6.
22	19	V_{INL7}	Analog input low for Channel 7.
23	20	V_{INH7}	Analog input high for Channel 7.
24	21	V_{INL8}	Analog input low for Channel 8.
25	22	V_{INH8}	Analog input high for Channel 8.
26	23	V_{CM}	Common mode voltage. Must be tied to the mid point of AV_{DD} and AV_{SS}.
27	24	V_{RLO}	External reference input. Should be negative referenced to V_{RHI}.
28	25	V_{RHI}	External reference input. Should be positive referenced to V_{RLO}.
29	26	AV_{DD}	Positive analog power supply (+5V).
32	31	$\overline{RST}$	Active low Reset pin. Used to initialize modulator, filter, RAMs, registers and state machines.
33	32	CA	Calibration active output. Indicates that at least one active channel is in a calibration mode.
34	33	MXC	Multiplexer control output. Indicates that the conversion for the active channel is complete.
35	34	A_0	Logical channel count output (LSB).
36	35	A_1	Logical channel count output.
37	36	A_2	Logical channel count output (MSB).
38	37	$\overline{EOS}$	End of scan output. Signals the end of a channel scan (all active channels have been converted) and data is available to be read. Remains low until data RAM is read.
39	38	$\overline{RSTI/O}$	I/O reset (active low) input. Resets serial interface state machine only.
40	40	$\overline{CS}$	Active low chip select pin. Used to select a serial data transfer cycle. When high the SDO and SDIO pins are three-state.

Absolute Maximum Ratings

Supply Voltage
- AV_{DD} to AV_{SS} 11V
- DV_{DD} to DGND . . . . . +5.5V

Analog Input Pins . . . . . AV_{SS} to AV_{DD}
Digital Input, Output and I/O Pins . . . . . DGND to DV_{DD}
ESD Tolerance (No Damage)
- Human Body Model 500V
- Machine Model 100V
- Charged Device Model 500V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
PDIP	50
MQFP	80

Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Junction Temperature . . . . . 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(MQFP - Lead Tips Only)

Operating Conditions

Operating Temperature Range . . . . . -40^{o}C to 85^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 3.6864MHz, Bipolar Input Range Selected

PARAMETER	TEST CONDITION	-40^{o}C TO 85^{o}C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution	Dependent on Gain (Note 2)	-	-	16	Bits
Integral Non-Linearity, INL	F_S = 25Hz, +FS, +MS, 0, -MS, -FS End Point Line Method (Notes 3, 5, 6)	-	±0.0015	±0.0045	%FS
Differential Non-Linearity	(Note 2)	No Missing Codes to 16-Bits			-
Offset Error, V_{OS} (Calibrated)	$V_{INHI} = V_{INLO}$ (Notes 3, 4)	-	±0.0015	-	%FS
Full Scale Error, FSE (Calibrated)	$V_{INHI} - V_{INLO}$ = +2.5V (Notes 3, 4)	-	±0.0015	-	%FS
Gain Error (Calibrated)	Slope = +Full Scale - (-Full Scale) (Notes 3, 4)	-	±0.0015	-	%FS
Noise, $V_{N(P-P)}$		-	1/4	-	LSB
Common Mode Rejection Ratio, CMRR	V_{CM} = 0V (Note 5) Delta V_{CM} = ±3V	-	-75	-	dB
Off Channel Isolation	(Note 2)	-120	-	-	dB
ANALOG INPUT					
Common Mode Input Range, V_{CM}	(Note 2)	AV_{SS}	-	AV_{DD}	-
Input Leakage Current, I_{IN}	$V_{IN} = AV_{DD}$ (Note 3)	-	-	1.0	nA
Input Capacitance, C_{IN}	(Note 2) See Table 2	-	4.0		pF
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic Current, I_I	V_{IN} = 0V, +5V	-	1.0	10	µA
Input Capacitance, C_{IN}	V_{IN} = 0V (Note 2)	-	5.0	-	pF
DIGITAL CMOS OUTPUTS					
Output Logic High Voltage, V_{OH}	I_{OUT} = -100µA (Note 7)	2.4	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OUT} = 3.2mA (Note 7)	-	-	0.4	V

Electrical Specifications AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 3.6864MHz, Bipolar Input Range Selected **(Continued)**

PARAMETER	TEST CONDITION	-40°C TO 85°C			UNITS
		MIN	TYP	MAX	
Output Three-State Leakage Current, I_{OZ}	V_{OUT} = 0V, +5V (Note 7)	-	1	10	µA
Digital Output Capacitance, C_{OUT}	(Note 2)	-	10	-	pF
TIMING CHARACTERISTICS					
SCLK Minimum Cycle Time, t_{SCLK}	(Notes 2, 7)	200	-	-	ns
SCLK Minimum Pulse Width, t_{SCLKPW}	(Notes 2, 7)	60	-	-	ns
$\overline{CS}$ to SCLK Precharge Time, t_{PRE}	(Notes 2, 7)	50	-	-	ns
Data Setup to SCLK Rising Edge (Write), t_{DSU}	(Notes 2, 7)	50	-	-	ns
Data Hold from SCLK Rising Edge (Write), t_{DHLD}	(Notes 2, 7)	0	-	-	ns
Data Read Access from Instruction Byte Write, t_{ACC}	(Notes 2, 7)	-	-	40	ns
Read Bit Valid from SCLK Falling Edge, t_{DV}	(Notes 2, 7)	-	-	40	ns
Last Data Transfer to Data Ready Inactive, $t_{\overline{DRDY}}$	(Notes 2, 7)	-	50	-	ns
$\overline{RESET}$ Low Pulse Width t_{RESET}	(Notes 2, 7)	100	-	-	ns
$\overline{RSTI/O}$ Low Pulse Width $t_{\overline{RSTI/O}}$	(Notes 2, 7)	100	-	-	ns
MUX High Pulse Width t_{MUX}	(Notes 2, 7)	14			µs
CADDR Valid to MUX High	(Notes 2, 7)			75	ns
Oscillator Clock Frequency	(Notes 2, 7)	-	3.6864	-	MHz
Output Rise/Fall Time	(Notes 2, 7)	-	-	30	ns
Input Rise/Fall Time	(Notes 2, 7)	-	-	1	µs
POWER SUPPLY CHARACTERISTICS					
IAV_{DD}	AV_{DD} = +5V, OSC_1 = 3.6864MHz (Note 3)	-	1.8	3.0	mA
IAV_{SS}	AV_{SS} = -5V, OSC_1 = 3.6864MHz (Note 3)	-	1.8	3.0	mA
IDV_{DD}	DV_{DD} = +5V, SCLK = 4MHz	-	2.0	4.0	mA
Power Dissipation, Active PD_A	AV_{DD} = +5V, AV_{SS} = -5V, SLP = '0' (Notes 3, 9)	-	28	50	mW
Power Dissipation, Sleep PD_S	AV_{DD} = +5V, AV_{SS} = -5V, SLP = '1' (Notes 3, 9)	-	5	-	mW
PSRR (ΔV_{supply} = 0.25V)	PSRR = 20log (ΔV_{supply} / ΔV_{OS}) (Note 3)	-	75	-	dB

NOTES:

2. Parameter guaranteed by design or characterization, not production tested.
3. DC PSRR is measured on all supplies individually and applies to both Bipolar and Unipolar Input Ranges.
4. These errors can be removed by re-calibrating at the desired operating temperature.
5. Applies after system calibration.
6. Fully differential input signal source is used.
7. See Load Test Circuit, Figure 1, R_1 = 10kΩ, C_L = 50pF (Includes Stray and Jig Capacitance).
8. For Line Noise Rejection, 3.6864MHz is required to develop internal clocks to reject 50/60Hz.
9. SLP is the sleep mode enable bit defined in bit 3 of the Control Register (CR <3>).

Test Circuits

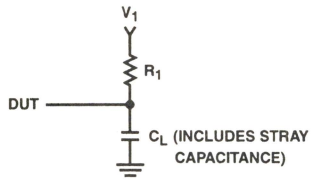
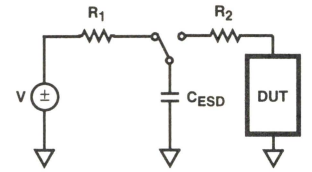


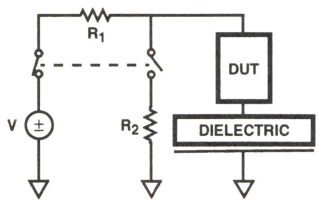
FIGURE 1. LOAD TEST CIRCUIT



HUMAN BODY
C_{ESD} = 100pF
R_1 = 10MΩ
R_2 = 1.5kΩ

MACHINE MODEL
C_{ESD} = 200pF
R_1 = 10MΩ
R_2 = 0Ω

FIGURE 2. HUMAN BODY AND MACHINE MODEL ESD TEST CIRCUIT



CHARGED DEVICE MODEL
R_1 = 1GΩ
R_2 = 1Ω

FIGURE 3. CHARGE DEVICE MODEL ESD TEST CIRCUIT

Waveforms

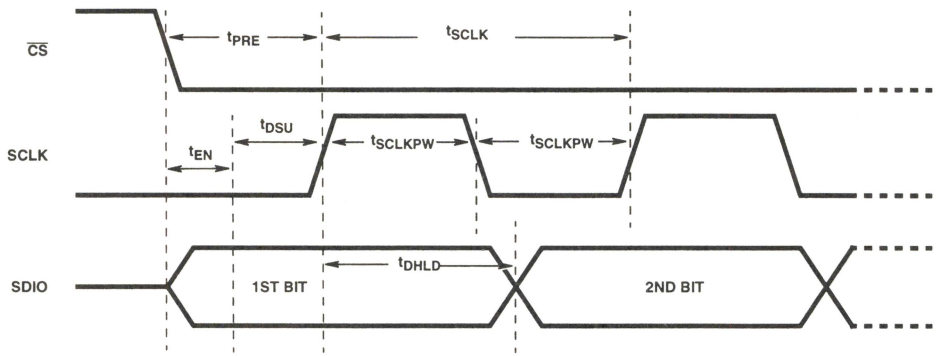


FIGURE 4. DATA WRITE TO HI7188

Waveforms (Continued)

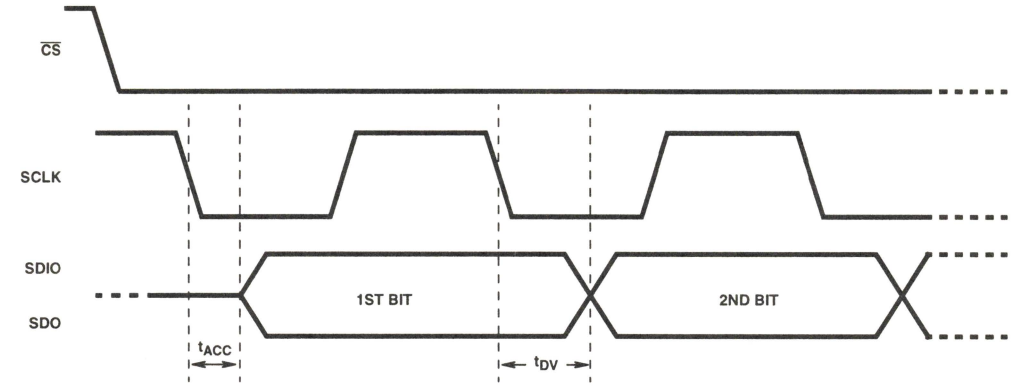


FIGURE 5. DATA READ FROM HI7188

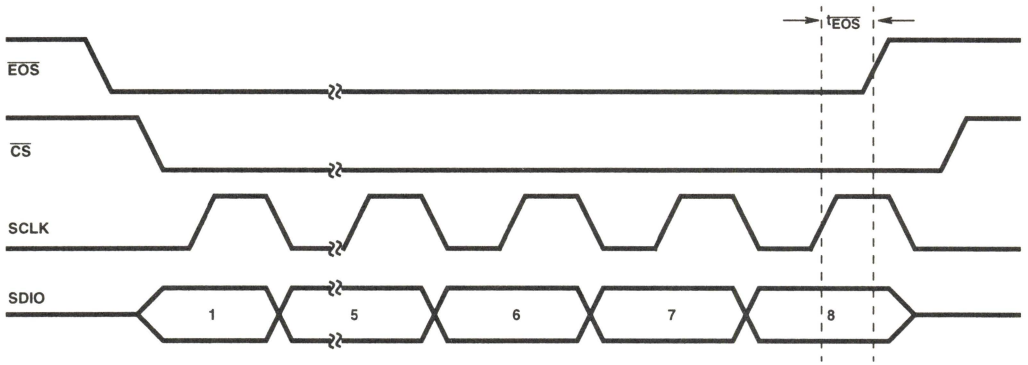


FIGURE 6. DATA READ FROM HI7188

Definitions

Integral Non-Linearity (INL) - This is the maximum deviation of any digital code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (a point 0.5 LSB below the first code transition 000...000 and 000...001) and full scale (a point 0.5 LSB above the last code transition 111...110 to 111...111).

Differential Non-Linearity (DNL) - This is the deviation from the actual difference between midpoints and the ideal difference between midpoints (1 LSB) for adjacent codes. If this difference is equal to or more negative than 1 LSB, a code will be missed.

Offset Error (V_{OS}) - The offset error is the deviation of the first code transition from the ideal input voltage (V_{IN} - 0.5 LSB).

Full Scale Error (FSE) - The full scale error is the deviation of the last code transition from the ideal input full-scale voltage (V_{IN}- + V_{REF}/Gain - 1.5 LSB).

Input Span - The input span defines the minimum and maximum input voltages the device can handle while still calibrating properly for gain.

End of Scan (EOS) - The end of scan is a signal used to indicate all active logical channels have been converted and data is available to be read.

Line Noise Rejection - Line noise rejection is the ability to attenuate (reject) signals at the frequency of power lines typically 50Hz or 60Hz.

Physical/Logical Channel - A physical channel pertains to channels which are directly connected to the device package pins identified in the pinout. Logical channels are predefined in the Channel Configuration Registers (CCR) with a physical channels reference (address) being made by the user. Refer to the Channel Configuration Registers section for examples.

Functional Description

The HI7188 contains a differential 8 channel multiplexer, Programmable Gain Instrumentation Amplifier (PGIA), 4th order sigma-delta ADC, integrating filter, line noise rejection filters, Calibration and data RAMs, bidirectional serial port, clock oscillator, and a microsequencer. The 8 to 1 multiplexer at the input combined with the resetable modulator on the HI7188 allow for conversions of up to 8 differential channels with each channel being updated at a rate of 240 samples per second (with 60Hz line noise rejection enabled). The device can be programmed for conversion of any combination of physical channels. After the signal has passed through the multiplexer, it moves into the PGIA. The PGIA can be configured in gains of 1, 2, 4 and 8 specific for each of the 8 logical channels. The signal then enters the sigma delta modulator. The patented one-shot sigma delta modulator is a fourth order modulator which converts the differential analog signal into a series of one bit outputs. The 1's density of this data stream provides a digital representation of the analog input. The output of the modulator is fed into the integrating low pass digital filter. Data out of the filter is available after 201 bits are received from the modulator.

If the device is in line noise rejection mode, the integrating filter data is routed to the Line Noise Rejection filters. This data is then calibrated using the offset and gain calibration coefficients. Data coding is performed and the result is stored in the data RAM. If line noise rejection is disabled, the averaging filter is bypassed, calibration is performed on the data from the integrating filter, the data is coded, and the result is stored in the data RAM.

This data flow of modulation, filter and calibrate is repeated for each of the active logical channels (up to 8). After all active logical channels are converted the HI7188 generates an active low interrupt, End Of Scan ($\overline{EOS}$), that indicates all logical channels have been updated and valid data is available to be read from the data RAM.

Converted data is read via the HI7188 serial I/O port which is compatible with most synchronous transfer formats including both the Motorola SPI and Intel 8051 series SSR protocols. All RAMs, including the Data RAM, are accessed in a "burst" mode. That is, the data for all active logical channels is accessed in a single read communication cycle.

Using the HI7188

This section describes how to use the device for a typical application. This includes power supply considerations, initial reset, calibration and conversion. Please refer to Figure 7.

The analog and digital supplies and grounds are separate on the HI7188 to minimize digital noise coupling into the analog circuitry. Nominal supply voltages are AV_{DD} = +5V, DV_{DD} = +5V, and AV_{SS} = -5V. If the same supply is used for AV_{DD} and DV_{DD} it is imperative that the supply is separately decoupled to the AV_{DD} and DV_{DD} pins on the HI7188. Separate analog and digital ground planes should be maintained on the system board and the grounds should be tied together back at the power supply.

When the HI7188 is powered up it needs to be reset by pulling the $\overline{RST}$ line low. This resets the internal registers as shown in Table 1. This initial configuration defines the part for one active logical channel (physical channel 1, address 000), conversion mode, unipolar operation, gain of one, no line noise rejection, offset binary coding, MSB first I/O bit order, descending I/O byte order, and single line interface. After the $\overline{RST}$ line returns high, the device immediately begins converting as described above without any further instruction. There is no correction for offset or gain errors on the converted data at this time. To ensure maximum performance, calibration should be done as defined in the operation mode section.

TABLE 1. REGISTER RESET VALUES

REGISTER	VALUE (HEX)
Data Output Registers	XXXX (undefined)
Channel Configuration Register #2	00XXXXXX
Channel Configuration Register #1	XXXXXXXX
Control Register	0000
Offset Calibration Registers	000000
Positive Full Scale Calibration Registers	800000
Negative Full Scale Calibration Registers	800000

The reset configuration should be updated to reflect the users system including chip level and channel level programming.

1. Chip level refers to programming common to all channels such as 50/60 Hertz Line Noise Rejection, number of active channels, etc. and is detailed in the Control Register (CR) section.

2. Channel level programming is custom for each channel such as gain, physical input and mode as detailed in the Channel Configuration Registers (CCR) section.

A calibration routine should be performed next to remove system offset and full scale errors (see Calibration section). The CCR is used to place each channel of the device in several operational modes including Conversion, System Offset Calibration, System Positive Full Scale Calibration and System Negative Full Scale Calibration. Each channel inputs should be connected and settled to the correct input condition before the CCR is programmed for each calibration point. After a complete system calibration is performed, the desired analog input is applied and accurate data can be read via the serial interface. The device should be recalibrated when there is a change in the user configuration (i.e. gain, unipolar/bipolar), supply voltage or ambient temperature.

The configuration can be saved by writing the contents of the CR, CCR and calibration RAMs to microprocessor system memory (see Serial Interface section). After this has occurred, the configuration can easily be restored back to the HI7188 in the event of power failure or reset.

Analog Section Description

The analog portion of the HI7188 consists of a 8 to 1 fully differential Multiplexer, Programmable Gain Instrumentation amplifier (PGIA) and a 4th order Sigma-Delta modulator. Please refer to the simplified analog block diagram in Figure 8.

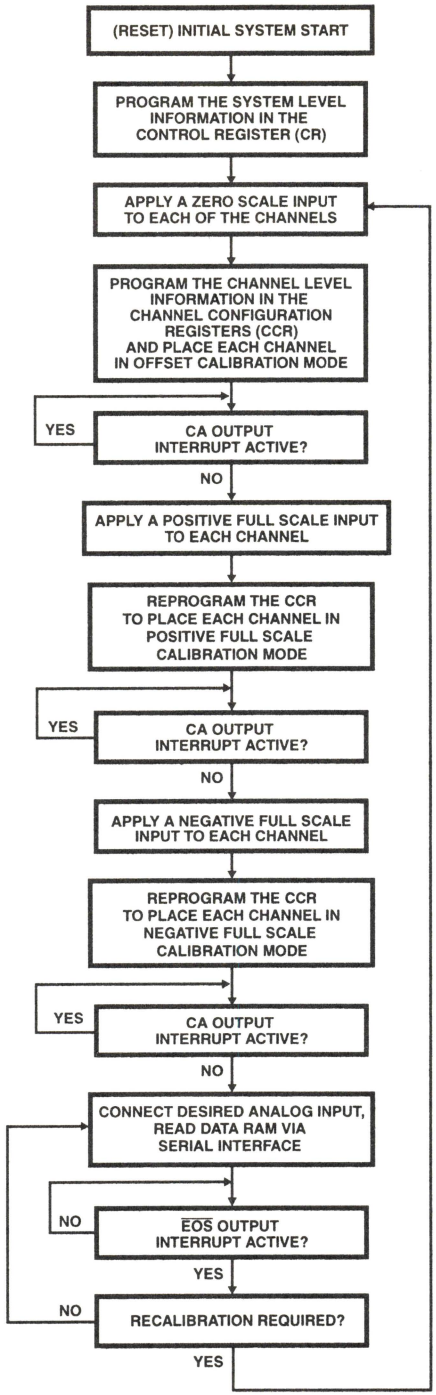


FIGURE 7. SYSTEM USAGE FLOWCHART

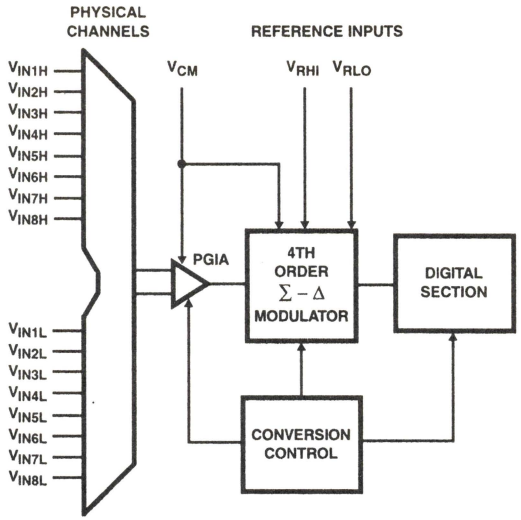


FIGURE 8. ANALOG BLOCK DIAGRAM

Analog Inputs

The analog inputs on the HI7188 are fully differential inputs with programmable gain capabilities. The inputs accept both unipolar and bipolar input signals and gains of 1, 2, 4 or 8. The gain for any given physical channel is independent of the gain of other physical channels. The gain is programmed via the Channel Configuration Register (CCR).

The input impedance of the HI7188 is dependent upon the modulator input sampling capacitors which varies with the selected PGIA gain. Table 2 shows the sampling capacitors and input impedances for the different gain settings of the HI7188. Note that this table is valid only for a 3.6864MHz master clock. If the input clock frequency is changed then the input impedance will change accordingly. The equation used to calculate the input impedance is

$$Z_{IN} = 1/(C_S \times F_S)$$

Where C_S is the internal sampling capacitance and F_S is the modulator sampling rate set by the master clock divided by six (F_S = 3.6864MHz/6 = 614.4kHz).

TABLE 2. EFFECTIVE INPUT IMPEDANCE vs GAIN

GAIN	SAMPLING RATE (kHz)	SAMPLING CAPACITOR (pF)	INPUT IMPEDANCE (kΩ)
1	614.4	4	407
2	614.4	8	203
4	614.4	16	102
8	614.4	32	51

Bipolar/Unipolar Input Ranges

The inputs can accept either unipolar or bipolar input voltages with each physical channel's mode being independent of other physical channels. Bipolar or unipolar options are chosen by programming the bipolar/unipolar ($B/\overline{U}$) bits of the Channel Configuration Registers (CCR). Programming the logical channels for either unipolar or bipolar operation does not change any of the input signal conditioning. The inputs are differential, and as a result are referenced to the voltage on the V_{INL} input. For example, if V_{INHX} is +3.75V and logical channel X is configured for unipolar operation with a gain of 1 and a V_{REF} of +2.5V, the input voltage range on the V_{INLX} input is +1.25V to +3.75V. If V_{INLX} is +1.25V and logical channel X is configured for bipolar mode with gain of 1 and a V_{REF} of +2.5V, the analog input range on the V_{INHX} input is -1.25V to +3.75V.

Multiplexer

The input multiplexer is a fully differential 8 channel device controlled by the internal microsequencer. Any number of inputs, up to 8, can be scanned and both the number of physical channels scanned and the scanning order are controlled by the users programming of the Channel Configuration Register (CCR). The output of the multiplexer feeds the input to the Programmable Gain Instrumentation Amplifier (PGIA).

External Multiplexers

For interfacing the HI7188 to external multiplexers several output pins are available. These pins include MXC, A_2, A_1 and A_0. Refer to Figure 9. The MXC pulse is active high during the modulator and integrating filter reset pulse. The pulse width is typically 14.6µs with LNR disabled and 54.6µs with LNR enabled. This signal can be used to "break before make" an external multiplexer. Referring to Figure 9, the data conversion time involves the actual input channel A/D conversion while the calibration time involves data calibration and coding of the conversion results. The address pins A_2, A_1 and A_0 describe the **logical** address which is currently being converted. The user can utilize these output pins to drive external multiplexer address pins.

The main critical issue is the external multiplexer output must switch and settle to 0.00153% (16 bits) of the final value during the MXC reset pulse and prior to Data Integration or data errors will occur. The input must be stable only during the data integration period but can be changed during the calibration period.

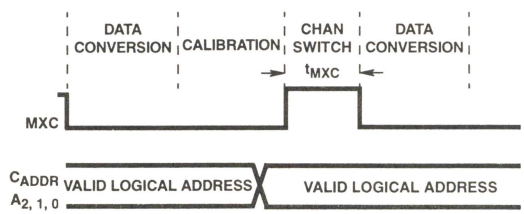


FIGURE 9. CHANNEL SWITCHING TIMING

Programmable Gain Instrumentation Amplifier

The Programmable Gain Instrumentation Amplifier (PGIA) allows the user to interface low level sensors and bridges directly to the HI7188. The PGIA has 4 selectable gain options of 1, 2, 4, and 8. The gain of each physical channel is independent of other physical channels and is programmable by writing the G1 and G0 bits in the Channel Configuration Registers (CCR).

Differential Reference Input

The reference inputs, V_{RHI} and V_{RLO}, provide a differential reference input capability. V_{RHI} must always be greater than V_{RLO} for proper operation of the device. The common mode range for these differential inputs is from AV_{SS} to AV_{DD} and the nominal differential voltage ($V_{REF} = V_{RHI} - V_{RLO}$) is +2.5V. Larger values of V_{REF} can be used with minor degradation in performance. Smaller values of V_{REF} can also be used but performance will be degraded since the system noise is larger relative to the LSB size. The full scale range of the HI7188 is defined as:

$$FSR_{BIPOLAR} = 2 \times V_{REF}/GAIN$$

$$FSR_{UNIPOLAR} = V_{REF}/GAIN$$

The reference inputs provide a high impedance dynamic load similar to the analog inputs. For proper circuit operation these pins must be driven by low impedance circuitry. Reference noise outside of the band of interest will be removed by the digital filter but excessive reference noise inside the band of interest will degrade performance.

V_{CM} Input

The V_{CM} input is the internal reference voltage for the HI7188 analog circuitry and should always be tied to the midpoint of the AV_{DD} and AV_{SS} supplies. This point provides a common mode input voltage for the internal operational amplifiers and must be driven from a low noise, low impedance source if it is not tied to analog ground. Failure to do so will result in degraded HI7188 performance. It is recommended that V_{CM} be tied to analog ground when operating off of AV_{DD} = +5V and AV_{SS} = -5V supplies. V_{CM} also determines the headroom at the upper and lower ends of the power supplies which is limited by the common mode input range where the internal operational amplifiers remain in the linear, high gain region of operation.

Sigma Delta Modulator

The sigma delta modulator is a fourth order modulator which converts the differential analog signal into a series of one bit outputs. The 1's density of this data stream provides a digital representation of the analog input. Figure 10 shows a simplified block diagram of the analog modulator front end of a Sigma-Delta A/D Converter. The input signal V_{IN} comes into a summing junction (the PGIA in this case) where the previous modulator output is subtracted from it. The resulting signal is then integrated and the output of the integrator goes into the comparator. The output of the comparator is then fed back via a one bit DAC to the summing junction. The feedback loop forces the average of the fed back signal to be equal to the input signal V_{IN}.

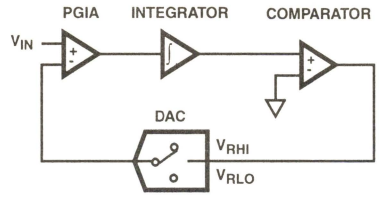


FIGURE 10. SIMPLE MODULATOR BLOCK DIAGRAM

Digital Section Description

A block diagram of the digital section of the HI7188 is shown in Figure 11. This section includes an integrating filter, averaging filters, calibration logic registers, output data RAM, digital serial interface and a clock generator.

Integrating Filters

The integrating filter receives a stream of 1s and 0s from the modulator at a rate of 614kHz. The 1's density of this data stream provides a digital representation of the analog input signal. The integrating filter provides the low pass function with a cutoff of 2kHz. The Integrating Filter works in concert with the modulator and is controlled by the same clock and reset signals. The filter integrates 201 1-bit samples from the modulator for a valid "conversion" to be completed. At that time the data is transferred to the Line Noise Rejection (LNR) Filters or straight to calibration if LNR is not selected.

Line Noise Rejection

The line noise rejection section is used to eliminate a periodic sine wave signal of either 50Hz or 60Hz line frequencies.

To understand the functionality of the HI7188 line noise rejection (LNR), it is useful to discuss the method utilized by a generic integrating analog to digital converter (ADC). This ADC uses an external summing/integrating capacitor to sum the line noise on a capacitor over one line noise cycle. The cycle period is 16.67ms and 20ms for 60Hz and 50Hz respectively. The ADC output is then the desired input with the line noise summed to zero with a conversion rate equal to the line noise frequency.

The HI7188 has the ability to do the same function as the Integrating ADC but samples the input **four** times during the line cycle (see Figure 12). For this discussion, the desired analog input signal will be zero. The HI7188 accomplishes this by instituting a four quadrant, four point running average system. The microsequencer samples all eight inputs at exactly the same point in time and for the exact amount of time for each of the four quadrants of a single line cycle and stores them separately. These four samples are then summed, on a per channels basis, which results in the same answer of the line synchronous noise as with the Integrating ADC.

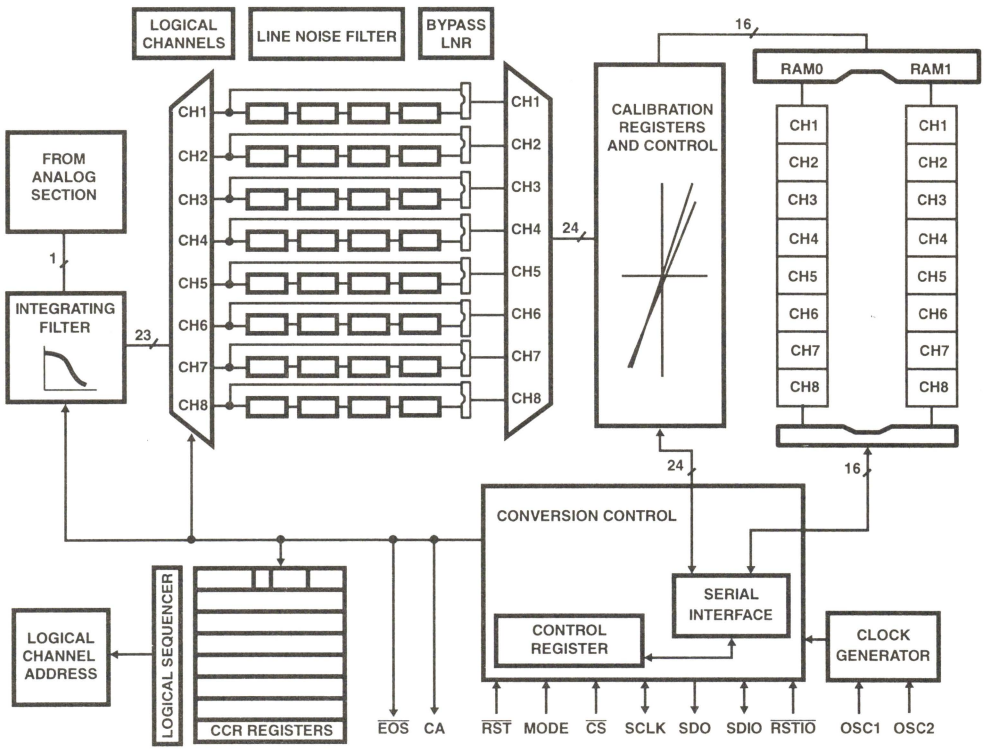


FIGURE 11. DIGITAL BLOCK DIAGRAM

A one channel example:

1. Channel 1 is sampled four times as labeled S1, S2, S3, and S4 in Figure 12. One sample for each 90 degrees quadrant of line cycle (quarter main cycle).
2. Each sample is equally spaced (From zero, S1 = 5 degrees, S2 = 95 degrees, S3 = 185 degrees and S4 = 275 degrees).
3. Each sample is of the same duration of time.
4. Samples S1 and S3 (180 degrees later) will have the equal magnitudes of line noise but have opposite signs.
5. Samples S2 and S4 (180 degrees later) will have the equal magnitudes but opposite signs.
6. The HI7188 sums the samples S1, S3, S2 and S4 which results in averaging the line noise signal to zero.
7. These four samples are placed, real time, in the 4x8 array of registers used for LNR. The next quadrant sampled (S5) replaces S1 in the running average. The new sample replaced S1 at the same point on the line cycle, 5 degrees but 360 degrees later. The line noise summation is still zero. Now for every quarter main cycle thereafter, the LNR will be updated and line noise free output will be available.

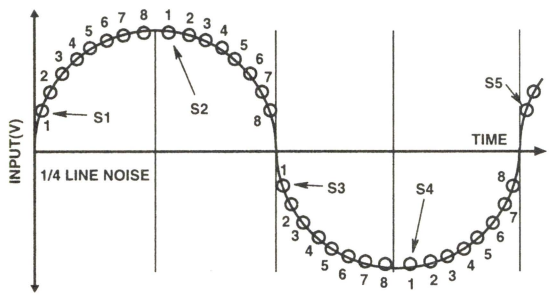


FIGURE 12. LINE NOISE CYCLE INCLUDING PATENTED TIME SPACED INPUT SAMPLING

Calibration

Calibration is the process of adjusting the conversion data based on known system offset and gain errors. For a complete system calibration to occur, the on-chip microcontroller must perform a three point calibration which involves recording conversion results for three different input conditions - "zero-scale," "positive full-scale," and "negative full-scale". With these readings, the HI7188 can null any system offset errors and calculate the positive and negative gain slope factors for the transfer function of the system. It is imperative that the zero-scale calibration be performed before either of the gain calibrations. The order of the gain calibrations is not important. Non-calibrated data can be obtained from the device by writing 000000 (h) to the Offset Calibration Register, 800000 (h) to the Positive Full Scale Calibration Register, and 800000 (h) to the Negative Full Scale Calibration Register. This sets the offset of the part to 0 and both the positive and negative gain slope factors to 1.

A calibration routine should be initiated whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the gain, bipolar, or unipolar input range.

The user may choose to ignore data during calibration or check whether any ACTIVE channel is in calibration. Bit 12, the SE bit, of the Control Register offers capability to suppress the $\overline{EOS}$ interrupt during calibration. If the SE bit is high the $\overline{EOS}$ interrupt will be suppressed if any active logical channel is in the calibration mode. If the SE bit is high and no active logical channels are in the calibration mode the $\overline{EOS}$ interrupt will function normally. If low, the suppress $\overline{EOS}$ function is disabled. To check whether any logical channel is in calibration the user can monitor the Calibration Active (CA) output pin. The CA output pin is high when at least one of the active logical channels are in calibration. If a non active logical channel is in calibration the CA will not be high. The user can monitor the CA pin to determine when all active logical channels are calibrated.

NOTE: When the user accesses the calibration RAMs, via the Serial Interface, the conversion process stops, resetting the modulator, integrating filter and clearing the $\overline{EOS}$ interrupt. When the calibration RAM I/O operation is completed the device automatically restarts beginning on logical channel 1. The contents of the CR and CCR are not affected by this I/O.

Calibration Time

The calibration time varies depending several factors including LNR (50Hz/60Hz) being enabled or disabled, and 2 point calibration. Table 3 contains a summary of the conversion time depending on these factors. Since line noise rejection is a major factor this discussion is divided accordingly.

TABLE 3. CALIBRATION TIME

LNR	LNR FREQ (Hz)	ACTIVE CHANS	CAL PNTS	EACH CAL POINT (ms)	TOTAL CAL (ms)
On	50	n/a	2	20	40
On	50	n/a	3	20	60
On	60	n/a	2	16.7	33.3
On	60	n/a	3	16.7	50.0
Off	n/a	N	2	N (0.4803)	2N (0.4803)
Off	n/a	N	3	N (0.4803)	3N (0.4803)

NOTE: N is the number of active channels. Total Cal column assumes zero switching time between calibration points.

Line Noise Rejection On

When line noise rejection is enabled, it takes 4 conversion scan periods to fill the averaging filters used for attenuating the periodic line noise. A conversion scan involves converting all 8 logical channels at a rate dependent on whether LNR is set to 50Hz or 60Hz. The scan period is 5ms (1/200Hz) and 4.167ms (1/240Hz) respectively. The number of active channels is not applicable in this calculation since the microsequencer converts on ALL logical channels to maintain LNR timing regardless of the number of user defined active channels.

Line Noise Rejection Off

Operation of the device is altered slightly when LNR is disabled. Since the microsequencer is not synchronizing for any line noise, the conversion rate increases to 260.3 conversions second/channel (10% increase). With LNR disabled, a conversion scan involves converting only the ACTIVE logical channels. When ACTIVELY converting on less than 8 channels, this is the major speed advantage over LNR enabled which sets conversion scan period based on ALL eight logical channels. Refer to Table 3.

System Offset Calibration

The system offset calibration mode is a process that allows the user to lump offset errors of external circuitry and the internal errors of the HI7188 together and null them out. This mode will convert the external differential signal applied to the V_{IN} inputs and then store that value in the offset calibration RAM for that physical channel. To invoke the system offset calibration the user applies the "zero scale" voltage to the physical channel requiring calibration, then writes the related CCR byte indicating offset calibration is required. The next time this logical channel is converted, the microsequencer performs calibration and updates the related offset RAM. Next the internal microsequencer places that logical channel back into the conversion mode and updates the CCR byte.

System Positive Full Scale Calibration

The system positive full scale calibration mode is a process that allows the user to lump positive gain errors of external circuitry and the internal gain errors of the HI7188 together to calculate the positive transfer function of the system. This mode will convert the external differential signal applied to the V_{IN} inputs and then store that value in the system positive full Scale calibration RAM for that physical channel. To invoke the system positive full scale calibration the user applies the "positive full scale" voltage to the physical channel requiring calibration, then writes the related CCR byte indicating positive full scale calibration is required. The next time this logical channel is converted, the microsequencer performs calibration and updates the related system positive full scale calibration RAM. Next the internal microsequencer places that logical channel back into the conversion mode and updates the CCR byte.

System Negative Full Scale Calibration

The system negative full scale calibration mode is a process that allows the user to lump negative gain errors of external circuitry and the internal gain errors of the HI7188 together to calculate the negative transfer function of the system. This mode will convert the external differential signal applied to the VIN inputs and then store that value in the system negative full scale calibration RAM for that physical channel. To invoke the system negative full scale calibration the user applies the "negative full scale voltage", which must be equal to Vref, to the physical channel requiring calibration, then writes the related CCR byte indicating negative full scale calibration is required(see note below). The next time this logical channel is converted, the microsequencer performs calibration and updates the related system negative full scale calibration RAM. Next the internal microsequencer places that logical channel back into the conversion mode and updates the CCR byte.

TEMPORARY NOTE: In bipolar mode, the user MUST perform negative full scale calibration with the exact differential voltage applied to the Vref pins, otherwise large errors will occur at the zero crossing point. During normal conversions, the error occurs when the input is at the offset calibration point. At this point, plus or minus 1/2 LSB, the output code will be either the true half scale reading of 7FFF/8000 (offset binary coding) or negative full scale 0000. This problem has been corrected with the HI7188A.

Offset and Gain Adjust Limits

Whenever a calibration mode is used, there are limits to the amount of offset and gain which can be adjusted. For both bipolar and unipolar modes the minimum and maximum input spans are 0.2 x V_{REF}/GAIN and 1.2 x V_{REF}/GAIN respectively. In the unipolar mode the offset plus the span cannot exceed the 1.2 x V_{REF}/GAIN limit. So, if the span is at its minimum value of 0.2 x V_{REF}/GAIN, the offset must be less than 1 x V_{REF}/GAIN. In bipolar mode the span is equidistant around the voltage used for the zero scale point. For this mode the offset plus half the span cannot exceed 1.2 x V_{REF}/GAIN. If the span is at ±0.2 x V_{REF}/GAIN, then the offset can not be greater than ±2 x V_{REF}/GAIN.

Range Detection

In addition to the calibration process, the converter detects over range above positive full scale and under range below minus full scale conditions. Over or under range detection affects the output data coding as described in the Data Coding section.

Over range detection is identical for both bipolar and unipolar operation. Over range is detected by comparing the offset corrected filter output to the positive gain coefficient. If the current offset corrected filter value is greater than the positive gain coefficient, an over range condition is detected.

In unipolar mode, under range is detected by sampling the sign bit of the offset calibrated data. If the sign bit is logic 1, signifying a negative voltage, an under range condition exists.

In bipolar mode, under range is detected by comparing the offset corrected filter output to the negative gain coefficient. If the current offset corrected filter value is less than the negative gain coefficient, an under range condition is detected.

Data Coding

The calibrated data can be obtained in one of various numerical codes depending on the bipolar/unipolar mode bit and the two's complement coding bit. In bipolar mode, if the two's complement bit is high, the output is two's complement. In bipolar mode, offset binary coding is used when the two's complement coding bit is low. In unipolar mode, only binary coding is available and the two's complement coding bit is a don't care.

The output coding for the HI7188 is shown in Tables 4 and 5. V_{ZS} represents the applied zero scale input during system offset calibration. V_{PFS} represents the applied positive full scale input during system positive full scale calibration. V_{NFS} represents the applied negative full scale input during system negative full scale calibration.

TABLE 4. BIPOLAR MODE OUTPUT CODES (HEX)

INPUT VOLTAGE	TWO'S COMPLEMENT CODE	OFFSET BINARY CODE
>(V_{PFS} - 1.5 LSB)	7FFF	FFFF
V_{PFS} - 1.5 LSB	7FFF/7FFE	FFFF/FFFE
V_{ZS} - 0.5 LSB	0000/FFFF	8000/7FFF
V_{NFS} + 0.5 LSB	8001/8000	0001/0000
<(V_{NFS} + 0.5 LSB)	8000	0000

TABLE 5. UNIPOLAR MODE DATA OUTPUT CODES (HEX)

INPUT VOLTAGE	BINARY CODE
>(V_{PFS} - 1.5 LSB)	FFFF
V_{PFS} - 1.5 LSB	FFFF/FFFE
V_{PFS}/2 - 0.5 LSB	8000/7FFF
V_{ZS} + .5 LSB	0001/0000
<(V_{ZS} + 0.5 LSB)	0000

When the range detection logic determines an over range, the converter output will clamp at the >(V_{PFS} - 1.5 LSB) output as described in Tables 4 and 5. When the range detection logic determines an under range, the converter output will clamp at the <(V_{NFS} + 0.5 LSB) output described in Table 4 or the <(V_{ZS} + 0.5 LSB) output described in Table 5.

Data RAM

The Data RAM block is comprised of two 8 x 16 memory elements which store conversion results after calibration and data coding. Two RAMs are required to allow a one channel scan buffer per logical channel. The user can only READ from the data RAM. For illustration, these elements are labeled RAM0 and RAM1. The RAMs are configured such that when one is internally writable the other is readable via serial I/O. The following paragraphs describe the data RAM operation. Please refer to the Functional Block Diagram.

For example, from initialization, RAM0 is writable, RAM1 is readable, $\overline{EOS}$ is inactive. Conversion completes on all active logical channels (RAM0 stores conversion N data) and the $\overline{EOS}$ interrupt is generated. Internally, the microsequencer switches RAM0 to readable, RAM1 to writable. The user can read the data RAM to obtain N conversion results, clearing the $\overline{EOS}$ interrupt.

The next conversion N+1 completes on all active logical channels (RAM1 stores N+1 data). If a data RAM (RAM0 containing N data) read has been completed before the N+1 conversion scan has completed, RAM1 will switch to being readable and RAM0 is writable. This is normal operation and no conversion results are lost.

If the data RAM (RAM0 containing N data) is not completely read before the N+1 conversion is completed, there are two possible results.

1. The data RAM read has not been started (RAM0 containing N data), EOS remains active low and the microsequencer will switch RAM1 to be readable and RAM0 to be writable. This has the effect of overwriting conversion N with N+2.
2. The data RAM (RAM0 containing N data) read has been started but is not complete, the read pointer remains with RAM0 and the write pointer remains with RAM1. This has the effect of overwriting conversion N+1 with N+2 before N+1 can be read, therefore conversion N+1 is lost.

Clocking/Oscillators

The master clock of the HI7188 can be supplied by either a crystal connected between the OSC_1 and OSC_2 pins as shown in Figure 13A or a CMOS compatible clock signal connected to the OSC_1 pin as shown in Figure 13B and floating the OSC_2 pin. The master clock is used by the internal clock generator to derive the clock edges required for both analog and digital sections. The HI7188 is designed or a 3.6864MHz clock to maintain Line Noise Rejection.

Crystal Operation

Using a crystal to generate the clock, care must be taken to minimize any external stray capacitance/inductance seen by the OSC_1 and OSC_2 pins. If care is not taken, the feedback (crystal) loop noise will result in a non reliable master clock, which in turn, will produce erroneous conversion results. The crystal should be connected as close to the HI7188 device as physically possible. If you cannot meet these requirements, we would recommend you use an External CMOS Clock instead of the crystal.

External CMOS Clock Operation

When driving the HI7188 with an external CMOS clock, the clock should never be turned off. If the clock is turned off, the device should be re-synchronized by resetting either manually via the RESET pin or by the following special software instructions. If the device is not re-synchronized erroneous conversion results may be observed. The hardware reset will clear all registers and RAMs as defined in the data sheet. The software reset is achieved by either performing an I/O access of any calibration RAM or cycling the device through a sleep cycle.

Calibration RAM Access

To re-synchronize the conversion process the user may perform an I/O access of any calibration RAM (read or write). When the user performs this I/O access the microsequencer stops the conversion process, resets the modulator, digital filter and waits until the I/O is complete. After the I/O is completed the microsequencer automatically restarts the conversion process.

Sleep Cycle

Another method to re-synchronize the conversion process is to cycle the device through a sleep cycle. The user places the device in SLEEP mode by writing the SLP bit (CR<3>) of the Control Register to logic one. The microsequencer will stop the conversion process, reset the conversion pointer to logical channel one, clear the four line noise rejection filters and deactivate $\overline{EOS}$. The serial interface, calibration/data RAMs, CR and CCR are not affected.

To return from sleep mode the user changes the SLP bit from high to low. This restarts the conversion process beginning with logical channel 1. If line noise rejection (LNR) is enabled, it takes four complete scans (all eight channels) to

refill the four line noise rejection filters before an $\overline{EOS}$ interrupt. If LNR is not enabled, it takes one conversion scan of only the active channels before an $\overline{EOS}$ interrupt. Recalibration is not required since the calibration RAMs are not effected by the sleep operation.

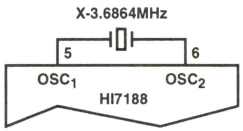


FIGURE 13A. Crystal Operation

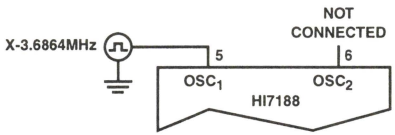


FIGURE 13B. External CMOS clock operation

Serial Interface

The HI7188 has a flexible, synchronous serial communication port to allow easy interfacing to most industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6805/11, SPI and Intel 8051 SSR protocols. The interface supports 2-wire transfers of reading and writing on a single bidirectional line (SDIO) or 3-wire transfers of writing on SDIO and reading on the SDO line.

The Interface allows read/write access to the Control Register, Channel Configuration Registers, and Calibration RAMs. The interface allows read only access to the data RAM (refer to Table 7). The interface is byte organized with each register byte having a specific address. Single or multiple byte transfers are supported. In addition, the interface allows flexibility as to the byte and bit access order. That is, the user can specify MSB/LSB first bit positioning and can access bytes in ascending/descending order from any byte position.

Serial Interface Clock

The HI7188 supports two serial interface clock(SCLK) modes for all interface timing. This allows the greatest flexibility for different types of systems where the HI7188 can act either as master in the system (it provides the serial interface clock) or as slave (an external clock is provided to the HI7188). These two modes are defined as self clocking and external clocking respectively. Regardless of the clocking mode selected, all data is registered into the HI7188 on the rising edge of the SCLK while all data is driven out on the falling edge of SCLK. The HI7188 interface is designed to work with clock stalling in either high or low state. The clock mode is determined by the logic level applied to the MODE pin.

Synchronous Self Clocking

The device in a self-clocking scheme if the MODE pin is high. This defines the SCLK pin as an output which provides the serial clock signal used for the transfer of all data to and from the HI7188. This self-clocking mode can be used with processors which allow an external device to clock their serial port. The frequency of SCLK is one eighth of the external crystal connected between the OSC_1 and OSC_2 pins. The HI7188 is designed for a 3.6864MHz crystal which sets SCLK to 460.8kHz.

Synchronous External Clocking

The HI7188 is in a external clocking scheme if the MODE pin is low. This defines the SCLK pin as an input and an external clock must be provided to the SCLK pin. This external clocking mode is designed for direct interface to systems which provide a serial clock output which is synchronized to the serial data output. The maximum frequency of the external SCLK is 5MHz.

Burst RAM Access

The Data RAM, System Offset calibration RAM, System Positive Full Scale Calibration RAM and System Negative Full Scale Calibration RAM can **only** be accessed in a continuous RAM "Burst". RAM burst transfers are special instructions that perform a continuous data transfer for all bits of that RAM. That is, individual bytes of any RAM cannot be accessed without reading all of the bytes. See Table 7. Each transfer occurs such that the first word transferred corresponds to the first logical channel converted as specified in the Channel Configuration Register (CCR). The first byte transferred for each word is controlled by the RB bit of the instruction byte and the bit position is determined by the Control Register (CR) MSB/LSB bit. The number of words transferred is specified by the CR bits that describe the number of logical channels being converted as well as the size of the destination RAM. This transfer mode reduces the overhead of multiple IR writes as compared to individual byte access. The following two examples are useful in understanding the RAM burst transfer instructions.

Example 1. The physical channel conversion order as specified by the CCRs is 8, 2, 3, 4, 5, 6, 1, 7. The HI7188 is setup via the Control Register to convert 8 logical channels. The IR byte written is 0xx11100 (read the data RAM). The following occurs: After completing the IR write, 16 bytes of data will be transferred from the HI7188. The first byte transferred will be the most significant byte of the physical channel 8 conversion results. The second byte will be the least significant byte of the physical channel 8 conversion results. This pattern of most significant byte followed by least significant byte will repeat, in order for physical channels 2, 3, 4, 5, 6, 1, 7.

Example 2. The physical channel conversion order as specified by the CCRs is 8, 2, 3, 4, 5, 6, 1, 7. The HI7188 is setup via the Control Register to convert only 3 logical channels. The IR byte written is 1xx01101 (write the offset RAM). The following occurs: After completing the IR write, 9 bytes of data will be written to the offset RAM (recall that the Offset Calibration register is 3 bytes wide). The first byte is the least significant byte used for offset calibration of physical channel 8. The second byte will be the middle byte used for offset calibration of physical channel 8. The third byte will be the most significant byte used for offset calibration of physical channel 8. This pattern of least significant byte to most significant byte will repeat for all logical channels converted in the logical channel order as described above. For example, the last byte transferred will be the most significant byte of physical channel 3 used for offset calibration.

NOTE: When the user accesses the calibration RAMs, via the Serial Interface, the conversion process stops, resetting the modulator, integrating filter and clearing the $\overline{EOS}$ interrupt. When the calibration RAM I/O operation is completed the device automatically restarts beginning on logical channel 1. The contents of the CR and CCR are not affected by this I/O.

Detailed Register Descriptions

Instruction Register

The instruction register is an 8 bit register which is used during a communications cycle for setting up read/write operations. Below are the bit assignments.

INSTRUCTION REGISTER (BYTE)

MSB	6	5	4	3	2	1	LSB
$\overline{R}/W$	NB1	NB0	RB	A3	A2	A1	A0

$\overline{R}/W$ - Bit 7 of the Instruction Byte determines whether phase 2 of the communication cycle will be a read or write operation. If $\overline{R}/W$ is logic 1, a write transfer will occur in phase 2 of the communication cycle. If $\overline{R}/W$ is logic 0, a read transfer will occur in phase 2 of the communication cycle.

NB1, NB0 - Bits 6 and 5 of the Instruction Byte determine the number of bytes that will be transferred during phase 2 of a communication cycle, if a register is selected for I/O access. If a RAM is selected for IO access, these bits are don't care. Any number of bytes from 1 to 4 is allowed. See Tables 6 and 7.

TABLE 6. MULTIPLE BYTE ACCESS BITS

NB1, NB0 IR [6:5]	DESCRIPTION
00	Transfer 1 Byte
01	Transfer 2 Bytes
10	Transfer 3 Bytes
11	Transfer 4 Bytes

RB - Bit 4 is used to determine the byte order when accessing a RAM address. When accessing a RAM address, if RB = 1, the data format is most significant byte first to least significant byte. When accessing a RAM address, if RB = 0, the data format is least significant byte first to most significant byte. When accessing a register address, this bit is a don't care.

A3, A2, A1, A0 - Bits 3 and 2 (A3 and A2) of the Instruction Byte determine which of the three internal registers will be accessed or if both bits are set (11b), that a RAM access is active. For register addresses, bits 1 and 0 (A1 and A0) determine which byte of that register will be accessed first. For RAM access (A3 = 1, A2 = 1), bits 1 and 0 (A1 and A0) determine which RAM is the source or destination.

TABLE 7. INTERNAL REGISTER ADDRESS

$\overline{R}/W$ IR [7]	NB1, NB0 IR [6:5]	A3, A2, A1, A0 IR [3:0]	DESCRIPTION
0/1	00	0000	CR, start byte 0, 1 byte transfer
0/1	01	0000	CR, start byte 0, 2 byte transfer
0/1	00	0001	CR, start byte 1, 1 byte transfer
0/1	01	0001	CR, start byte 1, 2 byte transfer
0/1	00	0100	CCR #1, start byte 0, 1 byte transfer

TABLE 7. INTERNAL REGISTER ADDRESS (Continued)

$\overline{R}/W$ IR [7]	NB1, NB0 IR [6:5]	A3, A2, A1, A0 IR [3:0]	DESCRIPTION
0/1	00	0101	CCR #1, start byte 1, 1 byte transfer
0/1	00	0110	CCR #1, start byte 2, 1 byte transfer
0/1	00	0111	CCR #1, start byte 3, 1 byte transfer
0/1	01	0100	CCR #1, start byte 0, 2 byte transfer
0/1	01	0101	CCR #1, start byte 1, 2 byte transfer
0/1	01	0110	CCR #1, start byte 2, 2 byte transfer
0/1	01	0111	CCR #1, start byte 3, 2 byte transfer
0/1	10	0100	CCR #1, start byte 0, 3 byte transfer
0/1	10	0101	CCR #1, start byte 1, 3 byte transfer
0/1	10	0110	CCR #1, start byte 2, 3 byte transfer
0/1	10	0111	CCR #1, start byte 3, 3 byte transfer
0/1	11	0100	CCR #1, start byte 0, 4 byte transfer
0/1	11	0101	CCR #1, start byte 1, 4 byte transfer
0/1	11	0110	CCR #1, start byte 2, 4 byte transfer
0/1	11	0111	CCR #1, start byte 3, 4 byte transfer
0/1	00	1000	CCR #2, start byte 0, 1 byte transfer
0/1	00	1001	CCR #2, start byte 1, 1 byte transfer
0/1	00	1010	CCR #2, start byte 2, 1 byte transfer
0/1	00	1011	CCR #2, start byte 3, 1 byte transfer
0/1	01	1000	CCR #2, start byte 0, 2 byte transfer
0/1	01	1001	CCR #2, start byte 1, 2 byte transfer
0/1	01	1010	CCR #2, start byte 2, 2 byte transfer
0/1	01	1011	CCR #2, start byte 3, 2 byte transfer
0/1	10	1000	CCR #2, start byte 0, 3 byte transfer
0/1	10	1001	CCR #2, start byte 1, 3 byte transfer
0/1	10	1010	CCR #2, start byte 2, 3 byte transfer
0/1	10	1011	CCR #2, start byte 3, 3 byte transfer
0/1	11	1000	CCR #2, start byte 0, 4 byte transfer
0/1	11	1001	CCR #2, start byte 1, 4 byte transfer
0/1	11	1010	CCR #2, start byte 2, 4 byte transfer
0/1	11	1011	CCR #2, start byte 3, 4 byte transfer
0	xx	1100	Data RAM burst transfer, least significant byte first, READ ONLY
0	xx	1100	Data RAM burst transfer, most significant byte first, READ ONLY
0/1	xx	1101	Offset RAM burst transfer, least significant byte first.
0/1	xx	1101	Offset RAM burst transfer, most significant byte first.
0/1	xx	1110	Positive full scale RAM burst transfer, least significant byte first.
0/1	xx	1110	Positive full scale RAM burst transfer, most significant byte first.
0/1	xx	1111	Negative full scale RAM burst transfer, least significant byte first.
0/1	xx	1111	Negative full scale RAM burst transfer, most significant byte first.

Control Register

The Control Register (CR) is 16 bits wide and contains information that determines operating mode and the system/chip level configuration. This configuration applies to all logical channels and cannot be modified at the channel level. Following are the bit assignments:

CONTROL REGISTER BYTE 1

MSB	14	13	12	11	10	9	LSB
T3	**T2**	**T1**	**$\overline{\text{CHOP}}$**	**SE**	**LNR**	**FS**	**TC**

CONTROL REGISTER BYTE 0

MSB	6	5	4	3	2	1	LSB
N2	**N1**	**N0**	**TP**	**SLP**	**BD**	**$\overline{\text{MSB}}$**	**SDL**

T3, T2, T1 - Bits 15, 14 and 13 are reserved and MUST always be logic zero for normal operation. These bits are low after $\overline{\text{RESET}}$ is applied.

$\overline{\text{CHOP}}$. Bit 12 is the active low chop bit used to determine whether the chopper stabilized amplifier is used or bypassed. This bit is low (chop on) after $\overline{\text{RESET}}$ is applied.

SE. Bit 11 is the active high suppress $\overline{\text{EOS}}$ bit. If high, the $\overline{\text{EOS}}$ interrupt will not go active when any logical channel is in calibration mode. If this bit is high and no logical channels are in the calibration mode, or this bit is low, $\overline{\text{EOS}}$ functionality is as previously described. This bit allows the user to suppress false $\overline{\text{EOS}}$ interrupts during calibration. Only logical channels that are actively being converted are considered. That is, if only two logical channels are being converted but the CCR byte for a non active logical channel is in a calibration mode, the $\overline{\text{EOS}}$ functionality is active. This bit is low (suppress $\overline{\text{EOS}}$ off) after $\overline{\text{RESET}}$ is applied.

LNR. Bit 10 is the active high line noise rejection(LNR) bit. If high LNR is selected. This bit is low (LNR off) after $\overline{\text{RESET}}$ is applied.

FS. Bit 9 is the 50Hz/60Hz frequency select bit. If bit 9 is high, the clock generation logic synchronizes conversions for proper rejection of 50Hz line noise. If bit 9 is low, the clock generation logic synchronizes conversions for proper rejection of 60Hz line noise. This bit is low (60Hz LNR) after $\overline{\text{RESET}}$ is applied.

TC. Bit 8 is the active high two's complement bit used to select between 2's complementary and offset binary data coding for bipolar mode. In bipolar mode, a high selects two's complement; when low data is offset binary. Note that in unipolar mode the binary data coding is not affected by the TC bit. This bit is low (offset binary data) after RESET is applied.

N2, N1, N0. Bits 7, 6 and 5 are the bits that specify the number of active logical channels to be converted. See Table 8. These bits are low (one active channel) after RESET is applied.

TABLE 8. NUMBER OF CONVERSION CHANNELS

N2, N1, N0 CR [7:5]	NUMBER OF CHANNELS TO CONVERT
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

TP - Bit 4 is the active high two point calibration bit. When high, the positive gain slope factor is used for both positive and negative voltages. This bit is low (normal three point cal) after $\overline{\text{RESET}}$ is applied.

SLP - Bit 3 is the active high sleep mode bit used to put the device in a low power/standby mode. When high, conversion stops and the conversion pointer is reset to logical channel 1. The four line noise rejection filters are cleared and $\overline{\text{EOS}}$ is deactivated. The serial interface, calibration/data RAMs, CR and CCR are not affected.

To return from sleep mode the user changes this bit from high to low. This restarts the conversion process beginning with logical channel 1. If line noise rejection is enabled, it takes four complete scans (all active channels) to refill the four line noise rejection filters before an $\overline{\text{EOS}}$ interrupt. If line noise rejection not enabled, it takes 1 complete scan before an $\overline{\text{EOS}}$ interrupt.

This bit is low (sleep mode off) after $\overline{\text{RESET}}$ is applied.

BD. Bit 2 is the byte direction bit used to determine either ascending or descending order access for multi-byte transfers. When high, ascending order is enabled. When low, descending order is enabled. This bit is low (descending order) after $\overline{\text{RESET}}$ is applied.

$\overline{\text{MSB}}$. Bit 1 bit direction bit used to select whether a serial data transfer is MSB or LSB first. When low, MSB first mode is enabled while high selects LSB first. This bit is low (MSB first) after $\overline{\text{RESET}}$ is applied.

SDL. Bit 0 selects a two-wire or three-wire transfer protocol of the serial interface. When low, two-wire data transfers are done using the SDIO pin. Both data in and out of the part is uses the by-directional SDIO pin. When high, three-wire data transfers are done using the SDIO and SDO pins. Data into the part uses the SDIO pin while data out uses the SDO pin. This bit is low (two-wire, SDIO exclusively) after $\overline{\text{RESET}}$ is applied.

Channel Configuration Registers

The HI7188 Channel Configuration Registers (CCR) comprise a 64-bit memory element that defines the logical channel conversion order as well as each logical channel specific data such as physical channel address, mode, gain, and bipolar/unipolar operation. The 64 bits are divided into two 32 bit register blocks referred to as CCR#2 and CCR#1. Each register contains four

bytes pertaining to four logical channels. The register may be accessed 1, 2, 3 or 4 bytes at a time. Please refer to Table 10 to determine physical address assignments within the CCR and Table 9 for logical channel assignment. The physical channel conversion order is defined based on it's location in the CCR blocks. For example, if the CCR #2 <31:24> is set with the CCR <2:0> = 100, then physical channel 5 will be converted first. The CCR is byte wide accessible via the Serial Interface allowing the user to change the individual logical channel configuration on the fly. Following are the bit assignments.

TABLE 9. CHANNEL CONFIGURATION REGISTER

BLOCK	BIT LOCATION	DESCRIPTION
CCR #2	<31:24>	1st Logical Channel
CCR #2	<23:16>	2nd Logical Channel
CCR #2	<15:8>	3rd Logical Channel
CCR #2	<7:0>	4th Logical Channel
CCR #1	<31:24>	5th Logical Channel
CCR #1	<23:16>	6th Logical Channel
CCR #1	<15:8>	7th Logical Channel
CCR #1	<7:0>	8th Logical Channel

CHANNEL CONFIGURATION REGISTER (BYTE)

MSB	6	5	4	3	2	1	LSB
CH2	**CH1**	**CH0**	**B/$\overline{U}$**	**MD1**	**MD0**	**G1**	**G0**

CH2, CH1, CH0 - Bits 7, 6, 5 of the channel configuration byte determine which physical inputs are used as shown in Table 10.

TABLE 10. ACTIVE CHANNEL DECODE

CH2, CH1, CH0 CCR [2:0]	PHYSICAL INPUT PINS
000	V_{INH1}, V_{INL1}
001	V_{INH2}, V_{INL2}
010	V_{INH3}, V_{INL3}
011	V_{INH4}, V_{INL4}
100	V_{INH5}, V_{INL5}
101	V_{INH6}, V_{INL6}
110	V_{INH7}, V_{INL7}
111	V_{INH8}, V_{INL8}

B/$\overline{U}$ - Bit 4 of the channel configuration byte determine bipolar or unipolar mode. If Logic 1, bipolar mode is selected while logic 0 selects unipolar mode.

MD1, MD0 - Bit 3 and 2 of the channel configuration byte are the channel Mode bits. This defines the mode of operation for that logical channel, please see Table 11. All calibration modes automatically return to conversion mode after calibration is complete.

TABLE 11. HI7188 OPERATIONAL MODES

MD1	MD0	OPERATIONAL MODE
0	0	Conversion
0	1	System Offset Calibration
1	0	System Positive Full Scale Calibration
1	1	System Negative Full Scale Calibration

G1, G0 - Bit 1 and 0 defines the PGIA gain of 1, 2, 4 or 8. Please refer to Table 12.

TABLE 12. CHANNEL GAIN

G1, G0 CCR [1:0]	PGIA CHANNEL GAIN
00	1
01	2
10	4
11	8

Serial Interface Pin Description

The serial I/O port is a bidirectional port which is used to read and write the internal registers. The port contains two data lines, a synchronous clock, and two status flags. Figure 14 shows a diagram of the serial interface lines.

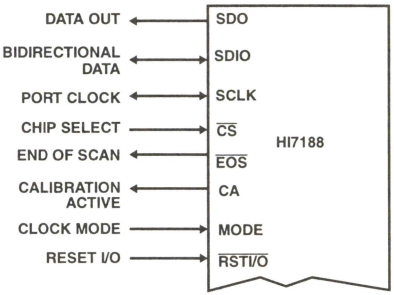


FIGURE 14. HI7188 SERIAL INTERFACE

SDO - Serial Data Out. Data is read from this line using those protocols with separate lines for transmitting and receiving data. An example of such a standard is the Motorola Serial Peripheral Interface (SPI) using the 68HC05 and 68HC11 family of microcontrollers, or other similar processors. In the case of using bidirectional data transfer on SDIO, the SDO does not output data and is set in a high impedance state.

SDIO - Serial Data In or Out. Data is always written to the device on this line. However, this line can be used as a bidirectional data line. This is done by properly setting up the Control Register. Bidirectional data transfer on this line can be used with Intel standard serial interfaces (SSR, Mode 0) in MCS51 and MCS96 family of microcontrollers, or other similar processors.

SCLK - Serial Clock. The serial clock pin is used to synchronize data to and from the HI7188 and to run the port state machines. In Synchronous External Clock Mode, SCLK is configured as an input, is supplied by the user, and can run up to a 5MHz rate. In Synchronous Self Clocking Mode, SCLK is configured as an output and runs at $OSC_1/8$ = 460.8kHz.

$\overline{CS}$ - Chip Select. This signal is an active low input that allows more than one device on the same serial communication lines. The SDO and SDIO will go to a high impedance state when this signal is high. If driven high during any communication cycle, that cycle will be suspended until $\overline{CS}$ reactivation. Chip select can be tied low in systems that maintain control of SCLK.

$\overline{EOS}$ - End Of Scan. Signals the end of a logical channel scan (all programmed logical channels have been converted) and data is available for reading. $\overline{EOS}$ is useful as an edge or level sensitive interrupt signal to a microprocessor or microcontroller. $\overline{EOS}$ low indicates that new data is available and the Data RAM can be read. $\overline{EOS}$ will return high upon completion of a complete Data RAM read cycle. Please refer to the Data RAM section for details.

CA - Calibration Active. This pin is high if any active logical channel is in the calibration mode and stays high for the entire scan period. CA checks only those channels that are actively being converted on. For example, if the HI7188 is programmed to convert only two channels and any of the CCR bytes of the six nonactive channels are in the calibration mode, CA will NOT go active. The user can monitor the CA output to determine when all active channels have completed calibration.

MODE - Mode. This input is used to select between Synchronous Self Clocking Mode (high) or the Synchronous External Clocking Mode (low).

$\overline{RSTI/O}$ - Reset I/O. This active low asynchronous input is used to reset the serial interface state machine. This reset only affects the I/O logic and does not affect the Control Register, Channel Configuration Register or Calibration RAMs. This effectively aborts any communication cycle and places the device in a standby mode awaiting the next IR cycle.

Serial Interface Communication

It is useful to think of the HI7188 interface in terms of communication cycles. Each communication cycle happens in 2 phases. The first phase is the writing of an instruction byte while the second phase is the data transfer as described by the instruction byte. It is important to note that phase 2 of the communication cycle can be a single byte or a multi-byte transfer of data including a Burst RAM read/write. It is up to the user to maintain synchronism with respect to data transfers. If the system processor "gets lost", during an I/O operation, the only way to recover is to reset the Serial Interface via a $\overline{RSTI/O}$. Figure 15 shows both a 2-wire and a 3-wire data transfer.

Instruction Byte Phase

The instruction byte phase initiates a data transfer sequence. The processor writes an eight bit byte to the "Instruction Register", known as the "Instruction Byte". The instruction byte informs the HI7188 about the Data cycle phase activities and includes the following information:

- Read or Write Cycle
- Number of Bytes to be Transferred
- Which Register and Starting Byte to be Accessed

Data Cycle Phase

In the data cycle phase, data transfer takes place as defined by the Instruction Register Byte. See Write Operation and Read Operation sections for detailed descriptions. It is important to note that phase 2 of the communication cycle can be a multi-byte transfer of data.

For example, the 4 byte Channel Configuration register can be read using one multi-byte communication cycle rather than four single byte communication cycles. After phase 2 is completed the HI7188 I/O logic enters a standby mode while waiting to receive a new instruction byte. It is up to the user to maintain synchronism with respect to data transfers. If the system processor "gets lost" the only way to recover is to reset the HI7188.

Serial Interface Format

Several formats are available for reading from and writing to the HI7188 registers in both the 2-wire and 3-wire protocols.

Please refer to Figure 15. A portion of these formats is controlled by the CR<2:1> (BD and $\overline{MSB}$) bits which control the byte direction and bit order of a data transfer respectively. These two bits can be written in any combination but only the two most useful will be discussed here. The first combination is to reset both the BD and $\overline{MSB}$ bits (BD = 0, $\overline{MSB}$ = 0). This sets up the interface for descending byte order and MSB first format. When this combination is used the user should always write the instruction register such that the starting byte is the most significant byte address. For example, read three bytes of data starting with the most significant byte. The first byte read will be the most significant in MSB to LSB format. The next byte will be the next least significant (recall descending byte order) again in MSB to LSB order. The last byte will be the next lesser significant byte in MSB to LSB order. THE ENTIRE WORD WAS READ MSB TO LSB format. The second combination is to set both the BD and $\overline{MSB}$ bits to 1. This sets up the interface for ascending byte order and LSB first format. When this combination is used the user should always write the instruction register such that the starting byte is the least significant byte address. For example, read three bytes of data starting with the least significant byte. The first byte read will be the least significant in LSB to MSB format. The next byte will be the next greater significant (recall ascending byte order) again in LSB to MSB order. The last byte will be the next greater significant byte in LSB to MSB order. THE ENTIRE WORD WAS READ LSB TO MSB format. After completion of each communication cycle, The HI7188 interface enters a standby mode while waiting to receive a new instruction byte.

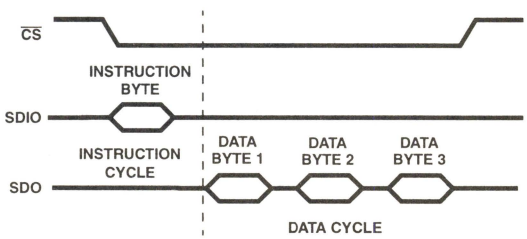


FIGURE 15. 3-WIRE, 3 BYTE READ TRANSFER

Die Characteristics

DIE DIMENSIONS:

215 mils x 257 mils
(5466µm x 6536µm)

METALLIZATION:

Type: AlSiCu
Thickness: Metal 2 16kÅ
Metal 1 6kÅ

SUBSTRATE POTENTIAL:

AV_{SS}

PASSIVATION:

Type: Sandwich
Nitride Thickness: 8kÅ
USG Thickness: 1kÅ

WORST CASE CURRENT DENSITY:

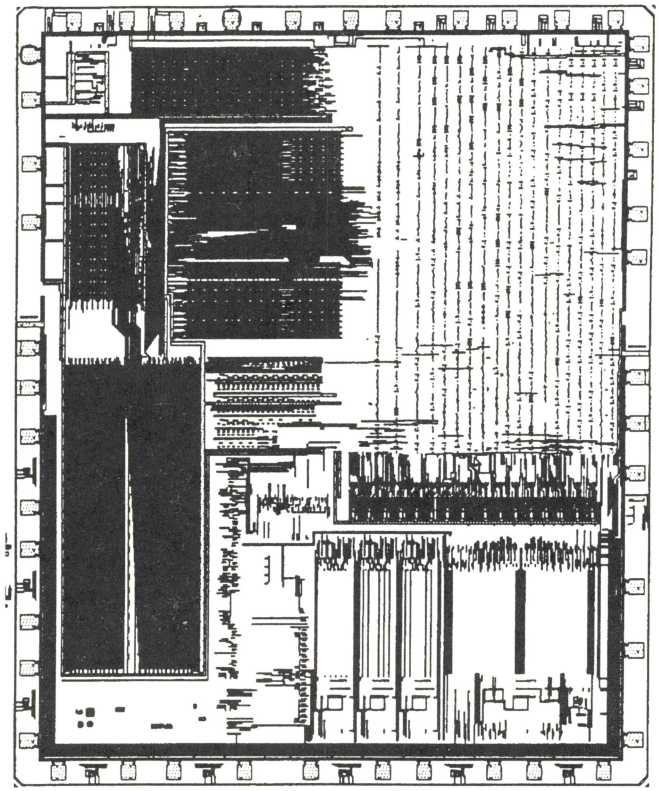
$<2.0 \times 10^5$ A/cm^2

PROCESS:

HBCIO

Metallization Mask Layout

HI7188



HARRIS SEMICONDUCTOR

HI7190

24-Bit, High Precision, Sigma Delta A/D Converter

August 1997

Features

- 22-Bit Resolution with No Missing Code
- 0.0007% Integral Non-Linearity (Typ)
- 20mV to ±2.5V Full Scale Input Ranges
- Internal PGIA with Gains of 1 to 128
- Serial Data I/O Interface, SPI Compatible
- Differential Analog and Reference Inputs
- Internal or System Calibration
- -120dB Rejection of 60/50Hz Line Noise
- Settling Time of 4 Conversions (Max) for a Step Input

Applications

- Process Control and Measurement
- Industrial Weight Scales
- Part Counting Scales
- Laboratory Instrumentation
- Motion Control
- Seismic Monitoring
- Magnetic Field Monitoring
- Intruder Detection
- Medical Patient Monitoring
- Additional Reference Literature
  - AN9504 "A Brief Intro to Sigma Delta Conversion"
  - TB329 "Harris Sigma Delta Calibration Technique"
  - AN9505 "Using the HI7190 Evaluation Kit"
  - TB331 "Using the HI7190 Serial Interface"
  - AN9527 "Interfacing HI7190 to a Microcontroller"
  - AN9532 "Using HI7190 in a Multiplexed System"
  - AN9601 "Using HI7190 with a Single +5V Supply"

Description

The Harris HI7190 is a monolithic instrumentation, sigma delta A/D converter which operates from ±5V supplies. Both the signal and reference inputs are fully differential for maximum flexibility and performance. An internal Programmable Gain Instrumentation Amplifier (PGIA) provides input gains from 1 to 128 eliminating the need for external pre-amplifiers. The on-demand converter auto-calibrate function is capable of removing offset and gain errors existing in external and internal circuitry. The on-board user programmable digital filter provides over -120dB of 60/50Hz noise rejection and allows fine tuning of resolution and conversion speed over a wide dynamic range.

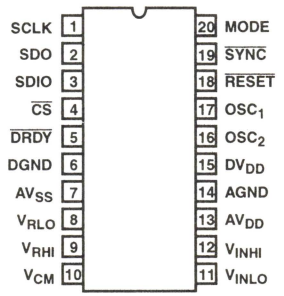
The HI7190 contains a serial I/O port and is compatible with most synchronous transfer formats including both the Motorola 6805/11 series SPI and Intel 8051 series SSR protocols. A sophisticated set of commands gives the user control over calibration, PGIA gain, device selection, standby mode, and several other features. The On-chip Calibration Registers allow the user to read and write calibration data.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI7190IP	-40 to 85	20 Ld PDIP	E20.3
HI7190IB	-40 to 85	20 Ld SOIC	M20.3
HI7190EVAL	Evaluation Kit		

Pinout

HI7190
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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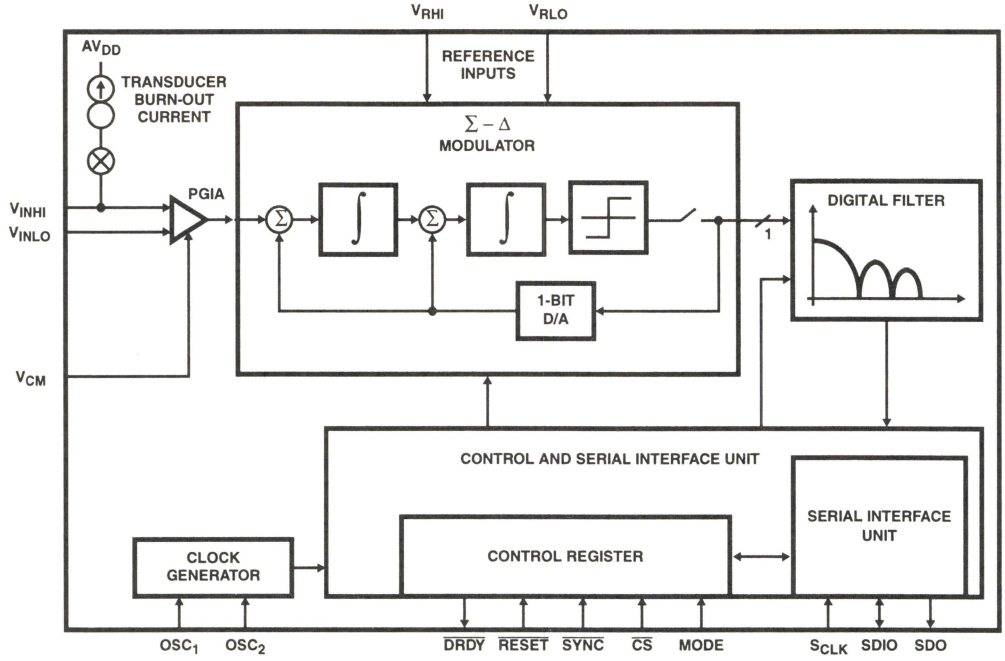
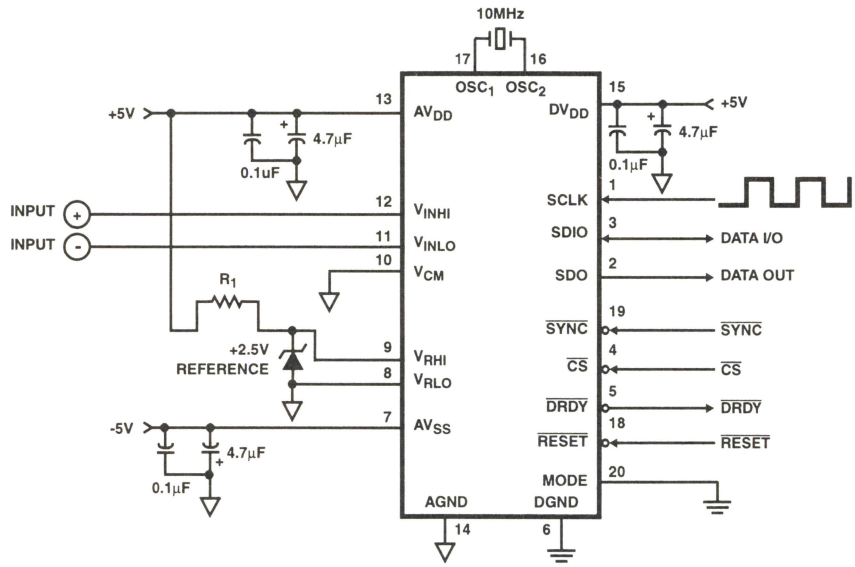
File Number **3612.4**

Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage
- AV_{DD} to AGND . . . . . +5.5V
- AV_{SS} to AGND . . . . . -5.5V
- DV_{DD} to DGND . . . . . +5.5V
- DGND to AGND . . . . . ±0.3V

Analog Input Pins . . . . . AV_{SS} to AV_{DD}
Digital Input, Output and I/O Pins . . . . . DGND to DV_{DD}
ESD Tolerance (No Damage)
- Human Body Model 500V
- Machine Model . . . . . +100V
- Charged Device Model 1000V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	125
SOIC Package	100

Maximum Junction Temperature
- Plastic Packages . . . . . 150°C

Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND = 0V, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 10MHz, Bipolar Input Range Selected, f_N = 10Hz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Integral Non-Linearity, INL	End Point Line Method (Notes 3, 5, 6)	-	±0.0007	±0.0015	%FS
Differential Non-Linearity	(Note 2)	No Missing codes to 22-Bits			LSB
Offset Error, V_{OS}	See Tables 1A and 1B	-	-	-	-
Offset Error Drift	$V_{INHI} = V_{INLO}$ (Notes 3, 8)	-	1	-	µV/ °C
Full Scale Error, FSE	$V_{INHI} - V_{INLO}$ = +2.5V (Notes 3, 5, 8, 10)	-	-	-	-
Noise, e_N	See Table 1	-	-	-	-
Common Mode Rejection Ratio, CMRR	V_{CM} = 0V, $V_{INHI} = V_{INLO}$ from -2V to +2V		-70	-	dB
Normal Mode 50Hz Rejection	Filter Notch = 10Hz, 25Hz, 50Hz (Note 2)	-120	-	-	dB
Normal Mode 60Hz Rejection	Filter Notch = 10Hz, 30Hz, 60Hz (Note 2)	-120	-	-	dB
Step Response Settling Time		-	2	4	Conversions
ANALOG INPUTS					
Input Voltage Range	Unipolar Mode (Note 9)	0	-	V_{REF}	V
Input Voltage Range	Bipolar Mode (Note 9)	- V_{REF}	-	V_{REF}	V
Common Mode Input Range	(Note 2)	AV_{SS}	-	AV_{DD}	V
Input Leakage Current, I_{IN}	$V_{IN} = AV_{DD}$ (Note 2)	-	-	1.0	nA
Input Capacitance, C_{IN}		-	5.0	-	pF
Reference Voltage Range, V_{REF} ($V_{REF} = V_{RHI} - V_{RLO}$)		2.5	-	5	V
Transducer Burn-Out Current, I_{BO}		-	200	-	nA
CALIBRATION LIMITS					
Positive Full Scale Calibration Limit		-	-	1.2(V_{REF}/Gain)	-
Negative Full Scale Calibration Limit		-	-	1.2(V_{REF}/Gain)	-
Offset Calibration Limit		-	-	1.2(V_{REF}/Gain)	-
Input Span		0.2(V_{REF}/Gain)	-	2.4(V_{REF}/Gain)	-
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}	(Note 11)	2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic Current, I_I	V_{IN} = 0V, +5V	-	1.0	10	µA

Electrical Specifications AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND = 0V, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 10MHz, Bipolar Input Range Selected, f_N = 10Hz **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance, C_{IN}	V_{IN} = 0V	-	5.0	-	pF
DIGITAL OUTPUTS					
Output Logic High Voltage, V_{OH}	I_{OUT} = -100µA (Note 7)	2.4	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OUT} = 3mA (Note 7)	-	-	0.4	V
Output Three-State Leakage Current, I_{OZ}	V_{OUT} = 0V, +5V (Note 7)	-10	1	10	µA
Digital Output Capacitance, C_{OUT}		-	10	-	pF
TIMING CHARACTERISTICS					
SCLK Minimum Cycle Time, t_{SCLK}		200	-	-	ns
SCLK Minimum Pulse Width, t_{SCLKPW}		50	-	-	ns
$\overline{CS}$ to SCLK Precharge Time, t_{PRE}		50	-	-	ns
$\overline{DRDY}$ Minimum High Pulse Width	(Notes 2, 7)	500	-	-	ns
Data Setup to SCLK Rising Edge (Write), t_{DSU}		50	-	-	ns
Data Hold from SCLK Rising Edge (Write), t_{DHLD}		0	-	-	ns
Data Read Access from Instruction Byte Write, t_{ACC}	(Note 7)	-	-	40	ns
Read Bit Valid from SCLK Falling Edge, t_{DV}	(Note 7)	-	-	40	ns
Last Data Transfer to Data Ready Inactive, $t_{\overline{DRDY}}$	(Note 7)	-	35	-	ns
$\overline{RESET}$ Low Pulse Width	(Note 2)	100	-	-	ns
$\overline{SYNC}$ Low Pulse Width	(Note 2)	100	-	-	ns
Oscillator Clock Frequency	(Note 2)	0.1	-	10	MHz
Output Rise/Fall Time	(Note 2)	-	-	30	ns
Input Rise/Fall Time	(Note 2)	-	-	1	µs
POWER SUPPLY CHARACTERISTICS					
IAV_{DD}		-	-	1.5	mA
IAV_{SS}		-	-	1.5	mA
IDV_{DD}	SCLK = 4MHz	-	-	3.0	mA
Power Dissipation, Active PD_A	SB = '0'	-	15	30	mW
Power Dissipation, Standby PD_S	SB = '1'	-	5	-	mW
PSRR	(Note 3)	-	-70	-	dB

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Parameter guaranteed by design or characterization, not production tested.
3. Applies to both bipolar and unipolar input ranges.
4. These errors can be removed by re-calibrating at the desired operating temperature.
5. Applies after system calibration.
6. Fully differential input signal source is used.
7. See Load Test Circuit, Figure 10, R1 = 10kΩ, C_L = 50pF.
8. 1 LSB = 298nV at 24 bits for a Full Scale Range of 5V.
9. $V_{REF} = V_{RHI} - V_{RLO}$
10. These errors are on the order of the output noise shown in Table 1.
11. All inputs except OSC_1. The OSC_1 input V_{IH} is 3.5V minimum.

Timing Diagrams

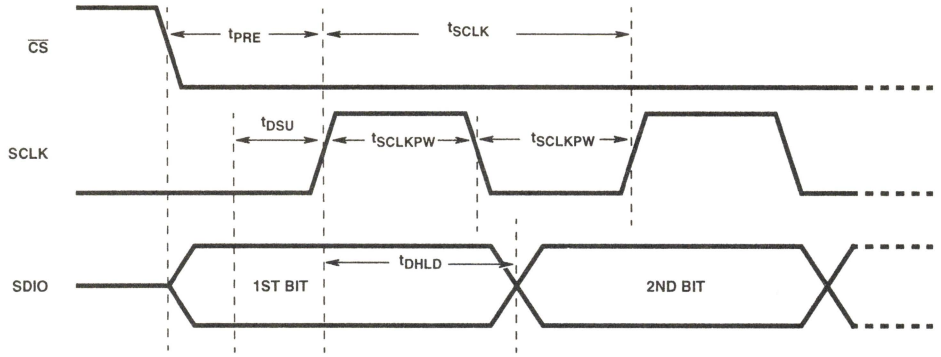


FIGURE 1. DATA WRITE TO HI7190

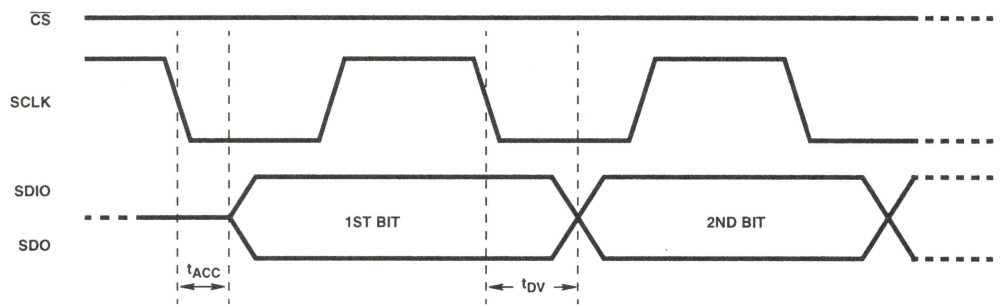


FIGURE 2. DATA READ FROM HI7190

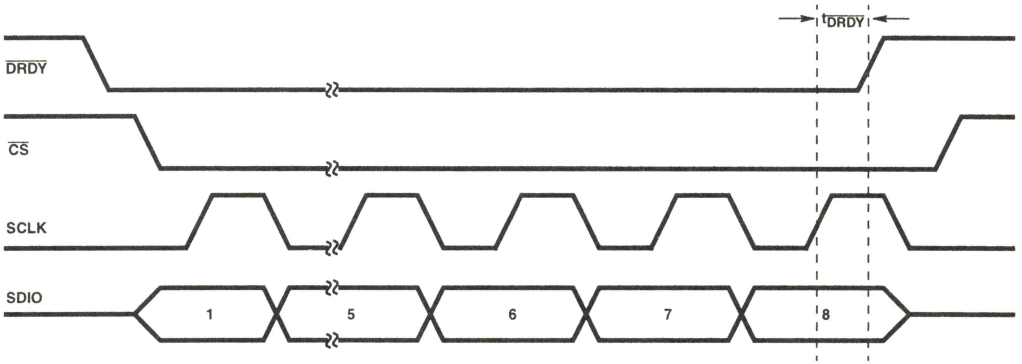


FIGURE 3. DATA READ FROM HI7190

Pin Descriptions

20 LEAD DIP, SOIC	PIN NAME	DESCRIPTION
1	SCLK	Serial Interface Clock. Synchronizes serial data transfers. Data is input on the rising edge and output on the falling edge.
2	SDO	Serial Data OUT. Serial data is read from this line when using a 3-wire serial protocol such as the Motorola Serial Peripheral Interface.
3	SDIO	Serial Data IN or OUT. This line is bidirectional programmable and interfaces directly to the Intel Standard Serial Interface using a 2-wire serial protocol.
4	$\overline{CS}$	Chip Select Input. Used to select the HI7190 for a serial data transfer cycle. This line can be tied to DGND.
5	$\overline{DRDY}$	An Active Low Interrupt indicating that a new data word is available for reading.
6	DGND	Digital Supply Ground.
7	AV_{SS}	Negative Analog Power Supply (-5V).
8	V_{RLO}	External Reference Input. Should be negative referenced to V_{RHI}.
9	V_{RHI}	External Reference Input. Should be positive referenced to V_{RLO}.
10	V_{CM}	Common Mode Input. Should be set to halfway between AV_{DD} and AV_{SS}.
11	V_{INLO}	Analog Input LO. Negative input of the PGIA.
12	V_{INHI}	Analog Input HI. Positive input of the PGIA. The V_{INHI} input is connected to a current source that can be used to check the condition of an external transducer. This current source is controlled via the Control Register.
13	AV_{DD}	Positive Analog Power Supply (+5V).
14	AGND	Analog Supply Ground.
15	DV_{DD}	Positive Digital Supply (+5V).
16	OSC_2	Used to connect a crystal source between OSC_1 and OSC_2. Leave open otherwise.
17	OSC_1	Oscillator Clock Input for the device. A crystal connected between OSC_1 and OSC_2 will provide a clock to the device, or an external oscillator can drive OSC_1. The oscillator frequency should be 10MHz (Typ).
18	$\overline{RESET}$	Active Low Reset Pin. Used to initialize the HI7190 registers, filter and state machines.
19	$\overline{SYNC}$	Active Low Sync Input. Used to control the synchronization of a number of HI7190s. A logic '0' initializes the converter.
20	MODE	Mode Pin. Used to select between Synchronous Self Clocking (Mode = 1) or Synchronous External Clocking (Mode = 0) for the Serial Port.

Load Test Circuit

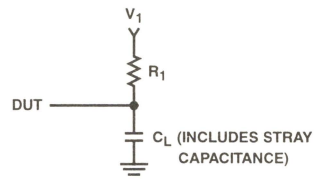
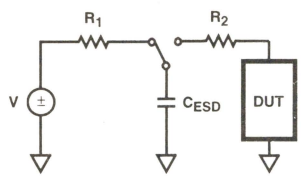


FIGURE 4.

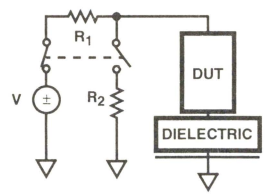
ESD Test Circuits



HUMAN BODY
C_{ESD} = 100pF
R_1 = 10MΩ
R_2 = 1.5kΩ

MACHINE MODEL
C_{ESD} = 200pF
R_1 = 10MΩ
R_2 = 0Ω

FIGURE 5A.



CHARGED DEVICE MODEL
R_1 = 1GΩ
R_2 = 1Ω

FIGURE 5B.

TABLE 1A. PEAK-TO-PEAK NOISE AND ENOB FOR VARIOUS GAINS AND CONVERSION FREQUENCIES

CONVERSION RATE (f_N)	INPUT CUTOFF FREQUENCY (-3dB, f_S)	GAIN = 1		GAIN = 2		GAIN = 4		GAIN = 8	
		P-P NOISE (μV)	NUMBER OF BITS	P-P NOISE (μV)	NUMBER OF BITS	P-P NOISE (μV)	NUMBER OF BITS	P-P NOISE (μV)	NUMBER OF BITS
10Hz	2.62Hz	2.87	23.5	3.24	23.3	3.54	23.2	6.63	22.2
25Hz	6.55Hz	3.99	23.0	4.43	22.8	5.95	22.4	13.0	21.3
30Hz	7.86Hz	4.54	22.8	10.5	21.6	14.7	21.1	17.3	20.9
50Hz	13.1Hz	5.96	22.4	8.30	22.3	9.02	21.8	27.9	20.2
60Hz	15.7Hz	6.89	22.2	7.26	22.1	10.0	21.7	18.5	20.8
100Hz	26.2Hz	16.5	20.9	13.8	21.2	16.6	20.9	41.5	19.6
250Hz	65.5Hz	44.4	19.5	33.0	19.9	33.8	19.9	66.8	18.9
500Hz	131Hz	128	18.0	101	18.3	388	18.4	134	17.9
1kHz	262Hz	638	15.7	431	16.2	486	16.1	583	15.8
2kHz	524Hz	3820	13.1	2610	13.6	2890	13.5	3310	13.3

TABLE 1A. PEAK-TO-PEAK NOISE AND ENOB FOR VARIOUS GAINS AND CONVERSION FREQUENCIES (Continued)

CONVERSION RATE (f_N)	INPUT CUTOFF FREQUENCY (-3dB, f_S)	GAIN = 16		GAIN = 32		GAIN = 64		GAIN = 128	
		P-P NOISE (μV)	NUMBER OF BITS	P-P NOISE (μV)	NUMBER OF BITS	P-P NOISE (μV)	NUMBER OF BITS	P-P NOISE (μV)	NUMBER OF BITS
10Hz	2.62Hz	6.93	22.2	28.2	20.2	29.4	20.1	50.5	19.3
25Hz	6.55Hz	25.0	20.3	44.4	19.5	93.1	18.4	176	17.5
30Hz	7.86Hz	17.2	20.9	16.4	20.9	44.2	19.5	201	17.3
50Hz	13.1Hz	27.2	20.2	93.4	18.4	94.7	18.4	308	16.7
60Hz	15.7Hz	30.9	20.0	90.4	18.5	148	17.8	276	16.9
100Hz	26.2Hz	42.84	19.6	142	17.8	175	17.5	419	16.3
250Hz	65.5Hz	70.6	18.8	232.8	17.1	1010	15	2030	14
500Hz	131Hz	148	17.8	468	16.1	1690	14.3	4050	13.0
1kHz	262Hz	544.6	15.9	2150	13.9	2030	13.9	4750	12.8
2kHz	524Hz	3570	13.2	22400	10.5	23300	10.5	20700	10.6

TABLE 1B. RMS INPUT REFERRED NOISE FOR VARIOUS GAINS AND CONVERSION FREQUENCIES

CONVERSION RATE (f_N)	INPUT CUTOFF FREQUENCY (-3dB, f_S)	GAIN = 1	GAIN = 2	GAIN = 4	GAIN = 8	GAIN = 16	GAIN = 32	GAIN = 64	GAIN = 128
		RMS NOISE (μV)	RMS NOISE (μV)	RMS NOISE (μV)	RMS NOISE (μV)	RMS NOISE (μV)	RMS NOISE (μV)	RMS NOISE (μV)	RMS NOISE (μV)
10Hz	2.62Hz	0.435	0.246	0.134	0.126	0.066	0.134	0.070	0.060
25Hz	6.55Hz	0.604	0.336	0.226	0.246	0.237	0.212	0.220	0.209
30Hz	7.86Hz	0.689	0.796	0.557	0.327	0.163	0.077	0.105	0.238
50Hz	13.1Hz	0.903	0.477	0.341	0.529	0.258	0.442	0.224	0.364
60Hz	15.7Hz	1.04	0.550	0.380	0.350	0.293	0.428	0.350	0.326
100Hz	26.2Hz	2.50	1.05	0.628	0.786	0.406	0.672	0.414	0.496
250Hz	65.5Hz	6.73	2.50	1.28	1.26	0.669	1.10	2.40	2.40
500Hz	131Hz	19.4	7.61	14.7	2.54	1.40	2.22	3.40	4.79
1kHz	262Hz	96.7	32.6	18.4	11.0	5.16	10.2	4.97	5.63
2kHz	524Hz	579	198	109	62.8	33.8	108	55.2	24.5

Definitions

Integral Non-Linearity, INL, is the maximum deviation of any digital code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (a point 0.5 LSB below the first code transition 000...000 and 000...001) and full scale (a point 0.5 LSB above the last code transition 111...110 to 111...111).

Differential Non-Linearity, DNL, is the deviation from the actual difference between midpoints and the ideal difference between midpoints (1 LSB) for adjacent codes. If this difference is equal to or more negative than 1 LSB, a code will be missed.

Offset Error, V_{OS}, is the deviation of the first code transition from the ideal input voltage (V_{IN} - 0.5 LSB). This error can be calibrated to the order of the noise level shown in Table 1.

Full Scale Error, FSE, is the deviation of the last code transition from the ideal input full scale voltage (V_{IN}- + V_{REF}/Gain - 1.5 LSB). This error can be calibrated to the order of the noise level shown in Table 1.

Input Span, defines the minimum and maximum input voltages the device can handle while still calibrating properly for gain.

Noise, e_N, Table 1 shows the input referred peak-to-peak and RMS noise for some typical notch and -3dB frequencies. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5V which means the input range is ±2.5V. Measurements are taken for 100 conversions with the peak-to-peak output noise being the difference between the maximum and minimum readings over the 100 conversions.

Table 1A shows the output peak-to-peak noise of the device while Table 1B shows the RMS output noise referred back to the input. The RMS input referred noise data is calculated by converting the peak-to-peak numbers to RMS values by dividing by a crest factor of 6.6, and then dividing that result by the gain of the HI7190. Finally, the Effective Number of Bits (ENOB) or effective resolution is calculated by taking the $\log_2$ (5V/RMS output noise).

The noise from the part comes from two sources, the quantization noise from the analog-to-digital conversion process and device noise. Device noise (or Wideband Noise) is independent of gain and essentially flat across the frequency spectrum. Quantization noise is ratiometric to input full scale (and hence gain) and its frequency response is shaped by the modulator.

Looking at Tables 1A and 1B, as the cutoff frequency increases the output noise increases. This is due to more of the quantization noise of the part coming through to the output and, hence, the output noise increases with increasing -3dB frequencies. For the lower notch settings, the output noise is dominated by the device noise and, hence, altering the gain has little effect on the output noise. At higher notch frequencies, the quantization noise dominates the output noise and, in this case, the output noise tends to decrease with increasing gain.

Since the output noise comes from two sources, the effective resolution of the device (i.e., the ratio of the input full scale to the output RMS noise) does not remain constant with increasing gain or with increasing bandwidth. It is possible to do post-filtering (such as brick wall filtering) on the data to improve the overall resolution for a given -3dB frequency and also to further reduce the output noise.

Circuit Description

The HI7190 is a monolithic, sigma delta A/D converter which operates from ±5V supplies and is intended for measurement of wide dynamic range, low frequency signals. It contains a Programmable Gain Instrumentation Amplifier (PGIA), sigma delta ADC, digital filter, bidirectional serial port (compatible with many industry standard protocols), clock oscillator, and an on-chip controller.

The signal and reference inputs are fully differential for maximum flexibility and performance. Normally V_{RHI} and V_{RLO} are tied to +2.5V and AGND respectively. This allows for input ranges of 2.5V and 5V when operating in the unipolar and bipolar modes respectively (assuming the PGIA is configured for a gain of 1). The internal PGIA provides input gains from 1 to 128 and eliminates the need for external preamplifiers. This means the device will convert signals ranging from 0V to +20mV and 0V to +2.5V when operating in the unipolar mode or signals in the range of ±20mV to ±2.5V when operating in the bipolar mode.

The input signal is continuously sampled at the input to the HI7190 at a clock rate set by the oscillator frequency and the selected gain. This signal then passes through the sigma delta modulator (which includes the PGIA) and emerges as a pulse train whose code density contains the analog signal information. The output of the modulator is fed into the $sinc^3$ digital low pass filter. The filter output passes into the calibration block where offset and gain errors are removed. The calibrated data is then coded (2's complement, offset binary or binary) before being stored in the Data Output Register. The Data Output Register update rate is determined by the first notch frequency of the digital filter. This first notch frequency is programmed into HI7190 via the Control Register and has a range of 10Hz to 1.953kHz which corresponds to -3dB frequencies of 2.62Hz and 512Hz respectively.

Output data coding on the HI7190 is programmable via the Control Register. When operating in bipolar mode, data output can be either 2's complement or offset binary. In unipolar mode output is binary.

The $\overline{DRDY}$ signal is used to alert the user that new output data is available. Converted data is read via the HI7190 serial I/O port which is compatible with most synchronous transfer formats including both the Motorola 6805/11 series SPI and Intel 8051 series SSR protocols. Data Integrity is always maintained at the HI7190 output port. This means that if a data read of conversion N is begun but not finished before the next conversion (conversion N + 1) is complete, the $\overline{DRDY}$ line remains active (low) and the data being read is not overwritten.

The HI7190 provides many calibration modes that can be initiated at any time by writing to the Control Register. The device can perform system calibration where external components are included with the HI7190 in the calibration loop or self-calibration where only the HI7190 itself is in the calibration loop. The On-chip Calibration Registers are read/write registers which allow the user to read calibration coefficients as well as write previously determined calibration coefficients.

Circuit Operation

The analog and digital supplies and grounds are separate on the HI7190 to minimize digital noise coupling into the analog circuitry. Nominal supply voltages are AV_{DD} = +5V, DV_{DD} = +5V, and AV_{SS} = -5V. If the same supply is used for AV_{DD} and DV_{DD} it is imperative that the supply is separately decoupled to the AV_{DD} and DV_{DD} pins on the HI7190. Separate analog and digital ground planes should be maintained on the system board and the grounds should be tied together back at the power supply.

When the HI7190 is powered up it needs to be reset by pulling the $\overline{\text{RESET}}$ line low. The reset sets the internal registers of the HI7190 as shown in Table 2 and puts the part in the bipolar mode with a gain of 1 and offset binary coding. The filter notch of the digital filter is set at 30Hz while the I/O is set up for bidirectional I/O (data is read and written on the SDIO line and SDO is three-stated), descending byte order, and MSB first data format. A self calibration is performed before the device begins converting. $\overline{\text{DRDY}}$ goes low when valid data is available at the output.

TABLE 2. REGISTER RESET VALUES

REGISTER	VALUE (HEX)
Data Output Register	XXXX (Undefined)
Control Register	28B300
Offset Calibration Register	Self Calibration Value
Positive Full Scale Calibration Register	Self Calibration Value
Negative Full Scale Calibration Register	Self Calibration Value

The configuration of the HI7190 is changed by writing new setup data to the Control Register. Whenever data is written to byte 2 and/or byte 1 of the Control Register the part assumes that a critical setup parameter is being changed which means that $\overline{\text{DRDY}}$ goes high and the device is re-synchronized. If the configuration is changed such that the device is in any one of the calibration modes, a new calibration is performed before normal conversions continue. If the device is written to the conversion mode, a new calibration is NOT performed (A new calibration is recommended any time data is written to the Control Register.). In either case, $\overline{\text{DRDY}}$ goes low when valid data is available at the output.

If a single data byte is written to byte 0 of the Control Register, the device assumes the gain has NOT been changed. It is up to the user to re-calibrate the device if the gain is changed in this manner. For this reason it is recommended that the entire Control Register be written when changing the gain of the device. This ensures that the part is re-calibrated (if in a calibration mode) before the $\overline{\text{DRDY}}$ output goes low indicating that valid data is available.

The calibration registers can be read via the serial interface at any time. However, care must be taken when writing data to the calibration registers. If the HI7190 is internally updating any calibration register the user can not write to that calibration register. See the Operational Modes section for details on which calibration registers are updated for the various modes.

Since access to the calibration registers is asynchronous to the conversion process the user is cautioned that new calibration data may not be used on the very next set of "valid" data after a calibration register write. It is guaranteed that the new data will take effect on the second set of output data. Non-calibrated data can be obtained from the device by writing 000000 (h) to the Offset Calibration Register, 800000 (h) to the Positive Full Scale Calibration Register, and 800000 (h) to the Negative Full Scale Calibration Register. This sets the offset correction factor to 0 and the positive and negative gain slope factors to 1.

If several HI7190s share a system master clock the $\overline{\text{SYNC}}$ pin can be used to synchronize their operation. A common $\overline{\text{SYNC}}$ input to multiple devices will synchronize operation such that all output registers are updated simultaneously. Of course the $\overline{\text{SYNC}}$ pin would normally be activated only after each HI7190 has been calibrated or has had calibration coefficients written to it.

The $\overline{\text{SYNC}}$ pin can also be used to control the HI7190 when an external multiplexer is used with a single HI7190. The $\overline{\text{SYNC}}$ pin in this application can be used to guarantee a maximum settling time of 3 conversion periods when switching channels on the multiplexer.

Analog Section Description

Figure 6 shows a simplified block diagram of the analog modulator front end of a sigma delta A/D Converter. The input signal V_{IN} comes into a summing junction (the PGIA in this case) where the previous modulator output is subtracted from it. The resulting signal is then integrated and the output of the integrator goes into the comparator. The output of the comparator is then fed back via a 1-bit DAC to the summing junction. The feedback loop forces the average of the fed back signal to be equal to the input signal V_{IN}.

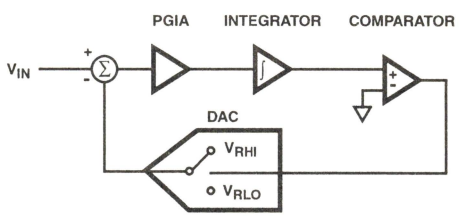


FIGURE 6. SIMPLE MODULATOR BLOCK DIAGRAM

Analog Inputs

The analog input on the HI7190 is a fully differential input with programmable gain capabilities. The input accepts both unipolar and bipolar input signals and gains range from 1 to 128. The common mode range of this input is from AV_{SS} to AV_{DD} provided that the absolute value of the analog input voltage lies within the power supplies. The input impedance of the HI7190 is dependent upon the modulator input sampling rate and the sampling rate varies with the selected PGIA gain. Table 3 below shows the sampling rates and input impedances for the different gain settings of the HI7190. Note that this table is valid only for a 10MHz master clock. If the input clock frequency is changed then the input impedance will change accordingly. The equation used to calculate the input impedance is:

$Z_{IN} = 1/(C_{IN} \times f_S)$,

where C_{in} is the nominal input capacitance (8pF) and f_S is the modulator sampling rate.

TABLE 3. EFFECTIVE INPUT IMPEDANCE vs GAIN

GAIN	SAMPLING RATE (kHz)	INPUT IMPEDANCE (MΩ)
1	78.125	1.6
2	156.25	0.8
4	312.5	0.4
8, 16, 32, 64, 128	625	0.2

Input Filter To Reduce Wideband Noise

The HI7190 internal digital filter does not remove noise that is located at integer multiples of the sampling frequency. To reduce this wideband noise an external RC low pass filter may be used. Below is a recommended input filter configuration. Tables 4 and 5 provide external component values for 16-bit and 20-bit performance, respectively.

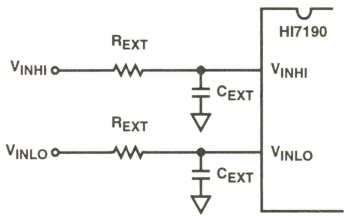


FIGURE 7. INPUT FILTER

TABLE 4. GAIN VERSUS EXTERNAL RC FILTER FOR 16-BIT PERFORMANCE

GAIN	f_S (kHz) APPROX.	t_S (μs)	C_{EXT} 0pF R_{EXT} (Ω)	C_{EXT} 50pF R_{EXT} (Ω)	C_{EXT} 100pF R_{EXT} (Ω)	C_{EXT} 500pF R_{EXT} (Ω)
1	80	5	55K	8K	4.2K	900
2	160	2.5	28K	4K	2.1K	450
4	315	1.25	13K	2K	1.2K	250
8 or more	625	0.640	6K	1.2K	700	150

TABLE 5. GAIN vs EXTERNAL RC FILTER FOR 20-BIT PERFORMANCE

GAIN	f_S (kHz) APPROX.	t_S (μs)	C_{EXT} 0pF R_{EXT} (Ω)	C_{EXT} 50pF R_{EXT} (Ω)	C_{EXT} 100pF R_{EXT} (Ω)	C_{EXT} 500pF R_{EXT} (Ω)
1	80	5	45K	6.5K	3.4K	720
2	160	2.5	23K	3.3K	1.7K	370
4	315	1.25	12K	1.7K	950	200
8 or more	625	0.640	7K	1.1K	620	130

NOTE: f_S = Sampling Rate, t_S = Settling Time = $^1/_2(1/f_S)(0.8)$.

Bipolar/Unipolar Input Ranges

The input on the HI7190 can accept either unipolar or bipolar input voltages. Bipolar or unipolar options are chosen by programming the B/$\overline{U}$ bit of the Control Register. Programming the part for either unipolar or bipolar operation does not change the input signal conditioning.

The inputs are differential, and as a result are referenced to the voltage on the V_{INLO} input. For example, if V_{INLO} is +1.25V and the HI7190 is configured for unipolar operation with a gain of 1 and a V_{REF} of +2.5V, the input voltage range on the V_{INLO} input is +1.25V to +3.75V. If V_{INLO} is +1.25V and the HI7190 is configured for bipolar mode with gain of 1 and a V_{REF} of +2.5V, the analog input range on the V_{INHI} input is -1.25V to +3.75V.

Programmable Gain Instrumentation Amplifier

The Programmable Gain Instrumentation Amplifier allows the user to directly interface low level sensors and bridges directly to the HI7190. The PGIA has 4 selectable gain options of 1, 2, 4, 8 which are implemented by multiple sampling of the input signal. Input signals can be gained up further to 16, 32, 64 or 128. These higher gains are implemented in the digital section of the design to maintain a high signal to noise ratio through the front end amplifiers. The gain is digitally programmable in the Control Register via the serial interface. For optimum PGIA performance the V_{CM} pin should be tied to the mid point of the analog supplies.

Differential Reference Input

The reference inputs of the of the HI7190, V_{RHI} and V_{RLO}, provide a differential reference input capability. The nominal differential voltage ($V_{REF} = V_{RHI} - V_{RLO}$) is +2.5V and the common mode voltage cab be anywhere between AV_{SS} and AV_{DD}. Larger values of V_{REF} can be used without degradation in performance with the maximum reference voltage being V_{REF} = +5V. Smaller values of V_{REF} can also be used but performance will be degraded since the LSB size is reduced.

The full scale range of the HI7190 is defined as:

$FSR_{BIPOLAR} = 2 \times V_{REF}/GAIN$

$FSR_{UNIPOLAR} = V_{REF}/GAIN$

and V_{RHI} must always be greater than V_{RLO} for proper operation of the device.

The reference inputs provide a high impedance dynamic load similar to the analog inputs and the effective input impedance for the reference inputs can be calculated in the same manner as it is for the analog input impedance. The only difference in the calculation is that C_{IN} for the reference inputs is 10.67pF. Therefor, the input impedance range for the reference inputs is from 149kΩ in a gain of 8 or higher mode to 833kΩ in the gain of 1 mode.

V_{CM} Input

The voltage at the V_{CM} input is the voltage that the internal analog circuitry is referenced to and should always be tied to the midpoint of the AV_{DD} and AV_{SS} supplies. This point provides a common mode input voltage for the internal operational amplifiers and must be driven from a low noise, low impedance source if it is not tied to analog ground. Failure to do so will result in degraded HI7190 performance. It is recommended that V_{CM} be tied to analog ground when operating off of AV_{DD} = +5V and AV_{SS} = -5V supplies.

V_{CM} also determines the headroom at the upper and lower ends of the power supplies which is limited by the common mode input range where the internal operational amplifiers remain in the linear, high gain region of operation. The HI7190 is designed to have a range of AV_{SS} +1.8V < V_{CM} < AV_{DD} - 1.8V. Exceeding this range on the V_{CM} pin will compromise the device performance.

Transducer Burn-Out Current Source

The V_{INHI} input of the HI7190 contains a 500nA (Typ) current source which can be turned on/off via the Control Register. This current source can be used in checking whether a transducer has burnt-out or become open before attempting to take measurements on that channel. When the current source is turned on an additional offset will be created indicating the presence of a transducer. The current source is controlled by the BO bit (Bit 4) in the Control Register and is disabled on power up. See Figure 8 for an applications circuit.

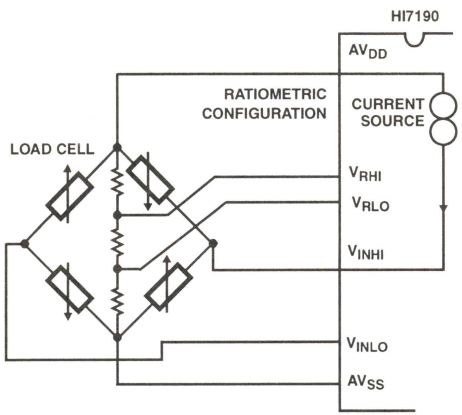


FIGURE 8. BURN-OUT CURRENT SOURCE CIRCUIT

Digital Section Description

A block diagram of the digital section of the HI7190 is shown in Figure 9. This section includes a low pass decimation filter, conversion controller, calibration logic, serial interface, and clock generator.

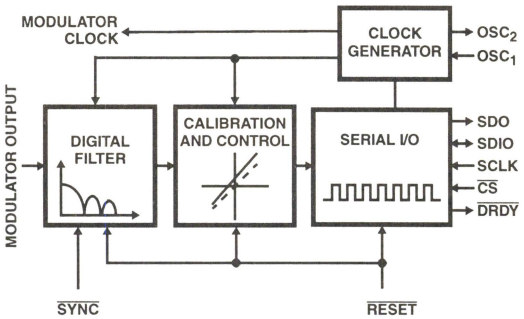


FIGURE 9. DIGITAL SECTION BLOCK DIAGRAM

Digital Filtering

One advantage of digital filtering is that it occurs after the conversion process and can remove noise introduced during the conversion. It can not, however, remove noise present on the analog signal prior to the ADC (which an analog filter can).

One problem with the modulator/digital filter combination is that excursions outside the full scale range of the device could cause the modulator and digital filter to saturate. This device has headroom built in to the modulator and digital filter which tolerates signal deviations up to 33% outside of the full scale range of the device. If noise spikes can drive the input signal outside of this extended range, it is recommended that an input analog filter is used or the overall input signal level is reduced.

Low Pass Decimation Filter

The digital low-pass filter is a Hogenauer ($sinc^3$) decimating filter. This filter was chosen because it is a cost effective low pass decimating filter that minimizes the need for internal multipliers and extensive storage and is most effective when used with high sampling or oversampling rates. Figure 10 shows the frequency characteristics of the filter where f_C is the -3dB frequency of the input signal and f_N is the programmed notch frequency. The analog modulator sends a one bit data stream to the filter at a rate of that is determined by:

$f_{MODULATOR} = f_{OSC}/128$

$f_{MODULATOR}$ = 78.125kHz for f_{OSC} = 10MHz.

The filter then converts the serial modulator data into 40-bit words for processing by the Hogenauer filter. The data is decimated in the filter at a rate determined by the CODE word FP10-FP0 (programed by the user into the Control Register) and the external clock rate. The equation is:

$f_{NOTCH} = f_{OSC}/(512 \times CODE)$.

The Control Register has 11 bits that select the filter cutoff frequency and the first notch of the filter. The output data update rate is equal to the notch frequency. The notch frequency sets the Nyquist sampling rate of the device while the -3dB point of the filter determines the frequency spectrum of interest (f_S). The FP bits have a usable range of 10 through 2047 where 10 yields a 1.953kHz Nyquist rate.

The Hogenauer filter contains alias components that reflect around the notch frequency. If the spectrum of the frequency of interest reaches the alias component, the data has been aliased and therefore undersampled.

Filter Characteristics

The FP10 to FP0 bits programmed into the Control Register determine the cutoff (or notch) frequency of the digital filter. The allowable code range is $00A_H$. This corresponds to a maximum and minimum cutoff frequency of 1.953kHz and 10Hz, respectively when operating at a clock frequency of 10MHz. If a 1MHz clock is used then the maximum and minimum cutoff frequencies become 195.3kHz and 1Hz, respectively. A plot of the $(\sin x/x)^3$ digital filter characteristics is shown in Figure 10. This filter provides greater than 120dB of 50Hz or 60Hz rejection. Changing the clock frequency or the programming of the FP bits does not change the shape of the filter characteristics, it merely shifts the notch frequency. This low pass digital filter at the output of the converter has an accompanying settling time for step inputs just as a low pass analog filter does. New data takes between 3 and 4 conversion periods to settle and update on the serial port with a conversion period t_{CONV} being equal to $1/f_N$.

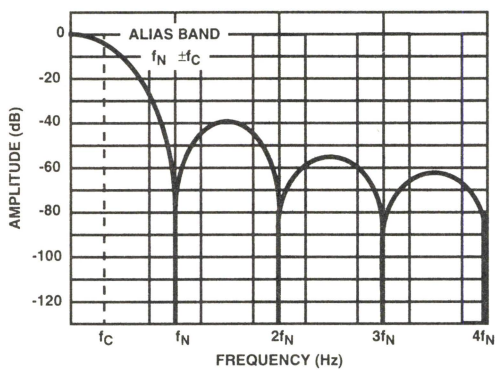


FIGURE 10. LOW PASS FILTER FREQUENCY CHARACTERISTICS

Input Filtering

The digital filter does not provide rejection at integer multiples of the modulator sampling frequency. This implies that there are frequency bands where noise passes to the output without attenuation. For most cases this is not a problem because the high oversampling rate and noise shaping characteristics of the modulator cause this noise to become a small portion of the broadband noise which is filtered. However, if an anti-alias filter is necessary a single pole RC filter is usually sufficient.

If an input filter is used the user must be careful that the source impedance of the filter is low enough not to cause gain errors in the system. The DC input impedance at the inputs is > 1GΩ but it is a dynamic load that changes with clock frequency and selected gain. The input sample rate, also dependent upon clock frequency and gain, determines the allotted time for the input capacitor to charge. The addition of external components may cause the charge time of the capacitor to increase beyond the allotted time. The result of the input not settling to the proper value is a system gain error which can be eliminated by system calibration of the HI7190.

Clocking/Oscillators

The master clock into the HI7190 can be supplied by either a crystal connected between the OSC_1 and OSC_2 pins as shown in Figure 11A or a CMOS compatible clock signal connected to the OSC_1 pin as shown in Figure 11B. The input sampling frequency, modulator sampling frequency, filter -3dB frequency, output update rate, and calibration time are all directly related to the master clock frequency, f_{OSC}. For example, if a 1MHz clock is used instead of a 10MHz clock, what is normally a 10Hz conversion rate becomes a 1Hz conversion rate. Lowering the clock frequency will also lower the amount of current drawn from the power supplies. Please note that the HI7190 specifications are written for a 10MHz clock only.

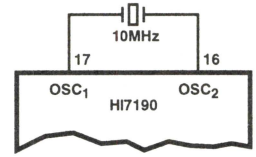


FIGURE 11A.

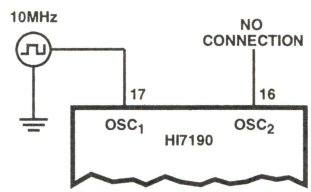


FIGURE 11B.

FIGURE 11. OSCILLATOR CONFIGURATIONS

Operational Modes

The HI7190 contains several operational modes including calibration modes for cancelling offset and gain errors of both internal and external circuitry. A calibration routine should be initiated whenever there is a change in the ambient operating temperature or supply voltage. Calibration should also be initiated if there is a change in the gain, filter notch, bipolar, or unipolar input range. Non-calibrated data can be obtained from the device by writing 000000 to the

Offset Calibration Register, 800000 (h) to the Positive Full Scale Calibration Register, and 800000 (h) to the Negative Full Scale Calibration Register. This sets the offset correction factor to 0 and both the positive and negative gain slope factors to 1.

The HI7190 offers several different modes of Self-Calibration and System Calibration. For calibration to occur, the on-chip microcontroller must convert the modulator output for three different input conditions - "zero-scale," "positive full scale," and "negative full scale". With these readings, the HI7190 can null any offset errors and calculate the gain slope factor for the transfer function of the converter. It is imperative that the zero-scale calibration be performed before either of the gain calibrations. However, the order of the gain calibrations is not important.

The calibration modes are user selectable in the Control Register by using the MD bits (MD2-MD0) as shown in Table 6. $\overline{DRDY}$ will go low indicating that the calibration is complete and there is valid data at the output.

TABLE 6. HI7190 OPERATIONAL MODES

MD2	MD1	MD0	OPERATIONAL MODE
0	0	0	Conversion
0	0	1	Self Calibration
0	1	0	System Offset Calibration
0	1	1	System Positive Full Scale Calibration
1	0	0	System Negative Full Scale Calibration
1	0	1	System Offset/Internal Gain Calibration
1	1	0	System Gain Calibration
1	1	1	Reserved

Conversion Mode

For Conversion Mode operation the HI7190 converts the differential voltage between V_{INHI} and V_{INLO}. From switching into this mode it takes 3 conversion periods ($3 \times 1/f_N$) for $\overline{DRDY}$ to go low and new data to be valid. No calibration coefficients are generated when operating in Conversion Mode as data is calibrated using the existing calibration coefficients.

Self-Calibration Mode

The Self-Calibration Mode is a three step process that updates the Offset Calibration Register, the Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. In this mode an internal offset calibration is done by disconnecting the external inputs and shorting the inputs of the PGIA together. After 3 conversion periods the Offset Calibration Register is updated with the value that corrects any internal offset errors.

After the offset calibration is completed the Positive and Negative Full Scale Calibration Registers are updated. The inputs V_{INHI} and V_{INLO} are disconnected and the external reference is applied across the modulator inputs. The HI7190 then takes 3 conversion cycles to sample the data and update the Positive Full Scale Calibration Register. Next the polarity of the reference voltage across the modulator input terminals is reversed and after 3 conversion cycles the Negative Full Scale Calibration Register is updated. The values stored in the Positive and Negative Full Scale Calibration Registers correct for any internal gain errors in the A/D transfer function. After 3 more conversion cycles the $\overline{DRDY}$ line will activate signaling that the calibration is complete and valid data is present in the Data Output Register.

Please note: Self-calibration is only valid when operating in a gain of one. In addition, the offset and gain errors are not reduced as with the full system calibration.

System Offset Calibration Mode

The System Offset Calibration Mode is a single step process that allows the user to lump offset errors of external circuitry and the internal errors of the HI7190 together and null them out. This mode will convert the external differential signal applied to the V_{IN} inputs and then store that value in the Offset Calibration Register. *The user must apply the zero point or offset voltage to the HI7190 analog inputs and allow the signal to settle **before** selecting this mode.* After 4 conversion periods the $\overline{DRDY}$ line will activate signaling that the calibration is complete and valid data is present in the Data Output Register.

System Positive Full Scale Calibration Mode

The System Positive Full Scale Calibration Mode is a single step process that allows the user to lump gain errors of external circuitry and the internal errors of the HI7190 together and null them out. This mode will convert the external differential signal applied to the V_{IN} inputs and stores the converted value in the Positive Full Scale Calibration Register. *The user must apply the +Full Scale voltage to the HI7190 analog inputs and allow the signal to settle **before** selecting this mode.* After 4 conversion periods the $\overline{DRDY}$ line will activate signaling the calibration is complete and valid data is present in the Data Output Register.

System Negative Full Scale Calibration Mode

The System Negative Full Scale Calibration Mode is a single-step process that allows the user to lump gain errors of external circuitry and the internal errors of the HI7190 together and null them out. This mode will convert the external differential signal applied to the V_{IN} inputs and stores the converted value in the Negative Full Scale Calibration Register. *The user must apply the -Full Scale voltage to the HI7190 analog inputs and allow the signal to settle **before** selecting this mode.* After 4 conversion periods the $\overline{DRDY}$ line will activate signaling the calibration is complete and valid data is present in the Data Output Register.

System Offset/Internal Gain Calibration Mode

The System Offset/Internal Gain Calibration Mode is a single step process that updates the Offset Calibration Register, the Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. First the external differential signal applied to the V_{IN} inputs is converted and that value is stored in the Offset Calibration Register. *The user must apply the zero point or offset voltage to the HI7190 analog inputs and allow the signal to settle **before** selecting this mode.*

After this is completed the Positive and Negative Full Scale Calibration Registers are updated. The inputs V_{INHI} and V_{INLO} are disconnected and the external reference is switched in. The HI7190 then takes 3 conversion cycles to sample the data and update the Positive Full Scale Calibration Register. Next the polarity of the reference voltage across the V_{INHI} and V_{INLO} terminals is reversed and after 3 conversion cycles the Negative Full Calibration Register is updated. The values stored in the Positive and Negative Full Scale Calibration Registers correct for any internal gain errors in the A/D transfer function. After 3 more conversion cycles, the DRDY line will activate signaling that the calibration is complete and valid data is present in the Data Output Register.

System Gain Calibration Mode

The Gain Calibration Mode is a single step process that updates the Positive and Negative Full Scale Calibration Registers. This mode will convert the external differential signal applied to the V_{IN} inputs and then store that value in the Negative Full Scale Calibration Register. Then the polarity of the input is reversed internally and another conversion is performed. This conversion result is written to the Positive Full Scale Calibration Register. The user must apply the +Full Scale voltage to the HI7190 analog inputs and allow the signal to settle before selecting this mode. After 1 more conversion period the $\overline{DRDY}$ line will activate signaling the calibration is complete and valid data is present in the data output register.

Reserved

This mode is not used in the HI7190 and should not be selected. There is no internal detection logic to keep this condition from being selected and care should be taken not to assert this bit combination.

Offset and Span Limits

There are limits to the amount of offset and gain which can be adjusted out for the HI7190. For both bipolar and unipolar modes the minimum and maximum input spans are $0.2 \times V_{REF}/GAIN$ and $1.2 \times V_{REF}/GAIN$ respectively.

In the unipolar mode the offset plus the span cannot exceed the $1.2 \times V_{REF}/GAIN$ limit. So, if the span is at its minimum value of $0.2 \times V_{REF}/GAIN$, the offset must be less than $1 \times V_{REF}/GAIN$. In bipolar mode the span is equidistant around the voltage used for the zero scale point. For this mode the offset plus half the span cannot exceed $1.2 \times V_{REF}/GAIN$. If the span is at $\pm 0.2 \times V_{REF}/GAIN$, then the offset can not be greater than $\pm 2 \times V_{REF}/GAIN$.

Serial Interface

The HI7190 has a flexible, synchronous serial communication port to allow easy interfacing to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6805/11 SPI and Intel 8051 SSR protocols. The Serial Interface is a flexible 2-wire or 3-wire hardware interface where the HI7190 can be configured to read and write on a single bidirectional line (SDIO) or configured for writing on SDIO and reading on the SDO line.

The interface is byte organized with each register byte having a specific address and single or multiple byte transfers are supported. In addition, the interface allows flexibility as to the byte and bit access order. That is, the user can specify MSB/LSB first bit positioning and can access bytes in ascending/descending order from any byte position.

The serial interface allows the user to communicate with 5 registers that control the operation of the device.

Data Output Register - a 24-bit, read only register containing the conversion results.

Control Register - a 24-bit, read/write register containing the setup and operating modes of the device.

Offset Calibration Register - a 24-bit, read/write register used for calibrating the zero point of the converter or system.

Positive Full Scale Calibration Register - a 24-bit, read/write register used for calibrating the Positive Full Scale point of the converter or system.

Negative Full Scale Calibration Register - a 24-bit, read/write register used for calibrating the Negative Full Scale point of the converter or system.

Two clock modes are supported. The HI7190 can accept the serial interface clock (SCLK) as an input from the system or generate the SCLK signal as an output. If the MODE pin is logic low the HI7190 is in external clocking mode and the SCLK pin is configured as an input. In this mode the user supplies the serial interface clock and all interface timing specifications are synchronous to this input. If the MODE pin is logic high the HI7190 is in self-clocking mode and the SCLK pin is configured as an output. In self-clocking mode, SCLK runs at $F_{SCLK} = OSC_1/8$ and stalls high at byte boundaries. SCLK does NOT have the capability to stall low in this mode. All interface timing specifications are synchronous to the SCLK output.

Normal operation in self-clocking mode is as follows (See Figure 13): $\overline{CS}$ is sampled low on falling OSC_1 edges. The first SCLK transition output is delayed 29 OSC_1 cycles from the next rising OSC_1. SCLK transitions eight times and then stalls high for 28 OSC_1 cycles. After this stall period is completed SCLK will again transition eight times and stall high. This sequence will repeat continuously while $\overline{CS}$ is active.

The extra OSC_1 cycle required when coming out of the $\overline{CS}$ inactive state is a one clock cycle latency required to properly sample the $\overline{CS}$ input. Note that the normal stall at byte boundaries is 28 OSC_1 cycles thus giving a SCLK rising to rising edge stall period of 32 OSC_1 cycles.

The affects of $\overline{CS}$ on the I/O are different for self-clocking mode (MODE = 1) than for external mode (MODE = 0). For external clocking mode $\overline{CS}$ inactive disables the I/O state machine, effectively freezing the state of the I/O cycle. That is, an I/O cycle can be interrupted using chip select and the HI7190 will continue with that I/O cycle when re-enabled via $\overline{CS}$. SCLK can continue toggling while $\overline{CS}$ is inactive. If $\overline{CS}$ goes inactive during an I/O cycle, it is up to the user to ensure that the state of SCLK is identical when reactivating $\overline{CS}$ as to what it was when $\overline{CS}$ went inactive. For read operations in external clocking mode, the output will go three-state immediately upon deactivation of $\overline{CS}$.

For self-clocking mode (MODE = 1), the affects of CS are different. If CS transitions high (inactive) during the period when data is being transferred (any non stall time) the HI7190 will complete the data transfer to the byte boundary. That is, once SCLK begins the eight transition sequence, it will always complete the eight cycles. If CS remains inactive after the byte has been transferred it will be sampled and SCLK will remain stalled high indefinitely. If CS has returned to active low before the data byte transfer period is completed the HI7190 acts as if CS was active during the entire transfer period.

It is important to realize that the user can interrupt a data transfer on byte boundaries. That is, if the Instruction Register calls for a 3 byte transfer and $\overline{CS}$ is inactive after only one byte has been transferred, the HI7190, when reactivated, will continue with the remaining two bytes before looking for the next Instruction Register write cycle.

Note that the outputs will NOT go three-state immediately upon CS inactive for read operations in self-clocking mode. In the case of CS going inactive during a read cycle the outputs remain driving until after the last data bit is transferred. In the case of CS inactive during the clock stall time it takes 1 OSC_1 cycle plus prop delay (Max) for the outputs to be disabled.

I/O Port Pin Descriptions

The serial I/O port is a bidirectional port which is used to read the data register and read or write the control register and calibration registers. The port contains two data lines, a synchronous clock, and a status flag. Figure 12 shows a diagram of the serial interface lines.

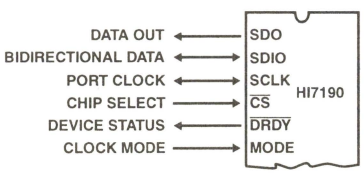


FIGURE 12. HI7190 SERIAL INTERFACE

SDO - Serial Data out. Data is read from this line using those protocols with separate lines for transmitting and receiving data. An example of such a standard is the Motorola Serial Peripheral Interface (SPI) using the 68HC05 and 68HC11 family of microcontrollers, or other similar processors. In the case of using bidirectional data transfer on SDIO, SDO does not output data and is set in a high impedance state.

SDIO - Serial Data in or out. Data is always written to the device on this line. However, this line can be used as a bidirectional data line. This is done by properly setting up the Control Register. Bidirectional data transfer on this line can be used with Intel standard serial interfaces (SSR, Mode 0) in MCS51 and MCS96 family of microcontrollers, or other similar processors.

SCLK - Serial clock. The serial clock pin is used to synchronize data to and from the HI7190 and to run the port state machines. In Synchronous External Clock Mode, SCLK is configured as an input, is supplied by the user, and can run up to a 5MHz rate. In Synchronous Self Clocking Mode, SCLK is configured as an output and runs at $OSC_1/8$.

$\overline{CS}$ - Chip select. This signal is an active low input that allows more than one device on the same serial communication lines. The SDO and SDIO will go to a high impedance state when this signal is high. If driven high during any communication cycle, that cycle will be suspended until $\overline{CS}$ reactivation. Chip select can be tied low in systems that maintain control of SCLK.

DRDY - Data Ready. This is an output status flag from the device to signal that the Data Output Register has been updated with the new conversion result. DRDY is useful as an edge or level sensitive interrupt signal to a microprocessor or microcontroller. DRDY low indicates that new data is available at the Data Output Register. DRDY will return high upon completion of a complete Data Output Register read cycle.

MODE - Mode. This input is used to select between Synchronous Self Clocking Mode ('1') or the Synchronous External Clocking Mode ('0'). When this pin is tied to V_{DD} the serial port is configured in the Synchronous Self Clocking mode where the synchronous shift clock (SCLK) for the serial port is generated by the HI7190 and has a frequency of $OSC_1/8$. When the pin is tied to DGND the serial port is configured for the Synchronous External Clocking Mode where the synchronous shift clock for the serial port is generated by an external device up to a maximum frequency of 5MHz.

Programming the Serial Interface

It is useful to think of the HI7190 interface in terms of communication cycles. Each communication cycle happens in 2 phases. The first phase of every communication cycle is the writing of an instruction byte. The second phase is the data transfer as described by the instruction byte. It is important to note that phase 2 of the communication cycle can be a single byte or a multi-byte transfer of data. For example, the 3-byte Data Output Register can be read using one multi-byte communication cycle rather than three single-byte communication cycles. It is up to the user to maintain synchronism with respect to data transfers. If the system processor "gets lost" the only way to recover is to reset the HI7190. Figure 14 shows both a 2-wire and a 3-wire data transfer.

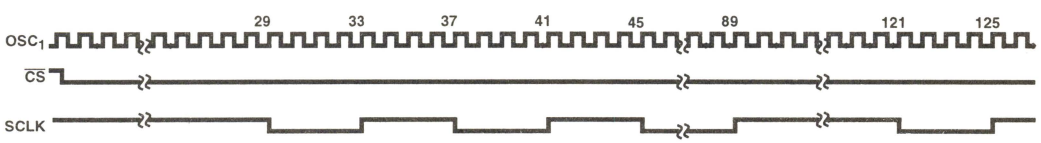


FIGURE 13. SCLK OUTPUT IN SELF-CLOCKING MODE

Several formats are available for reading from and writing to the HI7190 registers in both the 2-wire and 3-wire protocols. A portion of these formats is controlled by the CR<2:1> (BD and $\overline{MSB}$) bits which control the byte direction and bit order of a data transfer respectively. These two bits can be written in any combination but only the two most useful will be discussed here.

The first combination is to reset both the BD and MSB bits (BD = 0, MSB = 0). This sets up the interface for descending byte order and MSB first format. When this combination is used the user should always write the Instruction Register such that the starting byte is the most significant byte address. For example, read three bytes of DR starting with the most significant byte. The first byte read will be the most significant in MSB to LSB format. The next byte will be the next least significant (recall descending byte order) again in MSB to LSB order. The last byte will be the next lesser significant byte in MSB to LSB order. The entire word was read MSB to LSB format.

The second combination is to set both the BD and $\overline{MSB}$ bits to 1. This sets up the interface for ascending byte order and LSB first format. When this combination is used the user should always write the Instruction Register such that the starting byte is the least significant byte address. For example, read three bytes of DR starting with the least significant byte. The first byte read will be the least significant in LSB to MSB format. The next byte will be the next greater significant (recall ascending byte order) again in LSB to MSB order. The last byte will be the next greater significant byte in LSB to MSB order. *The entire word was read MSB to LSB format.*

After completion of each communication cycle, The HI7190 interface enters a standby mode while waiting to receive a new instruction byte.

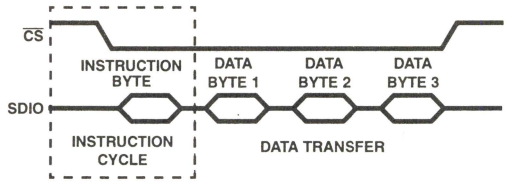


FIGURE 14A. 2-WIRE, 3-BYTE READ OR WRITE TRANSFER

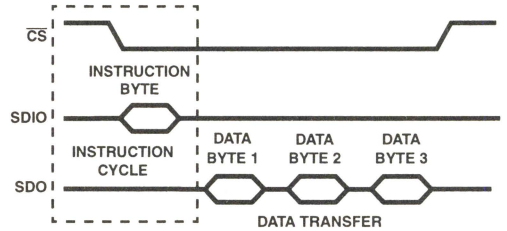


FIGURE 14B. 3-WIRE, 3-BYTE READ TRANSFER

FIGURE 14.

Instruction Byte Phase

The instruction byte phase initiates a data transfer sequence. The processor writes an 8-bit byte (Instruction Byte) to the Instruction Register. The instruction byte informs the HI7190 about the Data transfer phase activities and includes the following information:

- Read or Write cycle
- Number of Bytes to be transferred
- Which register and starting byte to be accessed

Data Transfer Phase

In the data transfer phase, data transfer takes place as set by the Instruction Register contents. See Write Operation and Read Operation sections for detailed descriptions.

Instruction Register

The Instruction Register is an 8-bit register which is used during a communications cycle for setting up read/write operations.

INSTRUCTION REGISTER

MSB	6	5	4	3	2	1	LSB
R/W	MB1	MB0	FSC	A3	A2	A1	A0

R/W - Bit 7 of the Instruction Register determines whether a read or write operation will be done following the instruction byte load. 0 = READ, 1 = WRITE.

MB1, MB0 - Bits 6 and 5 of the Instruction Register determine the number of bytes that will be accessed following the instruction byte load. See Table 7 for the number of bytes to transfer in the transfer cycle.

TABLE 7. MULTIPLE BYTE ACCESS BITS

MB1	MB0	DESCRIPTION
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

FSC - Bit 4 is used to determine whether a Positive Full Scale Calibration Register I/O transfer (FSC = 0) or a Negative Full Scale Calibration Register I/O transfer (FSC = 1) is being performed (see Table 8).

A3, A2, A1, A0 - Bits 3 and 2 (A3 and A2) of the Instruction Register determine which internal register will be accessed while bits 1 and 0 (A1 and A0) determine which byte of that register will be accessed first. See Table 8 for the address decode.

TABLE 8. INTERNAL DATA ACCESS DECODE STARTING BYTE

FSC	A3	A2	A1	A0	DESCRIPTION
X	0	0	0	0	Data Output Register, Byte 0
X	0	0	0	1	Data Output Register, Byte 1
X	0	0	1	0	Data Output Register, Byte 2
X	0	1	0	0	Control Register, Byte 0
X	0	1	0	1	Control Register, Byte 1
X	0	1	1	0	Control Register, Byte 2
X	1	0	0	0	Offset Cal Register, Byte 0
X	1	0	0	1	Offset Cal Register, Byte 1
X	1	0	1	0	Offset Cal Register, Byte 2
0	1	1	0	0	Positive Full Scale Cal Register, Byte 0
0	1	1	0	1	Positive Full Scale Cal Register, Byte 1
0	1	1	1	0	Positive Full Scale Cal Register, Byte 2
1	1	1	0	0	Negative Full Scale Cal Register, Byte 0
1	1	1	0	1	Negative Full Scale Cal Register, Byte 1
1	1	1	1	0	Negative Full Scale Cal Register, Byte 2

Write Operation

Data can be written to the Control Register, Offset Calibration Register, Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. Write operations are done using the SDIO, $\overline{CS}$ and SCLK lines only, as all data is written into the HI7190 via the SDIO line even when using the 3-wire configuration. Figures 15 and 16 show typical write timing diagrams.

The communication cycle is started by asserting the $\overline{CS}$ line low and starting the clock from its idle state. To assert a write cycle, during the instruction phase of the communication cycle, the Instruction Byte should be set to a write transfer ($\overline{R}/W = 1$).

When writing to the serial port, data is latched into the HI7190 on the rising edge of SCLK. Data can then be changed on the falling edge of SCLK. Data can also be changed on the rising edge of SCLK due to the 0ns hold time required on the data. This is useful in pipelined applications where the data is latched on the rising edge of the clock.

Read Operation - 3-Wire Transfer

Data can be read from the Data Output Register, Control Register, Offset Calibration Register, Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. When configured in 3-wire transfer mode, read operations are done using the SDIO, SDO, $\overline{CS}$ and SCLK lines. All data is read via the SDO line. Figures 17 and 18 show typical 3-wire read timing diagrams.

The communication cycle is started by asserting the $\overline{CS}$ line and starting the clock from its idle state. To assert a read cycle, during the instruction phase of the communication cycle, the Instruction Byte should be set to a read transfer ($\overline{R}/W = 0$).

When reading the serial port, data is driven out of the HI7190 on the falling edge of SCLK. Data can be registered externally on the next rising edge of SCLK.

Read Operation - 2-Wire Transfer

Data can be read from the Data Output Register, Control Register, Offset Calibration Register, Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. When configured in two-wire transfer mode, read operations are done using the SDIO, $\overline{CS}$ and SCLK lines. All data is read via the SDIO line. Figures 19 and 20 show typical 2-wire read timing diagrams.

The communication cycle is started by asserting the CS line and starting the clock from its idle state. To assert a read cycle, during the instruction phase of the communication cycle, the Instruction Byte should be set to a read transfer (R/W = 0).

When reading the serial port, data is driven out of the HI7190 on the falling edge of SCLK. Data can be registered externally on the next rising edge of SCLK.

Detailed Register Descriptions

Data Output Register

The Data Output Register contains 24 bits of converted data. This register is a read only register.

BYTE 2

MSB	22	21	20	19	18	17	16
D23	D22	D21	D20	D19	D18	D17	D16

BYTE 1

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8

BYTE 0

7	6	5	4	3	2	1	LSB
D7	D6	D5	D4	D3	D2	D1	D0

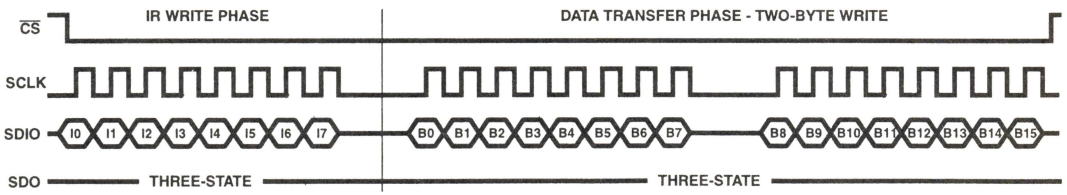


FIGURE 15. DATA WRITE CYCLE, SCLK IDLE LOW

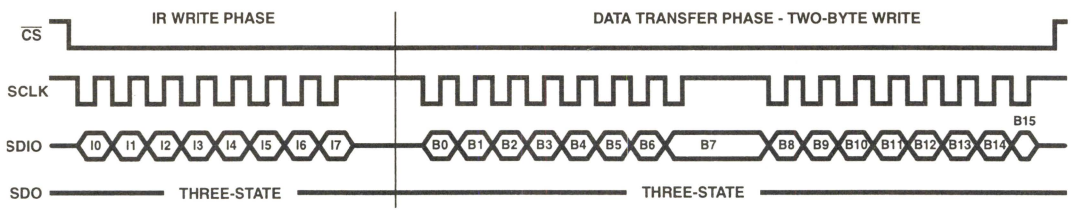


FIGURE 16. DATA WRITE CYCLE, SCLK IDLE HIGH

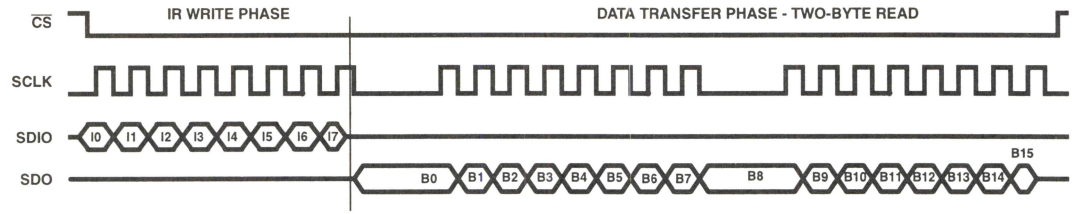


FIGURE 17. DATA READ CYCLE, 3-WIRE CONFIGURATION, SCLK IDLE LOW

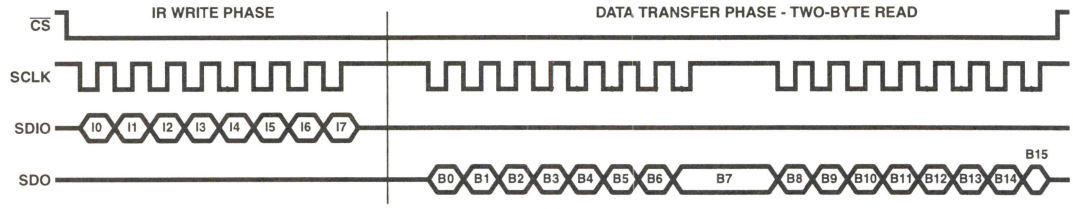


FIGURE 18. DATA READ CYCLE, 3-WIRE CONFIGURATION, SCLK IDLE HIGH

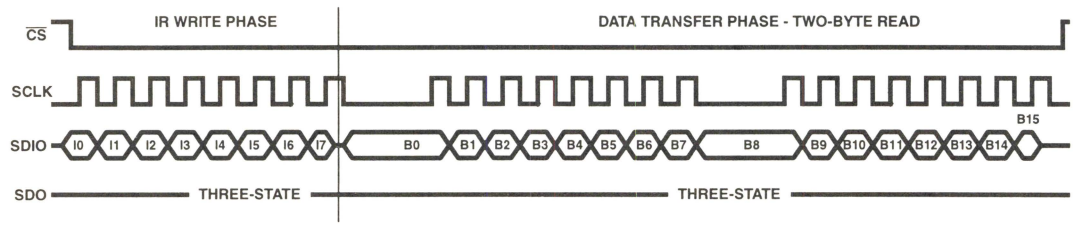


FIGURE 19. DATA READ CYCLE, 2-WIRE CONFIGURATION, SCLK IDLE LOW

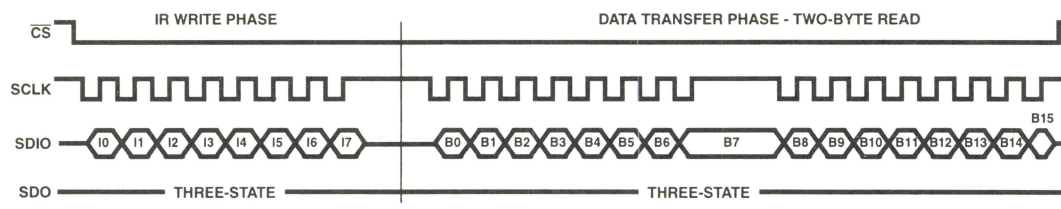


FIGURE 20. DATA READ CYCLE, 2-WIRE CONFIGURATION, SCLK IDLE HIGH

Control Register

The Control Register contains 24-bits to control the various sections of the HI7190. This register is a read/write register.

BYTE 2

MSB	22	21	20	19	18	17	16
DC	FP10	FP9	FP8	FP7	FP6	FP5	FP4

BYTE 1

15	14	13	12	11	10	9	8
FP3	FP2	FP1	FP0	MD2	MD1	MD0	B/U

BYTE 0

7	6	5	4	3	2	1	LSB
G2	G1	G0	BO	SB	BD	MSB	SDL

DC - Bit 23 is the Data Coding Bit used to select between two's complementary and offset binary data coding. When this bit is set (DC = 1) the data in the Data Output Register will be two's complement. When cleared (DC = 0) this data will be offset binary. When operating in the unipolar mode the output data is available in straight binary only (the DC bit is ignored). This bit is cleared after a $\overline{\text{RESET}}$ is applied to the part.

FP10 through FP0 - Bits 22 through 12 are the Filter programming bits that determine the frequency response of the digital filter. These bits determine the filter cutoff frequency, the position of the first notch and the data rate of the HI7190. The first notch of the filter is equal to the decimation rate and can be determined by the formula:

$$f_{NOTCH} = f_{OSC}/(512 \times CODE)$$

where CODE is the decimal equivalent of the value in FP10 through FP0. The values that can be programmed into these bits are 10 to 2047 decimal, which allows a conversion rate range of 9.54Hz to 1.953kHz when using a 10MHz clock.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch to the filter. For example, if the first notch of the filter is selected at 50Hz then a new word is available at a 50Hz rate or every 20ms. If the first notch is at 1kHz a new word is available every 1ms.

The settling-time of the converter to a full scale step input change is between 3 and 4 times the data rate. For example, with the first filter notch at 50Hz, the worst case settling time to a full scale step input change is 80ms. If the first notch is 1kHz, the settling time to a full scale input step is 4ms maximum.

The -3dB frequency is determined by the programmed first notch frequency according to the relationship:

$$f_{-3dB} = 0.262 \times f_{NOTCH}.$$

MD2 through MD0 - Bits 11 through 9 are the Operational Modes of the converter. See Table 6 for the Operational Modes description. After a $\overline{\text{RESET}}$ is applied to the part these bits are set to the self calibration mode.

B/U - Bit 8 is the Bipolar/Unipolar select bit. When this bit is set the HI7190 is configured for bipolar operation. When this bit is reset the part is in unipolar mode. This bit is set after a $\overline{\text{RESET}}$ is applied to the part.

G2 through G0 - Bits 7 through 5 select the gain of the input analog signal. The gain is accomplished through a programmable gain instrumentation amplifier that gains up incoming signals from 1 to 8. This is achieved by using a switched capacitor voltage multiplier network preceding the modulator. The higher gains (i.e., 16 to 128) are achieved through a combination of a PGIA gain of 8 and a digital multiply after the digital filter (see Table 9). The gain will affect noise and Signal to Noise Ratio of the conversion. These bits are cleared to a gain of 1 (G2, G1, G0 = 000) after a $\overline{\text{RESET}}$ is applied to the part.

TABLE 9. GAIN SELECT BITS

G2	G1	G0	GAIN	GAIN ACHIEVED
0	0	0	1	PGIA = 1, Filter Multiply = 1
0	0	1	2	PGIA = 2, Filter Multiply = 1
0	1	0	4	PGIA = 4, Filter Multiply = 1
0	1	1	8	PGIA = 8, Filter Multiply = 1
1	0	0	16	PGIA = 8, Filter Multiply = 2
1	0	1	32	PGIA = 8, Filter Multiply = 4
1	1	0	64	PGIA = 8, Filter Multiply = 8
1	1	1	128	PGIA = 8, Filter Multiply = 16

BO - Bit 4 is the Transducer Burn-Out Current source enable bit. When this bit is set (BO = 1) the burn-out current source connected to V_{INHI} internally is enabled. This current source can be used to detect the presence of an external connection to V_{INHI}. This bit is cleared after a $\overline{\text{RESET}}$ is applied to the part.

SB - Bit 3 is the Standby Mode enable bit used to put the HI7190 in a lower power/standby mode. When this bit is set (SB = 1) the filter nodes are halted, the $\overline{\text{DRDY}}$ line is set high and the modulator clock is disabled. When this bit is cleared the HI7190 begins operation as described by the contents of the Control Register. For example, if the Control Register is programmed for Self Calibration Mode and a notch frequency to 10Hz, the HI7190 will perform the self calibration before providing the data at the 10Hz rate. This bit is cleared after a $\overline{\text{RESET}}$ is applied to the part.

BD - Bit 2 is the Byte Direction bit used to select the multi-byte access ordering. The bit determines the either ascending or descending order access for the multi-byte registers. When set (BD = 1) the user can access multi-byte registers in ascending byte order and when cleared (BD = 0) the multi-byte registers are accessed in descending byte order. This bit is cleared after a $\overline{\text{RESET}}$ is applied to the part.

$\overline{\text{MSB}}$ - Bit 1 is used to select whether a serial data transfer is MSB or LSB first. This bit allows the user to change the order that data can be transmitted or received by the HI7190. When this bit is cleared ($\overline{\text{MSB}}$ = 0) the MSB is the first bit in a serial

data transfer. If set ($\overline{MSB}$ = 1), the LSB is the first bit transferred in the serial data stream. This bit is cleared after a $\overline{RESET}$ is applied to the part.

SDL - Bit 0 is the Serial Data Line control bit. This bit selects the transfer protocol of the serial interface. When this bit is cleared (SDL = 0), both read and write data transfers are done using the SDIO line. When set (SDL = 1), write transfers are done on the SDIO line and read transfers are done on the SDO line. This bit is cleared after a $\overline{RESET}$ is applied to the part.

Reading the Data Output Register

The HI7190 generates an active low interrupt ($\overline{DRDY}$) indicating valid conversion results are available for reading. At this time the Data Output Register contains the latest conversion result available from the HI7190. Data integrity is maintained at the serial output port but it is possible to miss a conversion result if the Data Output Register is not read within a given period of time. Maintaining data integrity means that if a Data Output Register read of conversion N is begun but not finished before the next conversion (conversion N + 1) is complete, the $\overline{DRDY}$ line remains active low and the data being read is not overwritten.

In addition to the Data Output Register, the HI7190 has a one conversion result storage buffer. No conversion results will be lost if the following constraints are met.

1) A Data Output Register read cycle is started for a given conversion (conversion X) $1/f_N - (128*1/f_{OSC})$ after $\overline{DRDY}$ initially goes active low. Failure to start the read cycle may result in conversion X + 1 data overwriting conversion X results. For example, with f_{OSC} = 10MHz, f_N = 2kHz, the read cycle must start within $1/2000 - 128(1/10^6) = 487\mu s$ after $\overline{DRDY}$ went low.

2) The Data Output Register read cycle for conversion X must be completed within $2(1/f_N)-1440(1/f_{OSC})$ after $\overline{DRDY}$ initially goes active low. If the read cycle for conversion X is not complete within this time the results of conversion X + 1 are lost and results from conversion X + 2 are now stored in the data output word buffer.

Completing the Data Output Register read cycle inactivates the $\overline{DRDY}$ interrupt. If the one word data output buffer is full when this read is complete this data will be immediately transferred to the Data Output Register and a new $\overline{DRDY}$ interrupt will be issued after the minimum $\overline{DRDY}$ pulse high time is met.

Writing the Control Register

If data is written to byte 2 and/or byte 1 of the Control Register the $\overline{DRDY}$ output is taken high and the device re-calibrates if written to a calibration mode. This action is taken because it is assumed that by writing byte 2 or byte 1 that the user either reprogrammed the filter or changed modes of the part. However, if a single data byte is written to byte 0, it is assumed that the gain has NOT been changed. It is up to the user to re-calibrate the HI7190 after the gain has been changed by this method. It is recommended that the entire Control Register be written to when changing the selected gain. This ensures that the part is re-calibrated before the $\overline{DRDY}$ signal goes low indicating valid data is available.

Offset Calibration Register

The Offset Calibration Register is a 24-bit register containing the offset correction factor. This register is indeterminate on power-up but will contain a Self Calibration correction value after a $\overline{RESET}$ has been applied.

BYTE 2

MSB	22	21	20	19	18	17	16
O23	O22	O21	O20	O19	O18	O17	O16

BYTE 1

15	14	13	12	11	10	9	8
O15	O14	O13	O12	O11	O10	O9	O8

BYTE 0

7	6	5	4	3	2	1	LSB
O7	O6	O5	O4	O3	O2	O1	O0

The Offset Calibration Register holds the value that corrects the filter output data to all 0's when the analog input is 0V.

Positive Full Scale Calibration Register

The Positive Full Scale Calibration Register is a 24-bit register containing the Positive Full Scale correction coefficient. This coefficient is used to determine the positive gain slope factor. This register is indeterminate on power-up but will contain a Self Calibration correction coefficient after a $\overline{RESET}$ has been applied.

BYTE 2

MSB	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16

BYTE 1

15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8

BYTE 0

7	6	5	4	3	2	1	LSB
P7	P6	P5	P4	P3	P2	P1	P0

Negative Full Scale Calibration Register

The Negative Full Scale Calibration Register is a 24-bit register containing the Negative Full Scale correction coefficient. This coefficient is used to determine the negative gain slope factor. This register is indeterminate on power-up but will contain a Self Calibration correction coefficient after a $\overline{RESET}$ has been applied.

BYTE 2

MSB	22	21	20	19	18	17	16
N23	N22	N21	N20	N19	N18	N17	N16

BYTE 1

15	14	13	12	11	10	9	8
N15	N14	N13	N12	N11	N10	N9	N8

BYTE 0

7	6	5	4	3	2	1	LSB
N7	N6	N5	N4	N3	N2	N1	N0

Die Characteristics

DIE DIMENSIONS:

3550µm x 6340µm

SUBSTRATE POTENTIAL (Powered Up):

AV_{SS}

METALLIZATION:

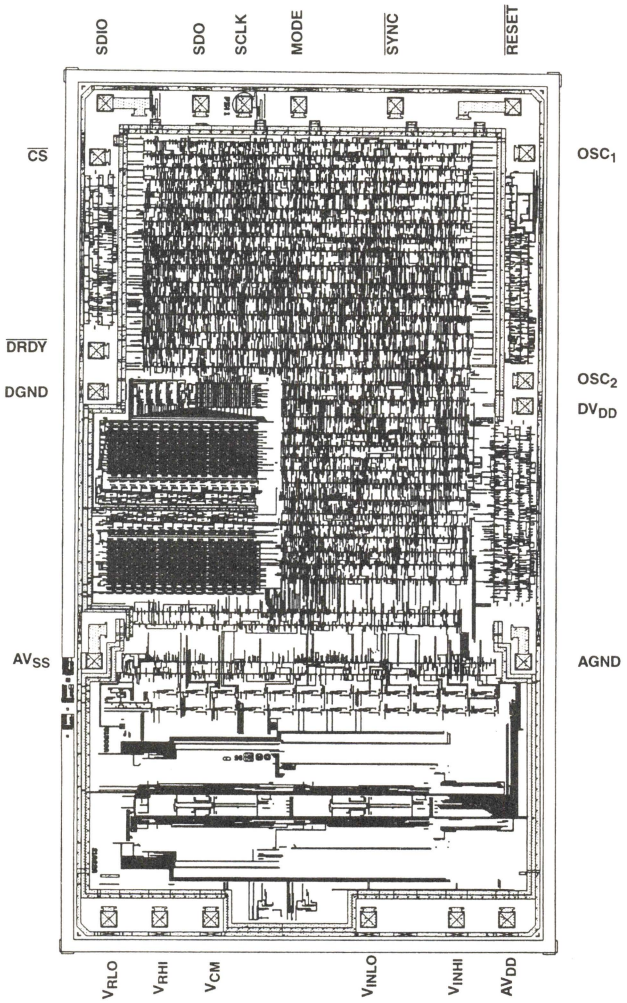
Type: AlSiCu
Thickness: Metal 2, 16kÅ
Metal 1, 6kÅ

PASSIVATION:

Type: Sandwich
Thickness: Nitride 8kÅ
USG 1kÅ

Metallization Mask Layout

HI7190



HARRIS SEMICONDUCTOR

HI7191

Low Cost, 24-Bit, High Precision, Sigma Delta A/D Converter

August 1997

Features

- 20-Bit Resolution with No Missing Code
- 0.0015% Integral Non-Linearity (Typ)
- 20mV to ±2.5V Full Scale Input Ranges
- Internal PGIA with Gains of 1 to 128
- Serial Data I/O Interface, SPI Compatible
- Differential Analog and Reference Inputs
- Internal or System Calibration
- -120dB Rejection of 60/50Hz Line Noise

Applications

- Low Cost Solution
- Process Control and Measurement
- Industrial Weight Scales
- Part Counting Scales
- Laboratory Instrumentation
- Motion Control
- Seismic Monitoring
- Magnetic Field Monitoring
- Intruder Detection
- Additional Reference Literature
  - AN9504 "A Brief Intro to Sigma Delta Conversion"
  - TB329 "Harris Sigma Delta Calibration Technique"
  - AN9505 "Using the HI7190 Evaluation Kit"
  - TB331 "Using the HI7190 Serial Interface"
  - AN9527 "Interfacing HI7190 to a Microcontroller"
  - AN9532 "Using HI7190 in a Multiplexed System"
  - AN9601 "Using HI7190 with a Single +5V Supply"

Description

The Harris HI7191 is a monolithic instrumentation, sigma delta A/D converter which operates from ±5V supplies. Both the signal and reference inputs are fully differential for maximum flexibility and performance. An internal Programmable Gain Instrumentation Amplifier (PGIA) provides input gains from 1 to 128 eliminating the need for external pre-amplifiers. The on-demand converter auto-calibrate function is capable of removing offset and gain errors existing in external and internal circuitry. The on-board user programmable digital filter provides over -120dB of 60/50Hz noise rejection and allows fine tuning of resolution and conversion speed over a wide dynamic range.

The HI7191 contains a serial I/O port and is compatible with most synchronous transfer formats including both the Motorola 6805/11 series SPI and Intel 8051 series SSR protocols. A sophisticated set of commands gives the user control over calibration, PGIA gain, device selection, standby mode, and several other features. The On-chip Calibration Registers allow the user to read and write calibration data.

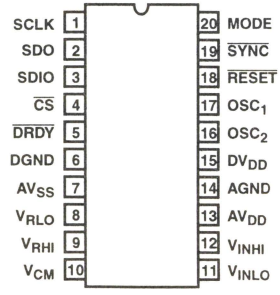
NOTE: The application notes and evaluation board for the HI7190 are applicable to the HI7191.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI7191IP	-40 to 85	20 Ld PDIP	E20.3
HI7191IB	-40 to 85	20 Ld SOIC	M20.3
HI7190EVAL	Evaluation Kit		

Pinout

HI7191
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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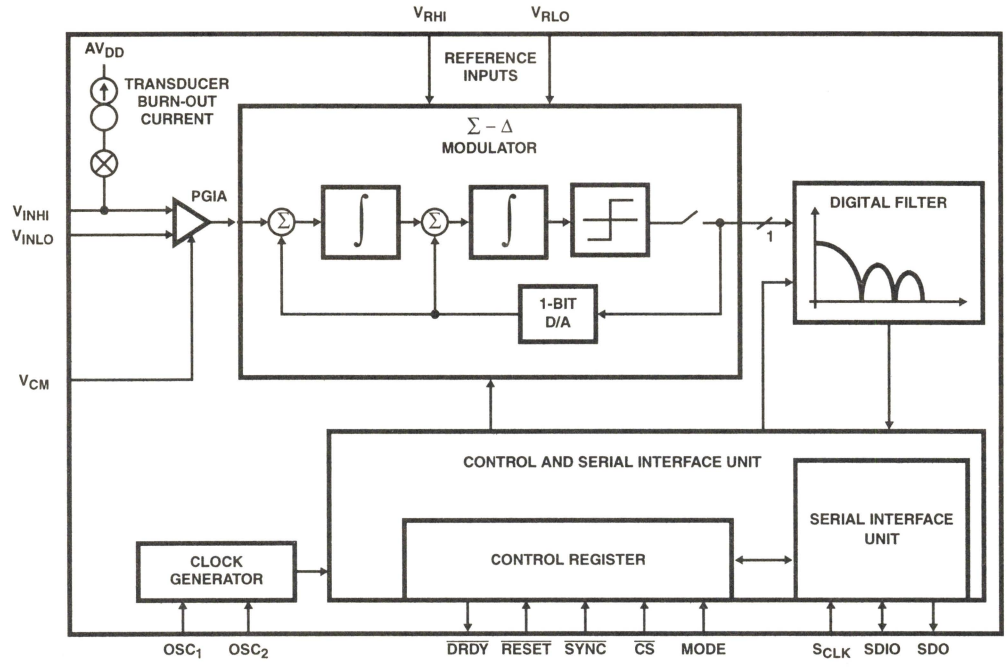
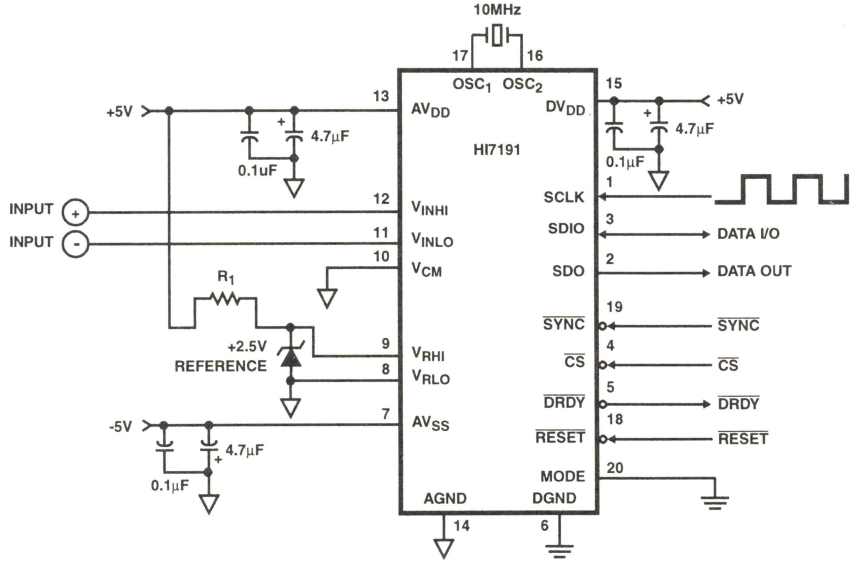
File Number **4138.2**

Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage
- AV_{DD} to AGND . . . . . +5.5V
- AV_{SS} to AGND . . . . . -5.5V
- DV_{DD} to DGND . . . . . +5.5V
- DGND to AGND . . . . . ±0.3V

Analog Input Pins . . . . . AV_{SS} to AV_{DD}
Digital Input, Output and I/O Pins . . . . . DGND to DV_{DD}
ESD Tolerance (No Damage)
- Human Body Model 500V
- Machine Model . . . . . +100V
- Charged Device Model 1000V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	125
SOIC Package	100

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND = 0V, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 10MHz, Bipolar Input Range Selected, f_N = 10Hz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Integral Non-Linearity, INL	End Point Line Method (Notes 3, 5, 6)	-	±0.0015	±0.003	%FS
Differential Non-Linearity	(Note 2)	No Missing codes to 20-Bits			LSB
Offset Error, V_{OS}	$V_{INHI} = V_{INLO}$ (Notes 3, 5, 8, 10)	-	-	-	-
Offset Error Drift	$V_{INHI} = V_{INLO}$ (Notes 3, 8)	-	1	-	µV/°C
Full Scale Error, FSE	$V_{INHI} - V_{INLO}$ = +2.5V (Notes 3, 5, 8, 10)	-	-	-	-
Noise, e_N	See Table 1	-	-	-	-
Common Mode Rejection Ratio, CMRR	V_{CM} = 0V $V_{INHI} = V_{INLO}$ from -2V to +2V		-70	-	dB
Normal Mode 50Hz Rejection	Filter Notch = 10Hz, 25Hz, 50Hz (Note 2)	-120	-	-	dB
Normal Mode 60Hz Rejection	Filter Notch = 10Hz, 30Hz, 60Hz (Note 2)	-120	-	-	dB
Step Response Settling Time		-	2	4	Conversions
ANALOG INPUTS					
Input Voltage Range	Unipolar Mode (Note 9)	0	-	V_{REF}	V
Input Voltage Range	Bipolar Mode (Note 9)	$-V_{REF}$	-	V_{REF}	V
Common Mode Input Range	(Note 2)	AV_{SS}	-	AV_{DD}	V
Input Leakage Current, I_{IN}	$V_{IN} = AV_{DD}$ (Note 2)	-	-	1.0	nA
Input Capacitance, C_{IN}		-	5.0	-	pF
Reference Voltage Range, V_{REF} ($V_{REF} = V_{RHI} - V_{RLO}$)		2.5	-	5	V
Transducer Burn-Out Current, I_{BO}		-	200	-	nA
CALIBRATION LIMITS					
Positive Full Scale Calibration Limit		-	-	$1.2(V_{REF}/Gain)$	-
Negative Full Scale Calibration Limit		-	-	$1.2(V_{REF}/Gain)$	-
Offset Calibration Limit		-	-	$1.2(V_{REF}/Gain)$	-
Input Span		$0.2(V_{REF}/Gain)$	-	$2.4(V_{REF}/Gain)$	-
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}	(Note 11)	2.0	-	-	V

Electrical Specifications AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND = 0V, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 10MHz, Bipolar Input Range Selected, f_N = 10Hz **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic Current, I_I	V_{IN} = 0V, +5V	-	1.0	10	µA
Input Capacitance, C_{IN}	V_{IN} = 0V	-	5.0	-	pF
DIGITAL OUTPUTS					
Output Logic High Voltage, V_{OH}	I_{OUT} = -100µA (Note 7)	2.4	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OUT} = 3.0mA (Note 7)	-	-	0.4	V
Output Three-State Leakage Current, I_{OZ}	V_{OUT} = 0V, +5V (Note 7)	-10	1	10	µA
Digital Output Capacitance, C_{OUT}		-	10	-	pF
TIMING CHARACTERISTICS					
SCLK Minimum Cycle Time, t_{SCLK}		200	-	-	ns
SCLK Minimum Pulse Width, t_{SCLKPW}		50	-	-	ns
$\overline{CS}$ to SCLK Precharge Time, t_{PRE}		50	-	-	ns
$\overline{DRDY}$ Minimum High Pulse Width	(Notes 2, 7)	500	-	-	ns
Data Setup to SCLK Rising Edge (Write), t_{DSU}		50	-	-	ns
Data Hold from SCLK Rising Edge (Write), t_{DHLD}		0	-	-	ns
Data Read Access from Instruction Byte Write, t_{ACC}	(Note 7)	-	-	40	ns
Read Bit Valid from SCLK Falling Edge, t_{DV}	(Note 7)	-	-	40	ns
Last Data Transfer to Data Ready Inactive, $t_{\overline{DRDY}}$	(Note 7)	-	35	-	ns
$\overline{RESET}$ Low Pulse Width	(Note 2)	100	-	-	ns
$\overline{SYNC}$ Low Pulse Width	(Note 2)	100	-	-	ns
Oscillator Clock Frequency	(Note 2)	0.1	-	10	MHz
Output Rise/Fall Time	(Note 2)	-	-	30	ns
Input Rise/Fall Time	(Note 2)	-	-	1	µs
POWER SUPPLY CHARACTERISTICS					
IAV_{DD}		-	-	1.5	mA
IAV_{SS}		-	-	1.5	mA
IDV_{DD}	SCLK = 4MHz	-	-	3.0	mA
Power Dissipation, Active PD_A	SB = '0'	-	15	30	mW
Power Dissipation, Standby PD_S	SB = '1'	-	5	-	mW
PSRR	(Note 3)	-	-70	-	dB

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Parameter guaranteed by design or characterization, not production tested.
3. Applies to both bipolar and unipolar input ranges.
4. These errors can be removed by re-calibrating at the desired operating temperature.
5. Applies after system calibration.
6. Fully differential input signal source is used.
7. See Load Test Circuit, Figure 10, R1 = 10kΩ, C_L = 50pF.
8. 1 LSB = 298nV at 24-bits for a Full Scale Range of 5V.
9. $V_{REF} = V_{RHI} - V_{RLO}$
10. These errors are on the order of the output noise shown in Table 1.
11. All inputs except OSC_1. The OSC_1 input V_{IH} is 3.5V minimum.

Timing Diagrams

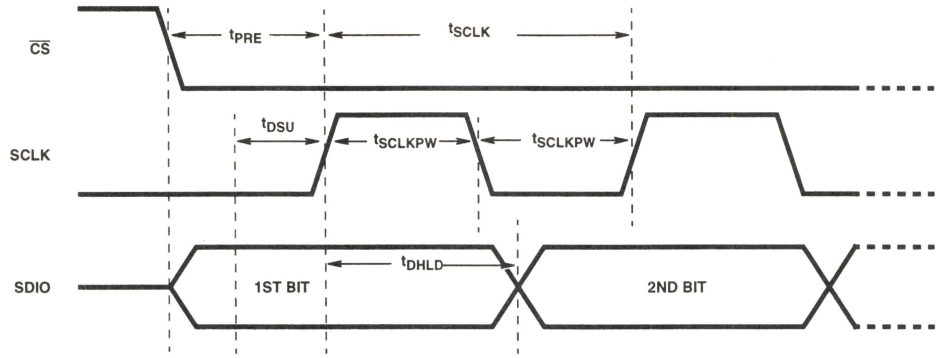


FIGURE 1. DATA WRITE TO HI7191

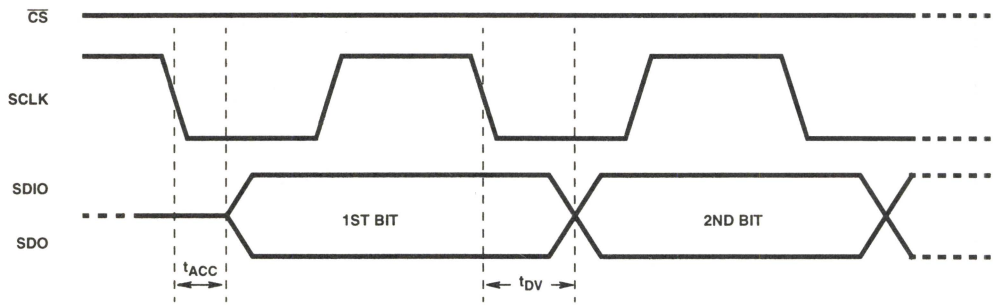


FIGURE 2. DATA READ FROM HI7191

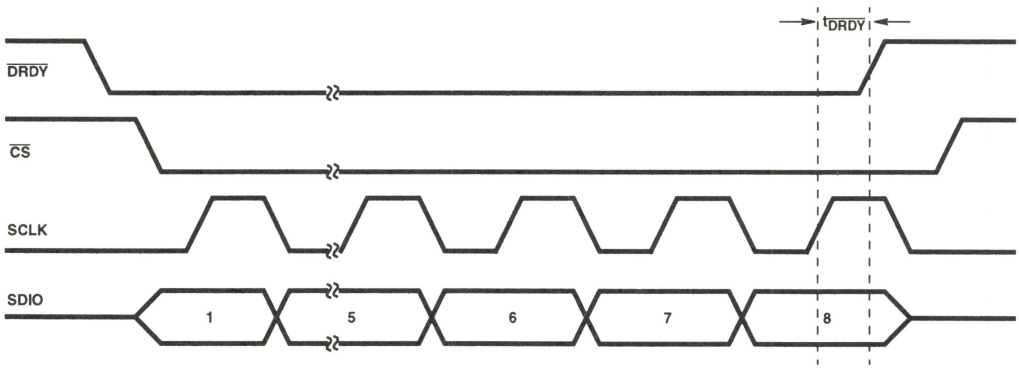


FIGURE 3. DATA READ FROM HI7191

Pin Descriptions

20 LEAD PDIP, SOIC	PIN NAME	PIN DESCRIPTION
1	SCLK	Serial Interface Clock. Synchronizes serial data transfers. Data is input on the rising edge and output on the falling edge.
2	SDO	Serial Data OUT. Serial data is read from this line when using a 3-HI7191 wire serial protocol such as the Motorola Serial Peripheral Interface.
3	SDIO	Serial Data IN or OUT. This line is bidirectional programmable and interfaces directly to the Intel Standard Serial Interface using a 2-wire serial protocol.
4	$\overline{CS}$	Chip Select Input. Used to select the HI7191 for a serial data transfer cycle. This line can be tied to DGND.
5	$\overline{DRDY}$	An Active Low Interrupt indicating that a new data word is available for reading.
6	DGND	Digital Supply Ground.
7	AV_{SS}	Negative Analog Power Supply (-5V).
8	V_{RLO}	External Reference Input. Should be negative referenced to V_{RHI}.
9	V_{RHI}	External Reference Input. Should be positive referenced to V_{RLO}.
10	V_{CM}	Common Mode Input. Should be set to halfway between AV_{DD} and AV_{SS}.
11	V_{INLO}	Analog Input LO. Negative input of the PGIA.
12	V_{INHI}	Analog Input HI. Positive input of the PGIA. The V_{INHI} input is connected to a current source that can be used to check the condition of an external transducer. This current source is controlled via the Control Register.
13	AV_{DD}	Positive Analog Power Supply (+5V).
14	AGND	Analog Supply Ground.
15	DV_{DD}	Positive Digital Supply (+5V).
16	OSC_2	Used to connect a crystal source between OSC_1 and OSC_2. Leave open otherwise.
17	OSC_1	Oscillator Clock Input for the device. A crystal connected between OSC_1 and OSC_2 will provide a clock to the device, or an external oscillator can drive OSC_1. The oscillator frequency should be 10MHz (Typ).
18	$\overline{RESET}$	Active Low Reset Pin. Used to initialize the HI7191 registers, filter and state machines.
19	$\overline{SYNC}$	Active Low Sync Input. Used to control the synchronization of a number of HI7191s. A logic '0' initializes the converter.
20	MODE	Mode Pin. Used to select between Synchronous Self Clocking (Mode = 1) or Synchronous External Clocking (Mode = 0) for the Serial Port.

Load Test Circuit

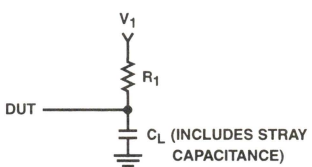
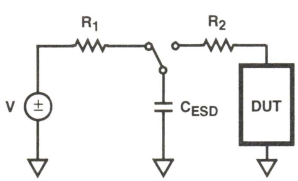


FIGURE 4.

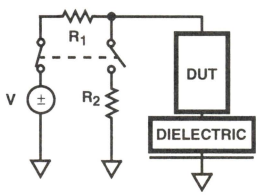
ESD Test Circuit



HUMAN BODY
C_{ESD} = 100pF
R_1 = 10MΩ
R_2 = 1.5kΩ

MACHINE MODEL
C_{ESD} = 200pF
R_1 = 10MΩ
R_2 = 0Ω

FIGURE 5A.



CHARGED DEVICE MODEL
R_1 = 1GΩ
R_2 = 1Ω

FIGURE 5B.

TABLE 1. RMS INPUT REFERRED NOISE FOR VARIOUS GAINS AND CONVERSION FREQUENCIES

CONVERSION RATE (f_N)	INPUT CUTOFF FREQUENCY (-3dB, f_S)	GAIN = 1 RMS NOISE (μV)	GAIN = 2 RMS NOISE (μV)	GAIN = 4 RMS NOISE (μV)	GAIN = 8 RMS NOISE (μV)	GAIN = 16 RMS NOISE (μV)	GAIN = 32 RMS NOISE (μV)	GAIN = 64 RMS NOISE (μV)	GAIN = 128 RMS NOISE (μV)
10Hz	2.62Hz	0.435	0.246	0.134	0.126	0.066	0.134	0.070	0.060
25Hz	6.55Hz	0.604	0.336	0.226	0.246	0.237	0.212	0.220	0.209
30Hz	7.86Hz	0.689	0.796	0.557	0.327	0.163	0.077	0.105	0.238
50Hz	13.1Hz	0.903	0.477	0.341	0.529	0.258	0.442	0.224	0.364
60Hz	15.7Hz	1.04	0.550	0.380	0.350	0.293	0.428	0.350	0.326
100Hz	26.2Hz	2.50	1.05	0.628	0.786	0.406	0.672	0.414	0.496
250Hz	65.5Hz	6.73	2.50	1.28	1.26	0.669	1.10	2.40	2.40
500Hz	131Hz	19.4	7.61	14.7	2.54	1.40	2.22	3.40	4.79
1kHz	262Hz	96.7	32.6	18.4	11.0	5.16	10.2	4.97	5.63
2kHz	524Hz	579	198	109	62.8	33.8	108	55.2	24.5

Definitions

Integral Non-Linearity, INL, is the maximum deviation of any digital code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (a point 0.5 LSB below the first code transition 000...000 and 000...001) and full scale (a point 0.5 LSB above the last code transition 111...110 to 111...111).

Differential Non-Linearity, DNL, is the deviation from the actual difference between midpoints and the ideal difference between midpoints (1 LSB) for adjacent codes. If this difference is equal to or more negative than 1 LSB, a code will be missed.

Offset Error, V_{OS}, offset error is the deviation of the first code transition from the ideal input voltage (V_{IN} - 0.5 LSB). This error can be calibrated to the order of the noise level shown in Table 1.

Full Scale Error, FSE, is the deviation of the last code transition from the ideal input full scale voltage (V_{IN}- + V_{REF}/Gain - 1.5 LSB). This error can be calibrated to the order of the noise level shown in Table 1.

Input Span, defines the minimum and maximum input voltages the device can handle while still calibrating properly for gain.

Noise, e_N, Table 1 shows the input referred peak-to-peak and RMS noise for some typical notch and -3dB frequencies. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5V which means the input range is ±2.5V. Measurements are taken for 100 conversions with the peak-to-peak output noise being the difference between the maximum and minimum readings over the 100 conversions.

The RMS input referred noise data is calculated by converting the peak-to-peak numbers to RMS values by dividing by a crest factor of 6.6, and then dividing that result by the gain of the HI7191. Finally, the Effective Number of Bits (ENOB) or effective resolution is calculated by taking the $\log_2$ (5V/RMS output noise).

The noise from the part comes from two sources, the quantization noise from the analog-to-digital conversion process and device noise. Device noise (or Wideband Noise) is independent of gain and essentially flat across the frequency spectrum. Quantization noise is ratiometric to input full scale (and hence gain) and its frequency response is shaped by the modulator.

Looking at Table 1, as the cutoff frequency increases the output noise increases. This is due to more of the quantization noise of the part coming through to the output and, hence, the output noise increases with increasing -3dB frequencies. For the lower notch settings, the output noise is dominated by the device noise and, hence, altering the gain has little effect on the output noise. At higher notch frequencies, the quantization noise dominates the output noise and, in this case, the output noise tends to decrease with increasing gain.

Since the output noise comes from two sources, the effective resolution of the device (i.e., the ratio of the input full scale to the output RMS noise) does not remain constant with increasing gain or with increasing bandwidth. It is possible to do post-filtering (such as brick wall filtering) on the data to improve the overall resolution for a given -3dB frequency and also to further reduce the output noise.

Circuit Description

The HI7191 is a monolithic sigma delta A/D converter which operates from ±5V supplies and is intended for measurement of wide dynamic range, low frequency signals. It contains a Programmable Gain Instrumentation Amplifier (PGIA), sigma delta ADC, digital filter, bidirectional serial port (compatible with many industry standard protocols), clock oscillator, and an on chip controller.

The signal and reference inputs are fully differential for maximum flexibility and performance. Normally V_{RHI} and V_{RLO} are tied to +2.5V and AGND respectively. This allows for input ranges of 2.5V and 5V when operating in the unipolar and bipolar modes respectively (assuming the PGIA is configured for a gain of 1). The internal PGIA provides input gains from 1 to 128 and eliminates the need for external pre-amplifiers. This means the device will convert signals

ranging from 0V to +20mV and 0V to +2.5V when operating in the unipolar mode or signals in the range of ±20mV to ±2.5V when operating in the bipolar mode.

The input signal is continuously sampled at the input to the HI7191 at a clock rate set by the oscillator frequency and the selected gain. This signal then passes through the sigma delta modulator (which includes the PGIA) and emerges as a pulse train whose code density contains the analog signal information. The output of the modulator is fed into the sinc3 digital low pass filter. The filter output passes into the calibration block where offset and gain errors are removed. The calibrated data is then coded (2's complement, offset binary or binary) before being stored in the Data Output Register. The Data Output Register update rate is determined by the first notch frequency of the digital filter. This first notch frequency is programmed into HI7191 via the Control Register and has a range of 10Hz to 1.953kHz which corresponds to -3dB frequencies of 2.62Hz and 512Hz respectively.

Output data coding on the HI7191 is programmable via the Control Register. When operating in bipolar mode, data output can be either 2's complement or offset binary. In unipolar mode output is binary.

The $\overline{DRDY}$ signal is used to alert the user that new output data is available. Converted data is read via the HI7191 serial I/O port which is compatible with most synchronous transfer formats including both the Motorola 6805/11 series SPI and Intel 8051 series SSR protocols. Data Integrity is always maintained at the HI7191 output port. This means that if a data read of conversion N is begun but not finished before the next conversion (conversion N + 1) is complete, the $\overline{DRDY}$ line remains active (low) and the data being read is not overwritten.

The HI7191 provides many calibration modes that can be initiated at any time by writing to the Control Register. The device can perform system calibration where external components are included with the HI7191 in the calibration loop or self-calibration where only the HI7191 itself is in the calibration loop. The On-chip Calibration Registers are read/write registers which allow the user to read calibration coefficients as well as write previously determined calibration coefficients.

Circuit Operation

The analog and digital supplies and grounds are separate on the HI7191 to minimize digital noise coupling into the analog circuitry. Nominal supply voltages are AV_{DD} = +5V, DV_{DD} = +5V, and AV_{SS} = -5V. If the same supply is used for AV_{DD} and DV_{DD} it is imperative that the supply is separately decoupled to the AV_{DD} and DV_{DD} pins on the HI7191. Separate analog and digital ground planes should be maintained on the system board and the grounds should be tied together back at the power supply.

When the HI7191 is powered up it needs to be reset by pulling the $\overline{RESET}$ line low. The reset sets the internal registers of the HI7191 as shown in Table 2 and puts the part in the bipolar mode with a gain of 1 and offset binary coding. The filter notch of the digital filter is set at 30Hz while the I/O is set up for bidirectional I/O (data is read and written on the SDIO line and SDO is three-stated), descending byte order, and MSB first data format. A self calibration is performed before the device begins converting. $\overline{DRDY}$ goes low when valid data is available at the output.

TABLE 2. REGISTER RESET VALUES

REGISTER	VALUE (HEX)
Data Output Register	XXXX (Undefined)
Control Register	28B300
Offset Calibration Register	Self Calibration Value
Positive Full Scale Calibration Register	Self Calibration Value
Negative Full Scale Calibration Register	Self Calibration Value

The configuration of the HI7191 is changed by writing new setup data to the Control Register. Whenever data is written to byte 2 and/or byte 1 of the Control Register the part assumes that a critical setup parameter is being changed which means that $\overline{DRDY}$ goes high and the device is re-synchronized. If the configuration is changed such that the device is in any one of the calibration modes, a new calibration is performed before normal conversions continue. If the device is written to the conversion mode, a new calibration is NOT performed (A new calibration is recommended any time data is written to the Control Register.). In either case, $\overline{DRDY}$ goes low when valid data is available at the output.

If a single data byte is written to byte 0 of the Control Register, the device assumes the gain has NOT been changed. It is up to the user to re-calibrate the device if the gain is changed in this manner. For this reason it is recommended that the entire Control Register be written when changing the gain of the device. This ensures that the part is re-calibrated (if in a calibration mode) before the $\overline{DRDY}$ output goes low indicating that valid data is available.

The calibration registers can be read via the serial interface at any time. However, care must be taken when writing data to the calibration registers. If the HI7191 is internally updating any calibration register the user can not write to that calibration register. See the Operational Modes section for details on which calibration registers are updated for the various modes.

Since access to the calibration registers is asynchronous to the conversion process the user is cautioned that new calibration data may not be used on the very next set of "valid" data after a calibration register write. It is guaranteed that the new data will take effect on the second set of output data. Non-calibrated data can be obtained from the device by writing 000000 (h) to the Offset Calibration Register, 800000 (h) to the Positive Full Scale Calibration Register, and 800000 (h) to the Negative Full Scale Calibration Register. This sets the offset correction factor to 0 and the positive and negative gain slope factors to 1.

If several HI7191s share a system master clock the $\overline{SYNC}$ pin can be used to synchronize their operation. A common $\overline{SYNC}$ input to multiple devices will synchronize operation such that all output registers are updated simultaneously. Of

course the $\overline{SYNC}$ pin would normally be activated only after each HI7191 has been calibrated or has had calibration coefficients written to it.

The $\overline{SYNC}$ pin can also be used to control the HI7191 when an external multiplexer is used with a single HI7191. The $\overline{SYNC}$ pin in this application can be used to guarantee a maximum settling time of 3 conversion periods when switching channels on the multiplexer.

Analog Section Description

Figure 6 shows a simplified block diagram of the analog modulator front end of a sigma delta A/D Converter. The input signal V_{IN} comes into a summing junction (the PGIA in this case) where the previous modulator output is subtracted from it. The resulting signal is then integrated and the output of the integrator goes into the comparator. The output of the comparator is then fed back via a one bit DAC to the summing junction. The feedback loop forces the average of the fed back signal to be equal to the input signal V_{IN}.

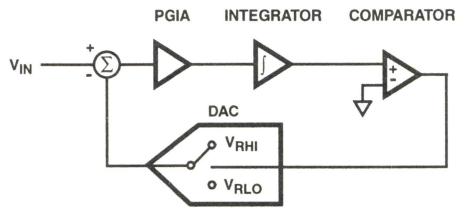


FIGURE 6. SIMPLE MODULATOR BLOCK DIAGRAM

Analog Inputs

The analog input on the HI7191 is a fully differential input with programmable gain capabilities. The input accepts both unipolar and bipolar input signals and gains range from 1 to 128. The common mode range of this input is from AVSS to AVDD provided that the absolute value of the analog input voltage lies within the power supplies. The input impedance of the HI7191 is dependent upon the modulator input sampling rate and the sampling rate varies with the selected PGIA gain. Table 3 below shows the sampling rates and input impedances for the different gain settings of the HI7191. Note that this table is valid only for a 10MHz master clock. If the input clock frequency is changed then the input impedance will change accordingly. The equation used to calculate the input impedance is:

$Z_{IN} = 1/(C_{IN} \times f_S)$,

where C_{in} is the nominal input capacitance (8pF) and f_S is the modulator sampling rate.

TABLE 3. EFFECTIVE INPUT IMPEDANCE vs GAIN

GAIN	SAMPLING RATE (kHz)	INPUT IMPEDANCE (MΩ)
1	78.125	1.6
2	156.25	0.8
4	312.5	0.4
8, 16, 32, 64, 128	625	0.2

Input Filter To Reduce Wideband Noise

The HI7191 internal digital filter does not remove noise that is located at integer multiples of the sampling frequency. To reduce this wideband noise an external RC low pass filter may be used. Below is a recommended input filter configuration. Tables 4 and 5 provide external component values for 16-bit and 20-bit performance respectively.

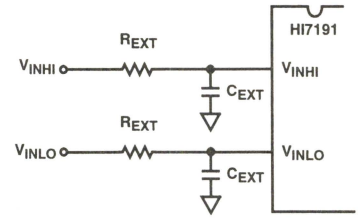


FIGURE 7. INPUT FILTER

TABLE 4. GAIN VERSUS EXTERNAL RC FILTER FOR 16-BIT PERFORMANCE

GAIN	f_S (kHz) APPROX.	t_S (μs)	C_{EXT} 0pF R_{EXT} (Ω)	C_{EXT} 50pF R_{EXT} (Ω)	C_{EXT} 100pF R_{EXT} (Ω)	C_{EXT} 500pF R_{EXT} (Ω)
1	80	5	55K	8K	4.2K	900
2	160	2.5	28K	4K	2.1K	450
4	315	1.25	13K	2K	1.2K	250
8 or more	625	0.640	6K	1.2K	700	150

TABLE 5. GAIN vs EXTERNAL RC FILTER FOR 20-BIT PERFORMANCE

GAIN	f_S (kHz) APPROX.	t_S (μs)	C_{EXT} 0pF R_{EXT} (Ω)	C_{EXT} 50pF R_{EXT} (Ω)	C_{EXT} 100pF R_{EXT} (Ω)	C_{EXT} 500pF R_{EXT} (Ω)
1	80	5	45K	6.5K	3.4K	720
2	160	2.5	23K	3.3K	1.7K	370
4	315	1.25	12K	1.7K	950	200
8 or more	625	0.640	7K	1.1K	620	130

NOTE: f_S = Sampling Rate, t_S = Settling Time = $^1/_2(1/f_S)(0.8)$.

Bipolar/Unipolar Input Ranges

The input on the HI7191 can accept either unipolar or bipolar input voltages. Bipolar or unipolar options are chosen by programming the B/$\overline{U}$ bit of the Control Register. Programming the part for either unipolar or bipolar operation does not change the input signal conditioning.

The inputs are differential, and as a result are referenced to the voltage on the V_{INLO} input. For example, if V_{INLO} is +1.25V and the HI7191 is configured for unipolar operation with a gain of 1 and a V_{REF} of +2.5V, the input voltage range on the V_{INLO} input is +1.25V to +3.75V. If V_{INLO} is +1.25V

and the HI7191 is configured for bipolar mode with gain of 1 and a V_{REF} of +2.5V, the analog input range on the V_{INHI} input is -1.25V to +3.75V.

Programmable Gain Instrumentation Amplifier

The Programmable Gain Instrumentation Amplifier allows the user to directly interface low level sensors and bridges directly to the HI7191. The PGIA has 4 selectable gain options of 1, 2, 4, 8 which are implemented by multiple sampling of the input signal. Input signals can be gained up further to 16, 32, 64 or 128. These higher gains are implemented in the digital section of the design to maintain a high signal to noise ratio through the front end amplifiers. The gain is digitally programmable in the Control Register via the serial interface. For optimum PGIA performance the V_{CM} pin should be tied to the mid point of the analog supplies.

Differential Reference Input

The reference inputs of the of the HI7191, V_{RHI} and V_{RLO}, provide a differential reference input capability. The nominal differential voltage ($V_{REF} = V_{RHI} - V_{RLO}$) is +2.5V and the common mode voltage cab be anywhere between AV_{SS} and AV_{DD}. Larger values of V_{REF} can be used without degradation in performance with the maximum reference voltage being V_{REF} = +5V. Smaller values of V_{REF} can also be used but performance will be degraded since the LSB size is reduced.

The full scale range of the HI7191 is defined as:

$FSR_{BIPOLAR} = 2 \times V_{REF}/GAIN$,

$FSR_{UNIPOLAR} = V_{REF}/GAIN$,

and V_{RHI} must always be greater than V_{RLO} for proper operation of the device.

The reference inputs provide a high impedance dynamic load similar to the analog inputs and the effective input impedance for the reference inputs can be calculated in the same manner as it is for the analog input impedance. The only difference in the calculation is that C_{IN} for the reference inputs is 10.67pF. Therefor, the input impedance range for the reference inputs is from 149kΩ in a gain of 8 or higher mode to 833kΩ in the gain of 1 mode.

V_{CM} Input

The voltage at the V_{CM} input is the voltage that the internal analog circuitry is referenced to and should always be tied to the midpoint of the AV_{DD} and AV_{SS} supplies. This point provides a common mode input voltage for the internal operational amplifiers and must be driven from a low noise, low impedance source if it is not tied to analog ground. Failure to do so will result in degraded HI7191 performance. It is recommended that V_{CM} be tied to analog ground when operating off of AV_{DD} = +5V and AV_{SS} = -5V supplies.

V_{CM} also determines the headroom at the upper and lower ends of the power supplies which is limited by the common mode input range where the internal operational amplifiers remain in the linear, high gain region of operation. The HI7191 is designed to have a range of AV_{SS} +1.8V < V_{CM} < AV_{DD} - 1.8V. Exceeding this range on the V_{CM} pin will compromise the device performance.

Transducer Burn-Out Current Source

The VINHI input of the HI7191 contains a 200nA (Typ) current source which can be turned on/off via the Control Register. This current source can be used in checking whether a transducer has burnt-out or become open before attempting to take measurements on that channel. When the current source is turned on an additional offset will be created indicating the presence of a transducer. The current source is controlled by the BO bit (Bit 4) in the Control Register and is disabled on power up. See Figure 8 for an applications circuit.

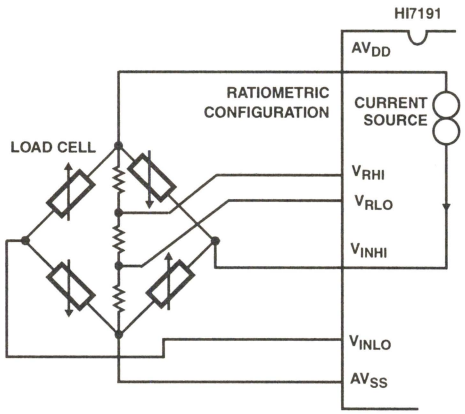


FIGURE 8. BURN-OUT CURRENT SOURCE CIRCUIT

Digital Section Description

A block diagram of the digital section of the HI7191 is shown in Figure 9. This section includes a low pass decimation filter, conversion controller, calibration logic, serial interface, and clock generator.

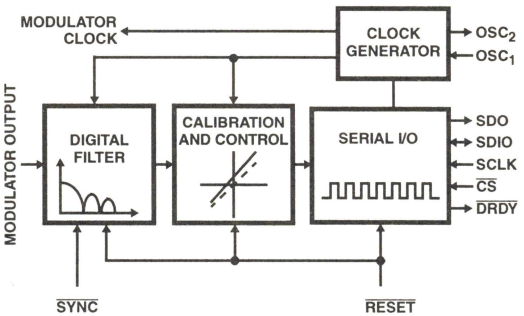


FIGURE 9. DIGITAL SECTION BLOCK DIAGRAM

Digital Filtering

One advantage of digital filtering is that it occurs after the conversion process and can remove noise introduced during the conversion. It can not, however, remove noise present on the analog signal prior to the ADC (which an analog filter can).

One problem with the modulator/digital filter combination is that excursions outside the full scale range of the device

could cause the modulator and digital filter to saturate. This device has headroom built in to the modulator and digital filter which tolerates signal deviations up to 33% outside of the full scale range of the device. If noise spikes can drive the input signal outside of this extended range it is recommended that an input analog filter is used or the overall input signal level is reduced.

Low Pass Decimation Filter

The digital low pass filter is a Hogenauer ($sinc^3$) decimating filter. This filter was chosen because it is a cost effective low pass decimating filter that minimizes the need for internal multipliers and extensive storage and is most effective when used with high sampling or oversampling rates. Figure 10 shows the frequency characteristics of the filter where f_C is the -3dB frequency of the input signal and f_N is the programmed notch frequency. The analog modulator sends a one bit data stream to the filter at a rate of that is determined by:

$f_{MODULATOR} = f_{OSC}/128$,

$f_{MODULATOR} = 78.125kHz$ for $f_{OSC} = 10MHz$.

The filter then converts the serial modulator data into 40-bit words for processing by the Hogenauer filter. The data is decimated in the filter at a rate determined by the CODE word FP10-FP0 (programed by the user into the Control Register) and the external clock rate. The equation is:

$f_{NOTCH} = f_{OSC}/(512 \times CODE)$.

The Control Register has 11 bits that select the filter cut off frequency and the first notch of the filter. The output data update rate is equal to the notch frequency. The notch frequency sets the Nyquist sampling rate of the device while the -3dB point of the filter determines the frequency spectrum of interest (f_S). The FP bits have a usable range of 10 through 2047 where 10 yields a 1.953kHz Nyquist rate.

The Hogenauer filter contains alias components that reflect around the notch frequency. If the spectrum of the frequency of interest reaches the alias component, the data has been aliased and therefore undersampled.

Filter Characteristics

The FP10 to FP0 bits programmed into the Control Register determine the cutoff (or notch) frequency of the digital filter. The allowable code range is $000A_H$ to $7A1_H$. This corresponds to maximum and minimum cutoff frequencies of 1.953kHz and 10Hz respectively when operating at a clock frequency of 10MHz. If a 1MHz clock is used then the maximum and minimum cutoff frequencies become 0.1953kHz and 1Hz respectively. A plot of the $(sinx/x)^3$ digital filter characteristics is shown in Figure 10. This filter provides greater than 120dB of 50Hz or 60Hz rejection. Changing the clock frequency or the programming of the FP bits does not change the shape of the filter characteristics, it merely shifts the notch frequency. This low pass digital filter at the output of the converter has an accompanying settling time for step inputs just as a low pass analog filter does. New data takes between 3 and 4 conversion periods to settle and update on the serial port with a conversion period t_{CONV} being equal to $1/f_N$.

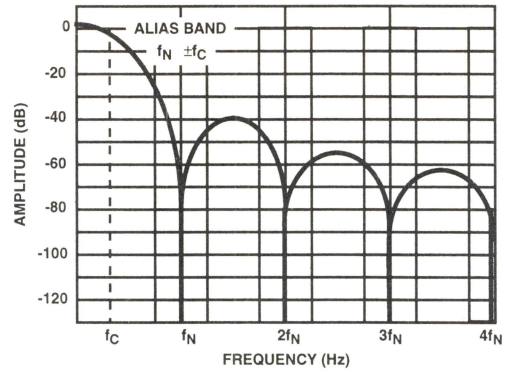


FIGURE 10. LOW PASS FILTER FREQUENCY CHARACTERISTICS

Input Filtering

The digital filter does not provide rejection at integer multiples of the modulator sampling frequency. This implies that there are frequency bands where noise passes to the output without attenuation. For most cases this is not a problem because the high oversampling rate and noise shaping characteristics of the modulator cause this noise to become a small portion of the broadband noise which is filtered. However, if an anti-alias filter is necessary a single pole RC filter is usually sufficient.

If an input filter is used the user must be careful that the source impedance of the filter is low enough not to cause gain errors in the system. The DC input impedance at the inputs is > 1GW but it is a dynamic load that changes with clock frequency and selected gain. The input sample rate, also dependent upon clock frequency and gain, determines the allotted time for the input capacitor to charge. The addition of external components may cause the charge time of the capacitor to increase beyond the allotted time. The result of the input not settling to the proper value is a system gain error which can be eliminated by system calibration of the HI7191.

Clocking/Oscillators

The master clock into the HI7191 can be supplied by either a crystal connected between the OSC_1 and OSC_2 pins as shown in Figure 11A or a CMOS compatible clock signal connected to the OSC_1 pin as shown in Figure 11B. The input sampling frequency, modulator sampling frequency, filter -3dB frequency, output update rate, and calibration time are all directly related to the master clock frequency, f_{OSC}. For example, if a 1MHz clock is used instead of a 10MHz clock, what is normally a 10Hz conversion rate becomes a 1Hz conversion rate. Lowering the clock frequency will also lower the amount of current drawn from the power supplies. Please note that the HI7191 specifications are written for a 10MHz clock only.

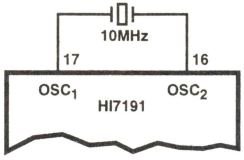


FIGURE 11A.

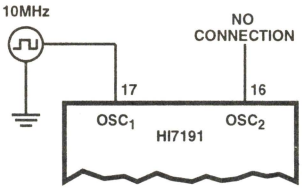


FIGURE 11B.

FIGURE 11. OSCILLATOR CONFIGURATIONS

Operational Modes

The HI7191 contains several operational modes including calibration modes for cancelling offset and gain errors of both internal and external circuitry. A calibration routine should be initiated whenever there is a change in the ambient operating temperature or supply voltage. Calibration should also be initiated if there is a change in the gain, filter notch, bipolar, or unipolar input range. Non-calibrated data can be obtained from the device by writing 000000 to the Offset Calibration Register, 800000 (h) to the Positive Full Scale Calibration Register, and 800000 (h) to the Negative Full Scale Calibration Register. This sets the offset correction factor to 0 and both the positive and negative gain slope factors to 1.

The HI7191 offers several different modes of Self-Calibration and System Calibration. For calibration to occur, the on-chip microcontroller must convert the modulator output for three different input conditions - "zero scale," "positive full scale," and "negative full scale". With these readings, the HI7191 can null any offset errors and calculate the gain slope factor for the transfer function of the converter. It is imperative that the zero-scale calibration be performed before either of the gain calibrations. However, the order of the gain calibrations is not important.

The calibration modes are user selectable in the Control Register by using the MD bits (MD2-MD0) as shown in Table 6. $\overline{DRDY}$ will go low indicating that the calibration is complete and there is valid data at the output.

TABLE 6. HI7191 OPERATIONAL MODES

MD2	MD1	MD0	OPERATIONAL MODE
0	0	0	Conversion
0	0	1	Self Calibration
0	1	0	System Offset Calibration
0	1	1	System Positive Full Scale Calibration
1	0	0	System Negative Full Scale Calibration
1	0	1	System Offset/Internal Gain Calibration
1	1	0	System Gain Calibration
1	1	1	Reserved

Conversion Mode

For Conversion Mode operation the HI7191 converts the differential voltage between V_{INHI} and V_{INLO}. From switching into this mode it takes 3 conversion periods ($3 \times 1/f_N$) for $\overline{DRDY}$ to go low and new data to be valid. No calibration coefficients are generated when operating in Conversion Mode as data is calibrated using the existing calibration coefficients.

Self Calibration Mode

The Self Calibration Mode is a three step process that updates the Offset Calibration Register, the Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. In this mode an internal offset calibration is done by disconnecting the external inputs and shorting the inputs of the PGIA together. After 3 conversion periods the Offset Calibration Register is updated with the value that corrects any internal offset errors.

After the offset calibration is completed the Positive and Negative Full Scale Calibration Registers are updated. The inputs V_{INHI} and V_{INLO} are disconnected and the external reference is applied across the modulator inputs. The HI7191 then takes 3 conversion cycles to sample the data and update the Positive Full Scale Calibration Register. Next the polarity of the reference voltage across the modulator input terminals is reversed and after 3 conversion cycles the Negative Full Calibration Register is updated. The values stored in the Positive and Negative Full Scale Calibration Registers correct for any internal gain errors in the A/D transfer function. After 3 more conversion cycles the $\overline{DRDY}$ line will activate signaling that the calibration is complete and valid data is present in the Data Output Register.

Please note, self calibration is only valid when operating in a gain of one. In addition, the offset and gain errors are not reduced as with the full system calibration.

System Offset Calibration Mode

The System Offset Calibration Mode is a single step process that allows the user to lump offset errors of external circuitry and the internal errors of the HI7191 together and null them out. This mode will convert the external differential signal applied to the VIN inputs and then store that value in the Offset Calibration Register. *The user must apply the zero point or offset voltage to the HI7191 analog inputs and allow the signal to settle before selecting this mode.* After 4 conversion periods the $\overline{DRDY}$ line will activate signaling that the calibration is complete and valid data is present in the Data Output Register.

System Positive Full Scale Calibration Mode

The System Positive Full Scale Calibration Mode is a single step process that allows the user to lump gain errors of external circuitry and the internal errors of the HI7191 together and null them out. This mode will convert the external differential signal applied to the V_{IN} inputs and stores the converted value in the Positive Full Scale Calibration Register. *The user must apply the +Full Scale voltage to the HI7191 analog inputs and allow the signal to settle* ***before*** *selecting this mode.* After 4 conversion periods the $\overline{DRDY}$ line will activate signaling the calibration is complete and valid data is present in the Data Output Register.

System Negative Full Scale Calibration Mode

The System Negative Full Scale Calibration Mode is a single step process that allows the user to lump gain errors of external circuitry and the internal errors of the HI7191 together and null them out. This mode will convert the external differential signal applied to the V_{IN} inputs and stores the converted value in the Negative Full Scale Calibration Register. *The user must apply the -Full Scale voltage to the HI7191 analog inputs and allow the signal to settle* ***before*** *selecting this mode.* After 4 conversion periods the $\overline{DRDY}$ line will activate signaling the calibration is complete and valid data is present in the Data Output Register.

System Offset/Internal Gain Calibration Mode

The System Offset/Internal Gain Calibration Mode is a single step process that updates the Offset Calibration Register, the Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. First the external differential signal applied to the VIN inputs is converted and that value is stored in the Offset Calibration Register. *The user must apply the zero point or offset voltage to the HI7191 analog inputs and allow the signal to settle* ***before*** *selecting this mode.*

After this is completed the Positive and Negative Full Scale Calibration Registers are updated. The inputs V_{INHI} and V_{INLO} are disconnected and the external reference is switched in. The HI7191 then takes 3 conversion cycles to sample the data and update the Positive Full Scale Calibration Register. Next the polarity of the reference voltage across the V_{INHI} and V_{INLO} terminals is reversed and after 3 conversion cycles the Negative Full Calibration Register is updated. The values stored in the Positive and Negative Full Scale Calibration Registers correct for any internal gain errors in the A/D transfer function. After 3 more conversion cycles, the $\overline{DRDY}$ line will activate signaling that the calibration is complete and valid data is present in the Data Output Register.

System Gain Calibration Mode

The Gain Calibration Mode is a single step process that updates the Positive and Negative Full Scale Calibration Registers. This mode will convert the external differential signal applied to the V_{IN} inputs and then store that value in the Negative Full Scale Calibration Register. Then the polarity of the input is reversed internally and another conversion is performed. This conversion result is written to the Positive Full Scale Calibration Register. The user must apply the +Full Scale voltage to the HI7191 analog inputs and allow the signal to settle before selecting this mode. After 1 more conversion period the $\overline{DRDY}$ line will activate signaling the calibration is complete and valid data is present in the data output register.

Reserved

This mode is not used in the HI7191 and should not be selected. There is no internal detection logic to keep this condition from being selected and care should be taken not to assert this bit combination.

Offset and Span Limits

There are limits to the amount of offset and gain which can be adjusted out for the HI7191. For both bipolar and unipolar modes the minimum and maximum input spans are 0.2 x V_{REF}/GAIN and 1.2 x V_{REF}/GAIN respectively.

In the unipolar mode the offset plus the span cannot exceed the 1.2 x V_{REF}/GAIN limit. So, if the span is at its minimum value of 0.2 x V_{REF}/GAIN, the offset must be less than 1 x V_{REF}/GAIN. In bipolar mode the span is equidistant around the voltage used for the zero scale point. For this mode the offset plus half the span cannot exceed 1.2 x V_{REF}/GAIN. If the span is at ±0.2 x V_{REF}/GAIN, then the offset can not be greater than ±2 x V_{REF}/GAIN.

Serial Interface

The HI7191 has a flexible, synchronous serial communication port to allow easy interfacing to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6805/11 SPI and Intel 8051 SSR protocols. The Serial Interface is a flexible 2-wire or 3-wire hardware interface where the HI7191 can be configured to read and write on a single bidirectional line (SDIO) or configured for writing on SDIO and reading on the SDO line.

The interface is byte organized with each register byte having a specific address and single or multiple byte transfers are supported. In addition, the interface allows flexibility as to the byte and bit access order. That is, the user can specify MSB/LSB first bit positioning and can access bytes in ascending/descending order from any byte position.

The serial interface allows the user to communicate with 5 registers that control the operation of the device.

Data Output Register - a 24-bit, read-only register containing the conversion results.

Control Register - a 24-bit read/write register containing the setup and operating modes of the device.

Offset Calibration Register - a 24-bit, read/write register used for calibrating the zero point of the converter or system.

Positive Full Scale Calibration Register - a 24-bit, read/write register used for calibrating the Positive Full Scale point of the converter or system.

Negative Full Scale Calibration Register - a 24-bit, read/write register used for calibrating the Negative Full Scale point of the converter or system.

Two clock modes are supported. The HI7191 can accept the serial interface clock (SCLK) as an input from the system or generate the SCLK signal as an output. If the MODE pin is logic low the HI7191 is in external clocking mode and the SCLK pin is configured as an input. In this mode the user supplies the serial interface clock and all interface timing specifications are synchronous to this input. If the MODE pin is logic high the HI7191 is in self-clocking mode and the SCLK pin is configured as an output. In self-clocking mode, SCLK runs at F_{SCLK} = OSC_1/8 and stalls high at byte boundaries. SCLK does NOT have the capability to stall low in this mode. All interface timing specifications are synchronous to the SCLK output.

Normal operation in self-clocking mode is as follows (See Figure 13): $\overline{CS}$ is sampled low on falling OSC_1 edges. The first SCLK transition output is delayed 29 OSC_1 cycles from

the next rising OSC_1. SCLK transitions eight times and then stalls high for 28 OSC_1 cycles. After this stall period is completed SCLK will again transition eight times and stall high. This sequence will repeat continuously while $\overline{CS}$ is active.

The extra OSC_1 cycle required when coming out of the $\overline{CS}$ inactive state is a one clock cycle latency required to properly sample the $\overline{CS}$ input. Note that the normal stall at byte boundaries is 28 OSC_1 cycles thus giving a SCLK rising to rising edge stall period of 32 OSC_1 cycles.

The affects of $\overline{CS}$ on the I/O are different for self-clocking mode (MODE = 1) than for external mode (MODE = 0). For external clocking mode $\overline{CS}$ inactive disables the I/O state machine, effectively freezing the state of the I/O cycle. That is, an I/O cycle can be interrupted using chip select and the HI7191 will continue with that I/O cycle when re-enabled via $\overline{CS}$. SCLK can continue toggling while $\overline{CS}$ is inactive. If $\overline{CS}$ goes inactive during an I/O cycle, it is up to the user to ensure that the state of SCLK is identical when reactivating $\overline{CS}$ as to what it was when $\overline{CS}$ went inactive. For read operations in external clocking mode, the output will go three-state immediately upon deactivation of $\overline{CS}$.

For self-clocking mode (MODE = 1), the affects of CS are different. If CS transitions high (inactive) during the period when data is being transferred (any non stall time) the HI7191 will complete the data transfer to the byte boundary. That is, once SCLK begins the eight transition sequence, it will always complete the eight cycles. If CS remains inactive after the byte has been transferred it will be sampled and SCLK will remain stalled high indefinitely. If CS has returned to active low before the data byte transfer period is completed the HI7191 acts as if CS was active during the entire transfer period.

It is important to realize that the user can interrupt a data transfer on byte boundaries. That is, if the Instruction Register calls for a 3 byte transfer and $\overline{CS}$ is inactive after only one byte has been transferred, the HI7191, when reactivated, will continue with the remaining two bytes before looking for the next Instruction Register write cycle.

Note that the outputs will NOT go three-state immediately upon CS inactive for read operations in self-clocking mode. In the case of CS going inactive during a read cycle the outputs remain driving until after the last data bit is transferred. In the case of CS inactive during the clock stall time it takes 1 OSC_1 cycle plus prop delay (maximum) for the outputs to be disabled.

I/O Port Pin Descriptions

The serial I/O port is a bidirectional port which is used to read the data register and read or write the control register and calibration registers. The port contains two data lines, a synchronous clock, and a status flag. Figure 12 shows a diagram of the serial interface lines.

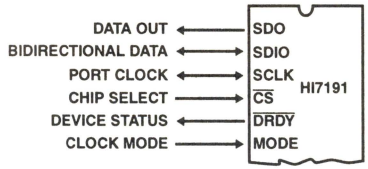


FIGURE 13. HI7191 SERIAL INTERFACE

SDO - Serial Data out. Data is read from this line using those protocols with separate lines for transmitting and receiving data. An example of such a standard is the Motorola Serial Peripheral Interface (SPI) using the 68HC05 and 68HC11 family of microcontrollers, or other similar processors. In the case of using bidirectional data transfer on SDIO, SDO does not output data and is set in a high impedance state.

SDIO - Serial Data in or out. Data is always written to the device on this line. However, this line can be used as a bidirectional data line. This is done by properly setting up the Control Register. Bidirectional data transfer on this line can be used with Intel standard serial interfaces (SSR, Mode 0) in MCS51 and MCS96 family of microcontrollers, or other similar processors.

SCLK - Serial clock. The serial clock pin is used to synchronize data to and from the HI7191 and to run the port state machines. In Synchronous External Clock Mode, SCLK is configured as an input, is supplied by the user, and can run up to a 5MHz rate. In Synchronous Self Clocking Mode, SCLK is configured as an output and runs at $OSC_1/8$.

$\overline{CS}$ - Chip select. This signal is an active low input that allows more than one device on the same serial communication lines. The SDO and SDIO will go to a high impedance state when this signal is high. If driven high during any communication cycle, that cycle will be suspended until $\overline{CS}$ reactivation. Chip select can be tied low in systems that maintain control of SCLK.

DRDY - Data Ready. This is an output status flag from the device to signal that the Data Output Register has been updated with the new conversion result. DRDY is useful as an edge or level sensitive interrupt signal to a microprocessor or microcontroller. DRDY low indicates that new data is available at the Data Output Register. DRDY will return high upon completion of a complete Data Output Register read cycle.

MODE - Mode. This input is used to select between Synchronous Self Clocking Mode ('1') or the Synchronous External Clocking Mode ('0'). When this pin is tied to VDD the serial port is configured in the Synchronous Self Clocking mode where the synchronous shift clock (SCLK) for the serial port is generated by the HI7191 and has a frequency of OSC1/8. When the pin is tied to DGND the serial port is configured for the Synchronous External Clocking Mode where

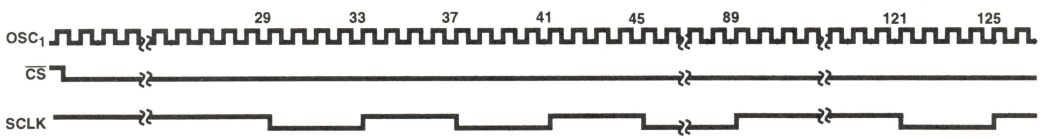


FIGURE 12. SCLK OUTPUT IN SELF CLOCKING MODE

the synchronous shift clock for the serial port is generated by an external device up to a maximum frequency of 5MHz.

Programming the Serial Interface

It is useful to think of the HI7191 interface in terms of communication cycles. Each communication cycle happens in 2 phases. The first phase of every communication cycle is the writing of an instruction byte. The second phase is the data transfer as described by the instruction byte. It is important to note that phase 2 of the communication cycle can be a single byte or a multi-byte transfer of data. For example, the 3 byte Data Output Register can be read using one multi-byte communication cycle rather than three single byte communication cycles. It is up to the user to maintain synchronism with respect to data transfers. If the system processor "gets lost" the only way to recover is to reset the HI7191. Figure 14 shows both a 2-wire and a 3-wire data transfer.

Several formats are available for reading from and writing to the HI7191 registers in both the 2-wire and 3-wire protocols. A portion of these formats is controlled by the CR<2:1> (BD and $\overline{MSB}$) bits which control the byte direction and bit order of a data transfer respectively. These two bits can be written in any combination but only the two most useful will be discussed here.

The first combination is to reset both the BD and MSB bits (BD = 0, MSB = 0). This sets up the interface for descending byte order and MSB first format. When this combination is used the user should always write the Instruction Register such that the starting byte is the most significant byte address. For example, read three bytes of DR starting with the most significant byte. The first byte read will be the most significant in MSB to LSB format. The next byte will be the next least significant (recall descending byte order) again in MSB to LSB order. The last byte will be the next lesser significant byte in MSB to LSB order. The entire word was read MSB to LSB format.

The second combination is to set both the BD and $\overline{MSB}$ bits to 1. This sets up the interface for ascending byte order and LSB first format. When this combination is used the user should always write the Instruction Register such that the starting byte is the least significant byte address. For example, read three bytes of DR starting with the least significant byte. The first byte read will be the least significant in LSB to MSB format. The next byte will be the next greater significant (recall ascending byte order) again in LSB to MSB order. The last byte will be the next greater significant byte in LSB to MSB order. *The entire word was read MSB to LSB format.*

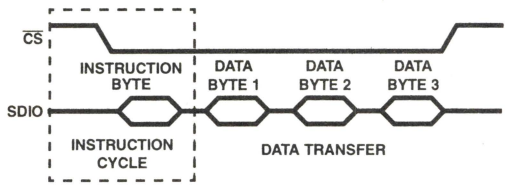


FIGURE 14A. 2-WIRE, 3 BYTE READ OR WRITE TRANSFER

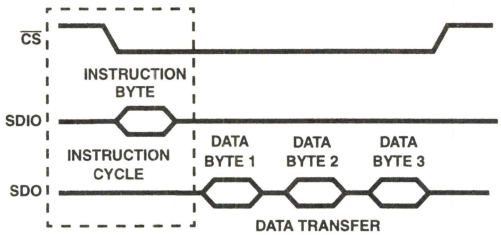


FIGURE 14B. 3-WIRE, 3 BYTE READ TRANSFER

FIGURE 14.

Instruction Byte Phase

The instruction byte phase initiates a data transfer sequence. The processor writes an 8-bit byte (Instruction Byte) to the Instruction Register. The instruction byte informs the HI7191 about the Data transfer phase activities and includes the following information:

- Read or Write cycle
- Number of Bytes to be transferred
- Which register and starting byte to be accessed

Data Transfer Phase

In the data transfer phase, data transfer takes place as set by the Instruction Register contents. See Write Operation and Read Operation sections for detailed descriptions.

Instruction Register

The Instruction Register is an 8-bit register which is used during a communications cycle for setting up read/write operations.

INSTRUCTION REGISTER

MSB	6	5	4	3	2	1	LSB
R/W	MB1	MB0	FSC	A3	A2	A1	A0

R/W - Bit 7 of the Instruction Register determines whether a read or write operation will be done following the instruction byte load. 0 = READ, 1 = WRITE.

MB1, MB0 - Bits 6 and 5 of the Instruction Register determine the number of bytes that will be accessed following the instruction byte load. See Table 7 for the number of bytes to transfer in the transfer cycle.

TABLE 7. MULTIPLE BYTE ACCESS BITS

MB1	MB0	DESCRIPTION
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

FSC - Bit 4 is used to determine whether a Positive Full Scale Calibration Register I/O transfer (FSC = 0) or a Negative Full Scale Calibration Register I/O transfer (FSC = 1) is being performed (see Table 8).

A3, A2, A1, A0 - Bits 3 and 2 (A3 and A2) of the Instruction Register determine which internal register will be accessed while bits 1 and 0 (A1 and A0) determine which byte of that register will be accessed first. See Table 8 for the address decode.

TABLE 8. INTERNAL DATA ACCESS DECODE STARTING BYTE

FSC	A3	A2	A1	A0	DESCRIPTION
X	0	0	0	0	Data Output Register Byte 0
X	0	0	0	1	Data Output Register Byte 1
X	0	0	1	0	Data Output Register Byte 2
X	0	1	0	0	Control Register Byte 0
X	0	1	0	1	Control Register Byte 1
X	0	1	1	0	Control Register Byte 2
X	1	0	0	0	Offset Cal Register Byte 0

TABLE 8. INTERNAL DATA ACCESS DECODE STARTING BYTE

FSC	A3	A2	A1	A0	DESCRIPTION
X	1	0	0	1	Offset Cal Register Byte 1
X	1	0	1	0	Offset Cal Register Byte 2
0	1	1	0	0	Positive Full Scale Cal Register Byte 0
0	1	1	0	1	Positive Full Scale Cal Register Byte 1
0	1	1	1	0	Positive Full Scale Cal Register Byte 2
1	1	1	0	0	Negative Full Scale Cal Register Byte 0
1	1	1	0	1	Negative Full Scale Cal Register Byte 1
1	1	1	1	0	Negative Full Scale Cal Register Byte 2

Write Operation

Data can be written to the Control Register, Offset Calibration Register, Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. Write operations are done using the SDIO, $\overline{CS}$ and SCLK lines only, as all data is written into the HI7191 via the SDIO line even when using the 3-wire configuration. Figures 15 and 16 show typical write timing diagrams.

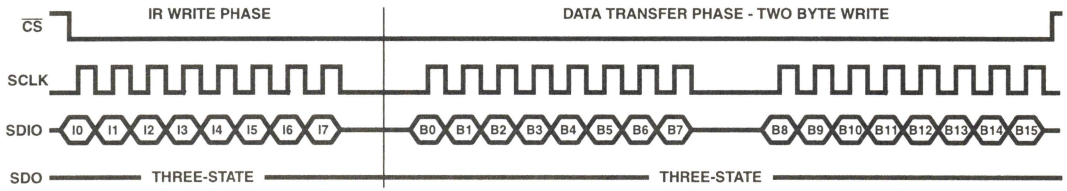


FIGURE 15. DATA WRITE CYCLE, SCLK IDLE LOW

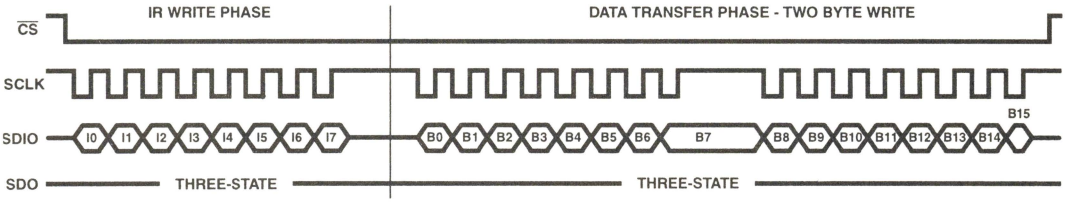


FIGURE 16. DATA WRITE CYCLE, SCLK IDLE HIGH

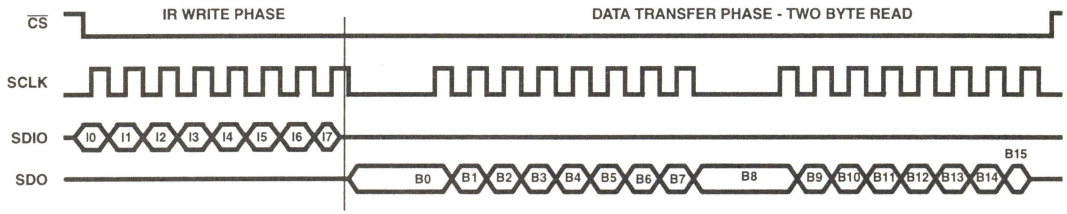


FIGURE 17. DATA READ CYCLE, 3-WIRE CONFIGURATION, SCLK IDLE LOW

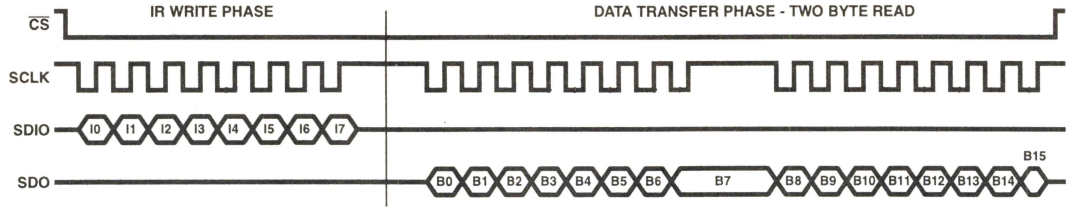


FIGURE 18. DATA READ CYCLE, 3-WIRE CONFIGURATION, SCLK IDLE HIGH

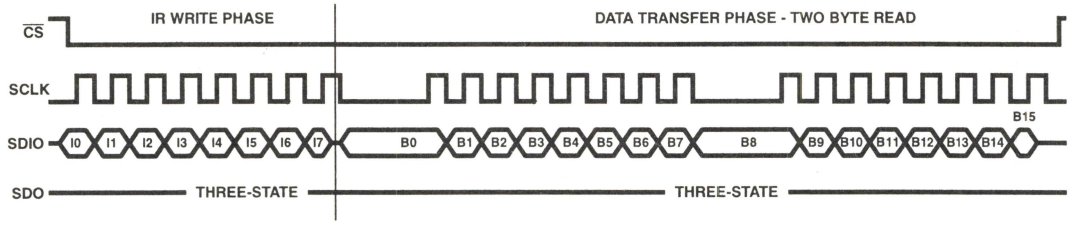


FIGURE 19. DATA READ CYCLE, 2-WIRE CONFIGURATION, SCLK IDLE LOW

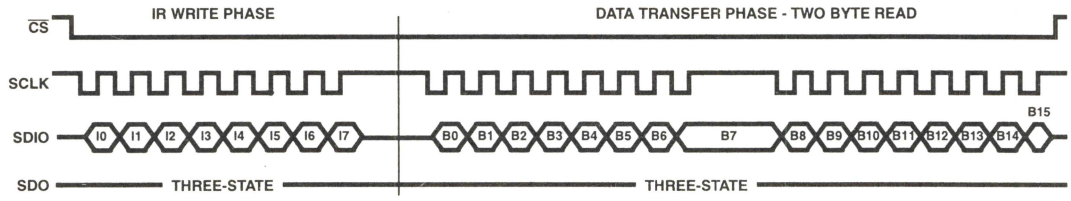


FIGURE 20. DATA READ CYCLE, 2-WIRE CONFIGURATION, SCLK IDLE HIGH

The communication cycle is started by asserting the $\overline{CS}$ line low and starting the clock from its idle state. To assert a write cycle, during the instruction phase of the communication cycle, the Instruction Byte should be set to a write transfer ($\overline{R}/W = 1$).

When writing to the serial port, data is latched into the HI7191 on the rising edge of SCLK. Data can then be changed on the falling edge of SCLK. Data can also be changed on the rising edge of SCLK due to the 0ns hold time required on the data. This is useful in pipelined applications where the data is latched on the rising edge of the clock.

Read Operation - 3-Wire Transfer

Data can be read from the Data Output Register, Control Register, Offset Calibration Register, Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. When configured in 3-wire transfer mode, read operations are done using the SDIO, SDO, $\overline{CS}$ and SCLK lines. All data is read via the SDO line. Figures 17 and 18 show typical 3-wire read timing diagrams.

The communication cycle is started by asserting the $\overline{CS}$ line and starting the clock from it's idle state. To assert a read cycle, during the instruction phase of the communication cycle, the Instruction Byte should be set to a read transfer ($\overline{R}/W = 0$).

When reading the serial port, data is driven out of the HI7191 on the falling edge of SCLK. Data can be registered externally on the next rising edge of SCLK.

Read Operation - 2-Wire Transfer

Data can be read from the Data Output Register, Control Register, Offset Calibration Register, Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. When configured in two wire transfer mode, read operations are done using the SDIO, $\overline{CS}$ and SCLK lines. All data is read via the SDIO line. Figures 19 and 20 show typical 2-wire read timing diagrams.

The communication cycle is started by asserting the CS line and starting the clock from it's idle state. To assert a read cycle, during the instruction phase of the communication cycle, the Instruction Byte should be set to a read transfer (R/W = 0).

When reading the serial port, data is driven out of the HI7191 on the falling edge of SCLK. Data can be registered externally on the next rising edge of SCLK.

Detailed Register Descriptions

Data Output Register

The Data Output Register contains 24-bits of converted data. This register is a read only register.

	BYTE 2						
MSB	**22**	**21**	**20**	**19**	**18**	**17**	**16**
D23	D22	D21	D20	D19	D18	D17	D16

BYTE 1

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8

BYTE 0

7	6	5	4	3	2	1	LSB
D7	D6	D5	D4	D3	D2	D1	D0

Control Register

The Control Register contains 24-bits to control the various sections of the HI7191. This register is a read/write register.

BYTE 2

MSB	22	21	20	19	18	17	16
DC	FP10	FP9	FP8	FP7	FP6	FP5	FP4

BYTE 1

15	14	13	12	11	10	9	8
FP3	FP2	FP1	FP0	MD2	MD1	MD0	B/U

BYTE 0

7	6	5	4	3	2	1	LSB
G2	G1	G0	BO	SB	BD	MSB	SDL

DC - Bit 23 is the Data Coding Bit used to select between two's complementary and offset binary data coding. When this bit is set (DC = 1) the data in the Data Output Register will be two's complement. When cleared (DC = 0) this data will be offset binary. When operating in the unipolar mode the output data is available in straight binary only (the DC bit is ignored). This bit is cleared after a RESET is applied to the part.

FP10 through FP0 - Bits 22 through 12 are the Filter programming bits that determine the frequency response of the digital filter. These bits determine the filter cutoff frequency, the position of the first notch and the data rate of the HI7191. The first notch of the filter is equal to the decimation rate and can be determined by the formula:

$f_{NOTCH} = f_{OSC} /(512 \times CODE)$,

where CODE is the decimal equivalent of the value in FP10 through FP0. The values that can be programmed into these bits are 10 to 2047 decimal, which allows a conversion rate range of 9.54Hz to 1.953kHz when using a 10MHz clock.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch to the filter. For example, if the first notch of the filter is selected at 50Hz then a new word is available at a 50Hz rate or every 20ms. If the first notch is at 1kHz a new word is available every 1ms.

The settling-time of the converter to a full scale step input change is between 3 and 4 times the data rate. For example, with the first filter notch at 50Hz, the worst case settling time to a full-scale step input change is 80ms. If the first notch is 1kHz, the settling time to a full-scale input step is 4ms maximum.

The -3dB frequency is determined by the programmed first notch frequency according to the relationship:

$f_{-3dB} = 0.262 \times f_{NOTCH}$.

MD2 through MD0 - Bits 11 through 9 are the Operational Modes of the converter. See Table 6 for the Operational Modes description. After a $\overline{RESET}$ is applied to the part these bits are set to the self calibration mode.

B/U - Bit 8 is the Bipolar/Unipolar select bit. When this bit is set the HI7191 is configured for bipolar operation. When this bit is reset the part is in unipolar mode. This bit is set after a $\overline{RESET}$ is applied to the part.

G2 through G0 - Bits 7 through 5 select the gain of the input analog signal. The gain is accomplished through a programmable gain instrumentation amplifier that gains up incoming signals from 1 to 8. This is achieved by using a switched capacitor voltage multiplier network preceding the modulator. The higher gains (i.e., 16 to 128) are achieved through a combination of a PGIA gain of 8 and a digital multiply after the digital filter (see Table 9). The gain will affect noise and Signal to Noise Ratio of the conversion. These bits are cleared to a gain of 1 (G2, G1, G0 = 000) after a RESET is applied to the part.

TABLE 9. GAIN SELECT BITS

G2	G1	G0	GAIN	GAIN ACHIEVED
0	0	0	1	PGIA = 1, Filter Multiply = 1
0	0	1	2	PGIA = 2, Filter Multiply = 1
0	1	0	4	PGIA = 4, Filter Multiply = 1
0	1	1	8	PGIA = 8, Filter Multiply = 1
1	0	0	16	PGIA = 8, Filter Multiply = 2
1	0	1	32	PGIA = 8, Filter Multiply = 4
1	1	0	64	PGIA = 8, Filter Multiply = 8
1	1	1	128	PGIA = 8, Filter Multiply = 16

BO - Bit 4 is the Transducer Burn-Out Current source enable bit. When this bit is set (BO = 1) the burn-out current source connected to V_{INHI} internally is enabled. This current source can be used to detect the presence of an external connection to V_{INHI}. This bit is cleared after a $\overline{RESET}$ is applied to the part.

SB - Bit 3 is the Standby Mode enable bit used to put the HI7191 in a lower power/standby mode. When this bit is set (SB = 1) the filter nodes are halted, the $\overline{DRDY}$ line is set high and the modulator clock is disabled. When this bit is cleared the HI7191 begins operation as described by the contents of the Control Register. For example, if the Control Register is programmed for Self Calibration Mode and a notch frequency to 10Hz, the HI7191 will perform the self calibration before providing the data at the 10Hz rate. This bit is cleared after a $\overline{RESET}$ is applied to the part.

BD - Bit 2 is the Byte Direction bit used to select the multi-byte access ordering. The bit determines the either ascending or descending order access for the multi-byte registers. When set (BD = 1) the user can access multi-byte registers in ascending byte order and when cleared (BD = 0) the multi-byte registers are accessed in descending byte order. This bit is cleared after a $\overline{RESET}$ is applied to the part.

$\overline{MSB}$ - Bit 1 is used to select whether a serial data transfer is MSB or LSB first. This bit allows the user to change the order that data can be transmitted or received by the HI7191. When

this bit is cleared ($\overline{MSB}$ = 0) the MSB is the first bit in a serial data transfer. If set ($\overline{MSB}$ = 1), the LSB is the first bit transferred in the serial data stream. This bit is cleared after a $\overline{RESET}$ is applied to the part.

SDL - Bit 0 is the Serial Data Line control bit. This bit selects the transfer protocol of the serial interface. When this bit is cleared (SDL = 0), both read and write data transfers are done using the SDIO line. When set (SDL = 1), write transfers are done on the SDIO line and read transfers are done on the SDO line. This bit is cleared after a $\overline{RESET}$ is applied to the part.

Reading the Data Output Register

The HI7191 generates an active low interrupt ($\overline{DRDY}$) indicating valid conversion results are available for reading. At this time the Data Output Register contains the latest conversion result available from the HI7191. Data integrity is maintained at the serial output port but it is possible to miss a conversion result if the Data Output Register is not read within a given period of time. Maintaining data integrity means that if a Data Output Register read of conversion N is begun but not finished before the next conversion (conversion N + 1) is complete, the $\overline{DRDY}$ line remains active low and the data being read is not overwritten.

In addition to the Data Output Register, the HI7191 has a one conversion result storage buffer. No conversion results will be lost if the following constraints are met.

1) A Data Output Register read cycle is started for a given conversion (conversion X) $1/f_N$ - $(128*1/f_{OSC})$ after $\overline{DRDY}$ initially goes active low. Failure to start the read cycle may result in conversion X + 1 data overwriting conversion X results. For example, with f_{OSC} = 10MHz, f_N = 2kHz, the read cycle must start within $1/2000 - 128(1/10^6) = 487\mu s$ after $\overline{DRDY}$ went low.

2) The Data Output Register read cycle for conversion X must be completed within $2(1/f_N)$-$1440(1/f_{OSC})$ after $\overline{DRDY}$ initially goes active low. If the read cycle for conversion X is not complete within this time the results of conversion X + 1 are lost and results from conversion X + 2 are now stored in the data output word buffer.

Completing the Data Output Register read cycle inactivates the $\overline{DRDY}$ interrupt. If the one word data output buffer is full when this read is complete this data will be immediately transferred to the Data Output Register and a new $\overline{DRDY}$ interrupt will be issued after the minimum $\overline{DRDY}$ pulse high time is met.

Writing the Control Register

If data is written to byte 2 and/or byte 1 of the Control Register the $\overline{DRDY}$ output is taken high and the device re-calibrates if written to a calibration mode. This action is taken because it is assumed that by writing byte 2 or byte 1 that the user either reprogrammed the filter or changed modes of the part. However, if a single data byte is written to byte 0, it is assumed that the gain has NOT been changed. It is up to the user to re-calibrate the HI7191 after the gain has been changed by this method. It is recommended that the entire Control Register be written to when changing the selected gain. This ensures that the part is re-calibrated before the $\overline{DRDY}$ signal goes low indicating valid data is available.

Offset Calibration Register

The Offset Calibration Register is a 24-bit register containing the offset correction factor. This register is indeterminate on power-up but will contain a Self Calibration correction value after a $\overline{RESET}$ has been applied.

BYTE 2

MSB	22	21	20	19	18	17	16
O23	O22	O21	O20	O19	O18	O17	O16

BYTE 1

15	14	13	12	11	10	9	8
O15	O14	O13	O12	O11	O10	O9	O8

BYTE 0

7	6	5	4	3	2	1	LSB
O7	O6	O5	O4	O3	O2	O1	O0

The Offset Calibration Register holds the value that corrects the filter output data to all 0's when the analog input is 0V.

Positive Full Scale Calibration Register

The Positive Full Scale Calibration Register is a 24-bit register containing the Positive Full Scale correction coefficient. This coefficient is used to determine the positive gain slope factor. This register is indeterminate on power-up but will contain a Self Calibration correction coefficient after a $\overline{RESET}$ has been applied.

BYTE 2

MSB	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16

BYTE 1

15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8

BYTE 0

7	6	5	4	3	2	1	LSB
P7	P6	P5	P4	P3	P2	P1	P0

Negative Full Scale Calibration Register

The Negative Full Scale Calibration Register is a 24-bit register containing the Negative Full Scale correction coefficient. This coefficient is used to determine the negative gain slope factor. This register is indeterminate on power-up but will contain a Self Calibration correction coefficient after a $\overline{RESET}$ has been applied.

BYTE 2

MSB	22	21	20	19	18	17	16
N23	N22	N21	N20	N19	N18	N17	N16

BYTE 1

15	14	13	12	11	10	9	8
N15	N14	N13	N12	N11	N10	N9	N8

BYTE 0

7	6	5	4	3	2	1	LSB
N7	N6	N5	N4	N3	N2	N1	N0

Die Characteristics

DIE DIMENSIONS:

3550µm x 6340µm

SUBSTRATE POTENTIAL (Powered Up):

AV_{SS}

METALLIZATION:

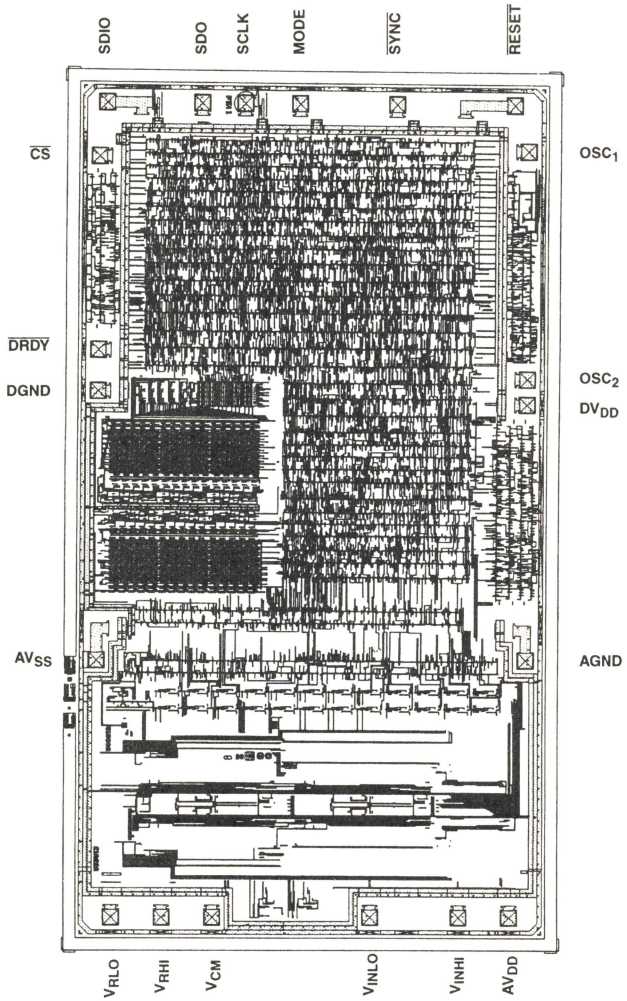
Type: Al, 1% Cu
Thickness: Metal 2, 16kÅ
Metal 1, 6kÅ

PASSIVATION:

Type: Sandwich
Thickness: Nitride 8kÅ
USG 1kÅ

Metallization Mask Layout

HI7191



DATA ACQUISITION 8

COMMUNICATION INTERFACE

		PAGE
Selection Guide		8-2
Communication Interface Data Sheets		
HIN200 thru HIN213	+5V Powered RS-232 Transmitters/Receivers with 0.1Microfarad External Capacitors	8-3
HIN202E thru HIN213E	+/-15kV, ESD-Protected, +5V Powered, RS-232 Transmitters/Receivers	8-17
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RS-232 INTERFACE FAMILY

PART NO.	POWER SUPPLY	DRIVERS	RECEIVERS	SHUTDOWN	THREE-STATE	NO. OF PINS	KBITS/s	CAPS ON LEADFRAME
HIN200	+5V	5	0	Yes	No	20-lead	120	No
HIN201	+5V/+12V	2	2	No	No	16-lead	120	No
HIN202	+5V	2	2	No	No	16-lead	120	No
HIN204	+5V	4	0	No	No	16-lead	120	No
HIN206	+5V	4	3	Yes	Yes	24-lead	120	No
HIN207	+5V	5	3	No	No	24-lead	120	No
HIN208	+5V	4	4	No	No	24-lead	120	No
HIN209	+5V/+12V	3	5	No	Yes	24-lead	120	No
HIN211	+5V	4	5	Yes	Yes	28-lead	120	No
HIN213	+5V	4	5	Yes	Yes	28-lead	120	No
HIN230	+5V	5	0	Yes	No	20-lead	120	No
HIN231	+5V/+12V	2	2	No	No	16-lead	120	No
HIN232, ICL232	+5V	2	2	No	No	16-lead	120	No
HIN234	+5V	4	0	No	No	16-lead	120	No
HIN236	+5V	4	3	Yes	Yes	24-lead	120	No
HIN237	+5V	5	3	No	No	24-lead	120	No
HIN238	+5V	4	4	No	No	24-lead	120	No
HIN239	+5V/+12V	3	5	No	Yes	24-lead	120	No
HIN241	+5V	4	5	Yes	Yes	28-lead	120	No
15kV ESD-Protected, RS-232 Serial Port								
HIN202E	+5V	2	2	No	No	16-lead	230	No
HIN203E	+5V	2	2	No	No	20-lead	230	Yes
HIN205E	+5V	5	5	Yes	Yes	24-lead	230	Yes
HIN207E	+5V	5	3	No	No	24-lead	230	No
HIN208E	+5V	4	4	No	No	24-lead	230	No
HIN211E	+5V	4	5	Yes	Yes	28-lead	230	No
HIN213E	+5V	4	5	Yes	Yes	28-lead	230	No
230K Bit/sec (.01µF) RS-232 Serial Port								
HIN232A	+5V	2	2	No	No	16-lead	230	No
Caps on Leadframe RS-232 Serial Port								
HIN203	+5V	2	2	No	No	20-lead	120	Yes
HIN205	+5V	5	5	Yes	Yes	24-lead	120	Yes
HIN233	+5V	2	2	No	No	20-lead	120	Yes
HIN235	+5V	5	5	Yes	Yes	24-lead	120	Yes

HARRIS SEMICONDUCTOR HIN200 thru HIN213

+5V Powered RS-232 Transmitters/Receivers with 0.1Microfarad External Capacitors

August 1997

Features

- Meets All RS-232E and V.28 Specifications
- HIN203 and HIN205 Require No External Capacitors
- Requires Only 0.1μF or Greater External Capacitors
- 120kbit/s Data Rate
- Two Receivers Active in Shutdown Mode (HIN213)
- Requires Only Single +5V Power Supply
  - (+5V and +12V - HIN201 and HIN209)
- Onboard Voltage Doubler/Inverter
- Low Power Consumption (Typ) 5mA
- Low Power Shutdown Function (Typ) 1μA
- Three-State TTL/CMOS Receiver Outputs
- Multiple Drivers
  - ±10V Output Swing for +5V Input
  - 300Ω Power-Off Source Impedance
  - Output Current Limiting
  - TTL/CMOS Compatible
  - 30V/μs Maximum Slew Rate
- Multiple Receivers
  - ±30V Input Voltage Range
  - 3kΩ to 7kΩ Input Impedance
  - 0.5V Hysteresis to Improve Noise Rejection

Description

The HIN200-HIN213 family of RS-232 transmitters/receivers interface circuits meet all EIA RS-232E and V.28 specifications, and are particularly suited for those applications where ±12V is not available. They require a single +5V power supply (except HIN201 and HIN209) and feature onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply. The HIN203 and HIN205 require no external capacitors and are ideally suited for applications where circuit board space is critical. The family of devices offers a wide variety of RS-232 transmitter/receiver combinations to accommodate various applications (see Selection Table).

The HIN200, HIN206, HIN211 and HIN213 feature a low power shutdown mode to conserve energy in battery powered applications. In addition, the HIN213 provides two active receivers in shutdown mode allowing for easy "wakeup" capability.

The drivers feature true TTL/CMOS input compatibility, slew rate-limited output, and 300Ω power-off source impedance. The receivers can handle up to ±30V input, and have a 3kΩ to 7kΩ input impedance. The receivers also feature hysteresis to greatly improve noise rejection.

Applications

- Any System Requiring RS-232 Communications Port
  - Computer - Portable, Mainframe, Laptop
  - Peripheral - Printers and Terminals
  - Instrumentation
  - Modems

Selection Table

PART NUMBER	POWER SUPPLY VOLTAGE	NUMBER OF RS-232 DRIVERS	NUMBER OF RS-232 RECEIVERS	NUMBER OF 0.1μF EXTERNAL CAPACITORS	LOW POWER SHUTDOWN/TTL THREE-STATE	NUMBER OF RECEIVERS ACTIVE IN SHUTDOWN
HIN200	+5V	5	0	4 Capacitors	Yes/No	0
HIN201	+5V and +9V to 13.2V	2	2	2 Capacitors	No/No	0
HIN202	+5V	2	2	4 Capacitors	No/No	0
HIN203	+5V	2	2	None	No/No	0
HIN204	+5V	4	0	4 Capacitors	No/No	0
HIN205	+5V	5	5	None	Yes/Yes	0
HIN206	+5V	4	3	4 Capacitors	Yes/Yes	0
HIN207	+5V	5	3	4 Capacitors	No/No	0
HIN208	5V	4	4	4 Capacitors	No/No	0
HIN209	+5V and +9V to 13.2V	3	5	2 Capacitors	No/Yes	0
HIN211	+5V	4	5	4 Capacitors	Yes/Yes	0
HIN213	+5V	4	5	4 Capacitors	Yes/Yes	2

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 3980.6

Ordering Information

PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN200CB	0 to 70	20 Ld SOIC	M20.3
HIN200IB	-40 to 85	20 Ld SOIC	M20.3
HIN201CB	0 to 70	16 Ld SOIC (W)	M16.3
HIN201IB	-40 to 85	16 Ld SOIC (W)	M16.3
HIN202CP	0 to 70	16 Ld PDIP	E16.3
HIN202CB	0 to 70	16 Ld SOIC (W)	M16.3
HIN202IP	-40 to 85	16 Ld PDIP	E16.3
HIN202CA	0 to 70	16 Ld SSOP	M16.209
HIN202IA	-40 to 85	16 Ld SSOP	M16.209
HIN202IB	-40 to 85	16 Ld SOIC (W)	M16.3
HIN202CBN	0 to 70	16 Ld SOIC (N)	M16.15
HIN202IBN	-40 to 85	16 Ld SOIC (N)	M16.15
HIN203CP	0 to 70	20 Ld PDIP	E20.3
HIN203CB	0 to 70	20 Ld SOIC (W)	M20.3
HIN204CB	0 to 70	16 Ld SOIC (W)	M16.3
HIN204IB	-40 to 85	16 Ld SOIC (W)	M16.3
HIN205CP	0 to 70	24 Ld PDIP (W)	E24.3
HIN206CP	0 to 70	24 Ld PDIP (N)	E24.3
HIN206CB	0 to 70	24 Ld SOIC	M24.3
HIN206CA	0 to 70	24 Ld SSOP	M24.209
HIN206IP	-40 to 85	24 Ld PDIP (N)	E24.3
HIN206IB	-40 to 85	24 Ld SOIC	M24.3
HIN206IA	-40 to 85	24 Ld SSOP	M24.209
HIN207CP	0 to 70	24 Ld PDIP (N)	E24.3

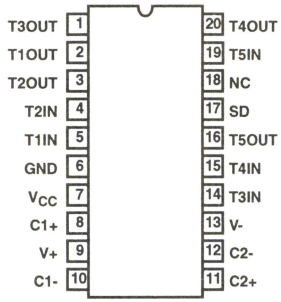
PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN207CB	0 to 70	24 Ld SOIC	M24.3
HIN207CA	0 to 70	24 Ld SSOP	M24.209
HIN207IP	-40 to 85	24 Ld PDIP (N)	E24.3
HIN207IB	-40 to 85	24 Ld SOIC	M24.3
HIN207IA	-40 to 85	24 Ld SSOP	M24.209
HIN208CP	0 to 70	24 Ld PDIP (N)	E24.3
HIN208CB	0 to 70	24 Ld SOIC	M24.3
HIN208CA	0 to 70	24 Ld SSOP	M24.209
HIN208IP	-40 to 85	24 Ld PDIP (N)	E24.3
HIN208IB	-40 to 85	24 Ld SOIC	M24.3
HIN208IA	-40 to 85	24 Ld SSOP	M24.209
HIN209CP	0 to 70	24 Ld PDIP (N)	E24.3
HIN209CB	0 to 70	24 Ld SOIC	M24.3
HIN209IP	-40 to 85	24 Ld PDIP (N)	E24.3
HIN209IB	-40 to 85	24 Ld SOIC	M24.3
HIN211CB	0 to 70	28 Ld SOIC	M28.3
HIN211CA	0 to 70	28 Ld SSOP	M28.209
HIN211IB	-40 to 85	28 Ld SOIC	M28.3
HIN211IA	-40 to 85	28 Ld SSOP	M28.209
HIN213CB	0 to 70	28 Ld SOIC	M28.3
HIN213CA	0 to 70	28 Ld SSOP	M28.209
HIN213IB	-40 to 85	28 Ld SOIC	M28.3
HIN213IA	-40 to 85	28 Ld SSOP	M28.209

Pin Descriptions

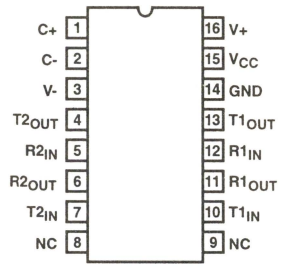
PIN	FUNCTION
V_{CC}	Power Supply Input 5V ±10%, 5V ±5% (HIN200, HIN207, HIN203, and HIN205).
V+	Internally generated positive supply (+10V nominal), HIN201 and HIN209 requires +9V to +13.2V.
V-	Internally generated negative supply (-10V nominal).
GND	Ground lead. Connect to 0V.
C1+	External capacitor (+ terminal) is connected to this lead.
C1-	External capacitor (- terminal) is connected to this lead.
C2+	External capacitor (+ terminal) is connected to this lead.
C2-	External capacitor (- terminal) is connected to this lead.
T_{IN}	Transmitter Inputs. These leads accept TTL/CMOS levels. An internal 400kΩ pull-up resistor to V_{CC} is connected to each lead.
T_{OUT}	Transmitter Outputs. These are RS-232 levels (nominally ±10V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 input levels. An internal 5kΩ pull-down resistor to GND is connected to each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$, EN	Enable input. This is an active low input which enables the receiver outputs. With $\overline{EN}$ = 5V, (HIN213 EN = 0V), the outputs are placed in a high impedance state.
SD, $\overline{SD}$	Shutdown Input. With SD = 5V (HIN213 $\overline{SD}$ = 0V), the charge pump is disabled, the receiver outputs are in a high impedance state (except R4 and R5 of HIN213) and the transmitters are shut off.
NC	No Connect. No connections are made to these leads.

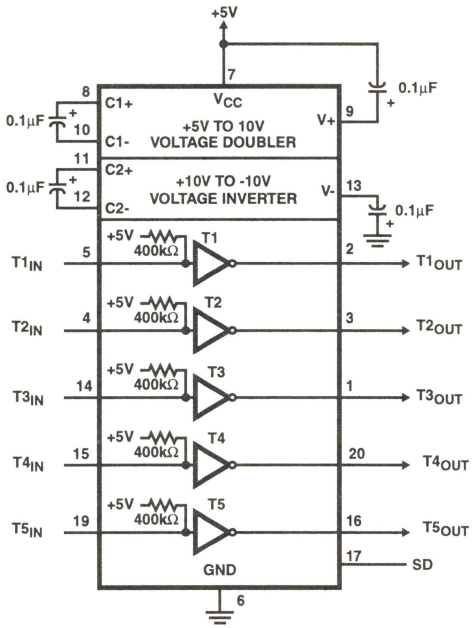
Pinouts

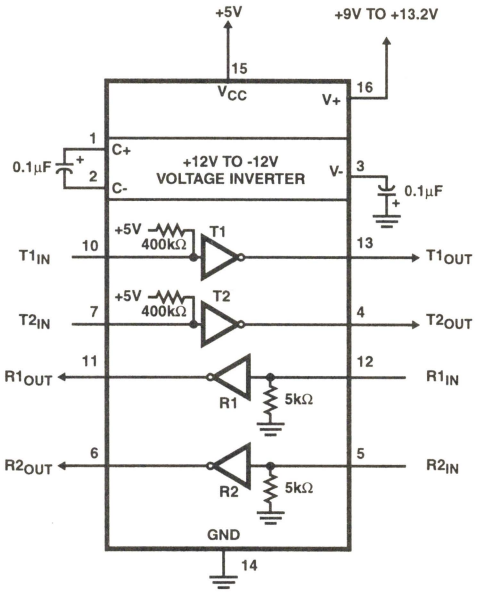
HIN200 (SOIC)
TOP VIEW



HIN201 (SOIC)
TOP VIEW

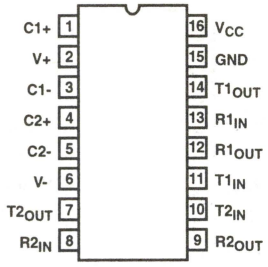




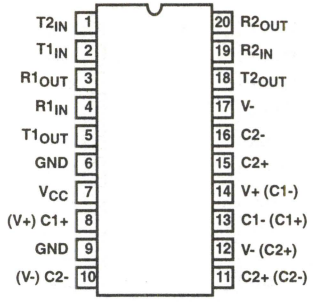


Pinouts (Continued)

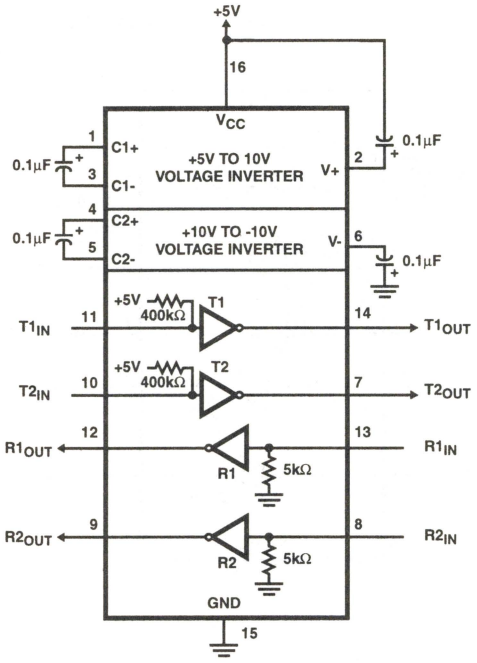
HIN202 (PDIP, SOIC, SSOP)
TOP VIEW

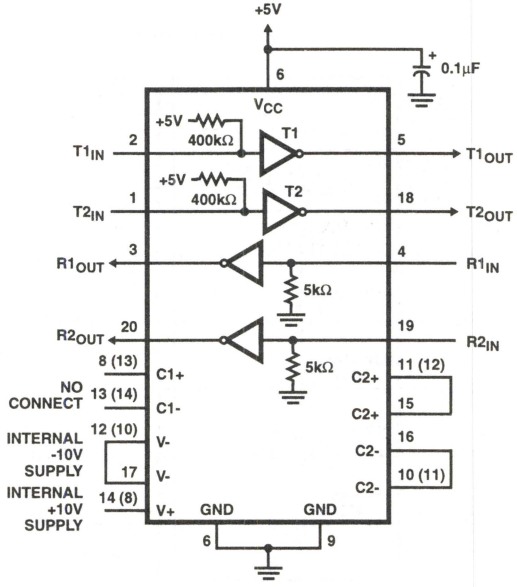


HIN203 (PDIP, SOIC)
TOP VIEW



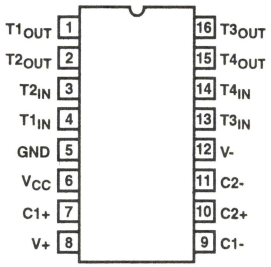
NOTE: Pin numbers in parentheses are for SOIC Package.



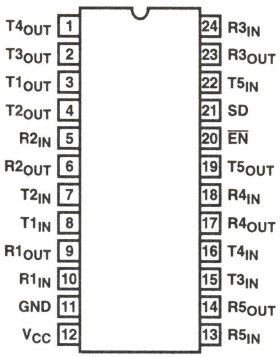


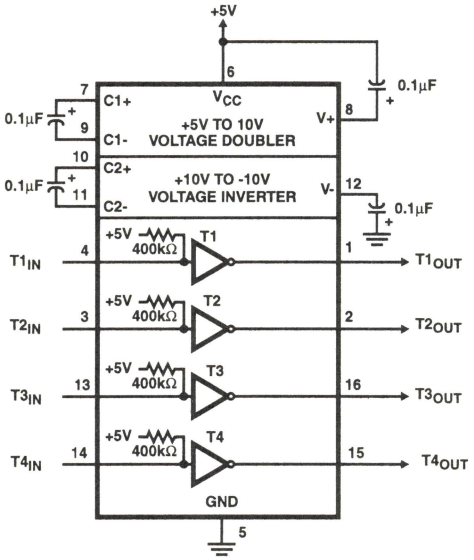
Pinouts (Continued)

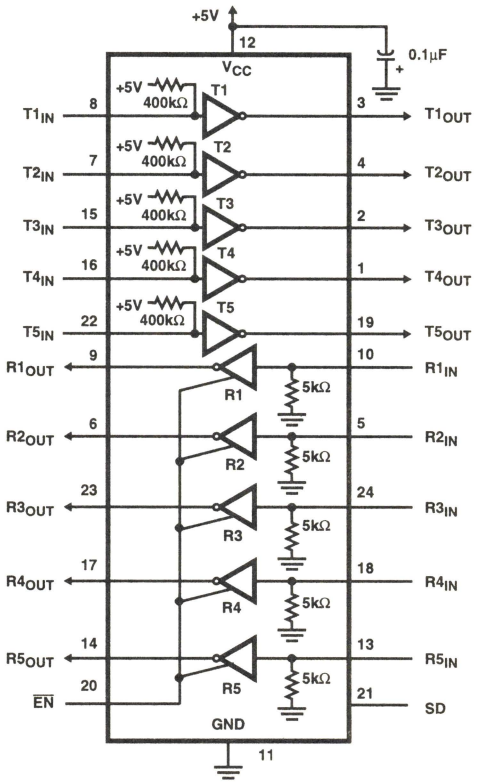
HIN204 (SOIC)
TOP VIEW



HIN205 (PDIP)
TOP VIEW

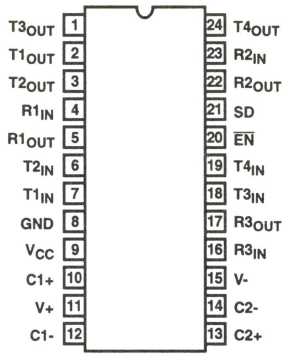




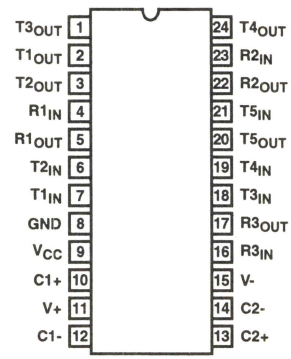


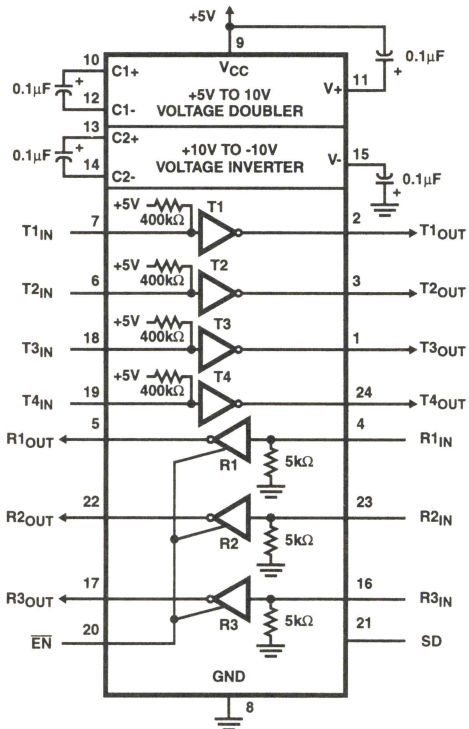
Pinouts (Continued)

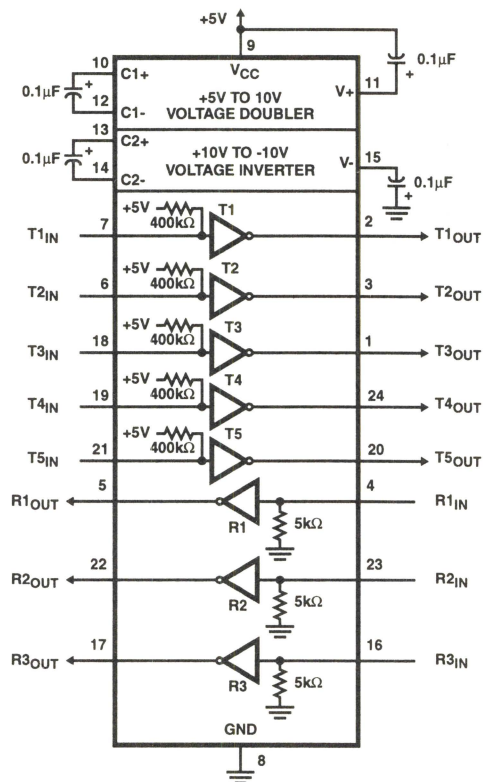
HIN206 (PDIP, SOIC, SSOP)
TOP VIEW



HIN207 (PDIP, SOIC, SSOP)
TOP VIEW

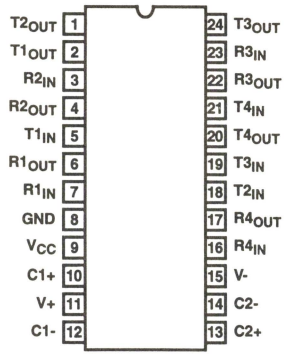




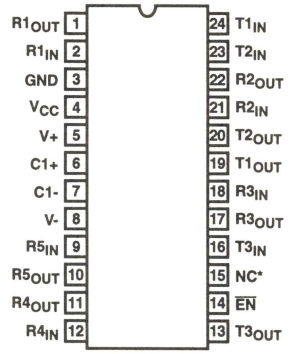


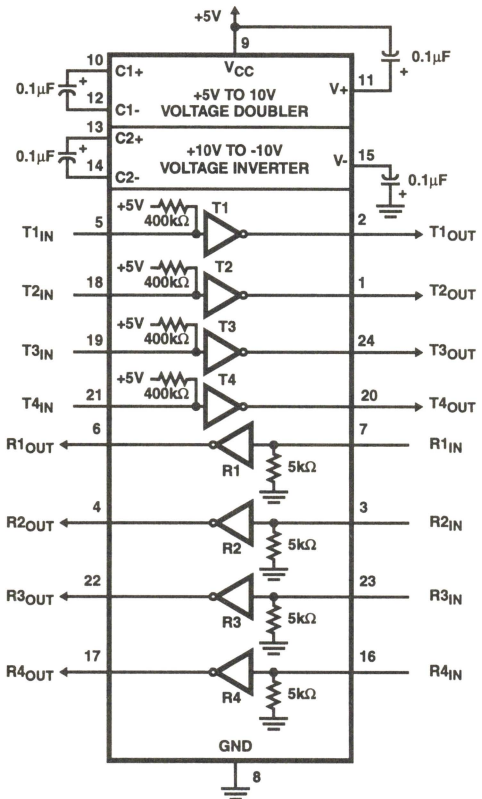
Pinouts (Continued)

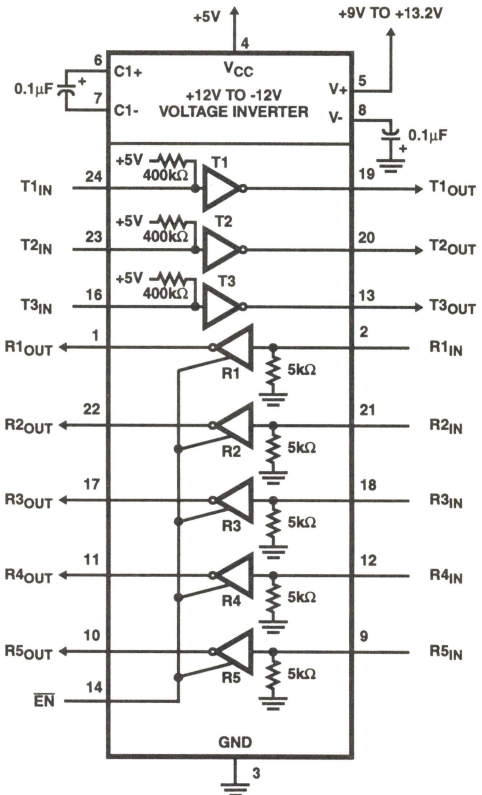
HIN208 (PDIP, SOIC, SSOP)
TOP VIEW



HIN209 (PDIP, SOIC, SSOP)
TOP VIEW

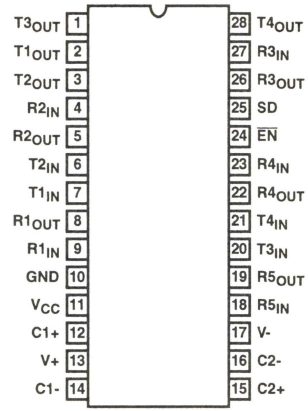




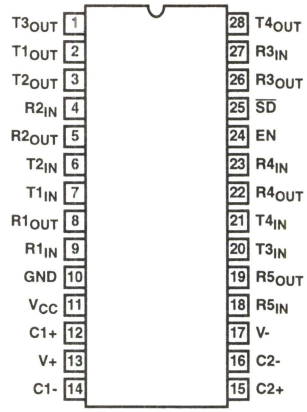


Pinouts (Continued)

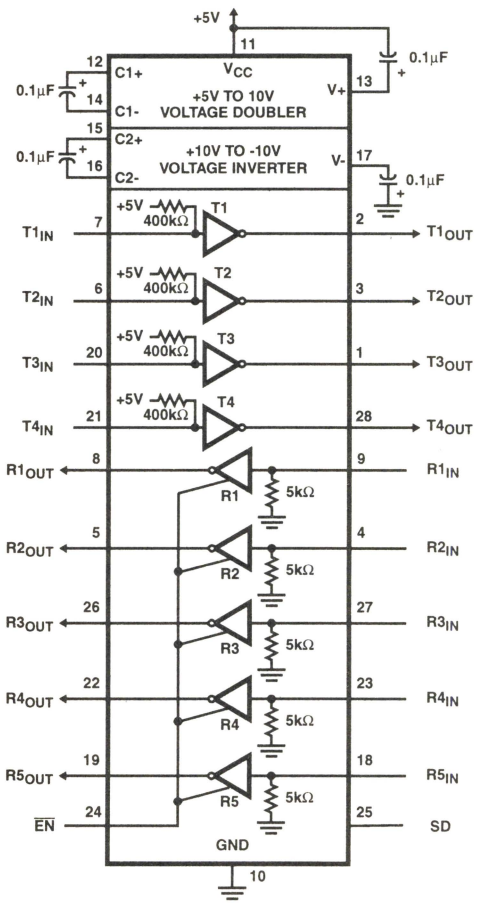
HIN211 (SOIC, SSOP)
TOP VIEW

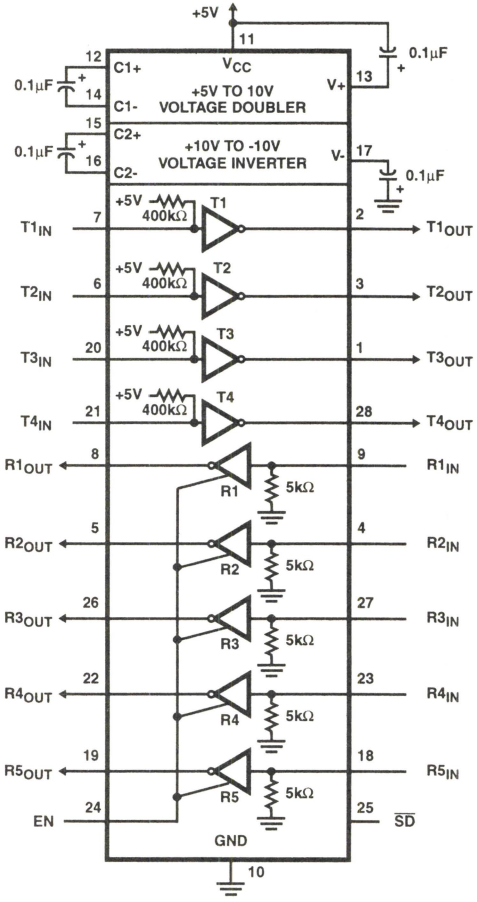


HIN213 (SOIC, SSOP)
TOP VIEW



NOTE: R4 AND R5 ACTIVE IN SHUTDOWN





Absolute Maximum Ratings

V_{CC} to Ground . . . . . (GND -0.3V) <V_{CC} < 6V
V+ to Ground . . . . . (V_{CC} -0.3V) <V+ < 12V
V- to Ground . . . . . -12V < V- < (GND +0.3V)
Input Voltages
T_{IN} . . . . . (V- -0.3V) < V_{IN} < (V+ +0.3V)
R_{IN} . . . . . ±30V
Output Voltages
T_{OUT} . . . . . (V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
R_{OUT} . . . . . (GND -0.3V) < V_{RXOUT} < (V+ +0.3V)
Short Circuit Duration
T_{OUT} . . . . . Continuous
R_{OUT} . . . . . Continuous
ESD Classification . . . . . Class 1

Operating Conditions

Temperature Range
HIN-XXXCX . . . . . 0°C to 70°C
HIN-XXXIX . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
16 Ld SOIC (N) Package	115
16 Ld SOIC (W) Package	100
16 Ld SSOP Package	155
16 Ld PDIP Package	90
20 Ld SOIC Package	100
24 Ld SOIC Package	75
24 Ld SSOP Package	135
24 Ld PDIP (N) Package	75
24 Ld PDIP (W) Package	60
28 Ld SOIC Package	70
28 Ld SSOP Package	100

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -40°C to 85°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, (V_{CC} = +5V ±5% HIN200, HIN203, HIN205, HIN207); V+ = 9V to 13.2V, HIN201 and HIN209), C1-C4 = 0.1µF; T_A = Operating Temperature Range

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing, T_{OUT}	Transmitter Outputs, 3kΩ to Ground		±5	±9	±10	V
Power Supply Current, I_{CC}	No Load, T_A = 25°C	HIN202, HIN203	-	8	15	mA
		HIN200, HIN204-208, HIN211-213	-	11	20	mA
		HIN201, HIN209	-	0.4	1	mA
V+ Power Supply Current, I_{CC}	No Load, T_A = 25°C	HIN201	-	5.0	10	mA
		HIN209	-	7.0	15	mA
Shutdown Supply Current, I_{CC}(SD)	T_A = 25°C	HIN200, HIN205, HIN206, HIN211	-	1	10	µA
		HIN213	-	15	50	µA
Input Logic Low, T_{IN}, $\overline{EN}$, V_{IL}	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$		-	-	0.8	V
Input Logic High, V_{IH}	T_{IN}		2.0	-	-	V
	$\overline{EN}$, SD, EN, $\overline{SD}$		2.4	-	-	V
Logic Pullup Current, I_P	T_{IN} = 0V		-	15	200	µA
RS-232 Input Voltage Range, V_{IN}			-30	-	+30	V
Receiver Input Impedance, R_{IN}	T_A = 25°C, V_{IN} = ±3V		3.0	5.0	7.0	kΩ
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5V, T_A = 25°C	Active Mode	0.8	1.2	-	V
		Shutdown Mode HIN213 R4 and R5	0.6	1.5	-	V

Electrical Specifications Test Conditions: V_{CC} = +5V ±10%, (V_{CC} = +5V ±5% HIN200, HIN203, HIN205, HIN207); V+ = 9V to 13.2V, HIN201 and HIN209), C1-C4 = 0.1µF; T_A = Operating Temperature Range **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5V, T_A = 25°C	Active Mode	-	1.7	2.4	V
		Shutdown Mode HIN213 R4 and R5	-	1.5	2.4	V
Receiver Input Hysteresis, V_{HYST}	V_{CC} = 5V No Hysteresis in Shutdown Mode		0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 1.6mA (HIN201-HIN203, I_{OUT} = 3.2mA)		-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	I_{OUT} = -1mA		3.5	4.6	-	V
Output Enable Time, t_{EN}	HIN205, HIN206, HIN209, HIN211, HIN213		-	400	-	ns
Output Disable Time, t_{DIS}	HIN205, HIN206, HIN209, HIN211, HIN213		-	200	-	ns
Transmit, Receive Propagation Delay, t_{PD}	HIN213 $\overline{SD}$ = 0V, R4, R5		-	0.5	40	µs
	HIN213 $\overline{SD}$ = V_{CC}, R1 - R5		-	0.5	10	µs
	HIN200 - HIN211		-	0.5	10	µs
Transmit Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V (Note 1)	HIN200, HIN204 to HIN211, HIN213	3	-	30	V/µs
		HIN201, HIN202, HIN203	3	-	30	V/µs
Output Resistance, R_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	T_{OUT} Shorted to GND		-	±10	-	mA
TTL/CMOS Receiver Output Leakage	$\overline{EN}$ = V_{CC}, EN = 0, 0V < R_{OUT} < V_{CC}		-	0.05	±10	µA

NOTE:

1. Guaranteed by design.

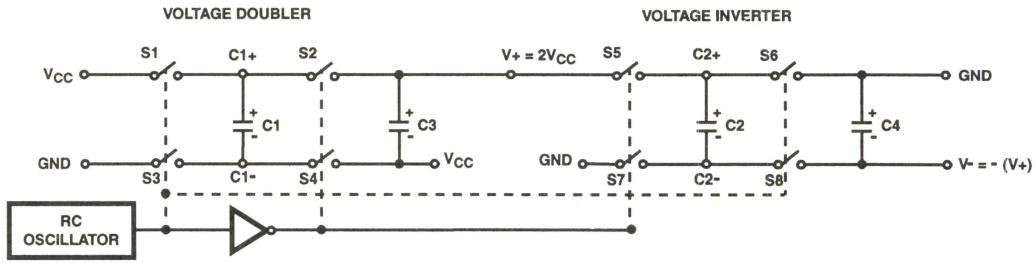


FIGURE 1. CHARGE PUMP

Detailed Description

The HIN200 thru HIN213 family of RS-232 transmitters/receivers are powered by a single +5V power supply (except HIN201 and HIN209), feature low power consumption, and meet all EIA RS232C and V.28 specifications. The circuit is divided into three sections: the charge pump, transmitter, and receiver.

Charge Pump

An equivalent circuit of the charge pump is illustrated in Figure 1. The charge pump contains two sections: the voltage doubler and the voltage inverter. Each section is driven by a two phase, internally generated clock to generate +10V and -10V. The nominal clock frequency is 125kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C3 equal to twice V_{CC}. During phase two, C2 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The charge pump accepts input voltages up to 5.5V. The output impedance of the voltage doubler section (V+) is approximately 200Ω, and the output impedance of the voltage inverter section (V-) is approximately 450Ω. A typical application uses 0.1μF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.

During shutdown mode (HIN200, HIN206 and HIN211, SD = V_{CC}, HIN213, $\overline{SD}$ = 0V) the charge pump is turned off, V+ is pulled down to V_{CC}, V- is pulled up to GND, and the supply current is reduced to less than 10μA. The transmitter outputs are disabled and the receiver outputs (except for HIN213, R4 and R5) are placed in the high impedance state.

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ -0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specifications of ±5V minimum with the worst case conditions of: all transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/μs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with ±2V applied to the outputs and V_{CC} = 0V.

Receivers

The receiver inputs accept up to ±30V while presenting the required 3kΩ to 7kΩ input impedance even if the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specifications. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis (except during shutdown) to improve noise rejection. The receiver Enable line ($\overline{EN}$, on HIN206, HIN209, and HIN211, EN on HIN213) when unasserted, disables the receiver outputs, placing them in the high impedance mode. The receiver outputs are also placed in the high impedance state when in shutdown mode (except HIN213 R4 and R5).

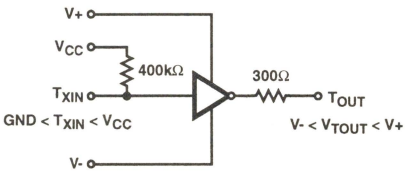


FIGURE 2. TRANSMITTER

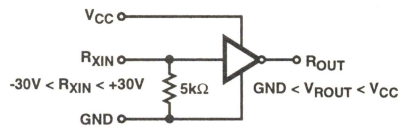
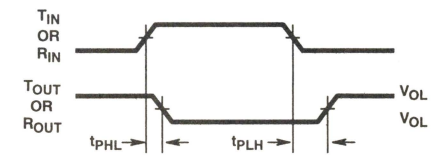


FIGURE 3. RECEIVER



$$\text{AVERAGE PROPAGATION DELAY} = \frac{t_{PHL} + t_{PLH}}{2}$$

FIGURE 4. PROPAGATION DELAY DEFINITION

HIN213 Operation in Shutdown

The HIN213 features two receivers, R4 and R5, which remain active in shutdown mode. During normal operation the receivers propagation delay is typically 0.5μs. This propagation delay may increase slightly during shutdown. When entering shut down mode, receivers R4 and R5 are not valid for 80μs after $\overline{SD}$ = V_{IL}. When exiting shutdown mode, all receiver outputs will be invalid until the charge pump circuitry reaches normal operating voltage. This is typically less than 2ms when using 0.1μF capacitors.

Typical Performance Curves

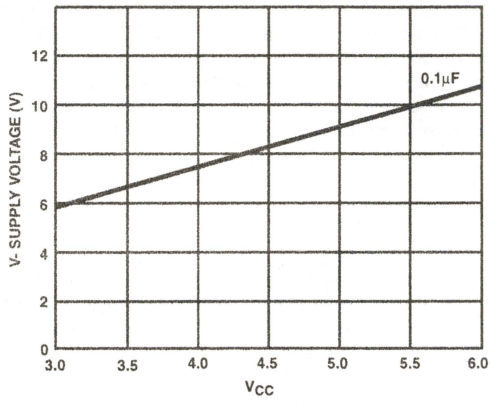


FIGURE 5. V- SUPPLY VOLTAGE vs V_{CC}

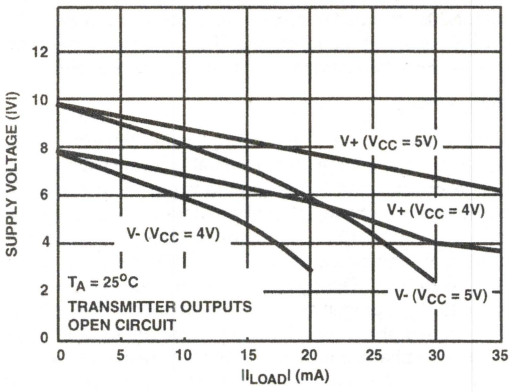


FIGURE 6. V+, V- OUTPUT VOLTAGE vs LOAD

Test Circuits (HIN202)

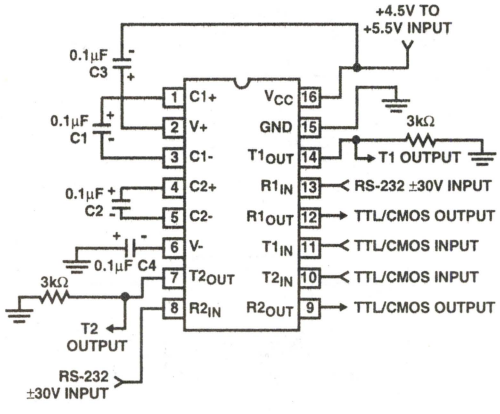


FIGURE 7. GENERAL TEST CIRCUIT

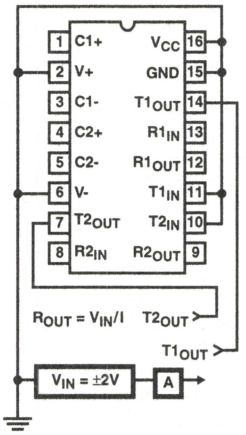


FIGURE 8. POWER-OFF SOURCE RESISTANCE CONFIGURATION

Application Information

The HINXXX may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 9. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

In applications requiring four RS-232 inputs and outputs (Figure 10), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

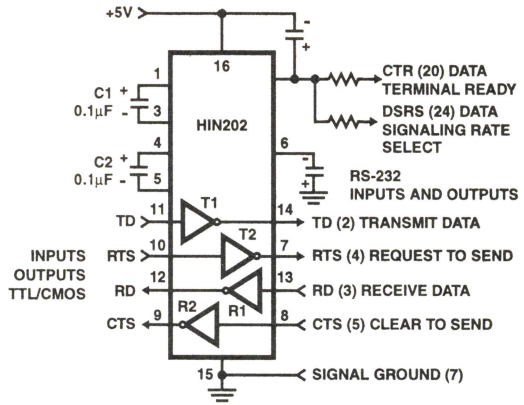


FIGURE 9. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

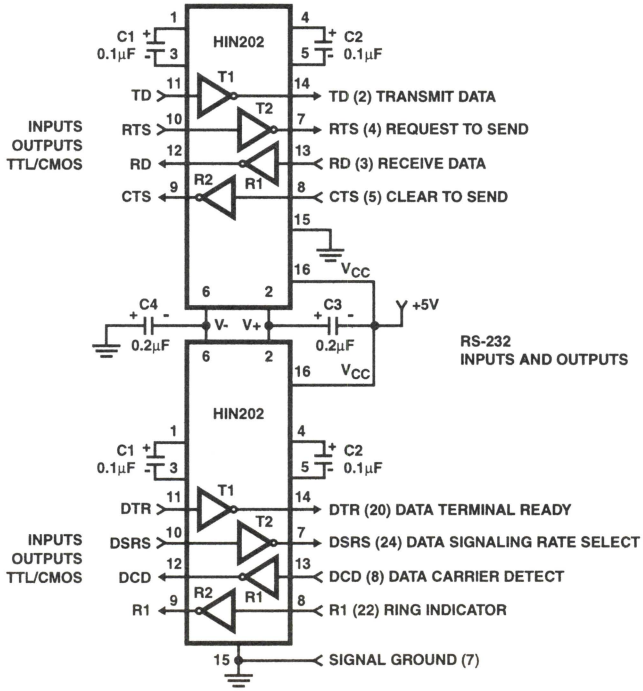


FIGURE 10. COMBINING TWO HIN202s FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

Die Characteristics

DIE DIMENSIONS:

160 mils x 140 mils

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

SUBSTRATE POTENTIAL

V+

PASSIVATION:

Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

TRANSISTOR COUNT:

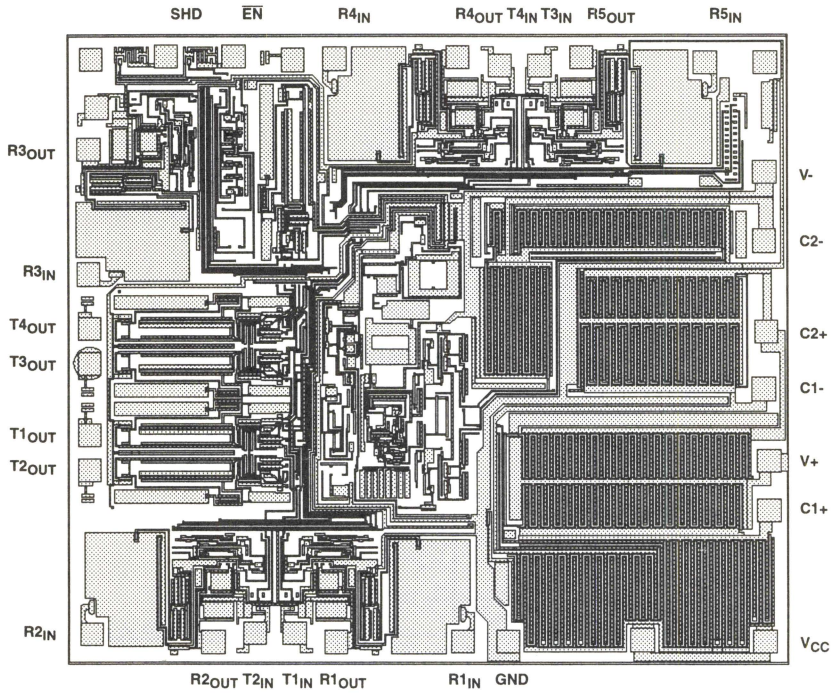
238

PROCESS:

CMOS Metal Gate

Metallization Mask Layout

HIN211



HARRIS SEMICONDUCTOR

HIN202E thru HIN213E

+/-15kV, ESD-Protected, +5V Powered, RS-232 Transmitters/Receivers

August 1997

Features

- High Speed ISDN Compatible 230kbits/s
- ESD Protection for RS-232 I/O Pins to ±15kV (IEC1000)
- Meets All RS-232E and V.28 Specifications
- HIN203E and HIN205E Require no External Capacitors
- Requires Only 0.1µF or Greater External Capacitors
- Two Receivers Active in Shutdown Mode (HIN213E)
- Requires Only Single +5V Power Supply
- Onboard Voltage Doubler/Inverter
- Low Power Consumption (202E Typ) 5mA
- Low Power Shutdown Function (Typ) 1µA
- Three-State TTL/CMOS Receiver Outputs
- Multiple Drivers
  - Output Swing for +5V Input . . . . . ±10V
  - Power-Off Source Impedance 300Ω
  - Output Current Limiting
  - TTL/CMOS Compatible
  - Maximum Slew Rate 30V/µs
- Multiple Receivers
  - Input Voltage Range . . . . . ±30V
  - Input Impedance . . . . . 3kΩ to 7kΩ
  - Hysteresis to Improve Noise Rejection 0.5V

Description

The HIN202E-HIN213E family of RS-232 transmitters/receivers interface circuits meet all EIA RS-232E and V.28 specifications, and are particularly suited for those applications where ±12V is not available. A redesigned transmitter circuit improves data rate and transmitter slew rate, which makes this suitable for ISDN and high speed modems. The transmitter outputs and the receiver inputs are protected to ±15kV ESD (Electrostatic Discharge). They require a single +5V power supply and feature onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply. The HIN203E and HIN205E require no external capacitors and are ideally suited for applications where circuit board space is critical. The family of devices offers a wide variety of RS-232 transmitter/receiver combinations to accommodate various applications (see Selection Table).

The HIN211E and HIN213E feature a low power shutdown mode to conserve energy in battery powered applications. In addition, the HIN213E provides two active receivers in shutdown mode allowing for easy "wakeup" capability.

The drivers feature true TTL/CMOS input compatibility, slew rate-limited output, and 300Ω power-off source impedance. The receivers can handle up to ±30V input, and have a 3kΩ to 7kΩ input impedance. The receivers also feature hysteresis to greatly improve noise rejection.

Applications

- Any System Requiring RS-232 Communications Port
  - Computers - Portables, Mainframes, Laptops
  - Peripherals - Printers and Terminals
  - Portable Instrumentation
  - Modems

Selection Table

PART NUMBER	POWER SUPPLY VOLTAGE	NUMBER OF RS-232 DRIVERS	NUMBER OF RS-232 RECEIVERS	NUMBER OF 0.1µF EXTERNAL COMPONENTS	LOW POWER SHUTDOWN/TTL THREE-STATE	NUMBER OF RECEIVERS ACTIVE IN SHUTDOWN
HIN202E	+5V	2	2	4 Capacitors	No/No	0
HIN203E	+5V	2	2	None	No/No	0
HIN205E	+5V	5	5	None	Yes/Yes	0
HIN206E	+5V	4	3	4 Capacitors	Yes/Yes	0
HIN207E	+5V	5	3	4 Capacitors	No/No	0
HIN208E	5V	4	4	4 Capacitors	No/No	0
HIN211E	+5V	4	5	4 Capacitors	Yes/Yes	0
HIN213E	+5V	4	5	4 Capacitors	Yes/Yes	2

8 COMMUNICATION INTERFACE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 4315

Ordering Information

PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN202ECP	0 to 70	16 Ld PDIP	E16.3
HIN202ECB	0 to 70	16 Ld SOIC	M16.3
HIN202EIP	-40 to 85	16 Ld PDIP	E16.3
HIN202ECA	0 to 70	16 Ld SSOP	M16.209
HIN202EIA	-40 to 85	16 Ld SSOP	M16.209
HIN202EIB	-40 to 85	16 Ld SOIC	M16.3
HIN202ECBN	0 to 70	16 Ld SOIC	M16.15
HIN202EIBN	-40 to 85	16 Ld SOIC	M16.15
HIN203ECP	0 to 70	20 Ld PDIP	E20.3
HIN203ECB	0 to 70	20 Ld SOIC	M20.3
HIN205ECP	0 to 70	24 Ld PDIP	E24.6
HIN206ECP	0 to 70	24 Ld PDIP	E24.3
HIN206ECB	0 to 70	24 Ld SOIC (W)	M24.3
HIN206ECA	0 to 70	24 Ld SSOP	M24.209
HIN206EIP	-40 to 85	24 Ld PDIP	E24.3
HIN206EIB	-40 to 85	24 Ld SOIC (W)	M24.3
HIN206EIA	-40 to 85	24 Ld SSOP	M24.209
HIN207ECP	0 to 70	24 Ld PDIP	E24.3
HIN207ECB	0 to 70	24 Ld SOIC	M24.3

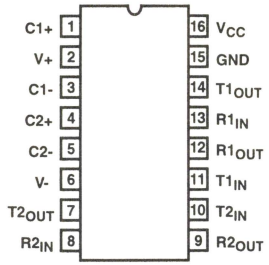
PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN207ECA	0 to 70	24 Ld SSOP	M24.209
HIN207EIP	-40 to 85	24 Ld PDIP	E24.3
HIN207EIB	-40 to 85	24 Ld SOIC	M24.3
HIN207EIA	-40 to 85	24 Ld SSOP	M24.209
HIN208ECP	0 to 70	24 Ld PDIP	E24.3
HIN208ECB	0 to 70	24 Ld SOIC	M24.3
HIN208ECA	0 to 70	24 Ld SSOP	M24.209
HIN208EIP	-40 to 85	24 Ld PDIP	E24.3
HIN208EIB	-40 to 85	24 Ld SOIC	M24.3
HIN208EIA	-40 to 85	24 Ld SSOP	M24.209
HIN211ECB	0 to 70	28 Ld SOIC	M28.3
HIN211ECA	0 to 70	28 Ld SSOP	M28.209
HIN211EIB	-40 to 85	28 Ld SOIC	M28.3
HIN211EIA	-40 to 85	28 Ld SSOP	M28.209
HIN213ECB	0 to 70	28 Ld SOIC	M28.3
HIN213ECA	0 to 70	28 Ld SSOP	M28.209
HIN213EIB	-40 to 85	28 Ld SOIC	M28.3
HIN213EIA	-40 to 85	28 Ld SSOP	M28.209

Pin Descriptions

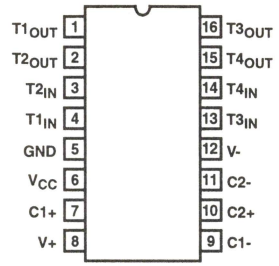
PIN	FUNCTION
V_{CC}	Power Supply Input 5V ±10%.
V+	Internally Generated Positive Supply (+10V Nominal).
V-	Internally Generated Negative Supply (-10V Nominal).
GND	Ground Lead. Connect to 0V.
C1+	External Capacitor (+ terminal) is connected to this lead.
C1-	External Capacitor (- terminal) is connected to this lead.
C2+	External Capacitor (+ terminal) is connected to this lead.
C2-	External Capacitor (- terminal) is connected to this lead.
T_{IN}	Transmitter Inputs. These leads accept TTL/CMOS levels. An internal 400kΩ pull-up resistor to V_{CC} is connected to each lead.
T_{OUT}	Transmitter Outputs. These are RS-232 levels (nominally ±10V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 input levels. An internal 5kΩ pull-down resistor to GND is connected to each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$, EN	Enable Input. This is an active low input which enables the receiver outputs. With $\overline{EN}$ = 5V, (HIN213E EN = 0V), the outputs are placed in a high impedance state.
SD, $\overline{SD}$	Shutdown Input. With SD = 5V (HIN213E $\overline{SD}$ = 0V), the charge pump is disabled, the receiver outputs are in a high impedance state (except R4 and R5 of HIN213E) and the transmitters are shut off.
NC	No Connect. No connections are made to these leads.

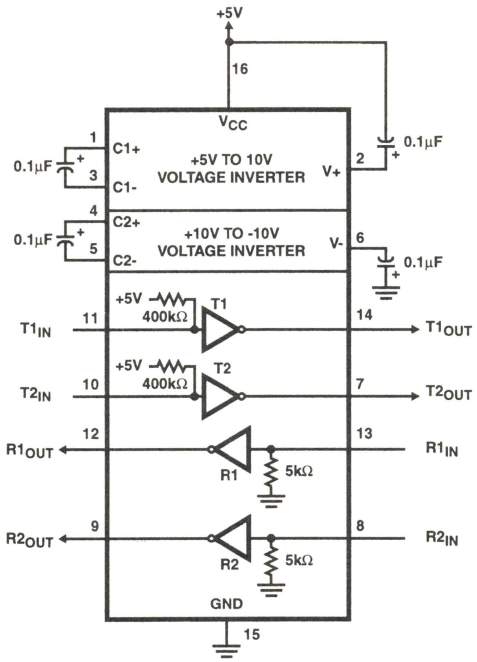
Pinouts

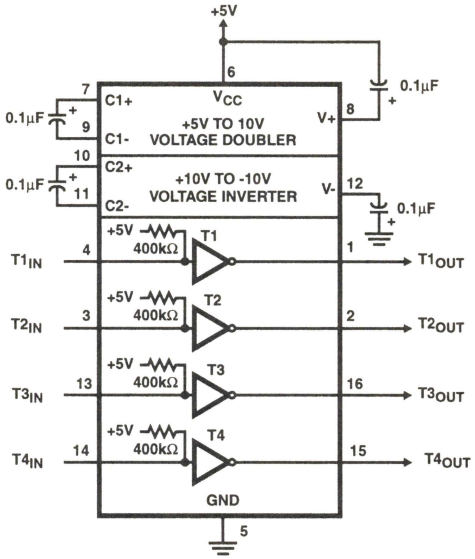
HIN202E (PDIP, SOIC, SSOP)
TOP VIEW



HIN204E (SOIC)
TOP VIEW

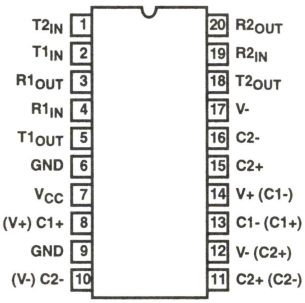




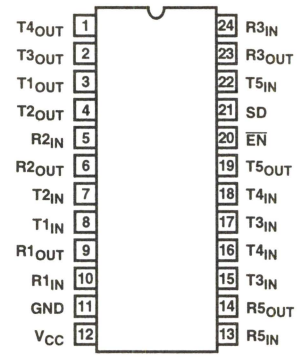


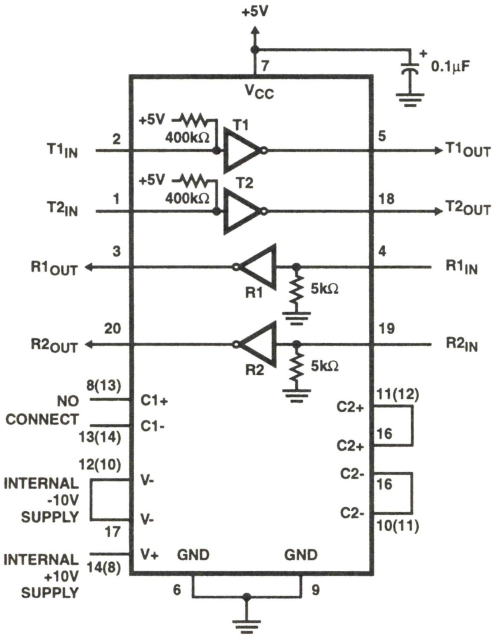
Pinouts (Continued)

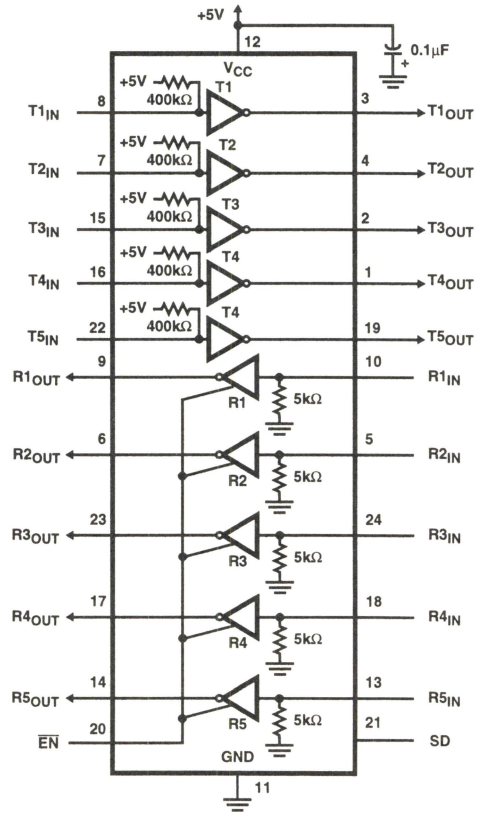
HIN203E (PDIP, SOIC)
TOP VIEW



HIN205E (PDIP, SOIC)
TOP VIEW

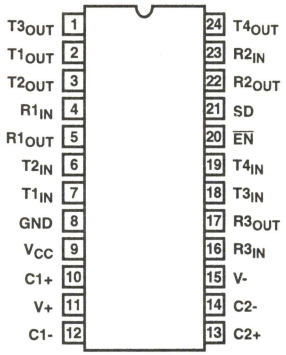




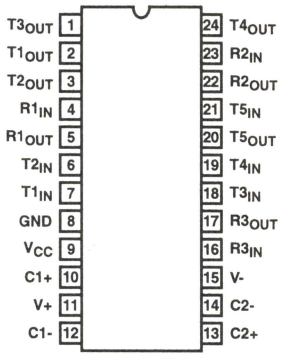


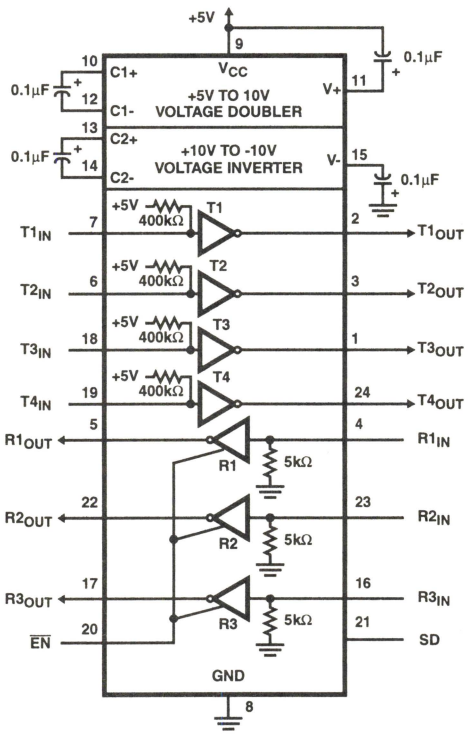
Pinouts (Continued)

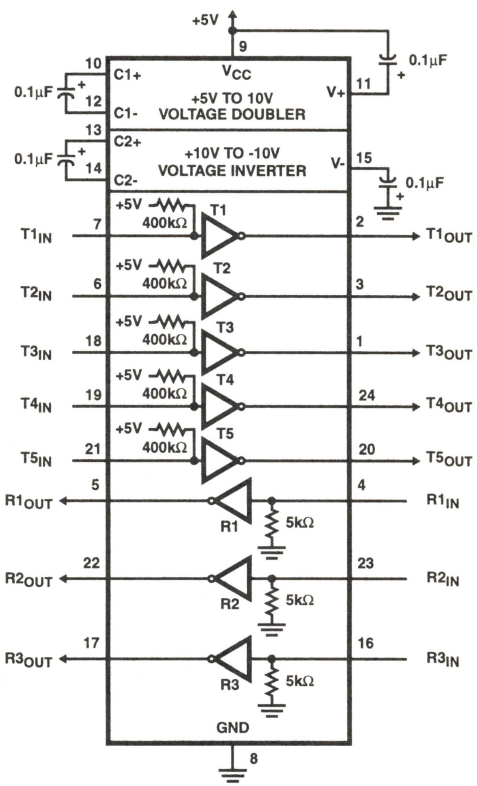
HIN206E (PDIP, SOIC, SSOP)
TOP VIEW



HIN207E (PDIP, SOIC, SSOP)
TOP VIEW

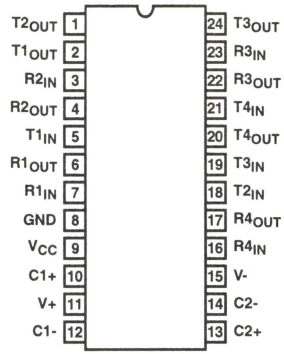




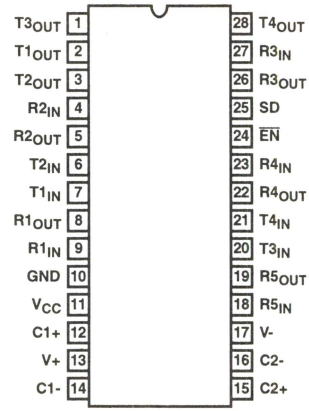


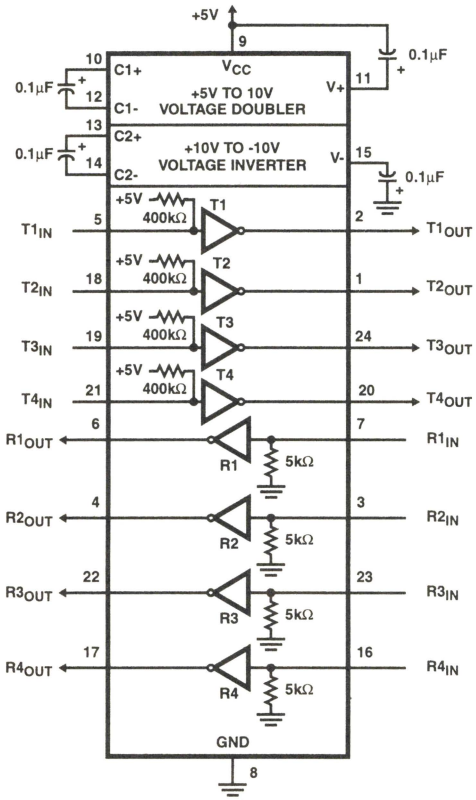
Pinouts (Continued)

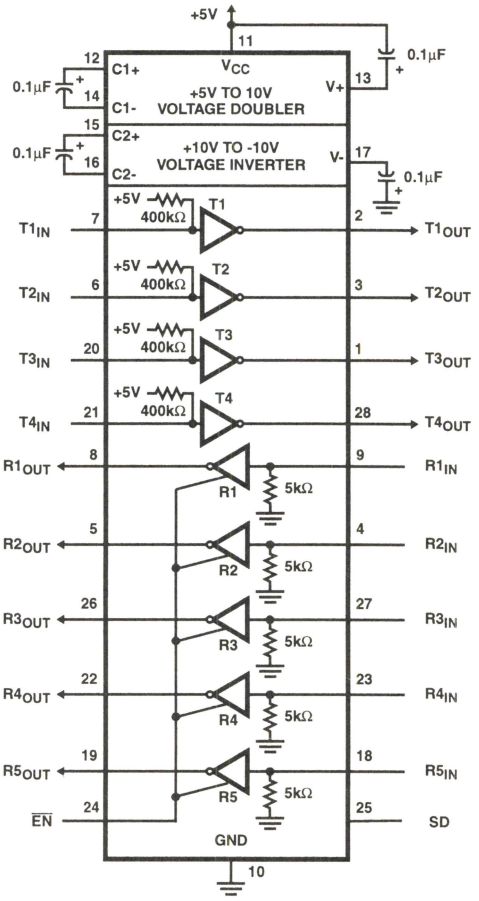
HIN208E (PDIP, SOIC, SSOP)
TOP VIEW



HIN211E (SOIC, SSOP)
TOP VIEW

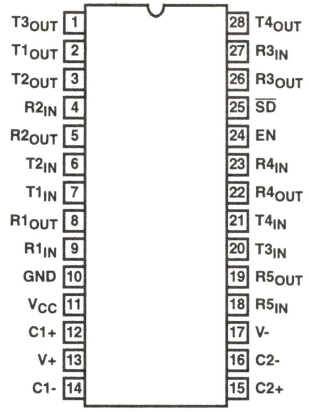




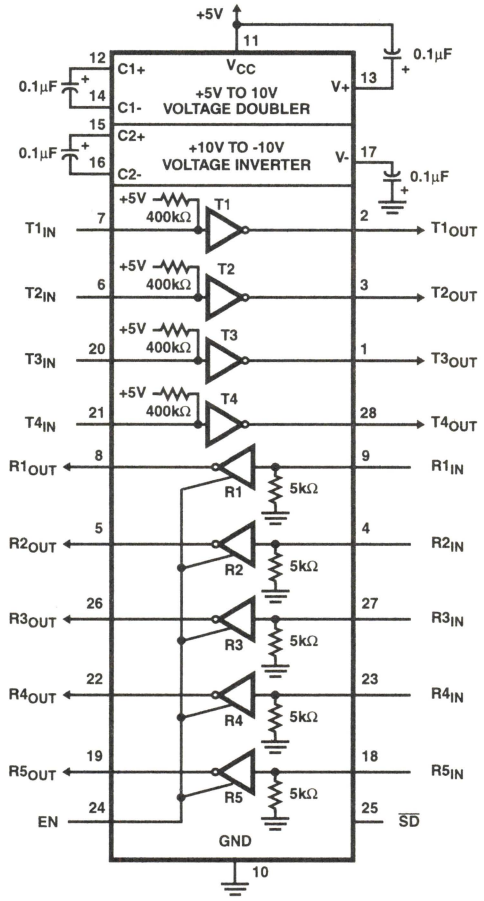


Pinouts (Continued)

HIN213E (SOIC, SSOP)
TOP VIEW



NOTE: R4 AND R5 ACTIVE IN SHUTDOWN



Absolute Maximum Ratings

V_{CC} to Ground . . . . . (GND -0.3V) <V_{CC} < 6V
V+ to Ground . . . . . (V_{CC} -0.3V) <V+ < 12V
V- to Ground . . . . . -12V < V- < (GND +0.3V)
Input Voltages
T_{IN} . . . . . (V- -0.3V) < V_{IN} < (V+ +0.3V)
R_{IN} . . . . . ±30V
Output Voltages
T_{OUT} . . . . . (V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
R_{OUT} . . . . . (GND -0.3V) < V_{RXOUT} < (V+ +0.3V)
Short Circuit Duration
T_{OUT} . . . . . Continuous
R_{OUT} . . . . . Continuous
ESD Classification . . . . . IEC1000 Compliant

Operating Conditions

Maximum Operating Temperature Range
HIN2XXECX . . . . . .0°C to 70°C
HIN2XXEIX . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
16 Ld PDIP Package	90
16 Ld SOIC (N) Package	115
16 Ld SOIC (W) Package	100
16 Ld SSOP Package	155
20 Ld PDIP Package	75
20 Ld SOIC Package	100
24 Ld PDIP (N) Package	75
24 Ld PDIP Package	60
24 Ld SOIC Package	75
24 Ld SSOP Package	135
28 Ld SOIC Package	70
28 Ld SSOP Package	100

Maximum Storage Temperature Range . . . . . -40°C to 85°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, (V_{CC} = +5V ±5% for HIN203E/205E/207E), C1-C4 = 0.1µF (except HIN203E and HIN205E), T_A = Operating Temperature Range

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing, T_{OUT}	Transmitter Outputs, 3kΩ to Ground		±5	±9	±10	V
Power Supply Current, I_{CC}	No Load, T_A = 25°C	HIN202E	-	8	15	mA
		HIN202E-208E, HIN211E-213E	-	11	20	mA
Shutdown Supply Current, I_{CC}(SD)	T_A = 25°C	HIN205E, HIN206E, HIN211E	-	1	10	µA
		HIN213E	-	15	50	µA
Input Logic Low, T_{IN}, $\overline{EN}$, V_{IL}	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$		-	-	0.8	V
Input Logic High, V_{IH}	T_{IN}		2.0	-	-	V
	$\overline{EN}$, SD, EN, $\overline{SD}$		2.4	-	-	V
Logic Pullup Current, I_P	T_{IN} = 0V		-	15	200	µA
RS-232 Input Voltage Range, V_{IN}			-30	-	+30	V
Receiver Input Impedance, R_{IN}	T_A = 25°C, V_{IN} = ±3V		3.0	5.0	7.0	kΩ
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5V, T_A = 25°C	Active Mode	0.8	1.2	-	V
		Shutdown Mode HIN213E R4 and R5	0.6	1.5	-	V
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5V, T_A = 25°C	Active Mode	-	1.7	2.4	V
		Shutdown Mode HIN213E R4 and R5	-	1.5	2.4	V
Receiver Input Hysteresis, V_{HYST}	V_{CC} = 5V No Hysteresis in Shutdown Mode		0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 1.6mA (HIN202E-HIN203E, I_{OUT} = 3.2mA)		-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	I_{OUT} = -1mA		3.5	4.6	-	V
Output Enable Time, t_{EN}	HIN205E, HIN206E, HIN211E, HIN213E		-	600	-	ns
Output Disable Time, t_{DIS}	HIN205E, HIN206E, HIN211E, HIN213E		-	200	-	ns

Electrical Specifications Test Conditions: V_{CC} = +5V ±10%, (V_{CC} = +5V ±5% for HIN203E/205E/207E), C1-C4 = 0.1µF (except HIN203E and HIN205E), T_A = Operating Temperature Range **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay, t_{PD}	HIN213E $\overline{SD}$ = 0V, R4, R5		-	4.0	40	µs
	HIN213E $\overline{SD}$ = V_{CC}		-	0.5	10	µs
	HIN202E - HIN211E		-	0.5	10	µs
Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V (Note 1)	HIN202E to HIN213E	6	15	30	V/µs
Output Resistance, R_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	T_{OUT} shorted to GND		-	±10	-	mA
TTL/CMOS Receiver Output Leakage	EN = V_{CC}, EN = 0, 0V < R_{OUT} < V_{CC}		-	0.5	±10	µA
ESD Performance	-	-	-	-	-	-
ESD Protection	Human Body Model		+/-15	-	-	kV
T_{IN}, R_{OUT}	IEC1000-4-2 Contact Discharge		+/-8	-	-	kV
	IEC1000-4-2 Air Gap		+/-15	-	-	kV
T_{IN}, R_{OUT}	Human Body Model		+/-2-	-	-	kV

NOTE:

1. Guaranteed by design.

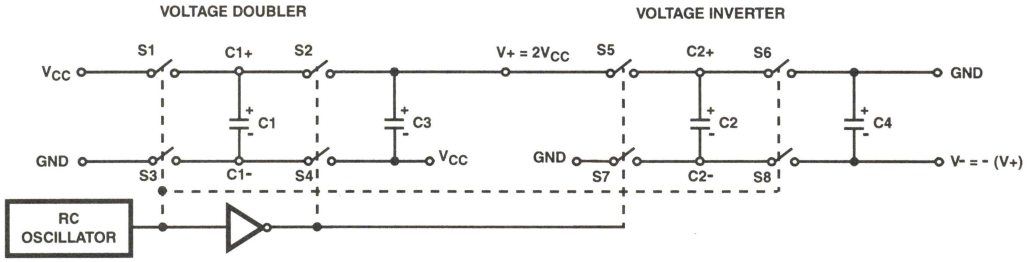


FIGURE 1. CHARGE PUMP

Detailed Description

The HIN202E thru HIN213E family of RS-232 transmitters/receivers are powered by a single +5V power supply and feature low power consumption, and meet all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: the charge pump, transmitter, and receiver.

Charge Pump

An equivalent circuit of the charge pump is illustrated in Figure 1. The charge pump contains two sections: the voltage doubler and the voltage inverter. Each section is driven by a two phase, internally generated clock to generate +10V and -10V. The nominal clock frequency is 125kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C3 equal to twice V_{CC}. During phase two, C2 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The charge pump accepts input voltages up to 5.5V. The output impedance of the voltage doubler section (V+) is approximately 200Ω, and the output impedance of the voltage inverter section (V-) is approximately 450Ω. A typical application uses 0.1µF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.

During shutdown mode (HIN205E, HIN211E and HIN213E, SD = V_{CC}, HIN213E, $\overline{SD}$ = 0V) the charge pump is turned off, V+ is pulled down to V_{CC}, V- is pulled up to GND, and the supply current is reduced to less than 10µA. The transmitter outputs are disabled and the receiver outputs (except for HIN213E, R4 and R5) are placed in the high impedance state.

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ -0.6V). Each transmitter input has an internal 400kW pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specifications of 5V minimum with the worst case conditions of: all transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/µs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with 2V applied to the outputs and V_{CC} = 0V.

Receivers

The receiver inputs accept up to 30V while presenting the required 3kΩ to 7kΩ input impedance even if the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the 3V limits known as the transition region, of the RS-232 specifications. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis (except during shutdown) to improve noise rejection. The receiver Enable line (EN, on HIN205E and HIN211E, EN on HIN213E) when unasserted, disables the receiver outputs, placing them in the high impedance mode. The receiver outputs are also placed in the high impedance state when in shutdown mode (except HIN213E R4 and R5).

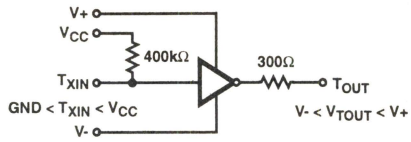


FIGURE 2. TRANSMITTER

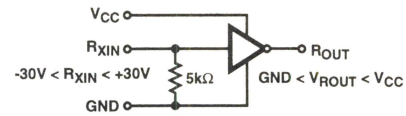


FIGURE 3. RECEIVER

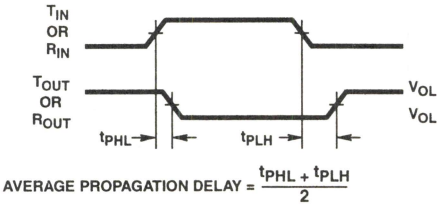


FIGURE 4. PROPAGATION DELAY DEFINITION

HIN213E Operation in Shutdown

The HIN213E features two receivers, R4 and R5, which remain active in shutdown mode. During normal operation the receivers propagation delay is typically 0.5µs. This propagation delay increases to 4µs (typical) during shutdown. When entering shut down mode, receivers R4 and R5 are not valid for 80µs after $\overline{SD}$ = V_{IL}. When exiting shutdown mode, all receiver outputs will be invalid until the charge pump circuitry reaches normal operating voltage. This is typically less than 2ms when using 0.1µF capacitors.

Test Circuits (HIN202E)

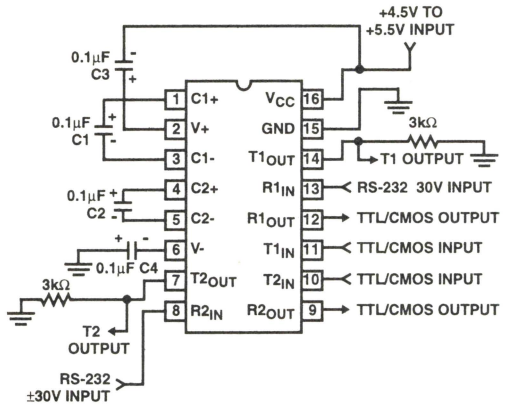


FIGURE 5. GENERAL TEST CIRCUIT

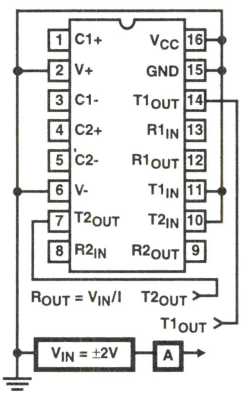


FIGURE 6. POWER-OFF SOURCE RESISTANCE CONFIGURATION

Application Information

The HIN2XXE may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where 12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 9. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

In applications requiring four RS-232 inputs and outputs (Figure 10), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

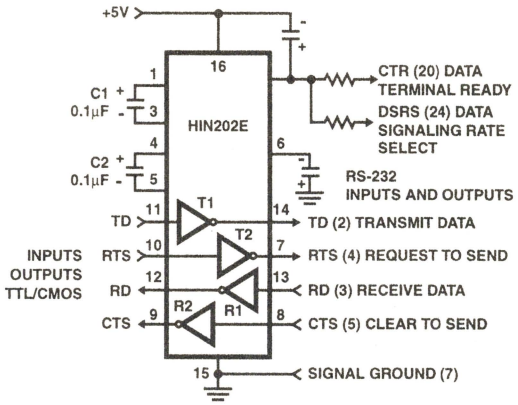


FIGURE 7. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

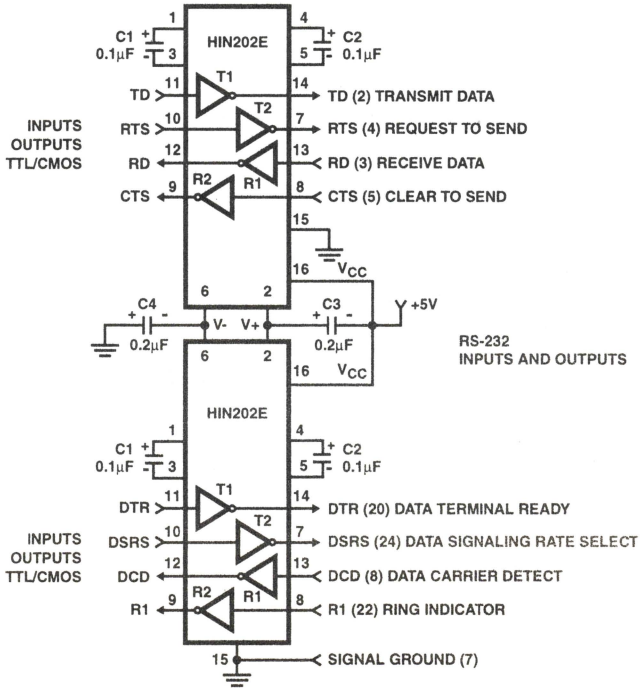


FIGURE 8. COMBINING TWO HIN202Es FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

Die Characteristics

DIE DIMENSIONS:

139 mils x 134 mils (HIN207E)

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

SUBSTRATE POTENTIAL

GND

PASSIVATION:

Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

TRANSISTOR COUNT:

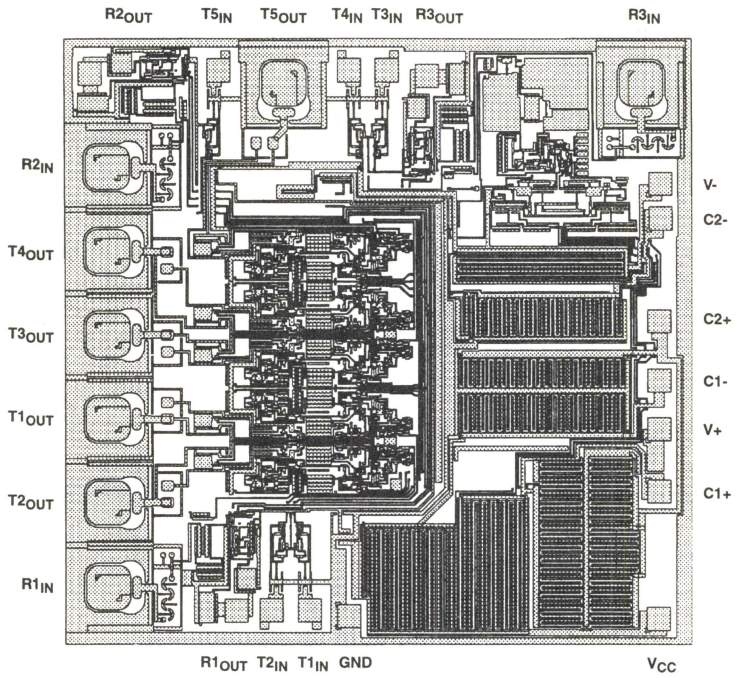
332 (HIN207E)

PROCESS:

CMOS Metal Gate

Metallization Mask Layout

HIN207E



HARRIS SEMICONDUCTOR HIN230 thru HIN241

August 1997

+5V Powered RS-232 Transmitters/Receivers

Features

- Meets All RS-232E and V.28 Specifications
- Requires Only Single +5V Power Supply
  - (+5V and +12V - HIN231 and HIN239)
- HIN233 and HIN235 Require No External Capacitors
- Onboard Voltage Doubler/Inverter
- Low Power Consumption
- Low Power Shutdown Function
- Three-State TTL/CMOS Receiver Outputs
- Multiple Drivers
  - ±10V Output Swing for +5V Input
  - 300Ω Power-Off Source Impedance
  - Output Current Limiting
  - TTL/CMOS Compatible
  - 30V/μs Maximum Slew Rate
- Multiple Receivers
  - ±30V Input Voltage Range
  - 3kΩ to 7kΩ Input Impedance
  - 0.5V Hysteresis to Improve Noise Rejection

Description

The HIN230-HIN241 family of RS-232 transmitters/receivers interface circuits meet all EIA RS-232E and V.28 specifications, and are particularly suited for those applications where ±12V is not available. They require a single +5V power supply (except HIN231 and HIN239) and features onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply. The HIN233 and HIN235 require no external capacitors and are ideally suited for applications where circuit board space is critical. The family of devices offer a wide variety of RS-232 transmitter/receiver combinations to accommodate various applications (see Selection Table).

The drivers feature true TTL/CMOS input compatibility, slew-rate-limited output, and 300Ω power-off source impedance. The receivers can handle up to ±30V, and have a 3kΩ to 7kΩ input impedance. The receivers also feature hysteresis to greatly improve noise rejection.

Applications

- Any System Requiring RS-232 Communications Port
  - Computer - Portable, Mainframe, Laptop
  - Peripheral - Printers and Terminals
  - Instrumentation
  - Modems

Selection Table

PART NUMBER	POWER SUPPLY VOLTAGE	NUMBER OF RS-232 DRIVERS	NUMBER OF RS-232 RECEIVERS	EXTERNAL COMPONENTS	LOW POWER SHUTDOWN/TTL THREE-STATE	NUMBER OF LEADS
HIN230	+5V	5	0	4 Capacitors	YES/NO	20
HIN231	+5V and +7.5V to 13.2V	2	2	2 Capacitors	NO/NO	16
HIN232	+5V	2	2	4 Capacitors	NO/NO	16
HIN233	+5V	2	2	None	NO/NO	20
HIN234	+5V	4	0	4 Capacitors	NO/NO	16
HIN235	+5V	5	5	None	YES/YES	24
HIN236	+5V	4	3	4 Capacitors	YES/YES	24
HIN237	+5V	5	3	4 Capacitors	NO/NO	24
HIN238	+5V	4	4	4 Capacitors	NO/NO	24
HIN239	+5V and +7.5V to 13.2V	3	5	2 Capacitors	NO/YES	24
HIN240	+5V	5	5	4 Capacitors	YES/YES	44
HIN241	+5V	4	5	4 Capacitors	YES/YES	28

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 3138.4

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN230CB	0 to 70	20 Ld SOIC	M20.3
HIN230IB	-40 to 85	20 Ld SOIC	M20.3
HIN230BY		Die	
HIN231CB	0 to 70	16 Ld SOIC	M16.3
HIN231IB	-40 to 85	16 Ld SOIC	M16.3
HIN231BY		Die	
HIN232CP	0 to 70	16 Ld PDIP	E16.3
HIN232CB	0 to 70	16 Ld SOIC	M16.3
HIN232IP	-40 to 85	16 Ld PDIP	E16.3
HIN232IJ	-40 to 85	16 Ld CERDIP	F16.3
HIN232IB	-40 to 85	16 Ld SOIC	M16.3
HIN232MJ	-55 to 125	16 Ld CERDIP	F16.3
HIN232BY		Die	
HIN233CP	0 to 70	20 Ld PDIP	E20.3
HIN233CB	0 to 70	20 Ld SOIC	M20.3
HIN234CB	0 to 70	16 Ld SOIC	M16.3
HIN234IB	-40 to 85	16 Ld SOIC	M16.3
HIN234BY		Die	
HIN235CP	0 to 70	24 Ld PDIP	E24.6
HIN236CP	0 to 70	24 Ld PDIP	E24.3
HIN236CB	0 to 70	24 Ld SOIC	M24.3
HIN236IP	-40 to 85	24 Ld PDIP	E24.3
HIN236IB	-40 to 85	24 Ld SOIC	M24.3

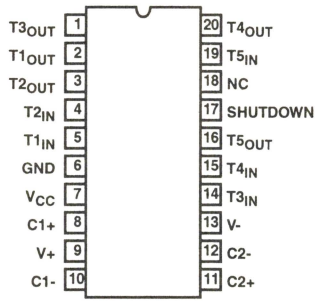
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN236BY		Die	
HIN237CP	0 to 70	24 Ld PDIP	E24.3
HIN237CB	0 to 70	24 Ld SOIC	M24.3
HIN237IP	-40 to 85	24 Ld PDIP	E24.3
HIN237IB	-40 to 85	24 Ld SOIC	M24.3
HIN237BY		Die	
HIN238CP	0 to 70	24 Ld PDIP	E24.3
HIN238CB	0 to 70	24 Ld SOIC	M24.3
HIN238IP	-40 to 85	24 Ld PDIP	E24.3
HIN238IB	-40 to 85	24 Ld SOIC	M24.3
HIN238BY		Die	
HIN239CB	0 to 70	24 Ld SOIC	M24.3
HIN239IB	-40 to 85	24 Ld SOIC	M24.3
HIN239BY		Die	
HIN240CN	0 to 70	44 Ld MQFP	Q44.10X10
HIN240IN	-40 to 85	44 Ld MQFP	Q44.10X10
HIN240BY		Die	
HIN241CB	0 to 70	28 Ld SOIC	M28.3
HIN241IB	-40 to 85	28 Ld SOIC	M28.3
HIN241CA	0 to 70	28 Ld SSOP	M28.209
HIN241IA	-40 to 85	28 Ld SSOP	M28.209
HIN241BY		Die	

Pin Descriptions

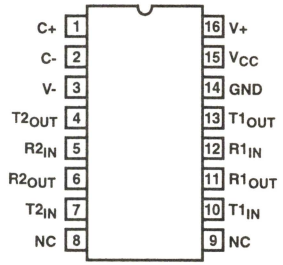
PIN	FUNCTION
V_{CC}	Power Supply Input 5V ±10%. HIN233 and HIN235 5V ±5%.
V+	Internally generated positive supply (+10V nominal), HIN231 and HIN239 requires +7.5V to +13.2V.
V-	Internally generated negative supply (-10V nominal).
GND	Ground lead. Connect to 0V.
C1+	External capacitor (+ terminal) is connected to this lead.
C1-	External capacitor (- terminal) is connected to this lead.
C2+	External capacitor (+ terminal) is connected to this lead.
C2-	External capacitor (- terminal) is connected to this lead.
T_{IN}	Transmitter Inputs. These leads accept TTL/CMOS levels. An internal 400kΩ pull-up resistor to V_{CC} is connected to each lead.
T_{OUT}	Transmitter Outputs. These are RS-232 levels (nominally ±10V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 input levels. An internal 5kΩ pull-down resistor to GND is connected to each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$	Enable input. This is an active low input which enables the receiver outputs. With $\overline{EN}$ = 5V, the outputs are placed in a high impedance state.
SD	Shutdown Input. With SD = 5V, the charge pump is disabled, the receiver outputs are in a high impedance state and the transmitters are shut off.
NC	No Connect. No connections are made to these leads.

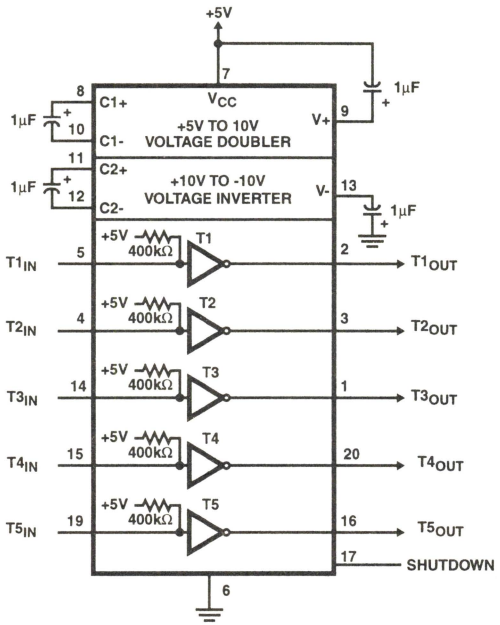
Pinouts

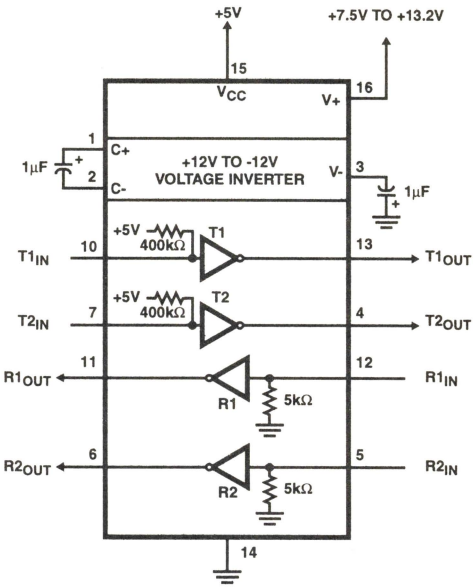
HIN230 (SOIC)
TOP VIEW



HIN231 (SOIC)
TOP VIEW

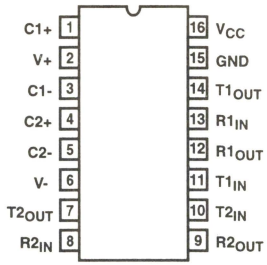




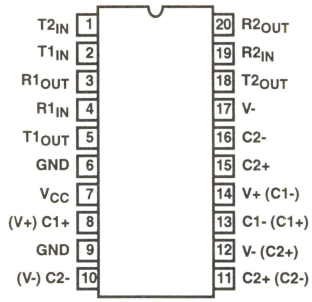


Pinouts (Continued)

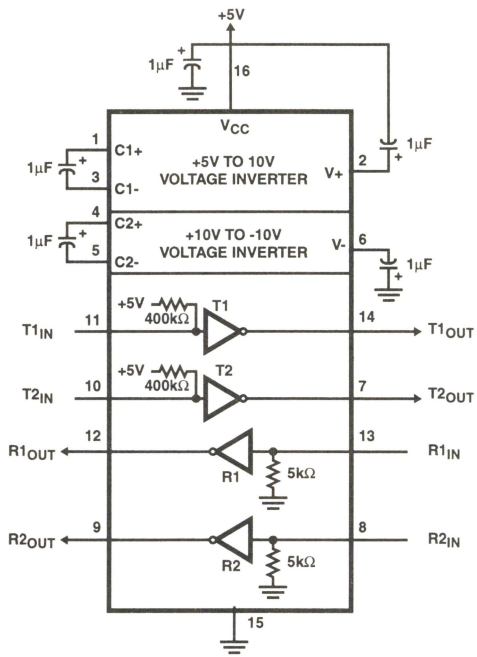
HIN232 (PDIP, CERDIP, SOIC)
TOP VIEW

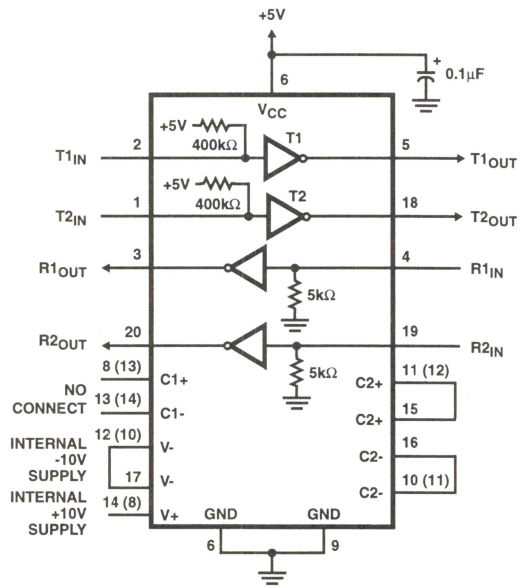


HIN233 (PDIP, SOIC)
TOP VIEW



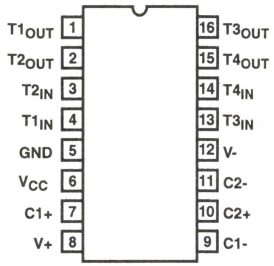
NOTE: Pin numbers in parentheses are for SOIC Package.



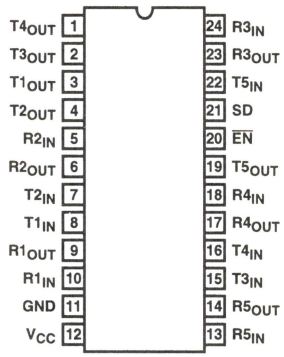


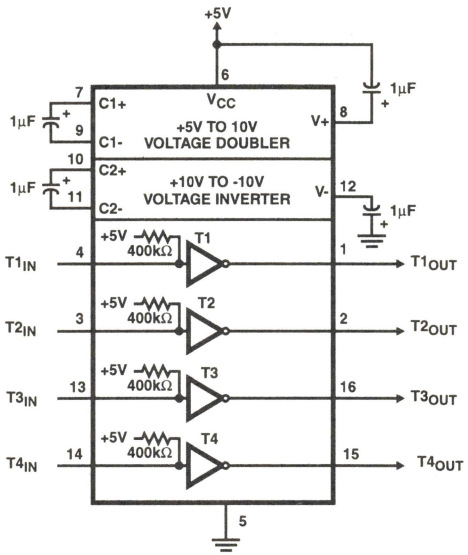
Pinouts (Continued)

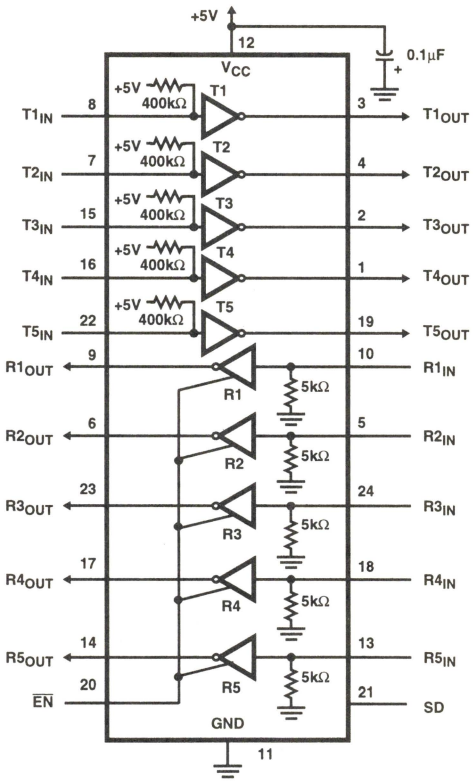
HIN234 (SOIC)
TOP VIEW



HIN235 (PDIP)
TOP VIEW

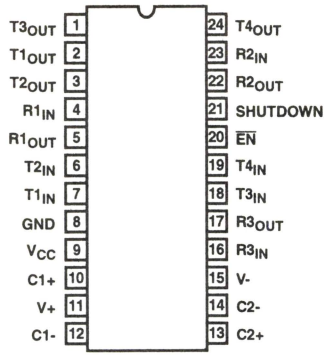




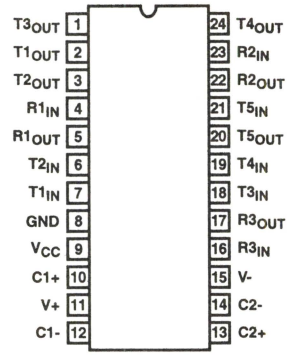


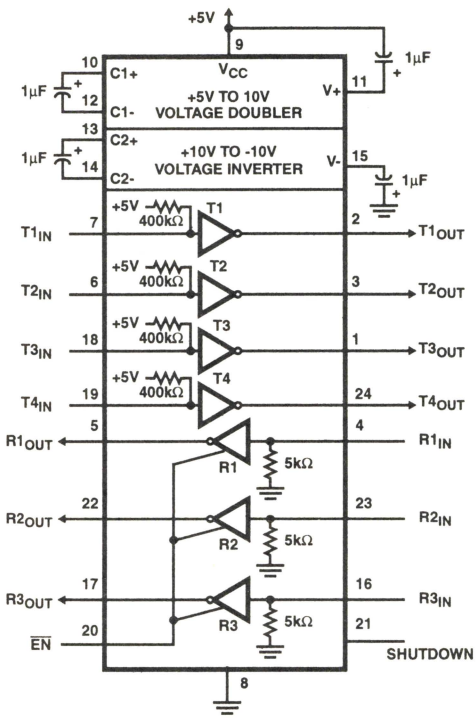
Pinouts (Continued)

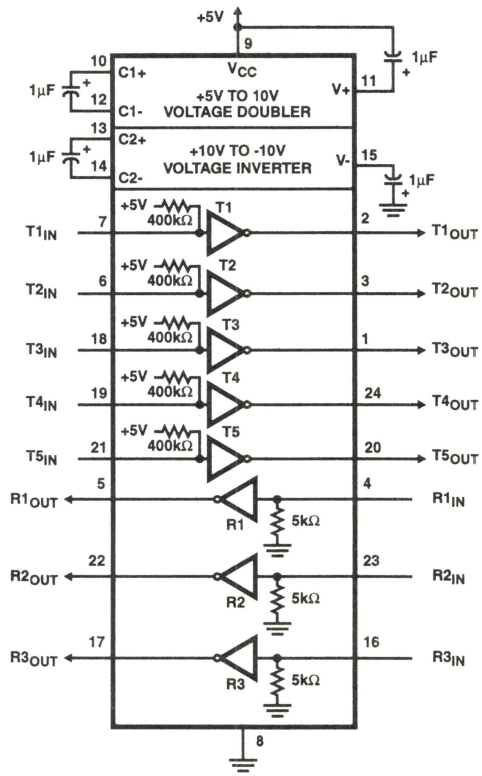
HIN236 (PDIP, SOIC)
TOP VIEW



HIN237 (PDIP, SOIC)
TOP VIEW

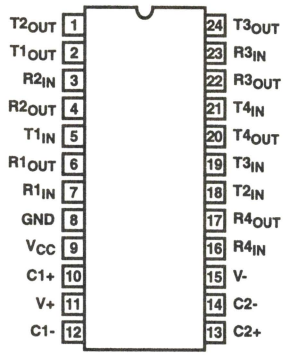




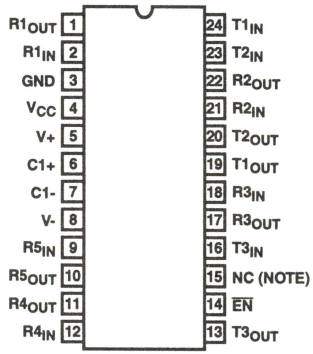


Pinouts (Continued)

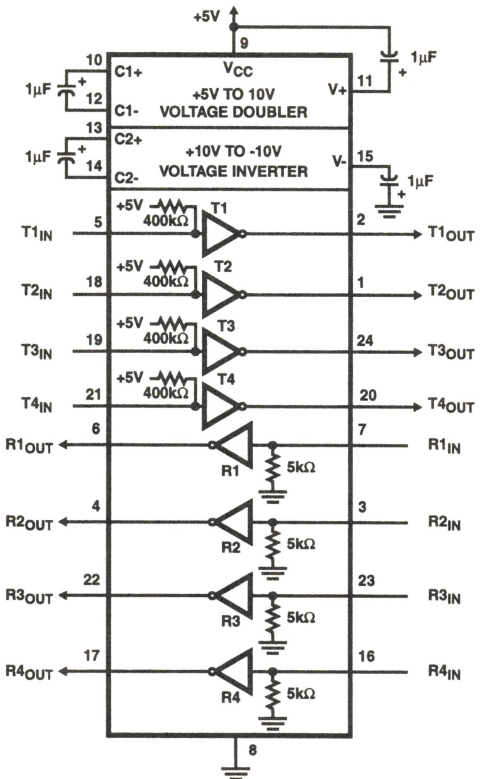
HIN238 (PDIP, SOIC)
TOP VIEW

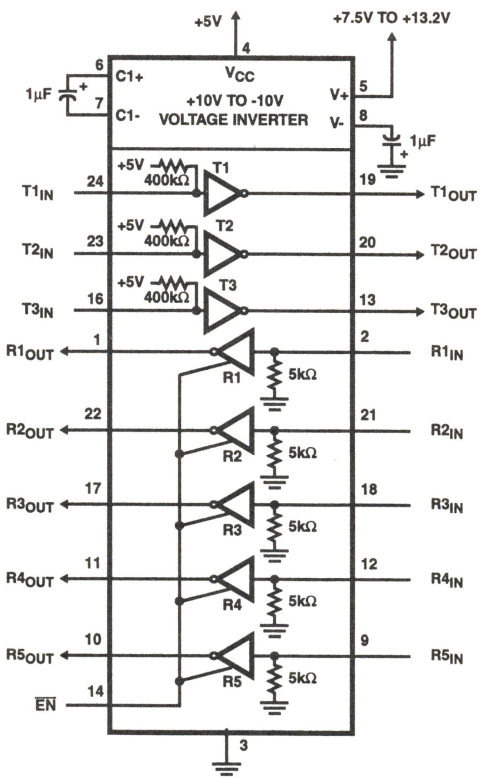


HIN239 (SOIC)
TOP VIEW



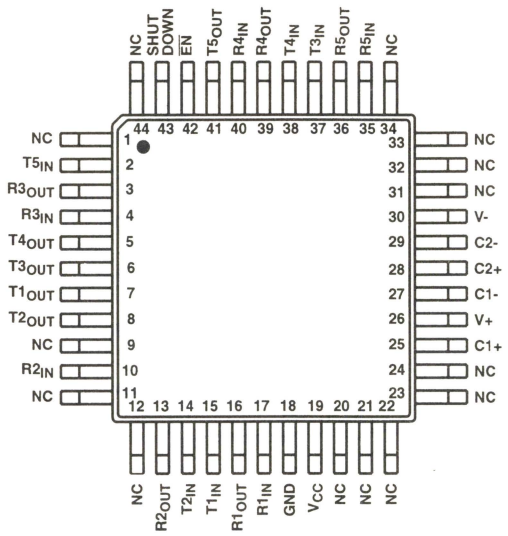
NOTE: No Connect



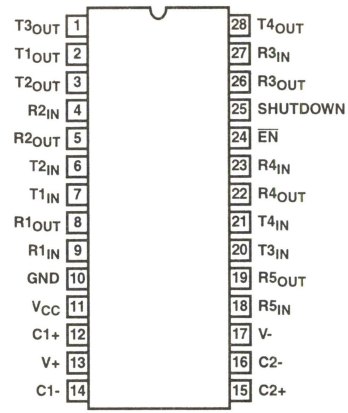


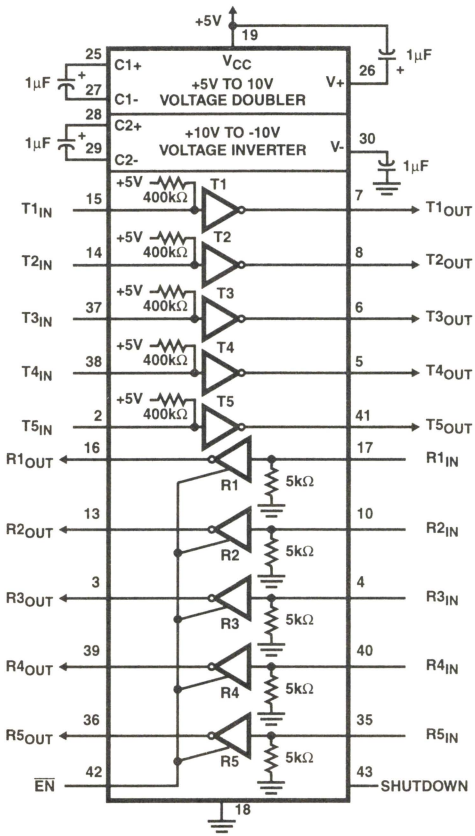
Pinouts (Continued)

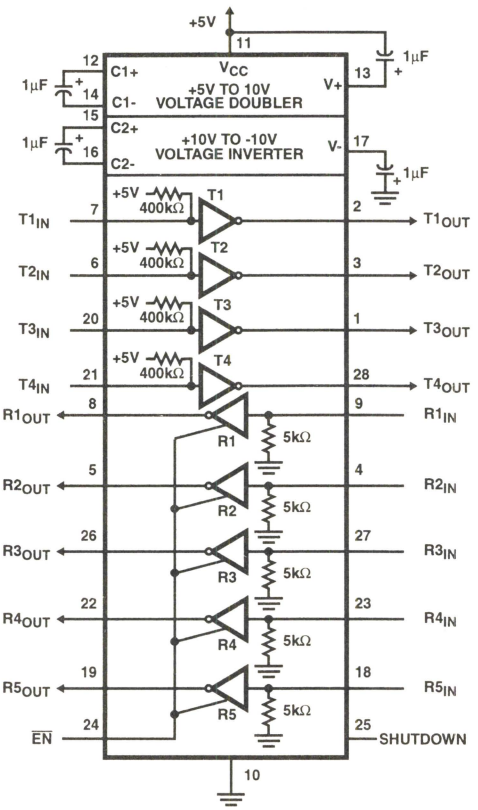
HIN240 (MQFP)



HIN241 (SOIC, SSOP)
TOP VIEW







Absolute Maximum Ratings

V_{CC} to Ground . . . . . (GND -0.3V) < V_{CC} < 6V
V+ to Ground . . . . . (V_{CC} -0.3V) < V+ < 12V
V- to Ground . . . . . -12V < V- < (GND +0.3V)
Input Voltages
  T_{IN} . . . . . (V- -0.3V) < V_{IN} < (V+ +0.3V)
  R_{IN} . . . . . ±30V
Output Voltages
  T_{OUT} . . . . . (V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
  R_{OUT} . . . . . (GND -0.3V) < V_{RXOUT} < (V+ +0.3V)
Short Circuit Duration
  T_{OUT} . . . . . Continuous
  R_{OUT} . . . . . Continuous

Operating Conditions

Temperature Range
  HIN-XXXCX . . . . . 0°C to 70°C
  HIN-XXXIX . . . . . -40°C to 85°C
  HIN-XXXMX . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld PDIP Package	90	N/A
24 Ld PDIP Package	75	N/A
16 Ld SOIC (W) Package	100	N/A
24 Ld SOIC Package	80	N/A
28 Ld SOIC Package	75	N/A
28 Ld SSOP Package	100	N/A
44 Ld MQFP Package	80	N/A
16 Ld CERDIP Package	80	18

Maximum Junction Temperature (Hermetic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC, SSOP, MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, (V_{CC} = +5V ±5% HIN233 and HIN235)
T_A = Operating Temperature Range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing, T_{OUT}	Transmitter Outputs, 3kΩ to Ground	±5	±9	±10	V
Power Supply Current, I_{CC}	No Load, T_A = 25°C, HIN232-233	-	5	10	mA
	HIN230, HIN234-238, HIN240-241	-	7	15	mA
	HIN231, HIN239	-	0.4	1	mA
V+ Power Supply Current, I_{CC}	HIN231	-	1.8	5	mA
	HIN239	-	5.0	15	mA
Shutdown Supply Current, I_{CC}(SD)		-	1	10	µA
Input Logic Low, T_{IN}, $\overline{EN}$, V_{IL}	T_{IN}, $\overline{EN}$, Shutdown	-	-	0.8	V
Input Logic High, V_{IH}	T_{IN}	2.0	-	-	V
	$\overline{EN}$, Shutdown	2.4	-	-	V
Logic Pullup Current, I_P	T_{IN} = 0V	-	15	200	µA
RS-232 Input Voltage Range, V_{IN}		-30	-	+30	V
Receiver Input Impedance, R_{IN}	V_{IN} = ±3V	3.0	5.0	7.0	kΩ
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5V, T_A = 25°C	0.8	1.2	-	V
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5V, T_A = 25°C	-	1.7	2.4	V
Receiver Input Hysteresis, V_{HYST}		0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 1.6mA (HIN231-HIN233 I_{OUT} = 3.2mA)	-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	I_{OUT} = -1.0mA	3.5	4.6	-	V
Output Enable Time, t_{EN}	HIN235, 236, 239, 240, 241	-	400	-	ns
Output Disable Time, t_{DIS}	HIN235, 236, 239, 240, 241	-	250	-	ns
Propagation Delay, t_{PD}	RS-232 to TTL	-	0.5	-	µs
Instantaneous Slew Rate, SR	C_L = 10pF, R_L = 3kΩ, T_A = 25°C (Note 2)	-	-	30	V/µs
Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V	-	3	-	V/µs
Output Resistance, R_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V	300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	T_{OUT} shorted to GND	-	±10	-	mA

NOTE:
2. Guaranteed by design.

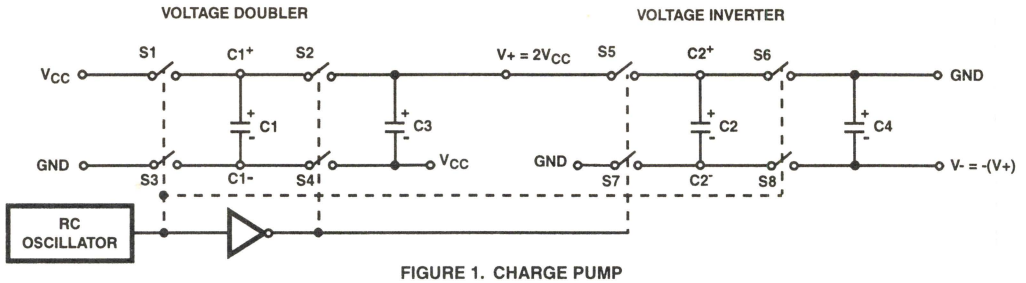


FIGURE 1. CHARGE PUMP

Detailed Description

The HIN230 thru HIN241 family of RS-232 transmitters/receivers are powered by a single +5V power supply (except HIN-231 and HIN239), feature low power consumption, and meet all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: the charge pump, transmitter, and receiver.

Charge Pump

An equivalent circuit of the charge pump is illustrated in Figure 1. The charge pump contains two sections: the voltage doubler and the voltage inverter. Each section is driven by a two phase, internally generated clock to generate +10V and -10V. The nominal clock frequency is 16kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C3 equal to twice V_{CC}. During phase one, C2 is also charged to $2V_{CC}$, and then during phase two, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The charge pump accepts input voltages up to 5.5V. The output impedance of the voltage doubler section (V+) is approximately 200Ω, and the output impedance of the voltage inverter section (V-) is approximately 450Ω. A typical application uses 1µF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.

During shutdown mode (HIN230, 236, 240 and 241), SHUTDOWN control line set to logic "1", the charge pump is turned off, V+ is pulled down to V_{CC}, V- is pulled up to GND, and the supply current is reduced to less than 10µA. The transmitter outputs are disabled and the receiver outputs are placed in the high impedance state.

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ -0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specifications of ±5V minimum with the worst case conditions of: all transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/µs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with ±2V applied to the outputs and V_{CC} = 0V.

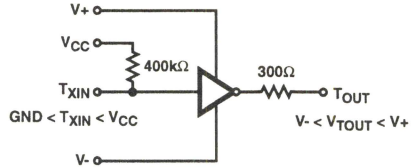


FIGURE 2. TRANSMITTER

Receivers

The receiver inputs accept up to ±30V while presenting the required 3kΩ to 7kΩ input impedance even it the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specifications. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis to improve noise rejection. The receiver Enable line $\overline{EN}$, when set to logic "1", (HIN236, 239, 240, and 241) disables the receiver outputs, placing them in the high impedance mode. The receiver outputs are also placed in the high impedance state when in shutdown mode.

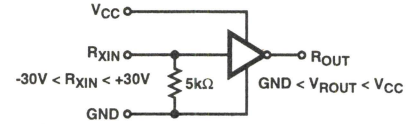
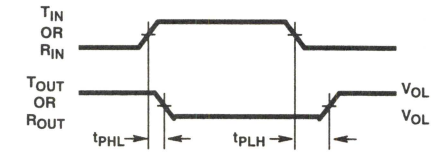


FIGURE 3. RECEIVER



$$\text{Average Propagation Delay} = \frac{t_{PHL} + t_{PLH}}{2}$$

FIGURE 4. PROPAGATION DELAY DEFINITION

Typical Performance Curves

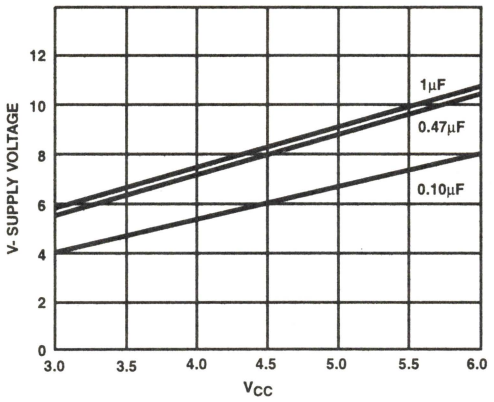


FIGURE 5. V- SUPPLY VOLTAGE vs V_{CC}, VARYING CAPACITORS

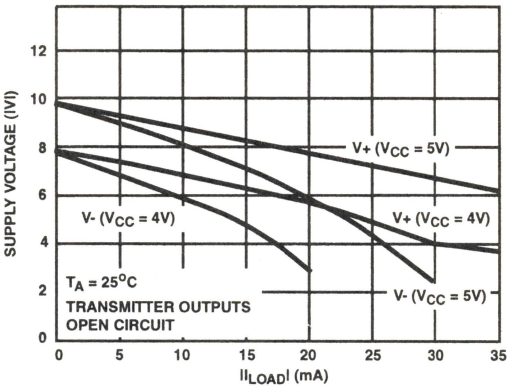


FIGURE 6. V+, V- OUTPUT VOLTAGE vs LOAD

Test Circuits (HIN232)

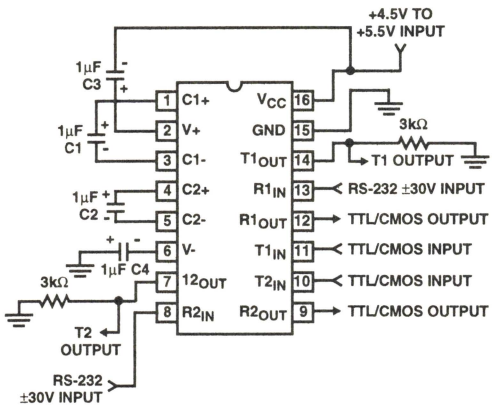


FIGURE 7. GENERAL TEST CIRCUIT

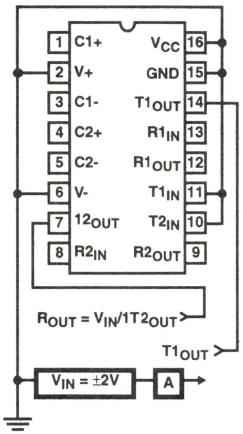


FIGURE 8. POWER-OFF SOURCE RESISTANCE CONFIGURATION

Applications

The HINXXX may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 9. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

In applications requiring four RS-232 inputs and outputs (Figure 10), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

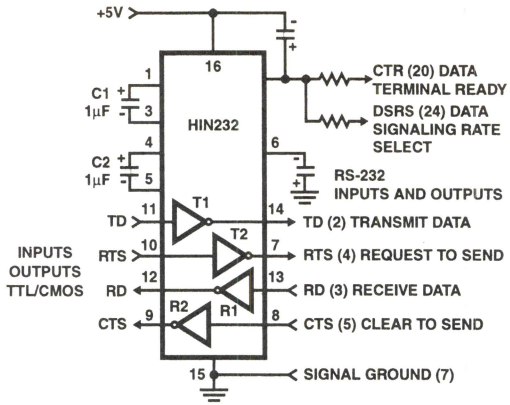


FIGURE 9. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

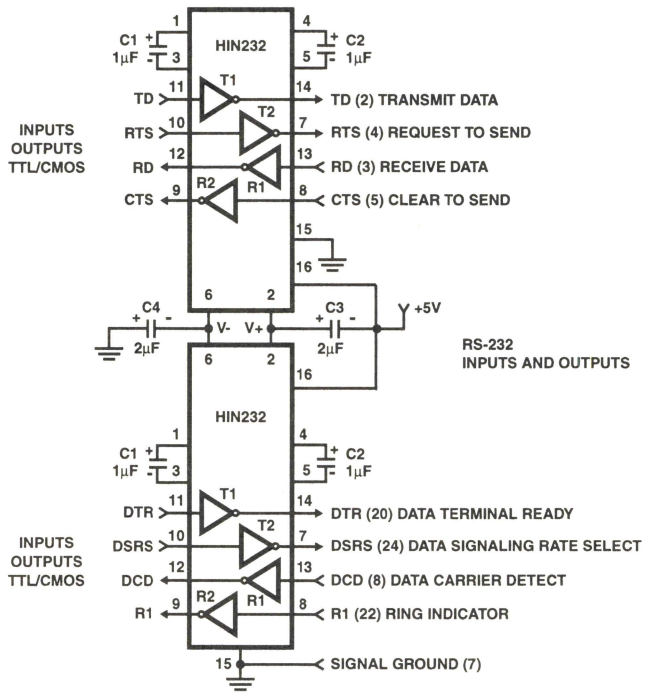


FIGURE 10. COMBINING TWO HIN232s FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

Die Characteristics

DIE DIMENSIONS:

160 mils x 140 mils

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

SUBSTRATE POTENTIAL

V+

PASSIVATION:

Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

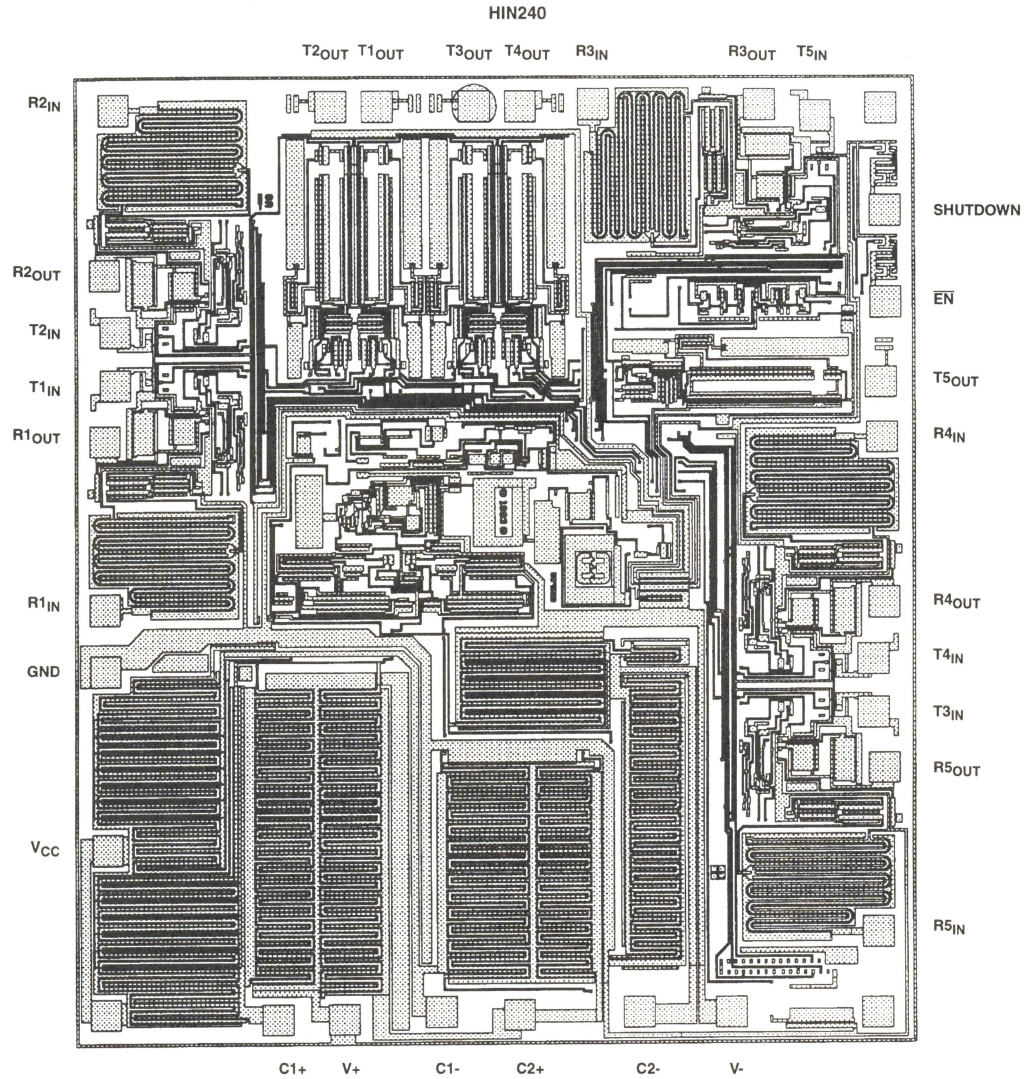
TRANSISTOR COUNT:

238

PROCESS:

CMOS Metal Gate

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HIN232A

High Speed, +5V, RS-232 Transmitter/Receiver with 0.1Microfarad External Capacitor

August 1997

Features

- Meets All EIA RS-232E and V.28/V.24 Specifications
- Requires Only 0.1µF or Greater External Capacitors
- Data Rate 230kbit/s
- Requires Only Single +5V Power Supply
- Onboard Voltage Doubler/Inverter
- Low Power Consumption (Typ) 4mA
- Multiple Drivers
  - Output Swing for +5V Input..... ±10V
  - Power-Off Source Impedance 300Ω
  - Output Current Limiting
  - TTL/CMOS Compatible
  - Typical Slew Rate (Typ) 12V/µs
- Multiple Receivers
  - Input Voltage Range..... ±30V
  - Input Impedance..... 3kΩ to 7kΩ
  - Hysteresis to Improve Noise Rejection 0.5V

Applications

- Any System Requiring RS-232 Communications Port
  - Computers - Portables, Mainframes, Laptops
  - Peripherals - Printers and Terminals
  - Portable Instrumentation
  - Modems

Description

The HIN232A High Speed RS-232 transmitter/receiver interface circuit meets all EIA RS-232E and V.28/V.24 specifications, and is particularly suited for those applications where ±12V is not available. The device requires a single +5V power supply and features onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply.

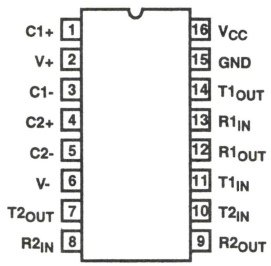
The drivers feature true TTL/CMOS input compatibility, slew rate-limited output, and 300Ω power-off source impedance, and operating speeds up to 230kbit/s. The receivers can handle up to ±30V input, and have a 3kΩ to 7kΩ input impedance. The receivers also feature hysteresis to greatly improve noise rejection.

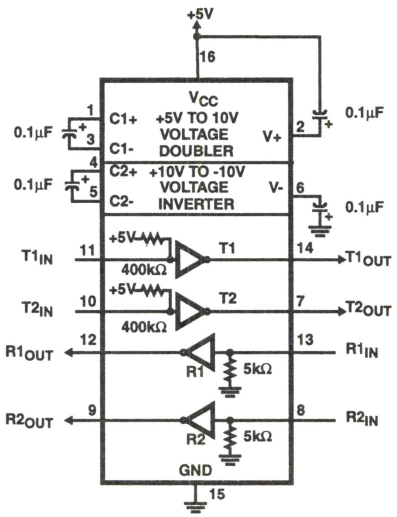
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN232ACP	0 to 70	16 Ld PDIP	E16.3
HIN232ACB	0 to 70	16 Ld SOIC (W)	M16.3
HIN232ACA	0 to 70	16 Ld SSOP	M16.209
HIN232ACBN	0 to 70	16 Ld SOIC (N)	M16.15

Pinout

HIN232A (PDIP, SOIC, SSOP)
TOP VIEW





CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **4316.1**

Pin Descriptions

PIN	FUNCTION
V_{CC}	Power Supply Input 5V ±10%.
V+	Internally Generated Positive Supply (+10V nominal).
V-	Internally Generated Negative Supply (-10V nominal).
GND	Ground Lead. Connect to 0V.
C1+	External Capacitor (+ terminal) is connected to this lead.
C1-	External Capacitor (- terminal) is connected to this lead.
C2+	External Capacitor (+ terminal) is connected to this lead.
C2-	External Capacitor (- terminal) is connected to this lead.
T_{IN}	Transmitter Inputs. These leads accept TTL/CMOS levels. An internal 400kΩ pull-up resistor to V_{CC} is connected to each lead.
T_{OUT}	Transmitter Outputs. These are RS-232 levels (nominally ±10V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 input levels. An internal 5kΩ pull-down resistor to GND is connected to each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.

Absolute Maximum Ratings

V_{CC} to Ground . . . . . (GND -0.3V) <V_{CC} < 6V
V+ to Ground . . . . . (V_{CC} -0.3V) <V+ < 12V
V- to Ground . . . . . -12V < V- < (GND +0.3V)
Input Voltages
  T_{IN} . . . . . (V- -0.3V) < V_{IN} < (V+ +0.3V)
  R_{IN} . . . . . ±30V
Output Voltages
  T_{OUT} . . . . . (V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
  R_{OUT} . . . . . (GND -0.3V) < V_{RXOUT} < (V+ +0.3V)
Short Circuit Duration
  T_{OUT} . . . . . Continuous
  R_{OUT} . . . . . Continuous
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package (W)	100
SOIC Package (N)	115
SSOP Package	155

Maximum Junction Temperature
  Plastic Package . . . . . 150°C
Maximum Storage Temperature Range . . . . . -40°C to 85°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
  (SOIC and SSOP - Lead Tips Only)

Operating Conditions

Temperature Range
  HIN232ACX . . . . . 0°C to 70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, C1-C4 = 0.1µF
T_A = Operating Temperature Range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing, T_{OUT}	Transmitter Outputs, 3kΩ to Ground	±5	±9	-	V
Power Supply Current, I_{CC}	No Load, T_A = 25°C	-	4	10	mA
Power Supply Current, I_{CC}	Load = 3kΩ, both outputs, T_A = 25°C	-	15	-	mA
Input Logic Low, V_{IL}	T_{IN}	-	1.4	0.8	V
Input Logic High, V_{IH}	T_{IN}	2.0	1.4	-	V
Logic Pullup Current, I_P	T_{IN} = 0V	-	5.0	40	µA
RS-232 Input Voltage Range, V_{IN}		-30	-	+30	V
Receiver Input Impedance, R_{IN}	T_A = 25°C, V_{IN} = ±3V	3.0	5.0	7.0	kΩ
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5.0V, T_A = 25°C	0.8	1.2	-	V
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5.0V, T_A = 25°C	-	1.7	2.4	V
Receiver Input Hysteresis, V_{HYST}	V_{CC} = 5.0V	0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 3.2mA	-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	I_{OUT} = -1.0mA	3.5	-	-	V
Propagation Delay, t_{PD}	TTL to RS-232	-	-	3.5	µs
Propagation Delay, R_{PD}	RS-232 to TTL	-	0.5	1.0	µs
Transmitter + to - Propagation Delay Difference		-	300	-	ns
Receiver + to - Propagation Delay Difference		-	100	-	ns
Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or-3V to +3V (Note 2)	6.0	12.0	30	V/µs
Output Resistance, R_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V	300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	T_{OUT} Shorted to GND	-	±10	-	mA

NOTE:

2. Guaranteed by design.

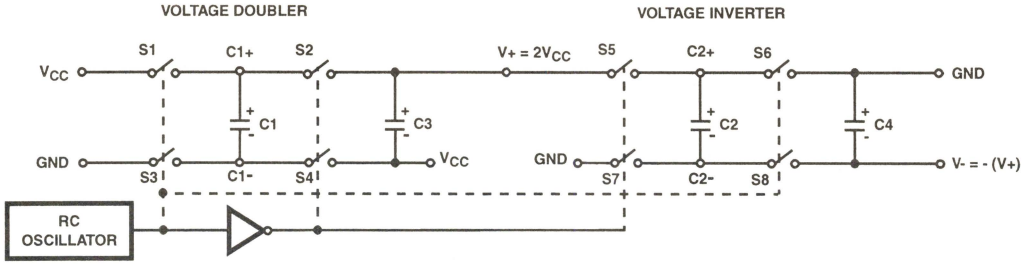


FIGURE 1. CHARGE PUMP

Detailed Description

The HIN232A High Speed RS-232 transmitters/receivers are powered by a single +5V power supply, feature low power consumption, and meet all EIA RS232E and V.28/V.24 specifications. The circuit is divided into three sections: the charge pump, transmitter, and receiver.

Charge Pump

An equivalent circuit of the charge pump is illustrated in Figure 1. The charge pump contains two sections: the voltage doubler and the voltage inverter. Each section is driven by a two phase, internally generated clock to generate +10V and -10V. The nominal clock frequency is 125kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C3 equal to twice V_{CC}. During phase two, C2 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The charge pump accepts input voltages up to 5.5V. The output impedance of the voltage doubler section (V+) is approximately 200Ω, and the output impedance of the voltage inverter section (V-) is approximately 450Ω. A typical application uses 0.1µF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ -0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specifications of ±5V minimum with the worst case conditions of: all transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/µs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with ±2V applied to the outputs and V_{CC} = 0V.

Receivers

The receiver inputs accept up to ±30V while presenting the required 3kΩ to 7kΩ input impedance even if the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specifications. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis to improve noise rejection.

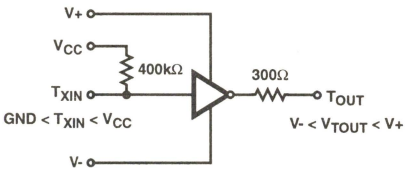


FIGURE 2. TRANSMITTER

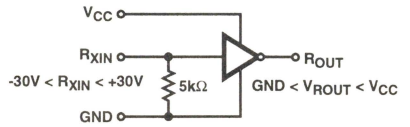
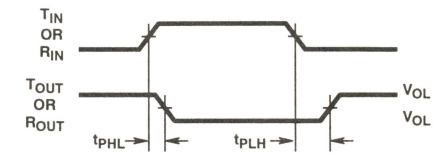


FIGURE 3. RECEIVER



$$\text{AVERAGE PROPAGATION DELAY} = \frac{t_{PHL} + t_{PLH}}{2}$$

FIGURE 4. PROPAGATION DELAY DEFINITION

Typical Performance Curves

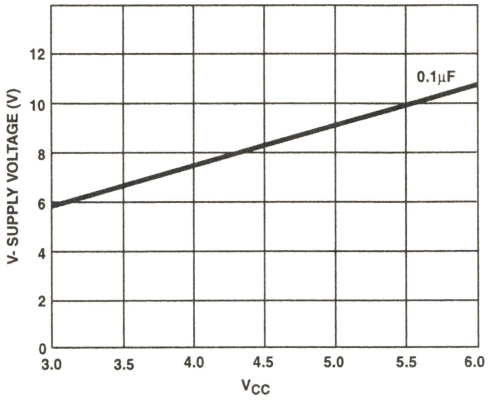


FIGURE 5. V- SUPPLY VOLTAGE vs V_{CC}

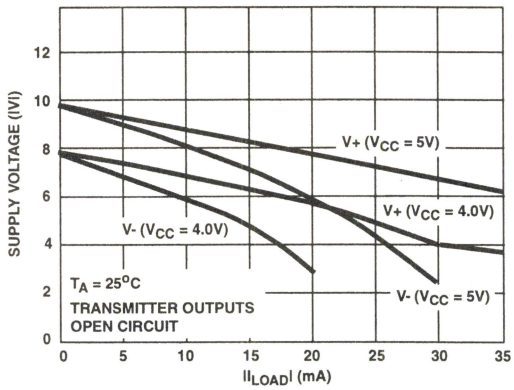


FIGURE 6. V+, V- OUTPUT VOLTAGE vs LOAD

Test Circuits (HIN232A)

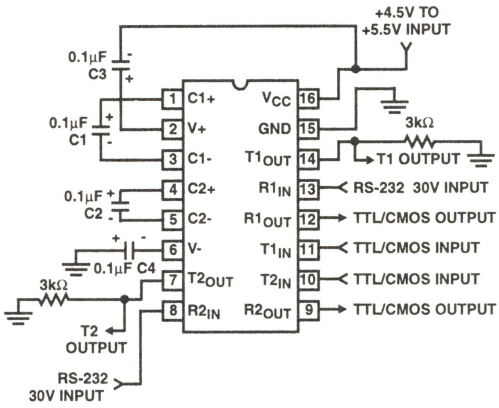


FIGURE 7. GENERAL TEST CIRCUIT

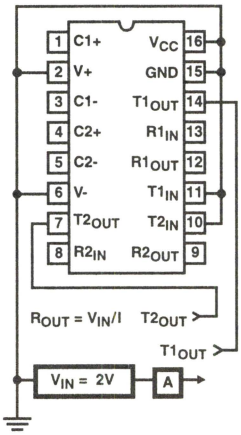


FIGURE 8. POWER-OFF SOURCE RESISTANCE CONFIGURATION

Typical Applications

The HIN232A may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 9. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

In applications requiring four RS-232 inputs and outputs (Figure 10), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

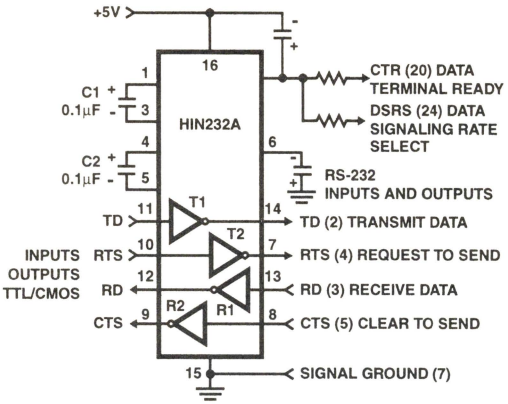


FIGURE 9. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

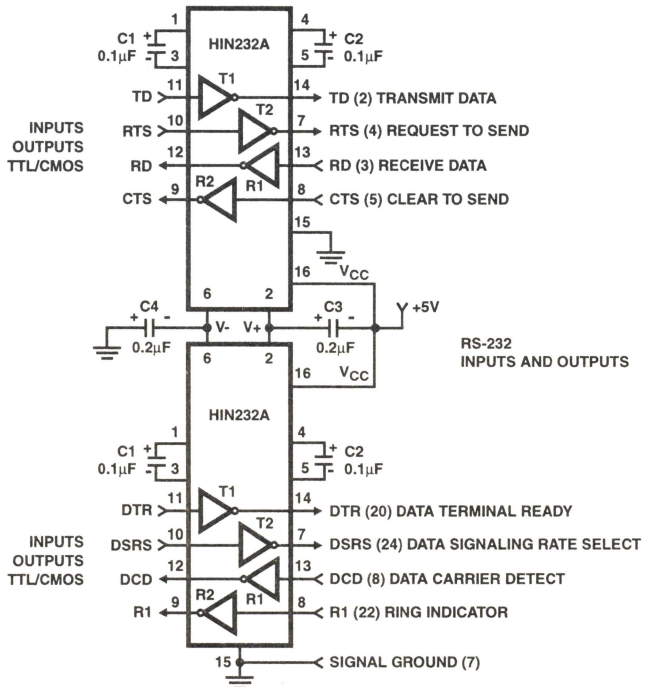


FIGURE 10. COMBINING TWO HIN232As FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

Die Characteristics

DIE DIMENSIONS:

120 mils x 75 mils

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

TRANSISTOR COUNT:

111

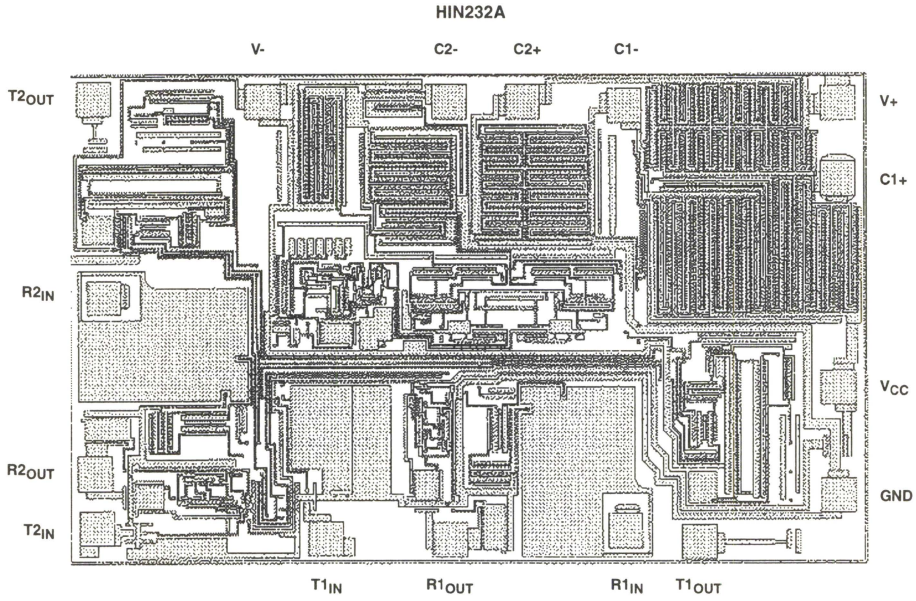
PROCESS:

CMOS Metal Gate

SUBSTRATE POTENTIAL:

V+

Metallization Mask Layout



ICL232

August 1997

+5V Powered, Dual RS-232 Transmitter/Receiver

Features

- Meets All RS-232C and V.28 Specifications
- Requires Only Single +5V Power Supply
- Onboard Voltage Doubler/Inverter
- Low Power Consumption
- 2 Drivers
  - ±9V Output Swing for +5V Input
  - 300Ω Power-off Source Impedance
  - Output Current Limiting
  - TTL/CMOS Compatible
  - 30V/μs Maximum Slew Rate
- 2 Receivers
  - ±30V Input Voltage Range
  - 3kΩ to 7kΩ Input Impedance
  - 0.5V Hysteresis to Improve Noise Rejection
- All Critical Parameters are Guaranteed Over the Entire Commercial, Industrial and Military Temperature Ranges

Applications

- Any System Requiring RS-232 Communications Port
  - Computer - Portable and Mainframe
  - Peripheral - Printers and Terminals
  - Portable Instrumentation
  - Modems
- Dataloggers

Description

The ICL232 is a dual RS-232 transmitter/receiver interface circuit that meets all EIA RS-232C and V.28 specifications. It requires a single +5V power supply, and features two onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply.

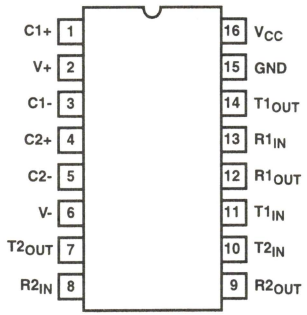
The drivers feature true TTL/CMOS input compatibility, slew-rate-limited output, and 300Ω power-off source impedance. The receivers can handle up to +30V, and have a 3kΩ to 7kΩ input impedance. The receivers also have hysteresis to improve noise rejection.

Ordering Information

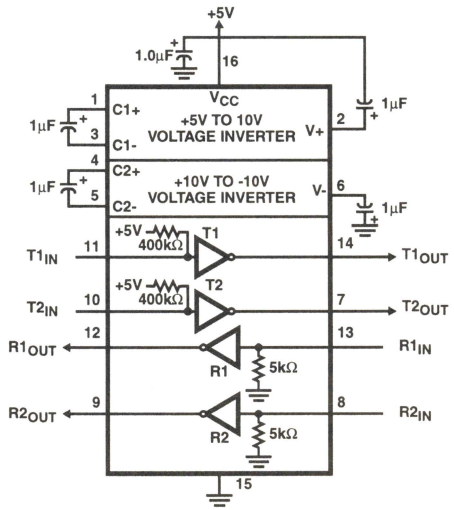
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL232CPE	0 to 70	16 Ld PDIP	E16.3
ICL232CBE	0 to 70	16 Ld SOIC	M16.3
ICL232IPE	-40 to 85	16 Ld PDIP	E16.3
ICL232IJE	-40 to 85	16 Ld CERDIP	F16.3
ICL232IBE	-40 to 85	16 Ld SOIC	M16.3
ICL232MJE	-55 to 125	16 Ld CERDIP	F16.3

Pinout

ICL232 (PDIP, CERDIP, SOIC)
TOP VIEW



Functional Diagram



8 COMMUNICATION INTERFACE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

File Number 3020.5

Absolute Maximum Ratings

V_{CC} to Ground . . . . . (GND -0.3V) < V_{CC} < 6V
V+ to Ground . . . . . (V_{CC} -0.3V) < V+ < 12V
V- to Ground . . . . . -12V < V- < (GND +0.3V)
Input Voltages
$T1_{IN}$, $T2_{IN}$ . . . . . (V- -0.3V) < V_{IN} < (V+ +0.3V)
$R1_{IN}$, $R2_{IN}$ . . . . . ±30V
Output Voltages
$T1_{OUT}$, $T2_{OUT}$ . . . . . (V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
$R1_{OUT}$, $R2_{OUT}$ . . . . . (GND -0.3V) < V_{RXOUT} < (V_{CC} +0.3V)
Short Circuit Duration
$T1_{OUT}$, $T2_{OUT}$ . . . . . Continuous
$R1_{OUT}$, $R2_{OUT}$ . . . . . Continuous

Operating Conditions

Temperature Ranges
ICL232C . . . . . 0°C to 70°C
ICL232I . . . . . -40°C to 85°C
ICL232M . . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	80	18
PDIP Package	100	N/A
SOIC Package	100	N/A

Maximum Junction Temperature
Plastic Packages . . . . . 150°C
Ceramic Package . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, T_A = Operating Temperature Range. Test Circuit as in Figure 8 Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter Output Voltage Swing, T_{OUT}	$T1_{OUT}$ and $T2_{OUT}$ Loaded with 3kΩ to Ground	±5	±9	±10	V
Power Supply Current, I_{CC}	Outputs Unloaded, T_A = 25°C	-	5	10	mA
T_{IN}, Input Logic Low, V_{IL}		-	-	0.8	V
T_{IN}, Input Logic High, V_{IH}		2.0	-	-	V
Logic Pullup Current, I_P	$T1_{IN}$, $T2_{IN}$ = 0V	-	15	200	µA
RS-232 Input Voltage Range, V_{IN}		-30	-	+30	V
Receiver Input Impedance, R_{IN}	V_{IN} = ±3V	3.0	5.0	7.0	kΩ
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5V, T_A = 25°C	0.8	1.2	-	V
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5V, T_A = 25°C	-	1.7	2.4	V
Receiver Input Hysteresis, V_{HYST}		0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 3.2mA	-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	I_{OUT} = -1.0mA	3.5	4.6	-	V
Propagation Delay, t_{PD}	RS-232 to TTL	-	0.5	-	µs
Instantaneous Slew Rate, SR	C_L = 10pF, R_L = 3kΩ, T_A = 25°C (Notes 2, 3)	-	-	30	V/µs
Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V	-	3	-	V/µs
Output Resistance, R_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V	300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	$T1_{OUT}$ or $T2_{OUT}$ Shorted to GND	-	±10	-	mA

NOTES:

2. Guaranteed by design.
3. See Figure 4 for definition.

Test Circuits

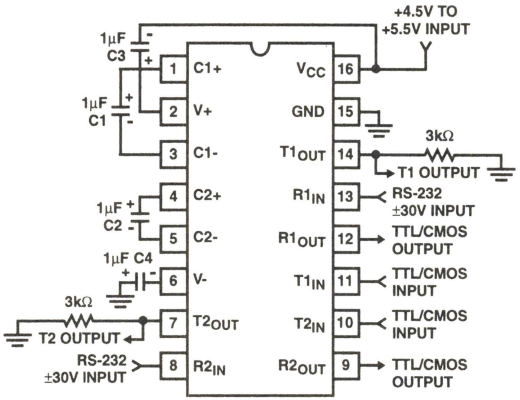


FIGURE 1. GENERAL TEST CIRCUIT

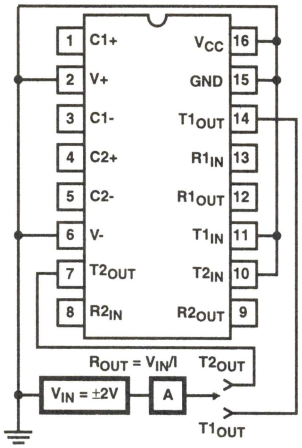


FIGURE 2. POWER-OFF SOURCE RESISTANCE CONFIGURATION

Typical Performance Curves

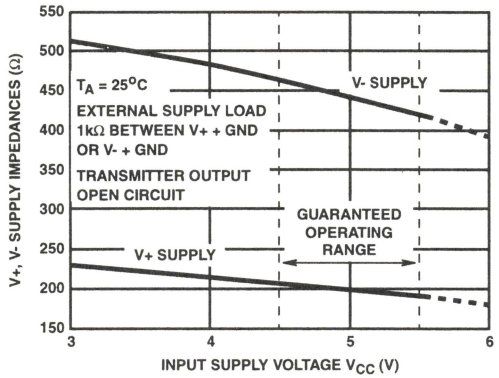


FIGURE 3. V+, V- OUTPUT IMPEDANCES vs V_{CC}

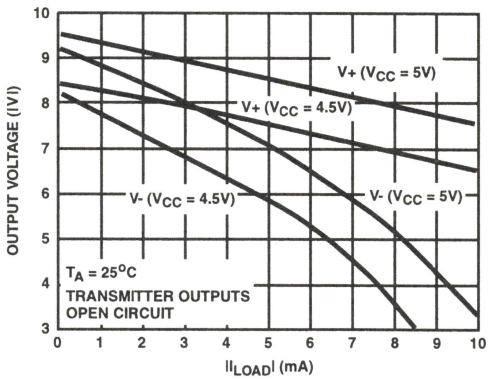


FIGURE 4. V+, V- OUTPUT VOLTAGES vs LOAD CURRENT

Pin Descriptions

PDIP, CERDIP	SOIC	PIN NAME	DESCRIPTION
1	1	C1+	External capacitor "+" for internal voltage doubler.
2	2	V+	Internally generated +10V (typical) supply.
3	3	C1-	External capacitor "-" for internal voltage doubler.
4	4	C2+	External capacitor "+" internal voltage inverter.
5	5	C2-	External capacitor "-" internal voltage inverter.
6	6	V-	Internally generated -10V (typical) supply.
7	7	$T2_{OUT}$	RS-232 Transmitter 2 output ±10V (typical).
8	8	$R2_{IN}$	RS-232 Receiver 2 input, with internal 5K pulldown resistor to GND.
9	9	R2out	Receiver 2 TTL/CMOS output.
10	10	$T2_{IN}$	Transmitter 2 TTL/CMOS input, with internal 400K pullup resistor to V_{CC}.
11	11	$T1_{IN}$	Transmitter 1 TTL/CMOS input, with internal 400K pullup resistor to V_{CC}.

Pin Descriptions (Continued)

PDIP, CERDIP	SOIC	PIN NAME	DESCRIPTION
12	12	$R1_{OUT}$	Receiver 1 TTL/CMOS output.
13	13	$R1_{IN}$	RS-232 Receiver 1 input, with internal 5K pulldown resistor to GND.
14	14	$T1_{OUT}$	RS-232 Transmitter 1 output ±10V (typical).
15	15	GND	Supply Ground.
16	16	V_{CC}	Positive Power Supply +5V ±10%

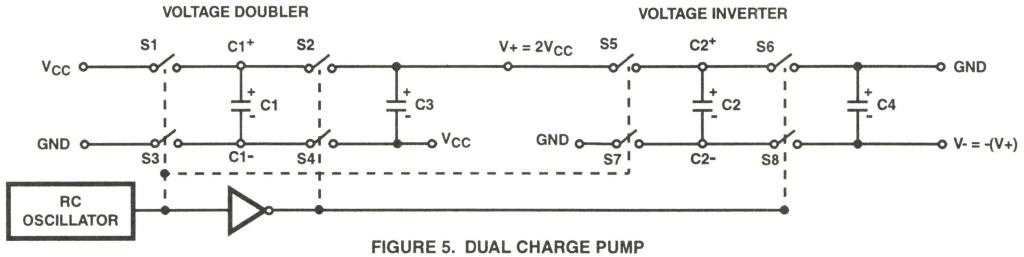


FIGURE 5. DUAL CHARGE PUMP

Detailed Description

The ICL232 is a dual RS-232 transmitter/receiver powered by a single +5V power supply which meets all EIA RS232C specifications and features low power consumption. The functional diagram illustrates the major elements of the ICL232. The circuit is divided into three sections: a voltage doubler/inverter, dual transmitters, and dual receivers Voltage Converter.

An equivalent circuit of the dual charge pump is illustrated in Figure 5.

The voltage quadrupler contains two charge pumps which use two phases of an internally generated clock to generate +10V and -10V. The nominal clock frequency is 16kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C2 equal to twice V_{CC}. At the same time, C3 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The voltage converter accepts input voltages up to 5.5V. The output impedance of the doubler (V+) is approximately 200Ω, and the output impedance of the inverter (V-) is approximately 450Ω. Typical graphs are presented which show the voltage converters output vs input voltage and output voltages vs load characteristics. The test circuit (Figure 3) uses 1µF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, and increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.

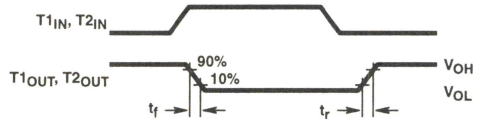


FIGURE 6. SLEW RATE DEFINITION

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ - 0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specification of ±5V minimum with the worst case conditions of: both transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/µs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with ±2V applied to the outputs and V_{CC} = 0V.

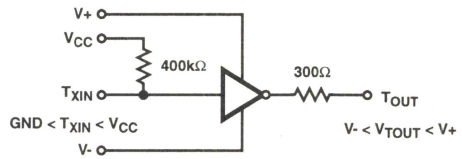


FIGURE 7. TRANSMITTER

Receivers

The receiver inputs accept up to ±30V while presenting the required 3kΩ to 7kΩ input impedance even it the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specification. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis to improve noise rejection.

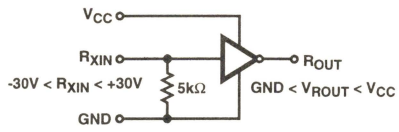
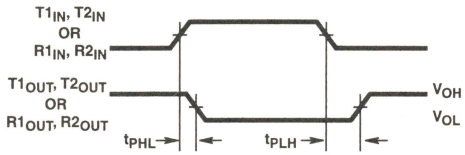


FIGURE 8. RECEIVER



$$\text{Average Propagation Delay} = \frac{t_{PHL} + t_{PLH}}{2}$$

FIGURE 9. PROPAGATION DELAY DEFINITION

Applications

The ICL232 may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 10. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

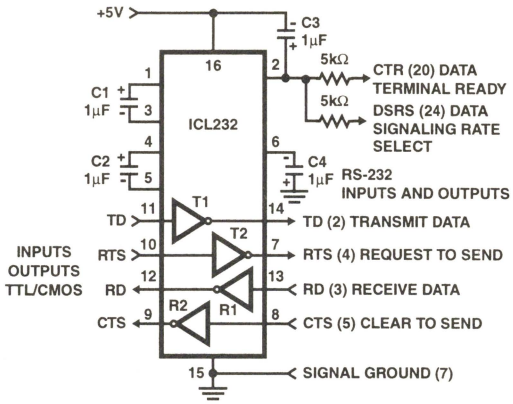


FIGURE 10. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

In applications requiring four RS-232 inputs and outputs (Figure 11), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

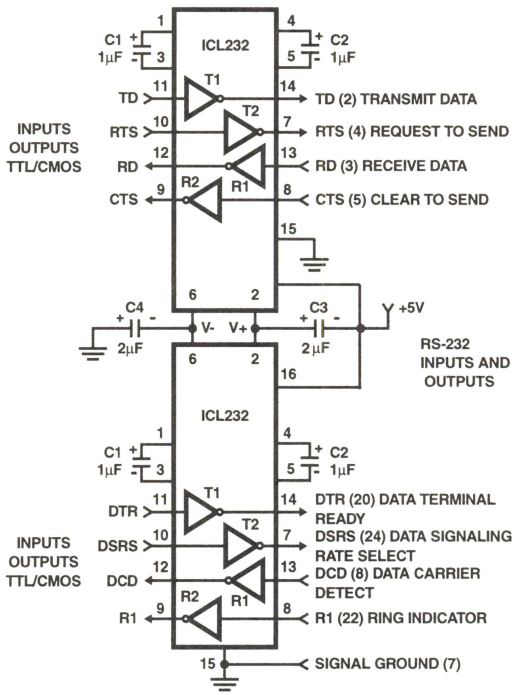


FIGURE 11. COMBINING TWO ICL232s FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

DATA ACQUISITION 9

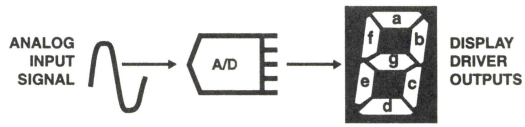
COUNTERS WITH DISPLAY DRIVERS/ TIMEBASE GENERATORS

		PAGE
Selection Guide		9-2
Counters With Display Drivers/Timebase Generators Data Sheets		
CA3161	BCD to Seven Segment Decoder/Driver	9-5
ICM7211, ICM7212	4-Digit, ICM7211 (LCD) and ICM7212 (LED) Display Drivers	9-6
ICM7213	One Second/One Minute Timebase Generator	9-9
ICM7216A, ICM7216B, ICM7216D	8-Digit, Multi-Function, Frequency Counters/Timers	9-10
ICM7217	4-Digit LED Display, Programmable Up/Down Counter	9-12
ICM7224	$4\frac{1}{2}$ Digit LCD Display Counter	9-14
ICM7226A, ICM7226B	8-Digit, Multi-Function, Frequency Counter/Timer	9-15
ICM7228	8-Digit, Microprocessor-Compatible, LED Display Decoder Driver	9-17
ICM7231, ICM7232	Numeric/Alphanumeric Triplexed LCD Display Drivers	9-19
ICM7243	8-Character, Microprocessor-Compatible, LED Display Decoder Driver	9-21
ICM7249	$5\frac{1}{2}$ Digit LCD, Micro-Power Event/Hour Meter	9-23

Selection Guide

ANALOG TO DIGITAL CONVERTERS WITH DISPLAY OUTPUTS (2 Chip Sets)

PART NUMBER	OUTPUT TYPE	RESOLUTION	CONVERSION TIME (SAMPLE RATE)	PACKAGE TYPES	FEATURES
CA3161	LED, CA, BCD	3 Digits	10ms/250ms (96SPS/4SPS)	16 Lead PDIP	2 Chip Set Makes a Complete DPM A/D Converter, 3 Digit Output, "EEE": Positive Over-Range Indication, "-": Negative Over-Range Display
CA3162					



TIMER/COUNTERS WITH DISPLAY DRIVERS

TYPE	COMMENTS AND APPLICATIONS	DISPLAY					FUNCTIONS																
		LED			LCD	VF	UNIT COUNT				UNIVERSAL COUNTERS												
		COMMON ANODE, NON-MUX	COMMON CATHODE, MUX	COMMON ANODE, MUX	DIRECT DRIVE, NON-MUX	NON-MUX	UP/DOWN	UP ONLY	DECADE	MODULE 60 (HR/MIN/SEC)	FREQUENCY	PERIOD	FREQUENCY RATIO	TIME INTERVAL	MUX BCD OUTPUTS	DISPLAY LATCH	DISPLAY BLANKING	COUNT ENABLE	LEADING ZERO BLANKING	PRESET COUNT	COMPARISON REGISTER	EQUAL AND ZERO OUTPUT	MAX COUNT SPEED (MHz)
4 DIGIT																							
ICM7217	Industrial Control: Preset Predetermining Counters, Sequencers, On Off Delay Timers, Batch Counters. Presets and Loads Compare Register From Thumbwheel Switches			•			•		•		(Note 1)				•	•	•		•	•	•	•	2
ICM7217A			•				•		•		(Note 1)				•	•	•		•	•	•	•	2
ICM7217B				•			•			•					•	•	•		•	•	•	•	2
ICM7217C			•				•			•					•	•	•		•	•	•	•	2
4.5 DIGIT																							
ICM7224	10μA Operating Current, Can Be Cascaded for More Digits				•			•	•		(Note 1)					•		•	•				15
5.5 DIGIT																							
ICM7249	Event Timer Counter, Hour Meter. 14 Programmable Modes. Selectable Input Filtering				•			•	•					•									
8 DIGIT																							
ICM7216A	Universal Frequency Counter with Display Drivers. 4 Internal Gate Times, Auto Decimal Point, Leading Zero Blanking, Overflow Indication. Display Off, Hold, and Reset Inputs.			•				•	•		•	•	•	•		•	•		•				10
ICM7216B			•					•	•		•	•	•	•		•	•		•				10
ICM7216D			•					•	•		•					•	•		•				10
ICM7226A	Same as ICM7216 Plus Period and Time Interval Averaging. BCD Outputs, μP PIA Compatible			•				•	•		•	•	•	•	•	•	•	•	•				10
ICM7226B			•					•	•		•	•	•	•	•	•	•	•	•				10

NOTE:

1. These counters will measure frequency when used with the ICM7207 (0.01s or 0.1s timebase) or the ICM7207A (0.1s and 1s timebase).

DISPLAY DRIVERS

TYPE	COMMENTS AND APPLICATIONS	NUMBER OF CHARACTERS OR DIGITS						DISPLAY TYPE						FONT			INTERFACE				
		NUMBER OF 7-SEGMENT DIGITS	NUMBER OF DECIMAL POINTS OR ANNUNCIATORS	NUMBER OF ALPHANUMERIC 14 SEGMENTS + DP	NUMBER OF ALPHANUMERIC 16 SEGMENTS + DP	NUMBER OF ALPHANUMERIC 18 SEGMENTS	NUMBER OF DOT MATRIX	LED, COMMON ANODE NON-MUX	LED, COMMON CATHODE MUX	LED, COMMON ANODE MUX	LCD, DIRECT DRIVE	LCD, NUMBER OF WAYS MUX'D	VACUUM FLUORESCENT	HEXADECIMAL (0-9, A-F)	CODE B (0-9, H, E, L, P, -, AND BLANK)	ASCII	MUX BCD (BCD + DIGIT SELECT STROBES)	RANDOM ACCESS (DATA + ADDRESS + WR)	BIT PARALLEL, DIGIT SERIAL	BIT SERIAL	CYCLE TIME (ns)
ICM7211	Drives Conventional LCD Displays. Includes RC Oscillator, Divider Chain, Latches, Interface and LCD Drivers	4									•			•			•				1000
ICM7211A		4									•				•		•				1000
ICM7211M		4									•			•				•			200
ICM7211AM		4									•				•			•			200
ICM7212AM	Drives Common Anode LED Displays. 28 Current Controlled Outputs. Includes Latches, Interface and Brightness Control.	4						•							•			•			200
ICM7228A	3 Decode Formats Drives Up to 64 Independent LEDs. Includes 8 x 8 Memory, Multiplexed LED Drivers, Encoders, Interface and Control. Applications Include Bar Graphs.	8	8							•				•	•				•		550
ICM7228B		8	8						•					•	•			•			550
ICM7228C		8	8							•				•	•				•		500
ICM7228D		8	8						•					•	•			•			500
ICM7231BF	8 Digits, 16 Annunciators on COM 3, Code B	8	16									3			•			•			500
ICM7232B	10 Digits, 20 Annunciators on COM 3, Code B	10	20									3			•					•	350
ICM7232C	10 Digits, 20 Annunciators on COM 1 +3, Code B	10	20									3			•					•	350
ICM7243A	8 Alphanumeric Characters + Decimal pt. can be Daisy Chained or Cascaded				8				•							•		•	•		250
ICM7243B				8					•							•		•	•		250
CA3161	BCD-to-Seven Segment Decoder Driver	1						•							•						2600

HARRIS SEMICONDUCTOR

Complete data sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

CA3161

August 1997

BCD to Seven Segment Decoder/Driver

Features

- TTL Compatible Input Logic Levels
- 25mA (Typ) Constant Current Segment Outputs
- Eliminates Need for Output Current Limiting Resistors
- Pin Compatible with Other Industry Standard Decoders
- Low Standby Power Dissipation . . . . . 18mW (Typ)

Description

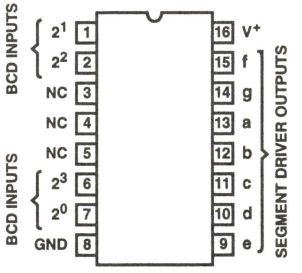
The CA3161E is a monolithic integrated circuit that performs the BCD to seven segment decoding function and features constant current segment drivers. When used with the CA3162E A/D Converter the CA3161E provides a complete digital readout system with a minimum number of external parts.

Ordering Information

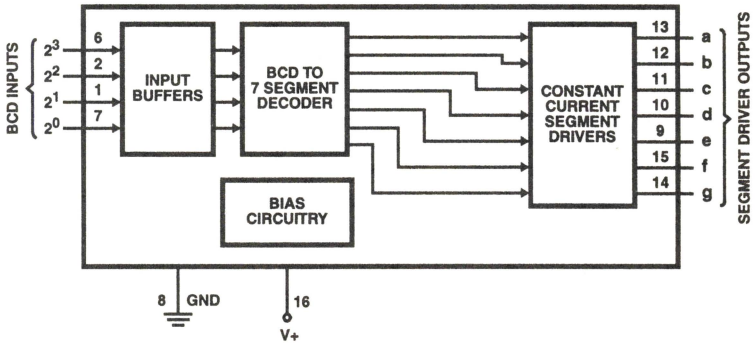
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3161E	0 to 70	16 Ld PDIP	E16.3

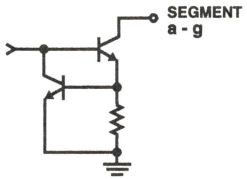
Pinout

CA3161
(PDIP)
TOP VIEW

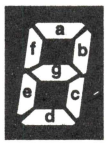


Functional Block Diagram





SEGMENT DRIVER



SEGMENT IDENTIFICATION

9 COUNTERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 1079.3

HARRIS SEMICONDUCTOR

ICM7211, ICM7212

Complete data sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

4-Digit, ICM7211 (LCD) and ICM7212 (LED) Display Drivers

Features ICM7211 (LCD)

- **Four Digit Non-Multiplexed 7 Segment LCD Display Outputs with Backplane Driver**
- **Complete Onboard RC Oscillator to Generate Backplane Frequency**
- **Backplane Input/Output Allows Simple Synchronization of Slave-Devices to a Master**
- **ICM7211 Devices Provide Separate Digit Select Inputs to Accept Multiplexed BCD Input (Pinout and Functionally Compatible with Siliconix DF411)**
- **ICM7211M Devices Provide Data and Digit Address Latches Controlled by Chip Select Inputs to Provide a Direct High Speed Processor Interface**
- **ICM7211 Decodes Binary to Hexadecimal; ICM7211A Decodes Binary to Code B (0-9, Dash, E, H, L, P, Blank)**
- **ICM7211A Available in Surface Mount Package**

Features ICM7212AM (LED)

- **28 Current-Limited Segment Outputs Provide 4-Digit Non-Multiplexed Direct LED Drive at >5mA Per Segment**
- **Brightness Input Allows Direct Control of LED Segment Current with a Single Potentiometer or Digitally as a Display Enable**
- **ICM7212AM Device Provides Same Input Configuration and Output Decoding Options as the ICM7211AM**

Description

The ICM7211 (LCD) and ICM7212 (LED) devices constitute a family of non-multiplexed four-digit seven-segment CMOS display decoder-drivers.

The ICM7211 devices are configured to drive conventional LCD displays by providing a complete RC oscillator, divider chain, backplane driver, and 28 segment outputs.

The ICM7212 devices are configured to drive common-anode LED displays, providing 28 current-controlled, low leakage, open-drain N-Channel outputs. These devices provide a brightness input, which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

These devices are available with multiplexed or microprocessor input configurations. The multiplexed versions provide four data inputs and four Digit Select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226, and ICL7135. The microprocessor versions provide data input latches and Digit Address latches under control of high-speed Chip Select inputs. These devices simplify the task of implementing a cost-effective alphanumeric seven-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices will provide two different decoder configurations. The basic device will decode the four bit binary inputs into a seven-segment alphanumeric hexadecimal output. The "A" versions will provide the "Code B" output code, i.e., 0-9, dash, E, H, L, P, blank. Either device will correctly decode true BCD to seven-segment decimal outputs.

Ordering Information

PART NUMBER	DISPLAY TYPE	DISPLAY DECODING	INPUT INTERFACING	DISPLAY DRIVE TYPE	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICM7211IPL	LCD	Hexadecimal	Multiplexed	Direct Drive	-40 to 85	40 Ld PDIP	E40.6
ICM7211MIPL	LCD	Hexadecimal	Microprocessor	Direct Drive	-40 to 85	40 Ld PDIP	E40.6
ICM7211AIPL	LCD	Code B	Multiplexed	Direct Drive	-40 to 85	40 Ld PDIP	E40.6
ICM7211AMIPL	LCD	Code B	Microprocessor	Direct Drive	-40 to 85	40 Ld PDIP	E40.6
ICM7211AIM44	LCD	Code B	Multiplexed	Direct Drive	-40 to 85	44 Ld MQFP	Q44.10x10
ICM7211AMIM44	LCD	Code B	Microprocessor	Direct Drive	-40 to 85	44 Ld MQFP	Q44.10x10
ICM7212AMIPL	LED	Code B	Microprocessor	Common Anode	-40 to 85	40 Ld PDIP	E40.6

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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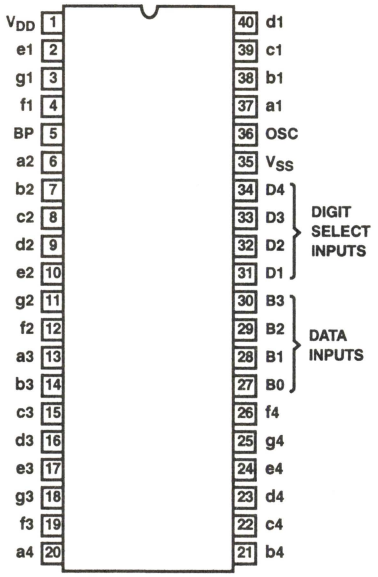
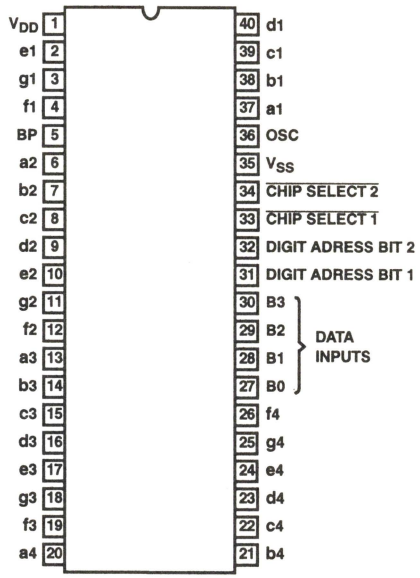
File Number **3158.1**

Pinouts

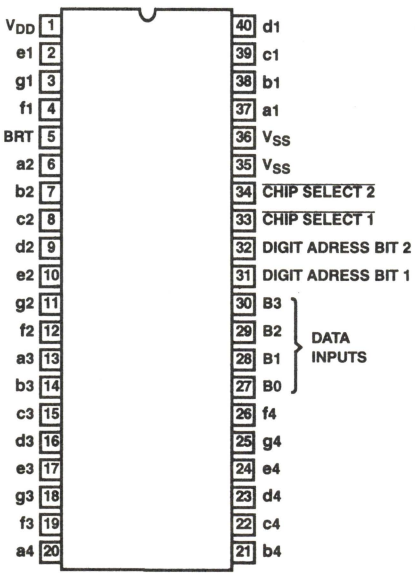
ICM7211, ICM7211A
(PDIP)
TOP VIEW



ICM7211M, ICM7211AM
(PDIP)
TOP VIEW

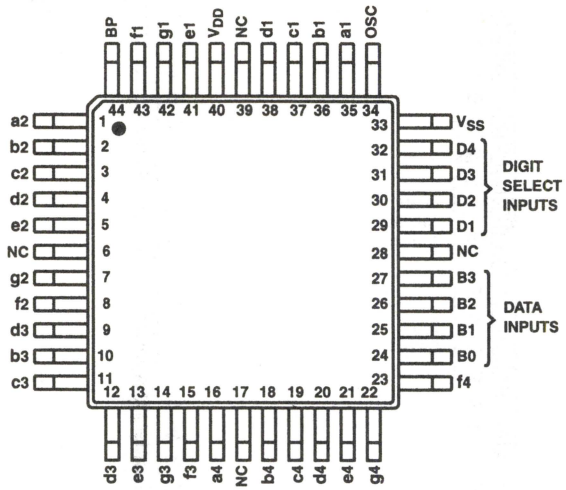


ICM7212AM
(PDIP)
TOP VIEW

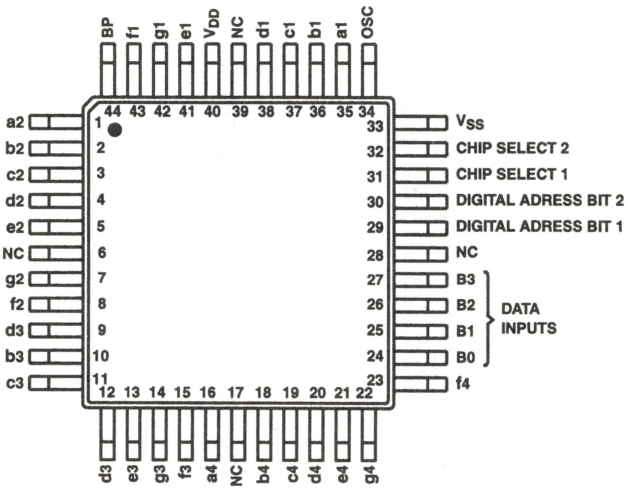


Pinouts (Continued)

ICM7211A
(MQFP)
TOP VIEW



ICM7211AM
(MQFP)
TOP VIEW



HARRIS SEMICONDUCTOR

ICM7213

One Second/One Minute Timebase Generator

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

Features

- **Guaranteed 2V Operation**
- **Very Low Current Consumption (Typ) . . . . 100μA at 3V**
- **All Outputs TTL Compatible**
- **On Chip Oscillator Feedback Resistor**
- **Oscillator Requires Only 3 External components: Fixed Capacitor, Trim Capacitor, and A Quartz Crystal**
- **Output Inhibit Function**
- **4 Simultaneous Outputs: One Pulse/s, One Pulse/Min, 16Hz and Composite 1024 + 16 + 2Hz Outputs**
- **Test Speed-Up Provides Other Frequency Outputs**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICM7213IPD	-25 to 85	14 Ld PDIP	E14.3

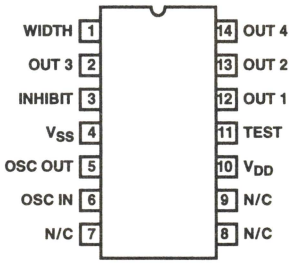
Description

The ICM7213 is a fully integrated micropower oscillator and frequency divider with four buffered outputs suitable for interfacing with most logic families. The power supply may be either a two battery stack (Ni-cad, alkaline, etc.) or a regular power supply greater than 2V. Depending upon the state of the WIDTH, INHIBIT, and TEST inputs, using a 4.194304MHz crystal will produce a variety of output frequencies including 2048Hz, 1024Hz, 34.133Hz, 16Hz, 1Hz, and $^1/_{60}$Hz (plus composites).

The ICM7213 utilizes a very high speed low power metal gate CMOS technology which uses 6.4V zeners between the drains and sources of each transistor and also across the supply terminals. Consequently, the ICM7213 is limited to a 6V maximum V_{SUPPLY}, although a simple dropping network can be used to extend the V_{SUPPLY} range well above 6V (See Figure 9).

Pinout

ICM7213
(PDIP)
TOP VIEW



9 COUNTERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3165.1**

HARRIS SEMICONDUCTOR

ICM7216A, ICM7216B, ICM7216D

8-Digit, Multi-Function, Frequency Counters/Timers

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

Features All Versions

- Functions as a Frequency Counter (DC to 10MHz)
- Four Internal Gate Times: 0.01s, 0.1s, 1s, 10s in Frequency Counter Mode
- Directly Drives Digits and Segments of Large Multiplexed LED Displays (Common Anode and Common Cathode Versions)
- Single Nominal 5V Supply Required
- Highly Stable Oscillator, Uses 1MHz or 10MHz Crystal
- Internally Generated Decimal Points, Interdigit Blanking, Leading Zero Blanking and Overflow Indication
- Display Off Mode Turns Off Display and Puts Chip Into Low Power Mode
- Hold and Reset Inputs for Additional Flexibility

Features ICM7216A and ICM7216B

- Functions Also as a Period Counter, Unit Counter, Frequency Ratio Counter or Time Interval Counter
- 1 Cycle, 10 Cycles, 100 Cycles, 1000 Cycles in Period, Frequency Ratio and Time Interval Modes
- Measures Period From 0.5μs to 10s

Features ICM7216D

- Decimal Point and Leading Zero Banking May Be Externally Selected.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICM7216AIJI	-25 to 85	28 Ld CERDIP	F28.6
ICM7216BIPI	-25 to 85	28 Ld PDIP	E28.6
ICM7216DIPI	-25 to 85	28 Ld PDIP	E28.6

Description

The ICM7216A and ICM7216B are fully integrated Timer Counters with LED display drivers. They combine a high frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexers and 8-segment and 8-digit drivers which directly drive large multiplexed LED displays. The counter inputs have a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7216A and ICM7216B can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10MHz or 1MHz quartz crystal timebase. For period and time interval, the 10MHz timebase gives a 0.1μs resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01s, 0.1s, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1Hz in the least significant digit. There is 0.2s between measurements in all ranges.

The ICM7216D functions as a frequency counter only, as described above.

All versions of the ICM7216 incorporate leading zero blanking. Frequency is displayed in kHz. In the ICM7216A and ICM7216B, time is displayed in μs. The display is multiplexed at 500Hz with a 12.2% duty cycle for each digit. The ICM7216A is designed for common anode displays with typical peak segment currents of 25mA. The ICM7216B and ICM7216D are designed for common cathode displays with typical peak segment currents of 12mA. In the display off mode, both digit and segment drivers are turned off, enabling the display to be used for other functions.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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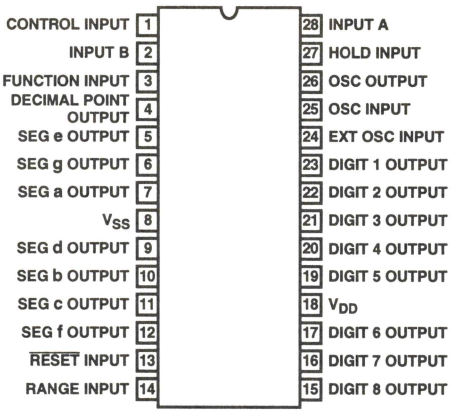
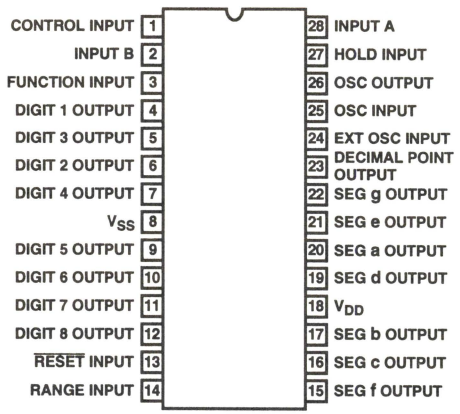
File Number **3166.1**

Pinouts

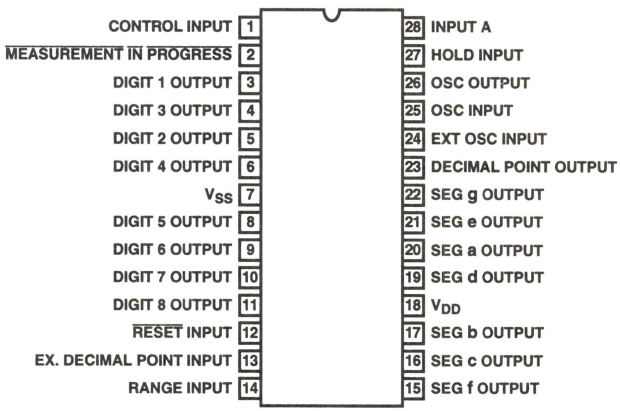
ICM7216A
COMMON ANODE
(CERDIP)
TOP VIEW



ICM7216B
COMMON CATHODE
(PDIP)
TOP VIEW



ICM7216D
COMMON CATHODE
(PDIP)
TOP VIEW



HARRIS SEMICONDUCTOR

ICM7217

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

4-Digit LED Display, Programmable Up/Down Counter

Features

- Four Decade, Presettable Up-Down Counter with Parallel Zero Detect
- Settable Register with Contents Continuously Compared to Counter
- Directly Drives Multiplexed 7 Segment Common Anode or Common Cathode LED Displays
- On-Board Multiplex Scan Oscillator
- Schmitt Trigger On Count Input
- TTL Compatible BCD I/O Port, Carry/Borrow, Equal, and Zero Outputs
- Display Blank Control for Lower Power Operation; Quiescent Power Dissipation <5mW
- All Terminals Fully Protected Against Static Discharge
- Single 5V Supply Operation

Description

The ICM7217 is a four digit, presettable up/down counter with an onboard presettable register continuously compared to the counter. The ICM7217 is intended for use in hard-wired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control.

This circuit provides multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to 0.8 inch character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeros can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

The ICM7217 (common anode) and ICM7217A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B (common anode) and ICM7217C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

This circuit provides 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters, a $\overline{\text{ZERO}}$ output, which indicates when the count is zero, and an $\overline{\text{EQUAL}}$ output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a three-state BCD I/O port. The CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$ outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2MHz, although the device will typically run with f_{IN} as high as 5MHz. Counting and comparing (EQUAL output) will typically run 750kHz maximum.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	DISPLAY DRIVER TYPE	COUNT OPTION/ MAX COUNT	PKG. NO.
ICM7217AIPI	-25 to 85	28 Ld PDIP	Common Cathode	Decade/9999	E28.6
ICM7217CIPI	-25 to 85	28 Ld PDIP	Common Cathode	Timing/5959	E28.6
ICM7217IJI	-25 to 85	28 Ld CERDIP	Common Anode	Decade/9999	F28.6
ICM7217BIJI	-25 to 85	28 Ld CERDIP	Common Anode	Timing/5959	F28.6

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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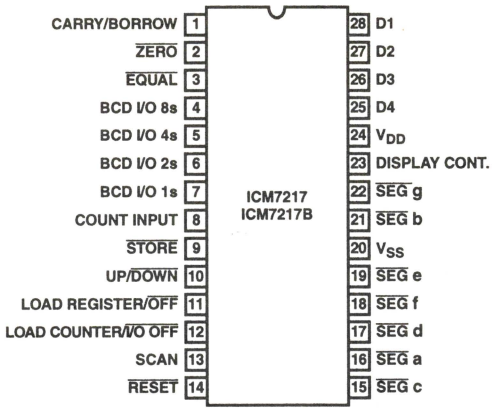
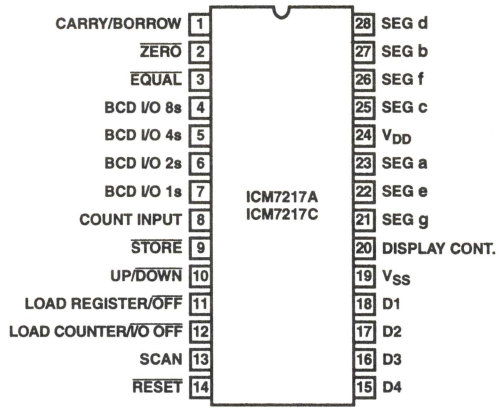
File Number **3167.1**

Pinouts

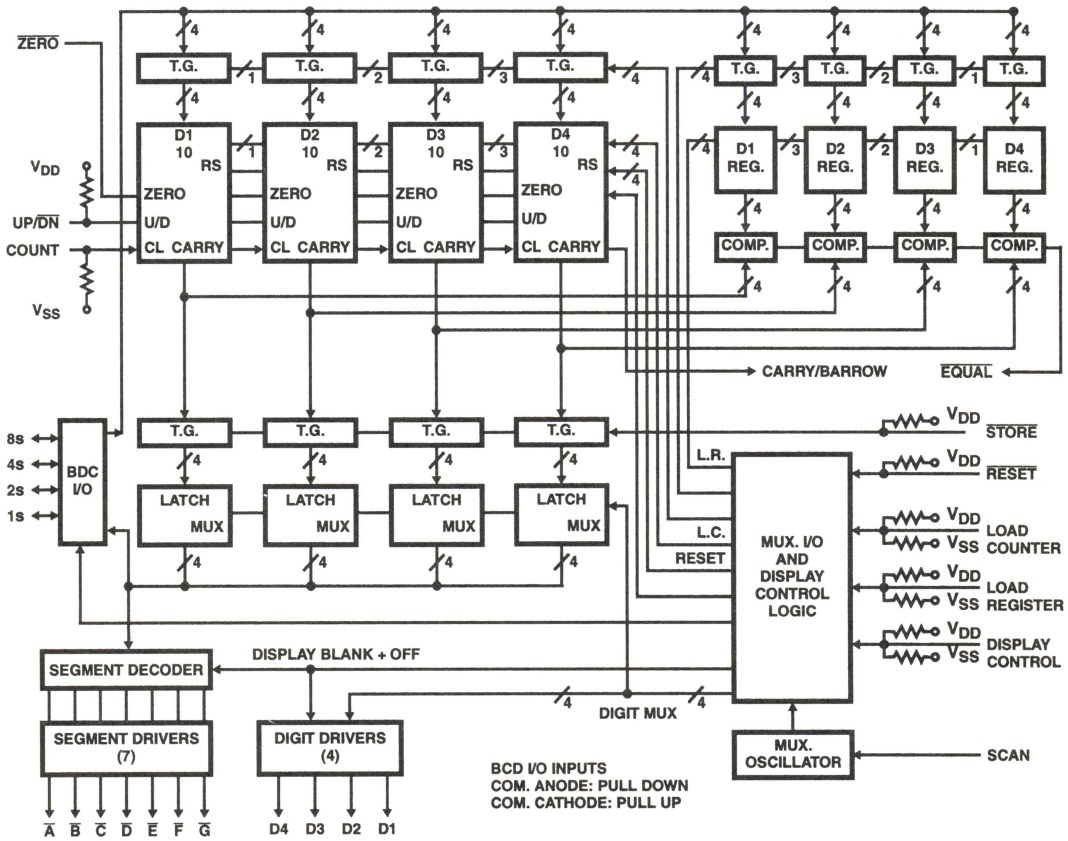
ICM7217 (PDIP)
COMMON ANODE
TOP VIEW



ICM7217 (CERDIP)
COMMON CATHODE
TOP VIEW



Functional Block Diagram



HARRIS SEMICONDUCTOR

ICM7224

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

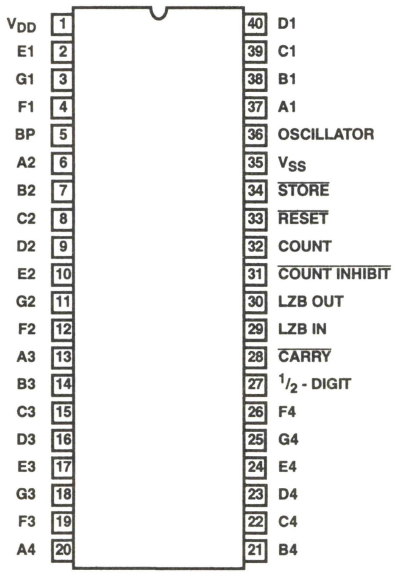
$4\frac{1}{2}$ Digit LCD Display Counter

Features

- High Frequency Counting - Guaranteed 15MHz, Typically 25MHz at 5V
- Low Power Operation - Typically Less Than 100µW Quiescent
- $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ Inputs Permit Operation as Frequency or Period Counter
- True $\overline{\text{COUNT INHIBIT}}$ Disables First Counter Stage
- $\overline{\text{CARRY}}$ Output for Cascading Four-Digit Blocks
- Schmitt-Trigger on the COUNT Input Allows Operation in Noisy Environments or with Slowly Changing Inputs
- Leading Zero Blanking INput and OUTput for Correct Leading Zero Blanking with Cascaded Devices
- Provides Complete Onboard Oscillator and Divider Chain to Generate Backplane Frequency, or Backplane Driver May be Disabled Allowing Segments to be Slaved to a Master Backplane Signal

Pinout

ICM7224
(PDIP)
TOP VIEW



Description

The ICM7224 device is a high-performance, CMOS $4\frac{1}{2}$ digit counter, including decoder, output latch, display driver, count inhibit, leading zero blanking, and reset circuitry.

The counter section provides direct static counting, guaranteed from DC to 15MHz, using a 5V ±10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25MHz. The COUNT input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. The COUNT INHIBIT, STORE and RESET inputs allow a direct interface with the ICM7207 and ICM7207A to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The $\overline{\text{CARRY}}$ output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allows correct Leading Zero Blanking between four-decade blocks. The BackPlane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, necessary when using an eight or twelve digit, single backplane display.

These devices provide maximum count of 19999. The display drivers are not of the multiplexed type and each display segment has its own individual drive pin, providing high quality display outputs.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICM7224IPL	-25 to 85	40 Ld PDIP	E40.6
ICM7224RIPL †	-25 to 85	40 Ld PDIP	E40.6

† "R" Indicates Device With Reversed Leads Configuration.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3168.1**

HARRIS SEMICONDUCTOR

ICM7226A, ICM7226B

8-Digit, Multi-Function, Frequency Counter/Timer

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

Features

- CMOS Design for Very Low Power
- Output Drivers Directly Drive Both Digits and Segments of Large 8-Digit LED Displays
- Measures Frequencies from DC to 10MHz; Periods from 0.5μs to 10s
- Stable High Frequency Oscillator uses either 1MHz or 10MHz Crystal
- Both Common Anode and Common Cathode Available
- Control Signals Available for External Systems Interfacing
- Multiplexed BCD Outputs

Applications

- Frequency Counter
- Period Counter
- Unit Counter
- Frequency Ratio Counter
- Time Interval Counter

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICM7226AIJL	-25 to 85	40 Ld CERDIP	F40.6
ICM7226BIPL	-25 to 85	40 Ld PDIP	E40.6

Description

The ICM7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexer and segment and digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7226 can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The devices require either a 10MHz or 1MHz quartz crystal timebase, or if desired an external timebase can also be used. For period and time interval, the 10MHz timebase gives a 0.1μs resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01s, 0.1s, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1Hz. There is 0.2s between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

Leading zero blanking has been incorporated with frequency display in kHz and time in μs. The display is multiplexed at a 500Hz rate with a 12.2% duty cycle for each digit. The ICM7226A is designed for common anode displays with typical peak segment currents of 25mA, and the ICM7226B is designed for common cathode displays with typical segment currents of 12mA. In the display off mode, both digit drivers and segment drivers are turned off, allowing the display to be used for other functions.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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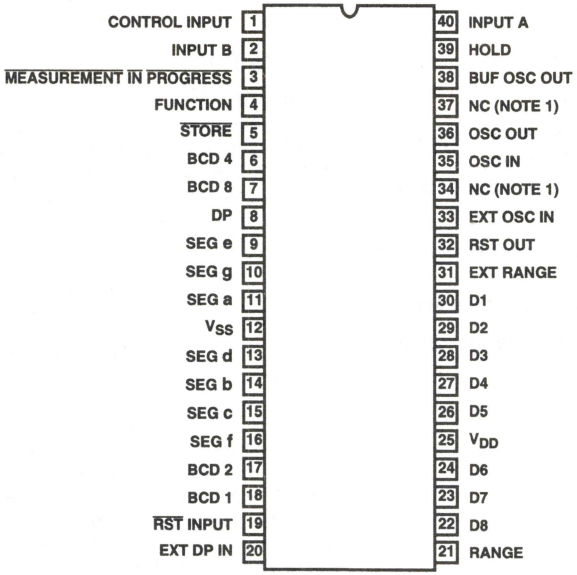
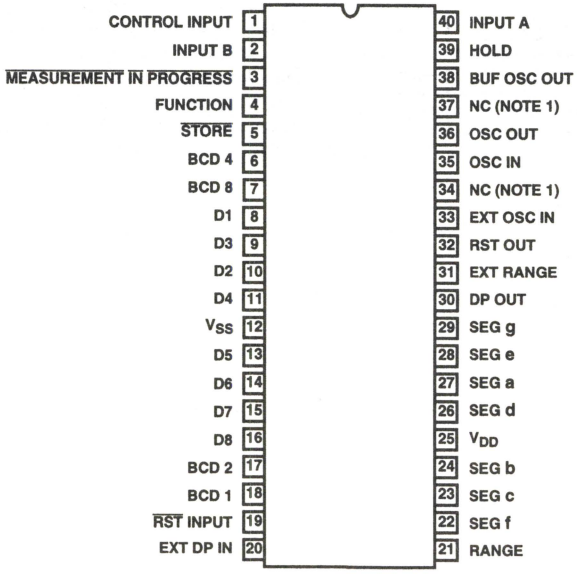
File Number **3169.1**

Pinouts

ICM7226A
COMMON ANODE (CERDIP)
TOP VIEW



ICM7226B
COMMON CATHODE (PDIP)
TOP VIEW



NOTE:

1. For maximum frequency stability, connect to V_{DD} or V_{SS}.

HARRIS SEMICONDUCTOR

ICM7228

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

8-Digit, Microprocessor-Compatible, LED Display Decoder Driver

Features

- Improved 2nd Source to Maxim ICM7218
- Fast Write Access Time of 200ns
- Multiple Microprocessor Compatible Versions
- Hexadecimal, Code B and No Decode Modes
- Individual Segment Control with "No Decode" Feature
- Digit and Segment Drivers On-Chip
- Non-Overlapping Digits Drive
- Common Anode and Common Cathode LED Versions
- Low Power CMOS Architecture
- Single 5V Supply

Applications

- Instrumentation
- Test Equipment
- Hand Held Instruments
- Bargraph Displays
- Numeric and Non-Numeric Panel Displays
- High and Low Temperature Environments where LCD Display Integrity is Compromised

Description

The Harris ICM7228 display driver interfaces microprocessors to an 8-digit, 7-segment, numeric LED display. Included on chip are two types of 7-segment decoder, multiplex scan circuitry, LED display segment drivers, LED display digit drivers and an 8-byte static memory as display RAM.

Data can be written to the ICM7228A and ICM7228B's display RAM in sequential 8-digit update or in single-digit update format. Data is written to the ICM7228C and ICM7228D display RAM in parallel random access format. The ICM7228A and ICM7228C drive common anode displays. The ICM7228B and ICM7228D drive common cathode displays. All versions can display the RAM data as either Hexadecimal or Code B format. The ICM7228A and ICM7228B incorporate a No Decode mode allowing each bit of each digit's RAM word to drive individual display segments resulting in independent control of all display segments. As a result, bargraph and other irregular display segments and formats can be driven directly by this chip.

The Harris ICM7228 is an alternative to both the Maxim ICM7218 and the Harris ICM7218 display drivers. Notice that the ICM7228A/B has an additional single digit access mode. This could make the Harris ICM7218A/B software incompatible with ICM7228A/B operation.

Ordering Information

PART NUMBER	DATA ENTRY PROTOCOL	DISPLAY TYPE	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICM7228AIPI	Sequential	Common Anode	-40 to 85	28 Ld PDIP	E28.6
ICM7228BIPI	Sequential	Common Cathode	-40 to 85	28 Ld PDIP	E28.6
ICM7228CIPI	Random	Common Anode	-40 to 85	28 Ld PDIP	E28.6
ICM7228DIPI	Random	Common Cathode	-40 to 85	28 Ld PDIP	E28.6
ICM7228AIJI	Sequential	Common Anode	-40 to 85	28 Ld CERDIP	F28.6
ICM7228BIJI	Sequential	Common Cathode	-40 to 85	28 Ld CERDIP	F28.6
ICM7228CIJI	Random	Common Anode	-40 to 85	28 Ld CERDIP	F28.6
ICM7228DIJI	Random	Common Cathode	-40 to 85	28 Ld CERDIP	F28.6
ICM7228AIBI	Sequential	Common Anode	-40 to 85	28 Ld SOIC	M28.3
ICM7228BIBI	Sequential	Common Cathode	-40 to 85	28 Ld SOIC	M28.3
ICM7228CIBI	Random	Common Anode	-40 to 85	28 Ld SOIC	M28.3
ICM7228DIBI	Random	Common Cathode	-40 to 85	28 Ld SOIC	M28.3
ICM7228AMJI883B	Sequential	Common Anode	-55 to 125	28 Ld CERDIP	F28.6
ICM7228BMJI883B	Sequential	Common Cathode	-55 to 125	28 Ld CERDIP	F28.6
ICM7228CMJI883B	Random	Common Anode	-55 to 125	28 Ld CERDIP	F28.6
ICM7228DMJI883B	Random	Common Cathode	-55 to 125	28 Ld CERDIP	F28.6

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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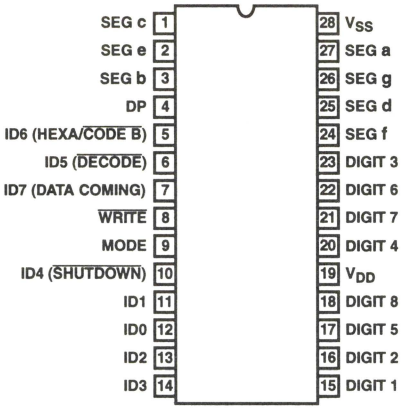
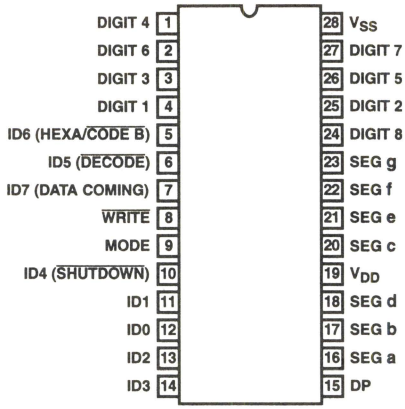
File Number **3160.1**

Pinouts

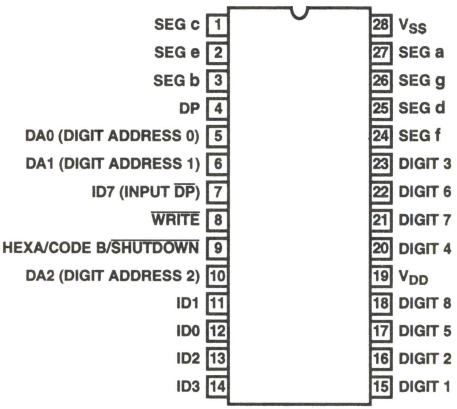
ICM7228A
(CERDIP, PDIP, SOIC)
COMMON ANODE
TOP VIEW



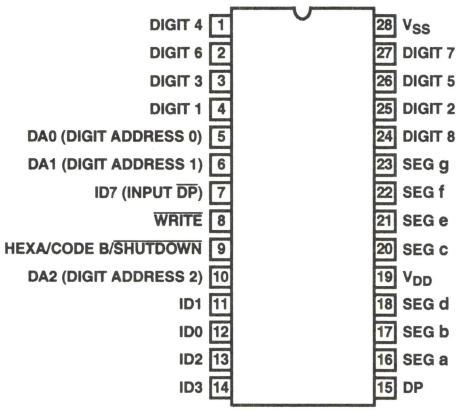
ICM7228B
(CERDIP, PDIP, SOIC)
COMMON CATHODE
TOP VIEW



ICM7228C
(CERDIP, PDIP, SOIC)
COMMON ANODE
TOP VIEW



ICM7228D
(CERDIP, PDIP, SOIC)
COMMON CATHODE
TOP VIEW



HARRIS SEMICONDUCTOR

ICM7231, ICM7232

August 1997

Complete data sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

Numeric/Alphanumeric Triplexed LCD Display Drivers

Features

- **ICM7231 Drives 8 Digits of 7 Segments with Two Independent Annunciators Per Digit Address and Data Input in Parallel Format**
- **ICM7232 Drives 10 Digits of 7 Segments with Two Independent Annunciators Per Digit Address and Data Input in Serial Format**
- **All Signals Required to Drive Rows and Columns of Triplexed LCD Display are Provided**
- **Display Voltage Independent of Power Supply**
- **On-Chip Oscillator Provides All Display Timing**
- **Total Power Consumption Typically 200μW, Maximum 500μW at 5V**
- **Low-Power Shutdown Mode Retains Data With 5μW Typical Power Consumption at 5V, 1μW at 2V**
- **Direct Interface to High-Speed Microprocessors**

Description

The ICM7231 and ICM7232 family of integrated circuits are designed to generate the voltage levels and switching waveforms required to drive triplexed liquid-crystal displays. These chips also include input buffer and digit address decoding circuitry allowing six bits of input data to be decoded into 64 independent combinations of the output segments of the selected digit.

The family is designed to interface to modern high-performance microprocessors and microcomputers and ease system requirements for ROM space and CPU time needed to service a display.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	NUMBER OF DIGITS	INPUT FORMAT	PKG. NO.
ICM7231BFIJL	-25 to 85	40 Ld CERDIP	8 Digit	Parallel	F40.6
ICM7231BFIPL	-25 to 85	40 Ld PDIP	8 Digit	Parallel	E40.6
ICM7232BFIPL	-25 to 85	40 Ld PDIP	10 Digit	Serial	E40.6
ICM7232CRIPL	-25 to 85	40 Ld PDIP	10 Digit	Serial	E40.6

NOTE:

All versions intended for triplexed LCD displays.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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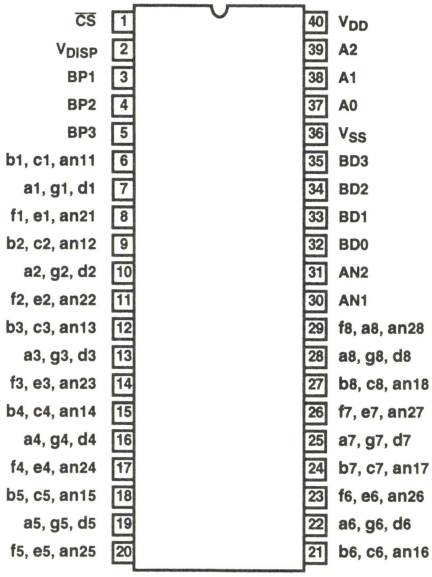
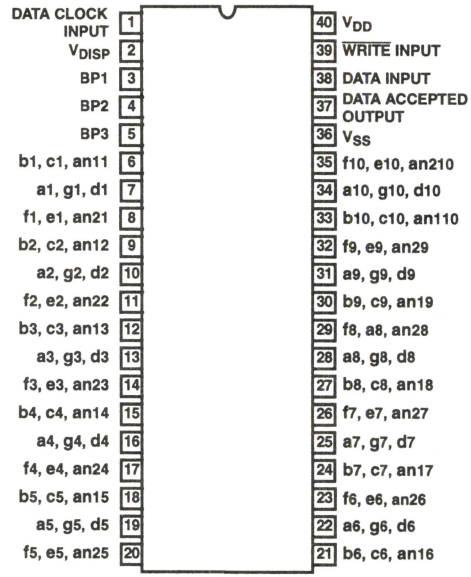
Pinouts

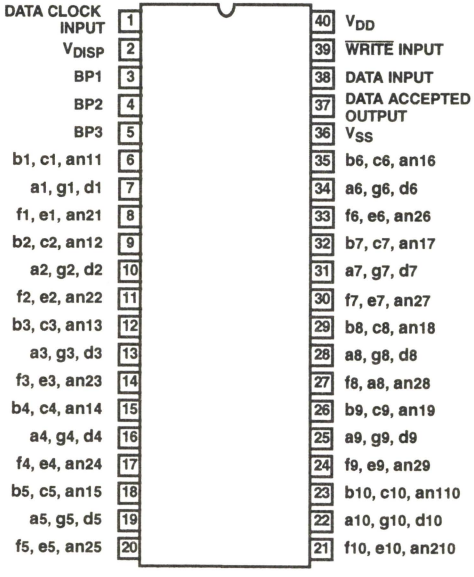
ICM7231BF
(PDIP, CERDIP)
TOP VIEW



ICM7232AF, BF
(PDIP, CERDIP)
TOP VIEW



ICM7232CR
(PDIP)
TOP VIEW



HARRIS SEMICONDUCTOR

ICM7243

Complete data sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

8-Character, Microprocessor-Compatible, LED Display Decoder Driver

Features

- **14-Segment and 16-Segment Fonts with Decimal Point**
- **Mask Programmable for Other Font-Sets Up to 64 Characters**
- **Microprocessor Compatible**
- **Directly Drives LED Common Cathode Displays**
- **Cascadable Without Additional Hardware**
- **Standby Feature Turns Display Off; Puts Chip in Low Power Mode**
- **Sequential Entry or Random Entry of Data Into Display**
- **Single +5V Operation**
- **Character and Segment Drivers, All MUX Scan Circuitry, 8 x 6 Static Memory and 64-Character ASCII Font Generator Included On-Chip**

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICM7243AIJL	-25^{o}C to 85	40 Ld CERPDIP	F40.6
ICM7243AIPL	-25^{o}C to 85	40 Ld PDIP	E40.6
ICM7243BIJL	-25^{o}C to 85	40 Ld CERPDIP	F40.6
ICM7243BIPL	-25 to 85	40 Ld PDIP	E40.6

Description

The ICM7243 is an 8-character, alphanumeric display driver and controller which provides all the circuitry required to interface a microprocessor or digital system to a 14-segment or 16-segment display. It is primarily intended for use in microprocessor systems, where it minimizes hardware and software overhead. Incorporated on-chip are a 64-character ASCII decoder, 8 x 6 memory, high power character and segment drivers, and the multiplex scan circuitry.

6-bit ASCII data to be displayed is written into the memory directly from the microprocessor data bus. Data location depends upon the selection of either **Sequential** (MODE = 1) or **Random** access mode (MODE = 0). In the **Sequential Access** mode the first entry is stored in the lowest location and displayed in the "left-most" character position. Each subsequent entry is automatically stored in the next higher location and displayed to the immediate "right" of the previous entry. A DISPlay FULL signal is provided after 8 entries; this signal can be used for cascading devices together. A $\overline{\text{CLeaR}}$ pin is provided to clear the memory and reset the location counter. The **Random Access** mode allows the processor to select the memory address and display digit for each input word.

The character multiplex scan runs whenever data is not being entered. It scans the memory and CHARacter drivers, and ensures that the decoding from memory to display is done in the proper sequence. Intercharacter blanking is provided to avoid display ghosting.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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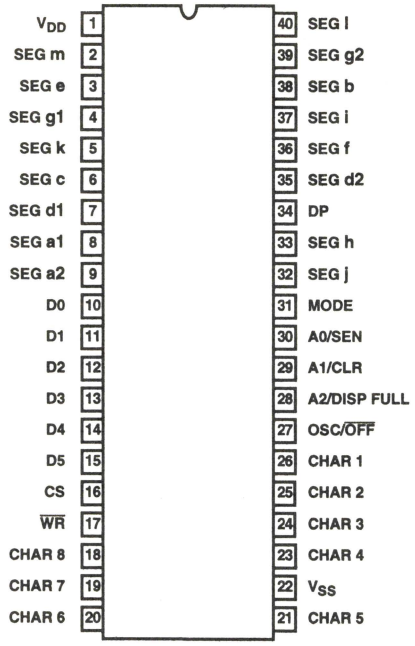
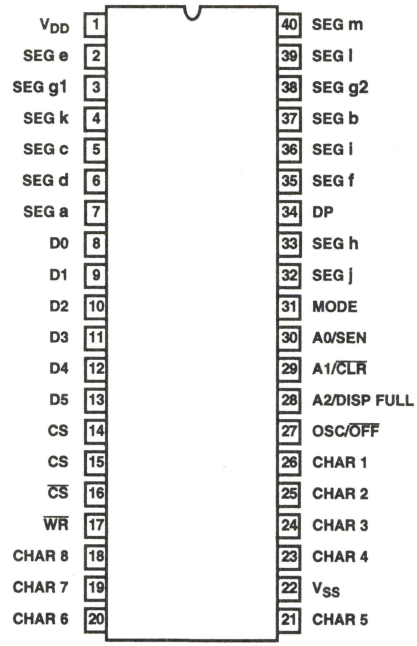
Pinouts

ICM7243A (16-SEGMENT CHARACTER)
(PDIP, CERDIP)
TOP VIEW



ICM7243B (14-SEGMENT CHARACTER)
(PDIP, CERDIP)
TOP VIEW



HARRIS SEMICONDUCTOR

ICM7249

$5^1/_2$ Digit LCD, Micro-Power Event/Hour Meter

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

Features

- Hour Meter Requires Only 4 Parts Total
- Micropower Operation: < 1µA at 2.8V (Typ)
- 10 Year Operation On One Lithium Cell. $2^1/_2$ Year Battery Life with Display Connected
- Directly Drives $5^1/_2$ Digit LCD
- 14 Programmable Modes of Operation
- Times Hrs., 0.1 Hrs., 0.01 Hrs., 0.1 Mins.
- Counts 1's, 10's, 100's, 1000's
- Dual Function Input Circuit
  - Selectable Debounce for Counter
  - High-Pass Filter for Timer
- Direct AC Line Triggering with Input Resistor
- Winking "Timer Active" Display Output
- Display Test Feature

Applications

- AC or DC Hour Meters
- AC or DC Totalizers
- Portable Battery Powered Equipment
- Long Range Service Meters

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
ICM7249IPM	-20 to 85	48 Ld PDIP	E48.6

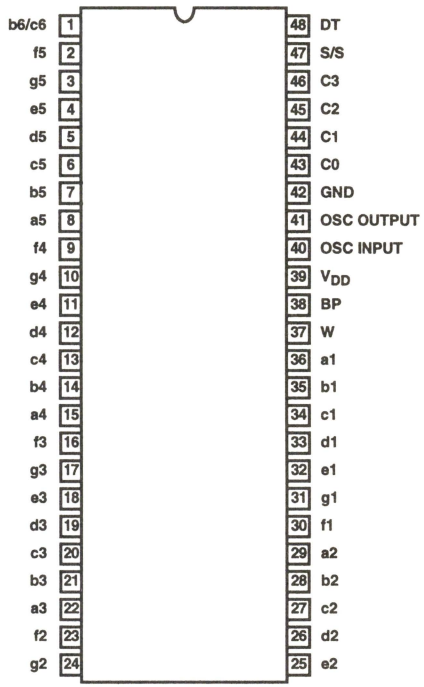
Description

The ICM7249 Timer/Counter is intended for long-term battery-supported industrial applications. The ICM7249 typically draws 1µA during active timing or counting, due to Harris' special low-power design techniques. This allows more than 10 years of continuous operation without battery replacement. The chip offers four timing modes, eight counting modes and four test modes.

The ICM7249 is a 48 lead device, powered by a single DC voltage source and controlled by a 32.768kHz quartz crystal. No other external components are required. Inputs to the chip are TTL-compatible and outputs drive standard direct drive LCD segments.

Pinout

ICM7249
(PDIP)
TOP VIEW



9 COUNTERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **3170.1**

DATA ACQUISITION 10

D/A CONVERTERS

Selection Guide 10-3

D/A Converter Data Sheets

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HI5731	12-Bit, 100 MSPS, High Speed D/A Converter	10-183
HI5735	12-Bit, 80 MSPS, High Speed Video D/A Converter	10-198
HI5741	14-Bit, 100 MSPS, High Speed D/A Converter	10-208
HI5760	10-Bit, 125 MSPS, High Speed D/A Converter	10-220
HI5780	10-Bit, 80 MSPS, High Speed, Low Power D/A Converter	10-227

8-BIT GENERAL PURPOSE D/A CONVERTERS

(NOTES 2, 3) DEVICE	SUFFIX CODES	INL (LSB)	DNL (LSB)	CONV. RATE	SETTLING TIME (μs)	TECH-NOLOGY	POWER SUPPLY (V)	MULTI-PLYING	OUTPUT I/V	INPUT BUFFER	TEMP. RANGE	V_{REF}	FEATURES
AD7523J	N	$\pm 1/2$	Monotonic	5	200 Max	CMOS-JI	+5V to +16V at 2.5mA (Excl I Ladder)	X	I	No	COM	External	Second Source, 3 Performance Grades, External Reference, Current Output
AD7523K		$\pm 1/4$											
AD7523L		$\pm 1/8$											

10-BIT GENERAL PURPOSE D/A CONVERTERS

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	INL (LSB)	CONV. RATE	SETTLING TIME (μs)	TECH-NOLOGY	POWER SUPPLY (V)	MULTI-PLYING	OUT-PUT I/V	INPUT BUFFER	TEMP. RANGE	V_{REF}	FEATURES
AD7520J	D		±2	2	500 Typ	CMOS-JI	+5V to +15V at 2mA (Excl I Ladder)	X	I	No	COM, MIL	External	Full Input Static Protection, Second Source, 3 Performance Grades, External Reference, Current Output
AD7520J	N		±2										
AD7520K	D		±1										
AD7520K	N		±1										
AD7520L	D		$\pm 1/2$										
AD7520L	N		$\pm 1/2$										
AD7520S	D	Y	±2										
AD7520T	D		±1										
AD7520U	D	Y	$\pm 1/2$										
AD7530J	N		±2	2	500 Typ	CMOS-JI	+5V to +15V at 2mA (Excl I Ladder)	X	I	No	COM, MIL	External	Full Input Static Protection, Full Input Static Protection, Second Source, 3 Performance Grades, External Reference, Current Output
AD7530K			±1										
AD7530L			$\pm 1/2$										
AD7533J	N		±2	1.25	800 Max	CMOS-JI	+5V to +15V at 2mA (Excl I Ladder)	X	I	No	COM	EXT	Full Input Static Protection, Second Source, Low Cost, External Reference, Current Output
AD7533K			±1										
AD7533L			$\pm 1/2$										

12-BIT GENERAL PURPOSE D/A CONVERTERS

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	INL (LSB)	DNL (LSB)	CONV. RATE	SETTLING TIME (µs)	TECH-NOLOGY	POWER SUPPLY (V)	MULTI-PLYING	OUT-PUT I/V	INPUT BUFFER	TEMP. RANGE	V_{REF}	FEATURES
HI3-DAC80V	-5		±1/2	±3/4		1.5 Max	Bipolar			V	No		INT	Low Cost, Internal Op Amp
HI3-DAC85V	-4		±1/2	±1/2										
HI1-565AJD	-5	Y	±1/2	±3/4	5	0.5 Typ	Bipolar-DI	±15 at +12mA/ -15mA		I	No	COM, MIL	INT	Industry Standard, DI Process, Internal Reference, Current Output
HI1-565AKD		Y	±1/4	±1/2										
HI1-565ASD	-2		±1/2	±3/4										
HI1-565ATD			±1/4	±1/2										
AD7521J	N		±8		2	0.5 Typ	CMOS-JI	+5V to +15V at 2mA (Excl I Ladder)	X	I	No	COM	EXT	12-Bit Versions of AD7520, AD7530
AD7521K			±4											
AD7521L			±2											
AD7531J	N		±8		2	0.5 Max	CMOS-JI	+5V to +15V at 2mA (Excl I Ladder)	X	I	No	COM	EXT	12-Bit Versions of AD7520, AD7530
AD7531K			±4											
AD7531L			±2											
AD7541J	N		±1		1	1.0 Max	CMOS-JI	+5V to +16V at 2mA (Excl I Ladder)	X	I	No	COM	EXT	Second Source, External Reference, Current Output
AD7541K			±1/2											
AD7541L			±1/2	Monotonic										
AD7545A	N		±2	±4.0	500	2.0 Max	CMOS-JI	+5V to +16V at 2mA (Excl I Ladder)	X	I	Yes	COM, MIL, IND	EXT	Second Source, External Reference, Current Output
AD7545B			±1	±1.0										
AD7545J			±2	±4.0										
AD7545K			±1	±1.0										

8-BIT HIGH SPEED D/A CONVERTERS

(NOTES 2, 3) DEVICE	SUFFIX CODES	INL (LSB)	DNL (LSB)	CONV. RATE (MHz)	SETTLING TIME (ns)	TECH-NOLOGY	POWER SUPPLY (V)	MULTI-PLYING	OUTPUT I/V	INPUT BUFFER	TEMP. RANGE	V_{REF}	FEATURES
HI20206	JCQ	±0.4	±0.5	3 x 35		Bipolar	+5			Yes	COM		Video DAC, 3 Channel , 3.3V
HI3338	KIP, KIB	±3/4	±1/2	50	20	CMOS	+5		V	Yes	IND	EXT	8-Bit Video Speed, Low Glitch

8-BIT HIGH SPEED D/A CONVERTERS (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	INL (LSB)	DNL (LSB)	CONV. RATE (MHz)	SETTLING TIME (ns)	TECH-NOLOGY	POWER SUPPLY (V)	MULTI-PLYING	OUTPUT I/V	INPUT BUFFER	TEMP. RANGE	V_{REF}	FEATURES
HI1171	JCB	±1.3	±1/4	40	25	CMOS	+5		I	Yes	COM	EXT	8-Bit Video Speed, Low Glitch, Low Power, Low Cost, 40 MSPS
HI20203	JCB, JCP	±1	±1/2	160	4.3	Bipolar	-5.2	Yes	I	Yes	COM	EXT	8-Bit 160MHz D/A with ECL Inputs,Low Glitch, Low Power
HI2304	JCQ	±2.5	±0.5	3 x 20		CMOS	+3.3	NO	I	Yes	COM	EXT	Video DAC, 3-chn
HI1260	JCQ	±1	±0.5	3 x 35			+5	NO	I	Yes	COM		3-chn, Video DAC
HI1106	JCP, JCB	±0.5	±0.5	35			+5	NO	I	Yes	COM		Video DAC, 2-chn
HI1177	JCQ	±0.5	±0.3	2 x 40			+5	NO	I	Yes	IND	EXT	Video DAC, 2-chn
HI1178	JCQ	±0.5	±0.3	3 x 40			+5	NO	I	Yes	IND	EXT	3-chn, Video DAC

10-BIT HIGH SPEED D/A CONVERTERS

(NOTES 2, 3) DEVICE	SUFFIX CODES	INL (LSB)	DNL (LSB)	CONV. RATE (MHz)	SETTLING TIME (ns)	TECH-NOLOGY	POWER SUPPLY (V)	MULTI-PLYING	OUT-PUT I/V	INPUT BUFFER	TEMP. RANGE	V_{REF}	FEATURES
HI5721	BIB BIP	±0.5	±0.5	125	4.5	BiCMOS	+5 / -5.2	Yes	I	Yes	IND	INT	10-Bit, 125MHz, Low Glitch, Low Power, TTL/CMOS Inputs, High Speed DAC for Communications Applications
HI20201	JCB, JCP	±1	±1/2	160	5.2 Typ	Bipolar	-5.2	Yes	I	Yes	COM	EXT	10-Bit 160MHz D/A with ECL Inputs, Low Glitch, Low Power
HI3050	JCQ	±2	±1/2	3 x 50		CMOS	+5		I	Yes	COM	EXT	Triple DAC, 50MHz
HI2307	JCQ	±2	±0.5	3 x 50			+5	NO	I	Yes	COM		3-chn, Video DAC
HI2309	JCQ	±2	±0.5	3 x 50			+5	NO	I	Yes	COM		3-chn, Video DAC
HI2315	JCQ	±1.5	±0.5	80			+5	NO	I	Yes	COM		Low Glitch Video DAC
HI5780	JCQ	±2.0	±0.5	80	6.0		+5	Yes	I	Yes	COM		Low Power 150mW
HI3197	JCQ	±0.5	±1.0	125	3.5	Bipolar	+5 or ±5						
HI5760	BIB	±1	±0.5	125		CMOS	+5 or +3	Yes	I	Yes	IND	INT	
HI5728	IQ	±1	±0.5	2 x 125		CMOS	+5 or +3	Yes	I	Yes	IND	INT	Dual D/A

12-BIT HIGH SPEED D/A CONVERTERS

(NOTES 2, 3) DEVICE	SUFFIX CODES	INL (LSB)	DNL (LSB)	CONV. RATE (MSPS)	SETTLING TIME (ns)	TECH-NOLOGY	POWER SUPPLY (V)	MULTI-PLYING	OUT-PUT I/V	INPUT BUFFER	TEMP. RANGE	V_{REF}	FEATURES
HI5731	BIB, BIP	1.5	±1.0	100	0.02	BiCMOS	5 and -5.2	Yes	I	Yes	IND	INT	Low Power, High Speed, Low Glitch, TTL/CMOS Input, High Speed DAC for Communications Applications
HI5735	KCP, KCB	1.5	±1.0	80	0.02	BiCMOS	5 and -5.2	Yes	I	Yes	COM	INT	Low Power, High Speed, TTL/CMOS Input, Low Glitch

14-BIT HIGH SPEED D/A CONVERTERS

(NOTES 2, 3) DEVICE	SUFFIX CODES	INL (LSB)	DNL (LSB)	CONV. RATE (MSPS)	SETTLING TIME (ns)	TECH-NOLOGY	POWER SUPPLY (V)	MULTI-PLYING	OUT-PUT I/V	INPUT BUFFER	TEMP. RANGE	V_{REF}	FEATURES
HI5741	BIB, BIP	1.5	±1.0	100	0.02	BiCMOS	5 and -5.2	Yes	I	Yes	IND	Internal	Low Power, High Speed, TTL/CMOS Input, Low Glitch, High Speed DAC for Communications Applications

HARRIS SEMICONDUCTOR

AD7520, AD7530
AD7521, AD7531

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

10-Bit, 12-Bit, Multiplying D/A Converters

Features

- **AD7520/AD7530, 10-Bit Resolution; 8-Bit, 9-Bit and 10-Bit Linearity**
- **AD7521/AD7531, 12-Bit Resolution; 8-Bit, 9-Bit and 10-Bit Linearity**
- **Low Power Dissipation (Max) 20mW**
- **Low Nonlinearity Tempco at 2ppm of FSR/°C**
- **Current Settling Time to 0.05% of FSR 1.0μs**
- **Supply Voltage Range . . . . . ±5V to +15V**
- **TTL/CMOS Compatible**
- **Full Input Static Protection**
- **/883B Processed Versions Available**

Description

The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). Harris' thin-film on CMOS processing gives up to 10-bit accuracy with TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

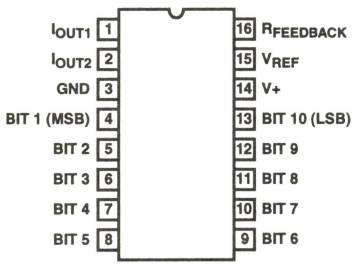
The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

Ordering Information

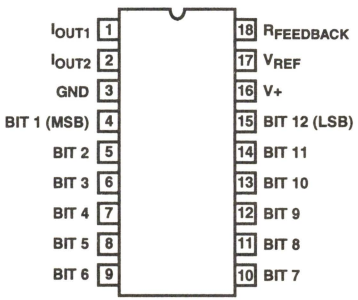
PART NUMBER	LINEARITY (INL, DNL)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
AD7520JN, AD7530JN	0.2% (8-Bit)	0 to 70	16 Ld PDIP	E16.3
AD7520KN, AD7530KN	0.1% (9-Bit)	0 to 70	16 Ld PDIP	E16.3
AD7521JN, AD7531JN	0.2% (8-Bit)	0 to 70	18 Ld PDIP	E18.3
AD7521KN, AD7531KN	0.1% (9-Bit)	0 to 70	18 Ld PDIP	E18.3
AD7520LN, AD7530LN	0.05% (10-Bit)	-40 to 85	16 Ld PDIP	E16.3
AD7521LN, AD7531LN	0.05% (10-Bit)	-40 to 85	18 Ld PDIP	E18.3
AD7520JD	0.2% (8-Bit)	-25 to 85	16 Ld CERDIP	F16.3
AD7520KD	0.1% (9-Bit)	-25 to 85	16 Ld CERDIP	F16.3
AD7520LD	0.05% (10-Bit)	-25 to 85	16 Ld CERDIP	F16.3
AD7520SD, AD7520SD/883B	0.2% (8-Bit)	-55 to 125	16 Ld CERDIP	F16.3
AD7520UD, AD7520UD/883B	0.05% (10-Bit)	-55 to 125	16 Ld CERDIP	F16.3

Pinouts

AD7520, AD7530
(CERDIP, PDIP)
TOP VIEW



AD7521, AD7531
(PDIP)
TOP VIEW



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File Number **3104.1**

AD7523, AD7533

HARRIS SEMICONDUCTOR

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

8-Bit, Multiplying D/A Converters

Features

- 8-Bit, 9-Bit and 10-Bit Linearity
- Low Gain and Linearity Temperature Coefficients
- Full Temperature Range Operation
- Static Discharge Input Protection
- TTL/CMOS Compatible
- Supply Range.....+5V to +15V
- Fast Settling Time at 25°C ..... 150ns (Max)
- Four Quadrant Multiplication
- AD7533 Direct AD7520 Equivalent

Description

The AD7523 and AD7533 are monolithic, low cost, high performance, 8-bit and 10-bit accurate, multiplying digital-to-analog converter (DAC), in a 16 pin DIP.

Harris' thin film resistors on CMOS circuitry provide 10-bit resolution (8-bit, 9-bit and 10-bit accuracy), with TTL/CMOS compatible operation.

The AD7523 and AD7533s accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND, and very low power dissipation make it a very versatile converter.

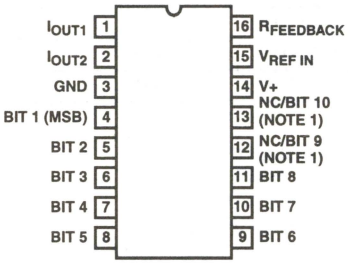
Low noise audio gain controls, motor speed controls, digitally controlled gain and digital attenuators are a few of the wide range of applications of the AD7523 and AD7533.

Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
AD7523JN, AD7533JN	0.2% (8-Bit)	0 to 70	16 Ld PDIP	E16.3
AD7523KN, AD7533KN	0.1% (9-Bit)	0 to 70	16 Ld PDIP	E16.3
AD7523LN, AD7533LN	0.05% (10-Bit)	0 to 70	16 Ld PDIP	E16.3

Pinout

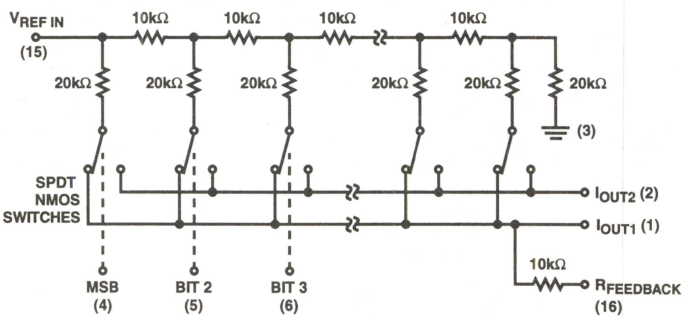
AD7523, AD7533
(PDIP)
TOP VIEW



NOTE:

1. NC for AD7523 only.

Functional Block Diagram



NOTE: Switches shown for digital inputs "High"

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HARRIS SEMICONDUCTOR

AD7541

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August 1997

12-Bit, Multiplying D/A Converter

Features

- 12-Bit Linearity 0.01%
- Pretrimmed Gain
- Low Gain and Linearity Tempcos
- Full Temperature Range Operation
- Full Input Static Protection
- TTL/CMOS Compatible
- +5V to +15V Supply Range
- 20mW Low Power Dissipation
- Current Settling Time 1µs to 0.01% of FSR
- Four Quadrant Multiplication

Description

The AD7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

Harris' wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V+ and ground, large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Harris AD7541.

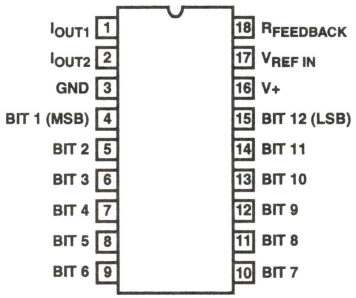
Pin compatible with AD7521, this DAC provides accurate four quadrant multiplication over the full military temperature range.

Ordering Information

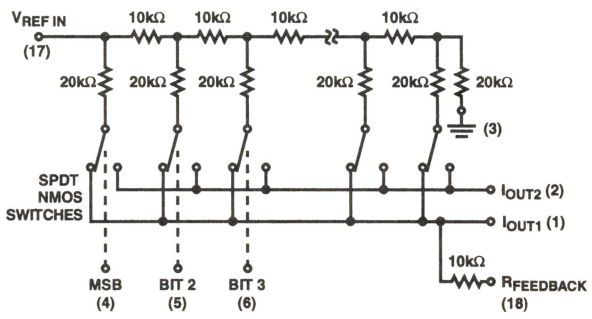
PART NUMBER	NONLINEARITY	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
AD7541JN	0.02% (11-Bit)	0 to 70	18 Ld PDIP	E18.3
AD7541KN	0.01% (12-Bit)	0 to 70	18 Ld PDIP	E18.3
AD7541LN	0.01% (12-Bit) Guaranteed Monotonic	0 to 70	18 Ld PDIP	E18.3

Pinout

AD7541
(PDIP)
TOP VIEW



Functional Block Diagram



NOTE: Switches shown for digital inputs "High".

10 D/A CONVERTERS

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HARRIS SEMICONDUCTOR

AD7545

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August 1997

12-Bit, Buffered, Multiplying CMOS DAC

Features

- 12-Bit Resolution
- Low Gain T.C. 2ppm/°C (Typ)
- Fast TTL/CMOS Compatible Data Latches
- Single +5V to +15V Supply
- Low Power
- Low Cost
- /883 Processed Versions Available

Description

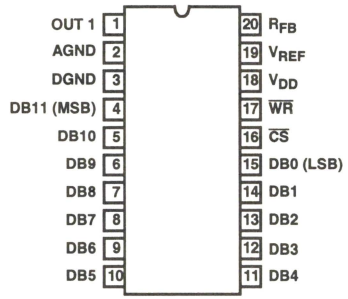
The AD7545 is a low cost monolithic 12-bit, CMOS multiplying DAC with on-board data latches. Data is loaded in a single 12-bit wide word which allows interfacing directly to most 12-bit and 16-bit bus systems. Loading of the input latches is under the control of the CS and WR inputs. A logic low on these control inputs makes the input latches transparent allowing direct unbuffered operation of the DAC.

Ordering Information

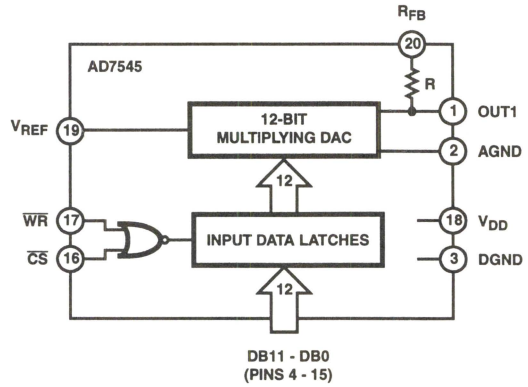
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
AD7545JN	0 to 70	20 Ld PDIP	E20.3
AD7545KN	0 to 70	20 Ld PDIP	E20.3
AD7545AN	-40 to 85	20 Ld PDIP	E20.3
AD7545BN	-40 to 85	20 Ld PDIP	E20.3

Pinout

AD7545
(PDIP)
TOP VIEW



Functional Diagram



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File Number **3108.1**

CA3338, CA3338A

HARRIS SEMICONDUCTOR

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

CMOS Video Speed, 8-Bit, 50 MSPS, R2R D/A Converters

Features

- CMOS/SOS Low Power
- R2R Output, Segmented for Low "Glitch"
- CMOS/TTL Compatible Inputs
- Fast Settling: (Typ) to $^1/_2$ LSB 20ns
- Feedthrough Latch for Clocked or Unclocked Use
- Accuracy (Typ) . . . . . ±0.5 LSB
- Data Complement Control
- High Update Rate (Typ) 50MHz
- Unipolar or Bipolar Operation

Applications

- TV/Video Display
- High Speed Oscilloscope Display
- Digital Waveform Generator
- Direct Digital Synthesis

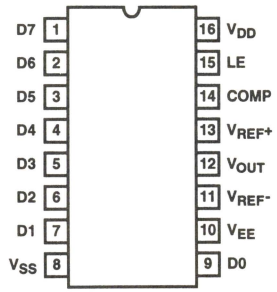
Description

The CA3338 family are CMOS/SOS high speed R2R voltage output digital-to-analog converters. They can operate from a single +5V supply, at video speeds, and can produce "rail-to-rail" output swings. Internal level shifters and a pin for an optional second supply provide for an output range below digital ground. The data complement control allows the inversion of input data while the latch enable control provides either feedthrough or latched operation. Both ends of the R2R ladder network are available externally and may be modulated for gain or offset adjustments. In addition, "glitch" energy has been kept very low by segmenting and thermometer encoding of the upper 3 bits.

The CA3338 is manufactured on a sapphire substrate to give low dynamic power dissipation, low output capacitance, and inherent latch-up resistance.

Pinout

CA3338, CA3338A
(PDIP, SBDIP, SOIC)
TOP VIEW



Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3338E	±1.0 LSB	-40 to 85	16 Ld PDIP	E16.3
CA3338AE	±0.75 LSB	-40 to 85	16 Ld PDIP	E16.3
CA3338D	±1.0 LSB	-55 to 125	16 Ld SBDIP	D16.3
CA3338AD	±0.75 LSB	-55 to 125	16 Ld SBDIP	D16.3
CA3338M	±1.0 LSB	-40 to 85	16 Ld SOIC	M16.3
CA3338AM	±0.75 LSB	-40 to 85	16 Ld SOIC	M16.3

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HARRIS SEMICONDUCTOR

HI-565A

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

High Speed, Monolithic D/A Converter with Reference

Features

- 12-Bit DAC and Reference on a Single Chip
- Pin Compatible With AD565A
- Very High Speed: Settles to ±0.5 LSB in 250ns (Max) Full Scale Switching Time 30ns (Typ)
- Guaranteed For Operation With ±12V Supplies
- Monotonicity Guaranteed Over Temperature
- Nonlinearity Guaranteed Over Temp (Max) . . ±0.5 LSB
- Low Gain Drift (Max, DAC Plus Ref) . . . . . 25ppm/°C
- Low Power Dissipation 250mW

Applications

- CRT Displays
- High Speed A/D Converters
- Signal Reconstruction
- Waveform Synthesis

Description

The HI-565A is a fast, 12-bit, current output, digital-to-analog converter. The monolithic chip includes a precision voltage reference, thin-film R2R ladder, reference control amplifier and twelve high speed bipolar current switches.

The Harris dielectric isolation process provides latch free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code dependent ground currents.

HI-565A dice are laser trimmed for a maximum integral non-linearity error of ±0.5 LSB at 25°C. In addition, the low noise buried zener reference is trimmed both for absolute value and temperature coefficient. Power dissipation is typically 250mW, with ±15V supplies.

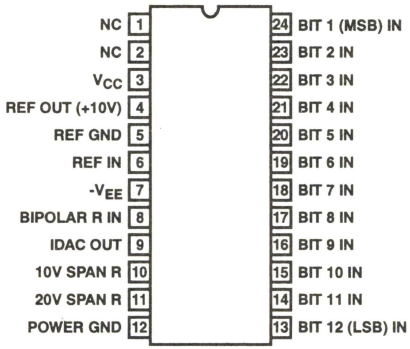
The HI-565A is offered in both commercial and military grades. See Ordering Information.

Ordering Information

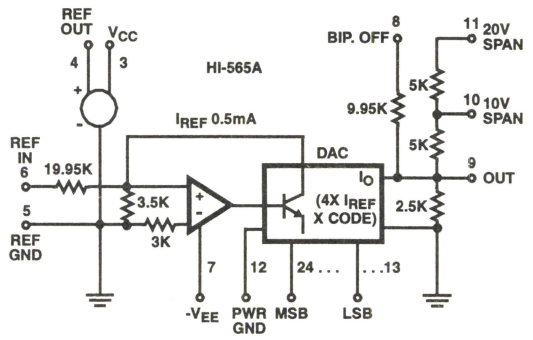
PART NUMBER	LINEARITY (INL)	LINEARITY (DNL)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-565AJD-5	0.50 LSB	0.75 LSB	0 to 75	24 Ld SBDIP	D24.6
HI1-565AKD-5	0.25 LSB	0.50 LSB	0 to 75	24 Ld SBDIP	D24.6
HI1-565ASD-2	0.50 LSB	0.75 LSB	-55 to 125	24 Ld SBDIP	D24.6
HI1-565ATD-2	0.25 LSB	0.50 LSB	-55 to 125	24 Ld SBDIP	D24.6
HI1-565ASD/883	0.50 LSB	0.50 LSB	-55 to 125	24 Ld SBDIP	D24.6
HI1-565ATD/883	0.25 LSB	0.50 LSB	-55 to 125	24 Ld SBDIP	D24.6

Pinout

HI-565A (SBDIP)
TOP VIEW



Functional Diagram



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HARRIS SEMICONDUCTOR

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HI-DAC80V, HI-DAC85V

August 1997

12-Bit, Low Cost, Monolithic D/A Converters

Features

- DAC 80V/DAC 85V Alternative Source
- Monolithic Construction
- Fast Settling Time (Typ) 1.5µs
- Guaranteed Monotonicity
- Wafer Laser Trimmed Linearity, Gain, Offset
- Span Resistors On-Chip
- On-Board Reference
- Supply Operation..... ±12V

Applications

- High Speed A/D Converters
- Precision Instrumentation
- CRT Display Generation

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3-DAC80V-5	0 to 75	24 Ld PDIP	E24.6
HI3-DAC85V-4	-25 to 85	24 Ld PDIP	E24.6

Description

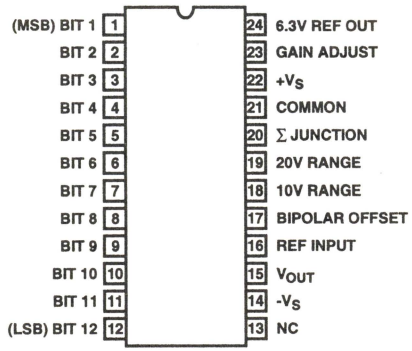
The HI-DAC80V is a monolithic direct replacement for the popular DAC80 and AD DAC80. The HI-DAC85V is a monolithic direct replacement for the popular DAC85 and AD DAC85 as well as the HI-5685V. Single chip construction along with several design innovations make the HI-DAC80V the optimum choice for low cost, high reliability applications. Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy.

Internally the HI-DAC80V/HI-DAC85V eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-DAC80V is available as a voltage output device which is guaranteed over the 0°C to 75°C temperature range. The HI-DAC85V is available as a voltage output device which is guaranteed over the -25°C to 85°C temperature range. It includes a buried zener reference featuring a low temperature coefficient as well as an on board operational amplifier. The HI-DAC80V requires only two power supplies and will operate in the range of ± (11.4V to 16.5V).

Pinout

HI-DAC80V/HI-DAC85V
(PDIP)
TOP VIEW



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HARRIS SEMICONDUCTOR

HI1106

8-Bit, 35 MSPS, High-Speed D/A Converter (TTL Input)

August 1997

Features

- Resolution 8-Bit
- High Speed Operation ..... 35MHz (Maximum Conversion Speed)
- Non-Linearity ..... Less Than $\pm 1/2$ LSB
- Low Glitch
- TTL Compatible Input
- Power Supply
  - Single ..... +5V
  - Dual ..... ±5V
- Low Power Consumption
  - +5V Single Power Supply (Typ) 200mW
  - ±5V Dual Power Supply (Typ) 400mW
- Direct Replacement for the Sony CXA1106

Description

The HI1106 is an 8-bit, 35MHz, high-speed D/A converter IC. Summing type current for the upper 2 bits and ladder type resistance for the lower 6 bits, ensures a low power consumption of 200mW (single power supply).

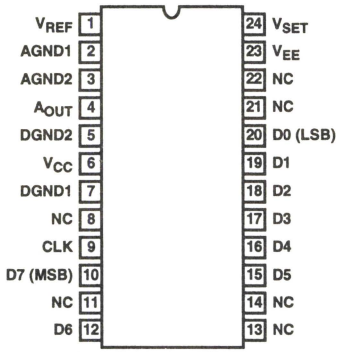
This IC is suitable for digital TVs, graphic displays and other applications.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1106JCB	-20 to 75	24 Ld SOIC	M24.2-S
HI1106JCP	-20 to 75	24 Ld PDIP	E24.4-S

Pinout

HI1106
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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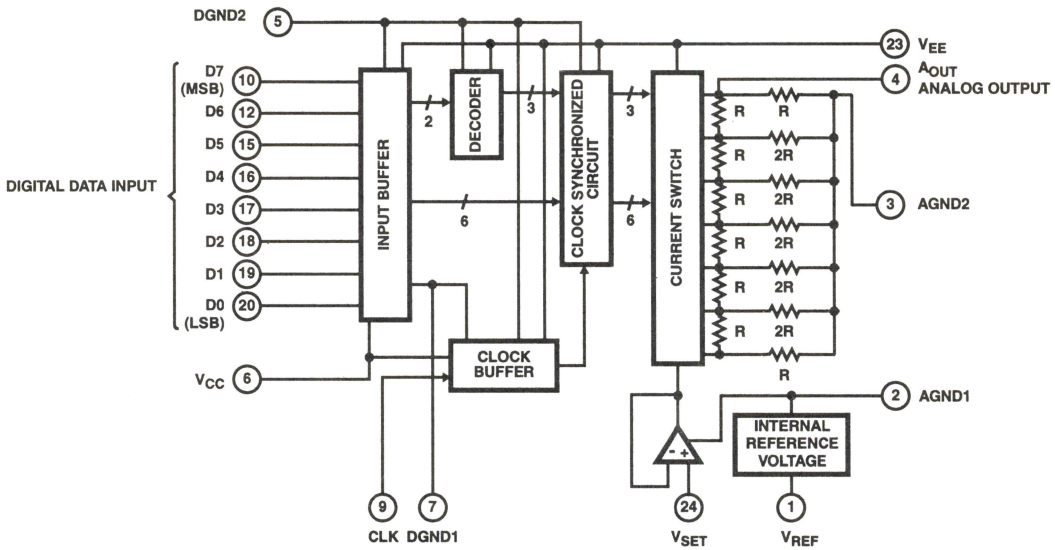
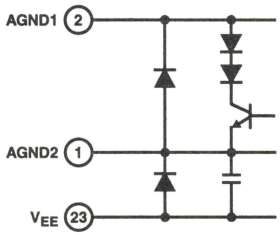
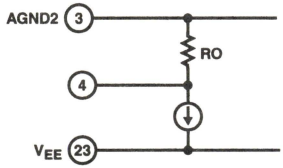
File Number **4113.2**

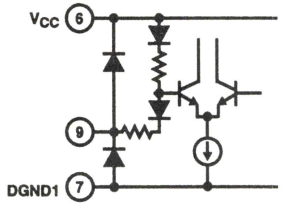
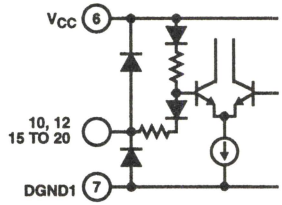
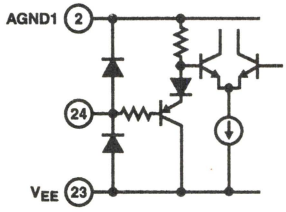
Functional Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1	V_{REF}		Internal Reference Voltage Output pin 1.2V (Typ). An external pull down resistance is necessary. For reference see Notes on Application 1.
2	AGND1		Set to Analog V_{CC} for signal power supply and to Analog GND for dual power supply. Connect to AGND2 and use.
3	AGND2		Connect to AGND1.
4	A_{OUT}		Analog Output pin.
5	DGND2		Set to Digital V_{CC} for signal power supply and to Digital GND for dual power supply.
6	V_{CC}		Digital V_{CC}.
7	DGND1		Digital GND.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
8	NC		No Connect.
9	CLK		Clock Input pin.
10, 12, 15 - 20	D7, D6, D5 - D0		Digital Input pin. D1 to MSB, D8 to LSB
11, 13, 14	NC		No Connect
21, 22	NC		Connect to AGND or V_{EE}.
23	V_{EE}		Set to Analog GND for single power supply and to V_{EE} for dual power supply.
24	V_{SET}		Bias Input pin. Normally set V_{SET} - V_{EE} to 0.84V. For reference see Notes on Application 1.

NOTE: See the Application Circuit for reference.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage
- V_{CC} - $DGND_1$ ..... .0V to 6V
- V_{EE} - AGND1, AGND2 ..... -6V to 0V
- DGND2 - DGND1 ..... .0V to 6V

Digital Input Voltage
- V_I ..... DGND1 - 0.3V to V_{CC} + 0.3V
- V_{CLK} ..... DGND1 - 0.3V to V_{CC} + 0.3V

Input Voltage (V_{SET} Pin), V_{SET} ..... V_{EE} - 0.3V to V_{EE} + 2.7V

Output Current (V_{REF} Pin), I_{REF} ..... -5mA to 0mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	90
SOIC Package	90

Maximum Power Dissipation, P_D 1.27W

Maximum Junction Temperature (Plastic Package) ..... 150^oC

Maximum Storage Temperature Range, T_{STG} .... -55^oC to 150^oC

Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(SOIC - Lead Tips Only)

Recommended Operating Conditions

SINGLE POWER SUPPLY	MIN	TYP	MAX
Supply Voltage			
V_{CC}, DGND2, AGND1, AGND2	4.75V	5V	5.25V
DGND2 - AGND1, DGND2 - AGND2	-0.2V	0V	0.2V
AGND1 - AGND2	-0.1V	0V	0.1V
Digital Input Voltage			
H Level, V_{IH}, V_{CLKH}	2.0V	-	V_{CC}
L Level, V_{IL}, V_{CLKL}	DGND1	-	1V
V_{SET} Input Voltage, V_{SET}	0.70V	0.84V	1V
V_{REF} Pin Current, I_{REF}	-3.0mA	-	-0.4mA
Clock Pulse Width (Note 1)			
t_{PW1}	10ns	-	-
t_{PW0}	10ns	-	-
Temperature Range, T_{OPR}	-20^oC to 75^oC		

DUAL POWER SUPPLY	MIN	TYP	MAX
Supply Voltage			
V_{CC}	4.75V	5V	5.25V
V_{EE}	-5.5V	5V	-4.75V
DGND2 - AGND1, DGND2 - AGND2	-0.2V	0V	-0.2V
AGND1 - AGND2	-0.1V	0V	0.1V
Digital Input Voltage			
H Level, V_{IH}, V_{CLKH}	2.0V	-	V_{CC}
L Level, V_{IL}, V_{CLKL}	DGND1	-	1V
V_{SET} Input Voltage, V_{SET}	-4.30V	-4.16V	-4.00V
V_{REF} Pin Current, I_{REF}	-3mA	-	-0.4mA
Clock Pulse Width			
t_{PW1}	10ns	-	-
t_{PW0}	10ns	-	-

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. See Figure 6 in the Timing Diagram.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, V_{CC} = DGND2 = AGND1 = AGND2 = 5V, DGND1 = V_{EE} = 0V, V_{SET} = 0.84V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINGLE POWER SUPPLY					
Resolution, n		-	8	-	Bit
Maximum Conversion Speed, f_{MAX}	$R_L > 10k\Omega$, $C_L < 20pF$	35	-	-	MHz
Linearity Error, EL	$R_L > 10k\Omega$	-0.5	-	0.5	LSB
Differential Linearity Error, ED		-0.5	-	0.5	LSB
Full Scale Output Voltage, V_{FS}	$R_L > 10k\Omega$	0.9	1.0	1.1	V
Offset Voltage (Note 2), V_{OS}	$R_L > 10k\Omega$	0	4	10	mV
Output Resistance, R_O		290	350	410	Ω
Power Supply Current, I_{CC}	$R_L > 10k\Omega$, $I_{REF} = -400\mu A$	32	40	48	mA
Digital Input Current					
H Level, I_{IH}		0	-	5	µA
L Level, I_{IL}		-400	-	0	µA
V_{SET} Input Current, I_{SET}		-3	-	0	µA
Internal Reference Output Voltage, V_{REF}	$I_{REF} = -400\mu A$	1.17	1.25	1.33	V
Accuracy Output Voltage Range, V_{OC}	$R_L > 10k\Omega$	0.5	1.0	1.50	V
Set-Up Time, t_S		10	-	-	ns
Hold Time, t_H		2	-	-	ns
Propagation Delay Time, t_{PD}	$R_L > 10k\Omega$	-	11	-	ns
Glitch Energy, GE	$R_L > 10k\Omega$, f_{CLK} = 1MHz, Digital Lamp Output	-	30	-	pV/s

NOTE:

3. V_{OS} = AGND2 - V255 (V255 is the output voltage when full input is at high level).

Electrical Specifications $T_A = 25^oC$, $V_{CC} = 5V$, DGND1 = DGND2 = AGND1 = AGND2 = 0V, $V_{EE} = -5V$, $V_{SET} - V_{EE} = 0.84V$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DUAL POWER SUPPLY					
Resolution, n		-	8	-	Bit
Maximum Conversion Speed, f_{MAX}	$R_L > 10k\Omega$, $C_L < 20pF$	35	-	-	MHz
Linearity Error, EL	$R_L > 10k\Omega$	-0.5	-	0.5	LSB
Differential Linearity Error, DNL		-0.5	-	0.5	LSB
Full Scale Output Voltage, V_{FS}	$R_L > 10k\Omega$	0.9	1.0	1.1	V
Offset Voltage, V_{OS}	$R_L > 10k\Omega$	0	4	10	mV
Output Resistance, R_O		290	350	410	Ω
Power Supply Current					
I_{CC}	$R_L > 10k\Omega$, $I_{REF} = -400\mu A$	24	30	36	mA
I_{EE}		40	50	60	mA
Digital Input Current					
H Level, I_{IH}		0	-	5	µA
L Level, I_{IL}		-400	-	0	µA
V_{SET} Input Current, I_{SET}		-3	-	0	µA
Internal Reference Output Voltage, V_{REF}	$I_{REF} = -400\mu A$	-3.83	-3.75	-3.67	V
Accuracy Output Voltage Range, V_{OC}	$R_L > 10k\Omega$	0.5	1.0	1.50	V
Set-Up Time, t_S		10	-	-	ns
Hold Time, t_H		2	-	-	ns
Propagation Delay Time, t_{PD}	$R_L > 10k\Omega$	-	11	-	ns
Glitch Energy, GE	$R_L > 10k\Omega$, f_{CLK} = 1MHz Digital Lamp Output	-	30	-	pV/s

INPUT/OUTPUT CODE TABLE
(When Output Full Scale Voltage at 1.00V)

INPUT CODE								OUTPUT VOLTAGE (SINGLE SUPPLY)	OUTPUT VOLTAGE (DUAL SUPPLY)
MSB							LSB		
1	1	1	1	1	1	1	1	V_{CC}	-0V
1	0	0	0	0	0	0	0	V_{CC} -0.5V	-0.5V
0	0	0	0	0	0	0	0	V_{CC} -1V	-1V

Test Circuits

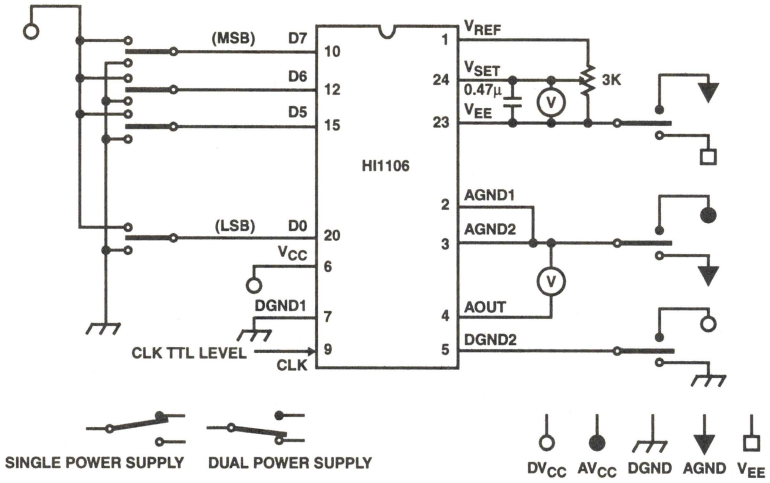


FIGURE 1. DC CHARACTERISTICS

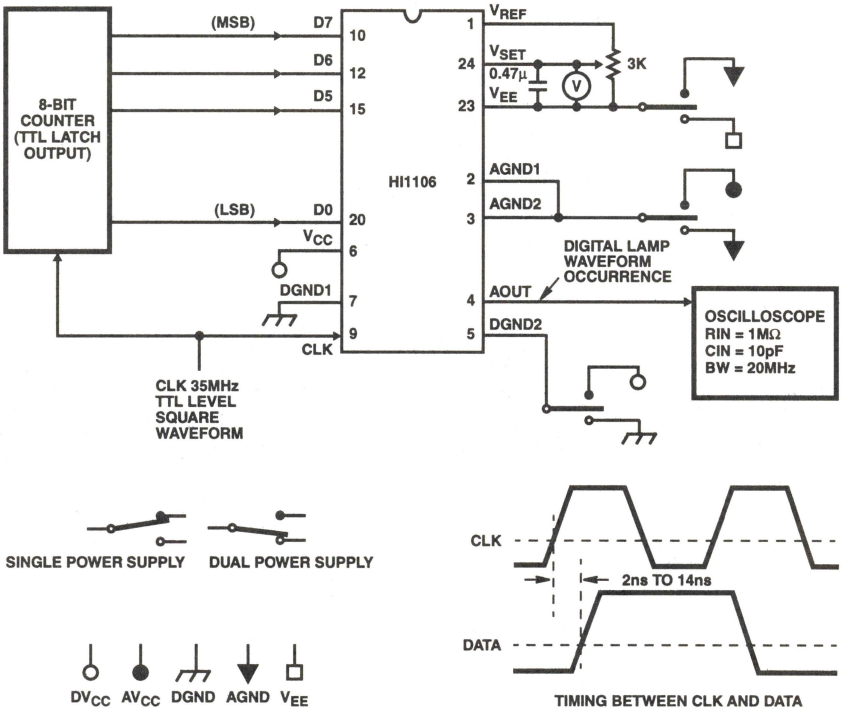


FIGURE 2. MAXIMUM CONVERSION SPEED

Test Circuits (Continued)

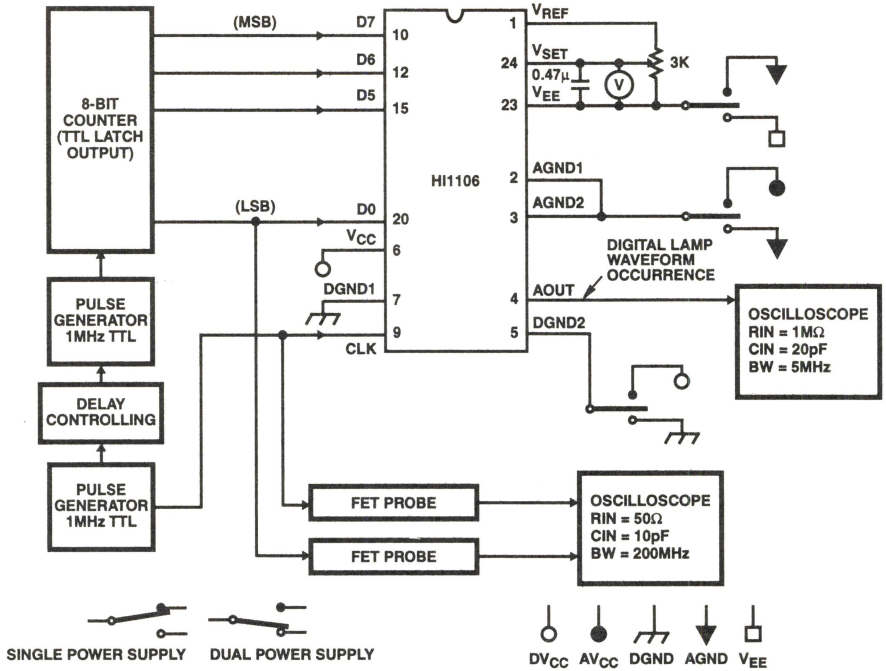


FIGURE 3. SET-UP TIME AND HOLD TIME

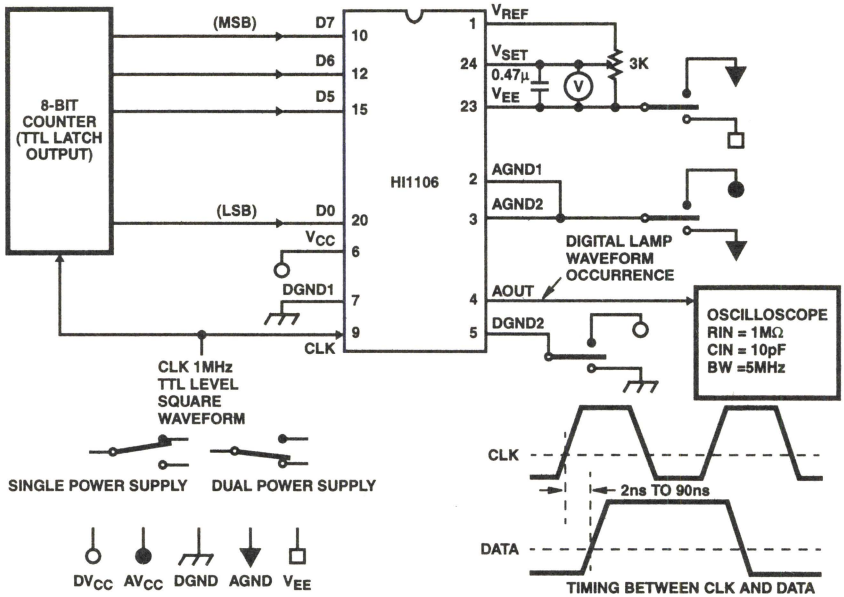


FIGURE 4. GLITCH AREA

Test Circuits (Continued)

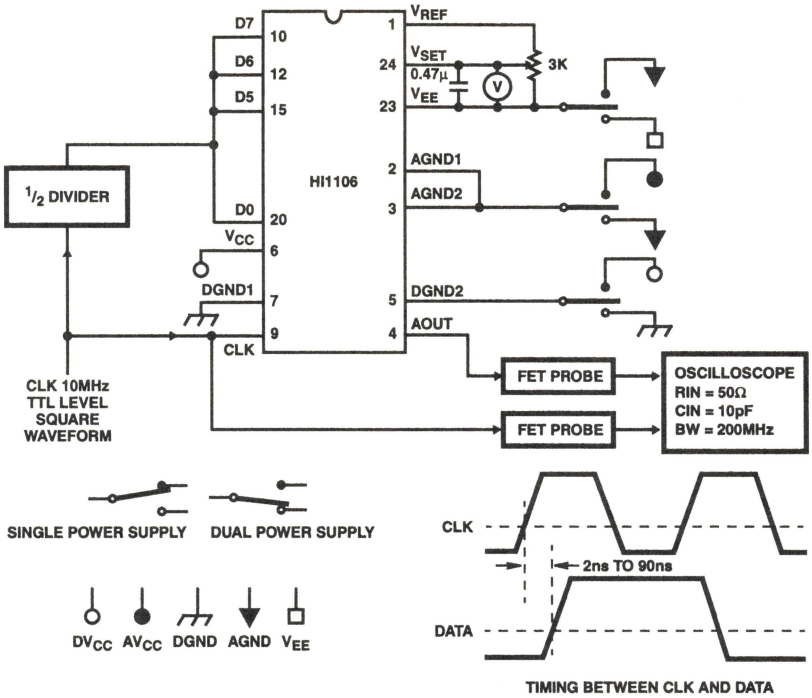


FIGURE 5. PROPAGATION DELAY TIME

Timing Diagram

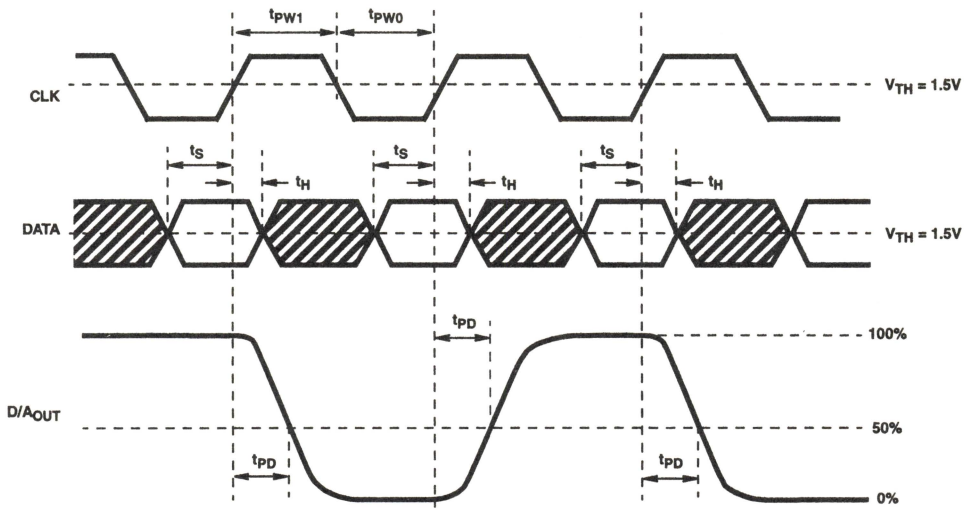


FIGURE 6.

Typical Performance Curves

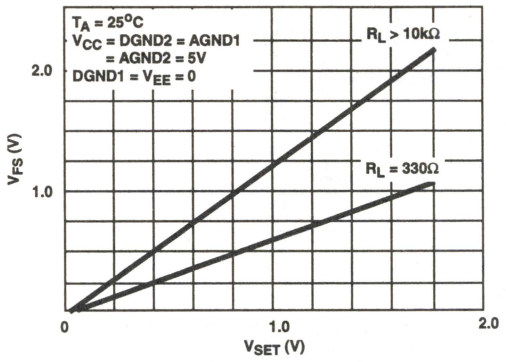


FIGURE 7. FULL-SCALE OUTPUT VOLTAGE (V_{FS}) vs V_{SET} (SINGLE POWER SUPPLY)

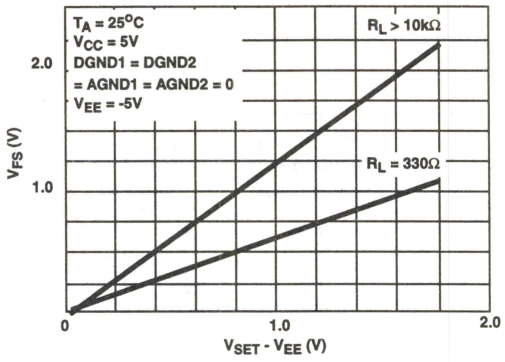


FIGURE 8. FULL-SCALE OUTPUT VOLTAGE (V_{FS}) vs V_{SET} - V_{EE} (DUAL POWER SUPPLY)

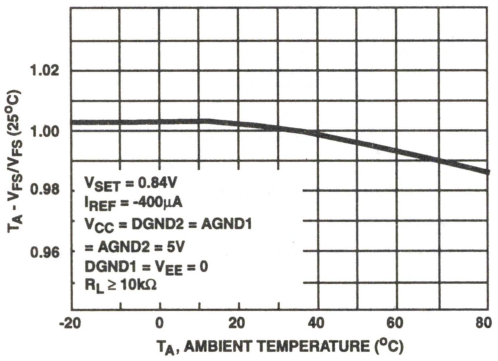


FIGURE 9. FULL-SCALE OUTPUT VOLTAGE (V_{FS}) vs TEMPERATURE (SINGLE POWER SUPPLY)

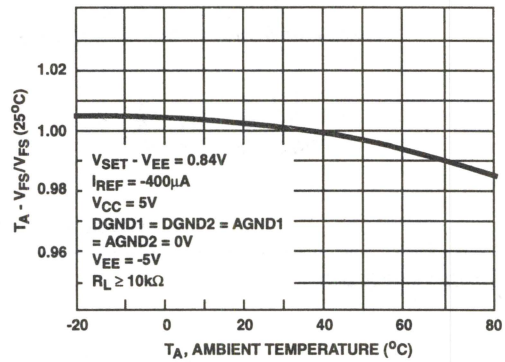


FIGURE 10. FULL-SCALE OUTPUT VOLTAGE (V_{FS}) vs TEMPERATURE (DUAL POWER SUPPLY)

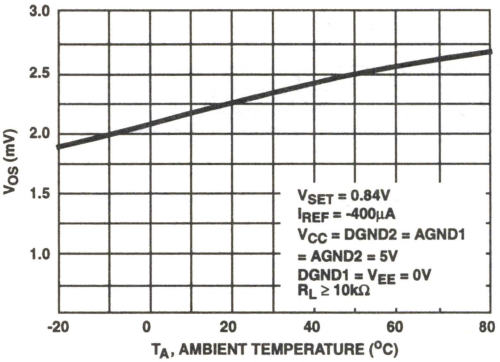


FIGURE 11. OUTPUT OFFSET VOLTAGE (V_{OS}) vs TEMPERATURE (SINGLE POWER SUPPLY)

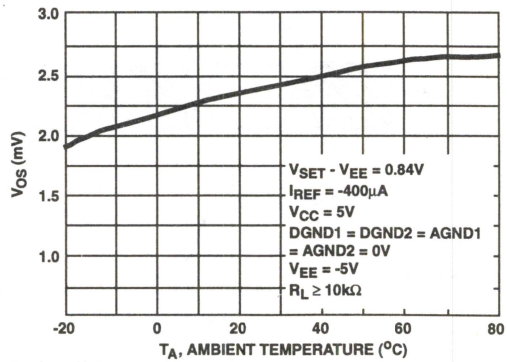


FIGURE 12. OUTPUT OFFSET VOLTAGE (V_{OS}) vs TEMPERATURE (DUAL POWER SUPPLY)

Typical Performance Curves (Continued)

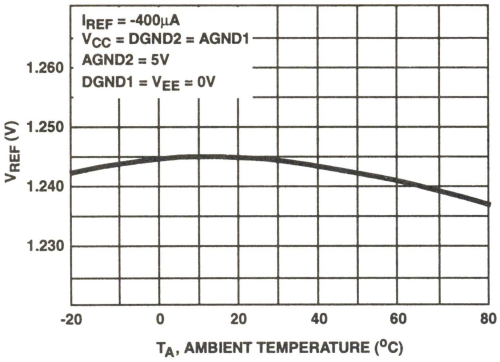


FIGURE 13. INTERNAL REFERENCE VOLTAGE (V_{REF}) vs TEMPERATURE (SINGLE POWER SUPPLY)

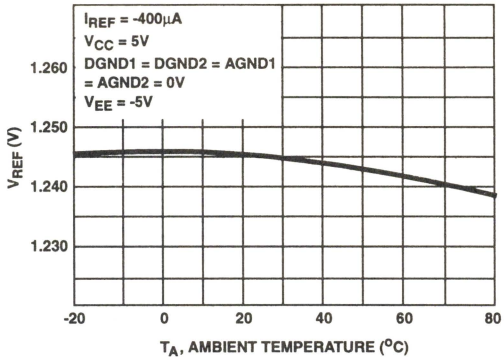


FIGURE 14. INTERNAL REFERENCE VOLTAGE (V_{REF}) vs TEMPERATURE (DUAL POWER SUPPLY)

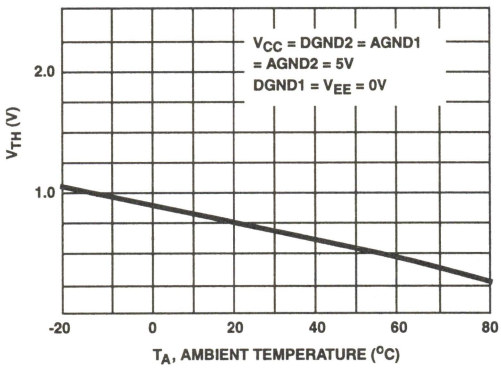


FIGURE 15. THRESHOLD VOLTAGE (V_{TH}) OF DIGITAL INPUT vs TEMPERATURE (SINGLE POWER SUPPLY)

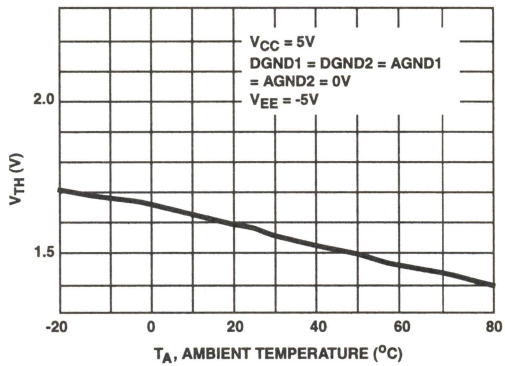


FIGURE 16. THRESHOLD VOLTAGE (V_{TH}) OF DIGITAL INPUT vs TEMPERATURE (DUAL POWER SUPPLY)

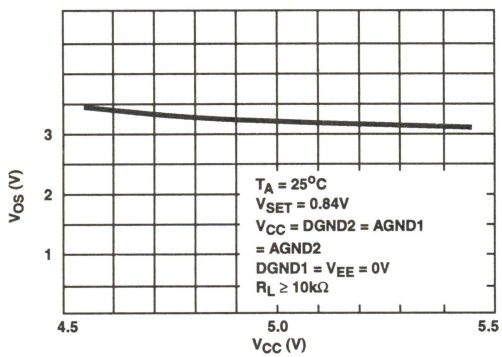


FIGURE 17. OUTPUT OFFSET VOLTAGE (V_{OS}) vs SUPPLY VOLTAGE (SINGLE POWER SUPPLY)

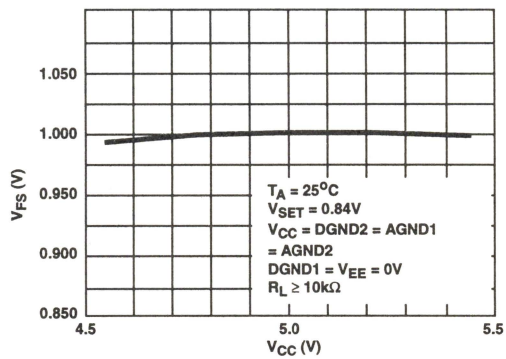


FIGURE 18. OUTPUT FULL-SCALE VOLTAGE (V_{FS}) vs SUPPLY VOLTAGE (DUAL POWER SUPPLY)

Typical Performance Curves (Continued)

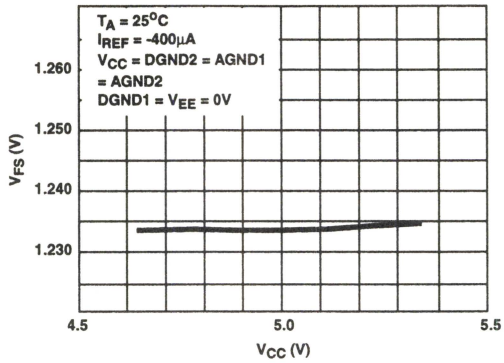


FIGURE 19. INTERNAL REFERENCE VOLTAGE (V_{REF}) vs SUPPLY VOLTAGE (SINGLE POWER SUPPLY)

Application Circuits

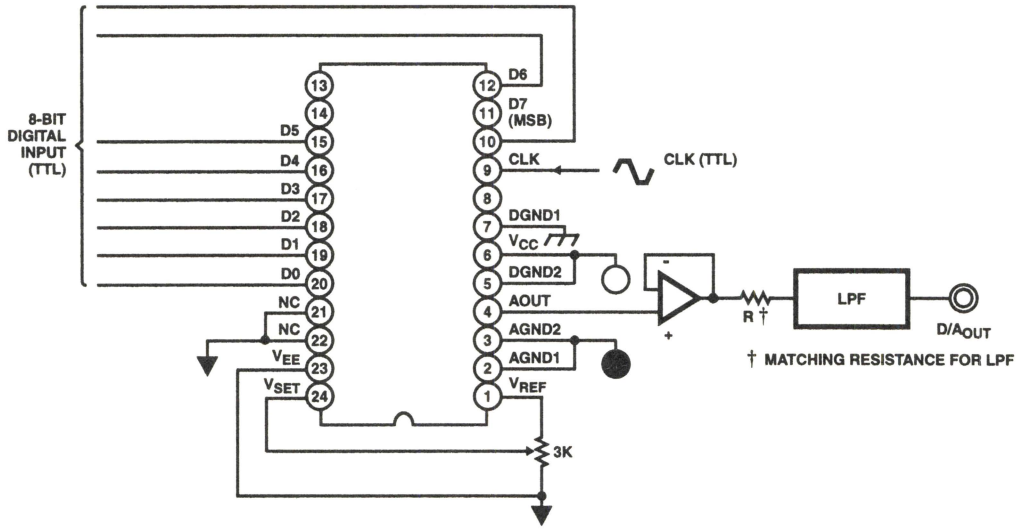


FIGURE 20. SINGLE POWER SUPPLY

Application Circuits

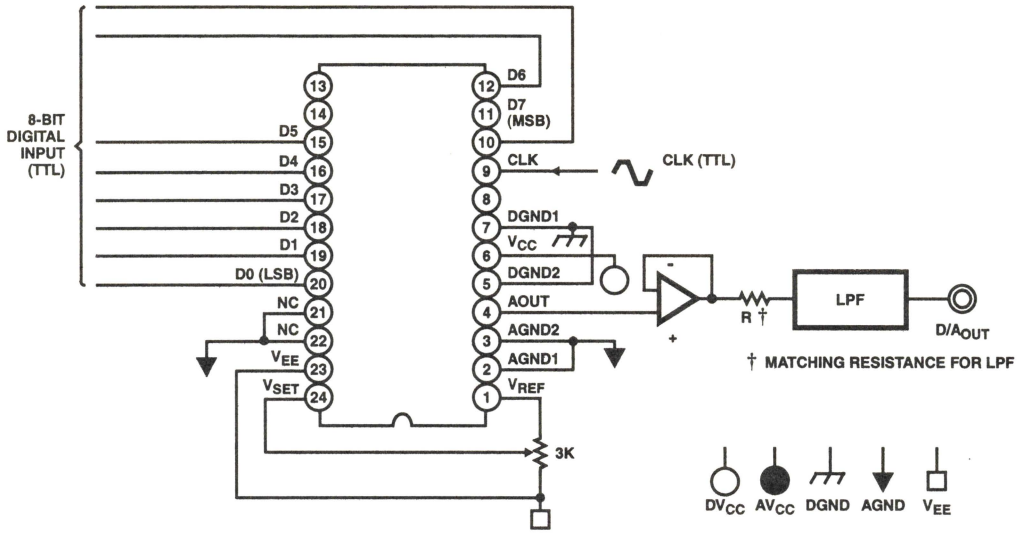


FIGURE 21. DUAL POWER SUPPLY

Notes On Application

1. Setting of V_{REF} Pin (Pin 24)
   The full-scale voltage of the D/A output is determined by V_{SET} input voltage. As about (1.2V - V_{EE}) DC voltage is generated at V_{REF} pin (Pin 1) by connecting an external resistor from V_{REF} pin to V_{EE} pin (Pin 23), divide this voltage using resistors and apply it to V_{SET} pin as Figure 22. Example of usage:

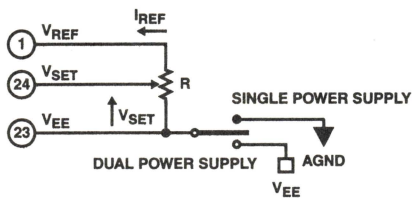


FIGURE 22.

The full-scale voltage of the D/A output can be determined from the following equation:
$V_{FS} = 1.2 (V_{SET} - V_{EE})$ ($R_L > 10k\Omega$, $0.4V \leq V_{SET} \leq 1.2V$
Select an external resistor R (connected to V_{REF} pin) so that I_{REF} (current of an external resistor) is within the value indicated as the Recommended Operating Conditions of ($-3mA < I_{REF} < -0.4mA$).

2. Phase Relation Between Data and Clock
   To make the best use of the inherent characteristics of this D/A converter the phase relation between the data and clock applied from the exterior, should be properly set. Set up time (t_S) and Hold time (t_H) should be as indicated in the Electrical Specifications. For t_S and t_H refer to Figure 6 in the Timing Waveform. Also, set the clock pulse width according to the Recommended Operating Conditions.

3. D/A Output Pin Load
   Receive the D/A output stage at high impedance, so as to obtain:
   $R_L > 10k\Omega$,
   $C_L < 20pF$.

4. Noise Reduction
   Refer to the following notes in order to minimize noise contamination that occurs from outside the IC and penatrates D/A output.
   - The power supply line and ground line should be made as wide as possible when fixed to the printed circuit board. Analog and Digital circuits should be separated.
   - Connected a bypass capacitor between each of DV_{CC} (Pin 6) and DGND1 (Pin 7); AGND1, 2 (Pins 2, 3) and V_{EE} (Pin 23); V_{SET} (Pin 24) and V_{EE} (Pin 23), respectively.

HARRIS SEMICONDUCTOR

HI1171

August 1997

8-Bit, 40 MSPS, High Speed D/A Converter

Features

- Throughput Rate 40MHz
- Resolution 8-Bit
- Integral Linearity Error . . . . . 0.25 LSB
- Low Glitch Noise
- Single Supply Operation . . . . . +5V
- Low Power Consumption (Max) 80mW
- Evaluation Board Available (HI1171-EV)
- Direct Replacement for the Sony CXD1171

Applications

- Wireless Telecommunications
- Signal Reconstruction
- Direct Digital Synthesis
- Imaging
- Presentation and Broadcast Video
- Graphics Displays
- Signal Generators

Description

The HI1171 is an 8-bit, 40MHz, high speed D/A converter. The converter incorporates an 8-bit input data register with blanking capability, and current outputs. The HI1171 features low glitch outputs. The architecture is a current cell arrangement to provide low linearity errors.

The HI1171 is available in an Industrial temperature range and is offered in a 24 lead (200 mil) SOIC plastic package.

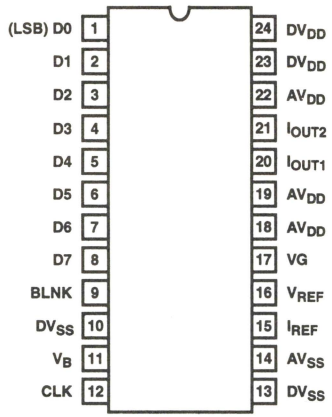
For dual version, please refer to the HI1177 Data Sheet. For triple version, please refer to the HI1178 Data Sheet.

Ordering Information

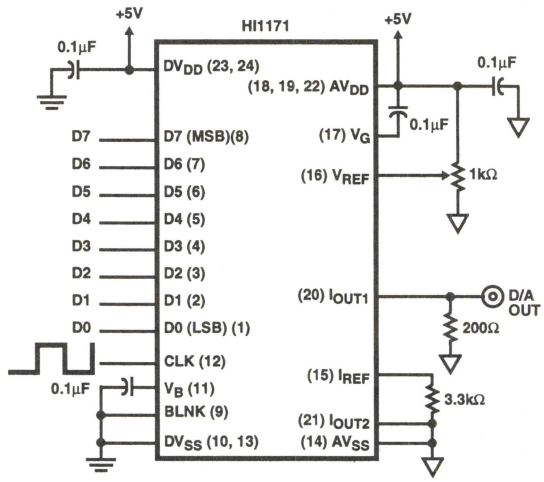
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1171JCB	-40 to 85	24 Ld SOIC	M24.2-S
HI1171-EV	25	Evaluation Board	

Pinout

HI1171
(SOIC)
TOP VIEW



Typical Application Circuit



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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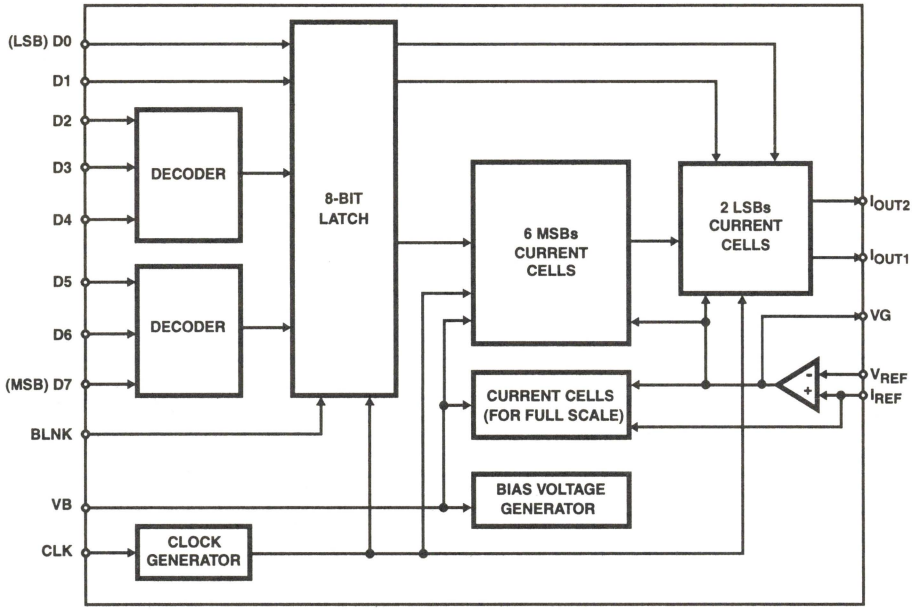
File Number **3662.2**

Functional Block Diagram



Absolute Maximum Ratings

Digital Supply Voltage DV_{DD} to DV_{SS} . . . . . +7.0V
Analog Supply Voltage AV_{DD} to AV_{SS} . . . . . +7.0V
Input Voltage . . . . . V_{DD} to V_{SS} V
Output Current . . . . . 0mA to 15mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
SOIC Package 98
Maximum Junction Temperature, Plastic Package . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{DD} = +4.75V to +5.25V, DV_{DD} = +4.75 to +5.25V, V_{REF} = +2.0V, f_S = 40MHz, CLK Pulse Width = 12.5ns, T_A = 25°C (Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution, n		-	8	-	Bits
Integral Linearity Error, INL	f_S = 40MHz (End Point)	-0.5	-	1.3	LSB
Differential Linearity Error, DNL	f_S = 40MHz	-	-	±0.25	LSB
Offset Error, V_{OS}	(Note 2)	-	-	1	mV
Full Scale Error, FSE (Adjustable to Zero)	(Note 2)	-	-	±13	LSB
Full Scale Output Current, I_{FS}		-	10	15	mA
Full Scale Output Voltage, V_{FS}		1.9	2.0	2.1	V
Output Voltage Range, V_{FSR}		0.5	2.0	2.1	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	See Figure 7	40.0	-	-	MHz
Glitch Energy, GE	R_{OUT} = 75Ω	-	30	-	pV-s
Differential Gain, ΔA_V (Note 3)		-	1.2	-	%
Differential Phase, $\Delta\phi$ (Note 3)		-	0.5	-	Degree
REFERENCE INPUT					
Voltage Reference Input Range		0.5	-	2.0	V
Reference Input Resistance	(Note 3)	1.0	-	-	MΩ
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}	(Note 3)	3.0	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 3)	-	-	1.5	V
Input Logic Current, I_{IL}, I_{IH}	(Note 3)	-	-	±5.0	µA
Digital Input Capacitance, C_{IN}	(Note 3)	-	5.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 1	5	-	-	ns
Data Hold Time, t_{HLD}	See Figure 1	10	-	-	ns
Propagation Delay Time, t_{PD}	See Figure 9	-	10	-	ns

Electrical Specifications AV_{DD} = +4.75V to +5.25V, DV_{DD} = +4.75 to +5.25V, V_{REF} = +2.0V, f_S = 40MHz, CLK Pulse Width = 12.5ns, T_A = 25°C (Note 4) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Settling Time, t_{SET} (to $^1/_2$ LSB)	See Figure 1	-	10	15	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 1	12.5	-	-	ns
POWER SUPPLY CHARACTERISITICS					
IAV_{DD}	14.3MHz, at Color Bar Data Input	-	10.9	11.5	mA
IDV_{DD}	14.3MHz, at Color Bar Data Input	-	4.2	4.8	mA
Power Dissipation	200Ω load at $2V_{P-P}$ Output	-	-	80	mW

NOTES:

2. Excludes error due to external reference drift.
3. Parameter guaranteed by design or characterization and not production tested.
4. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagram

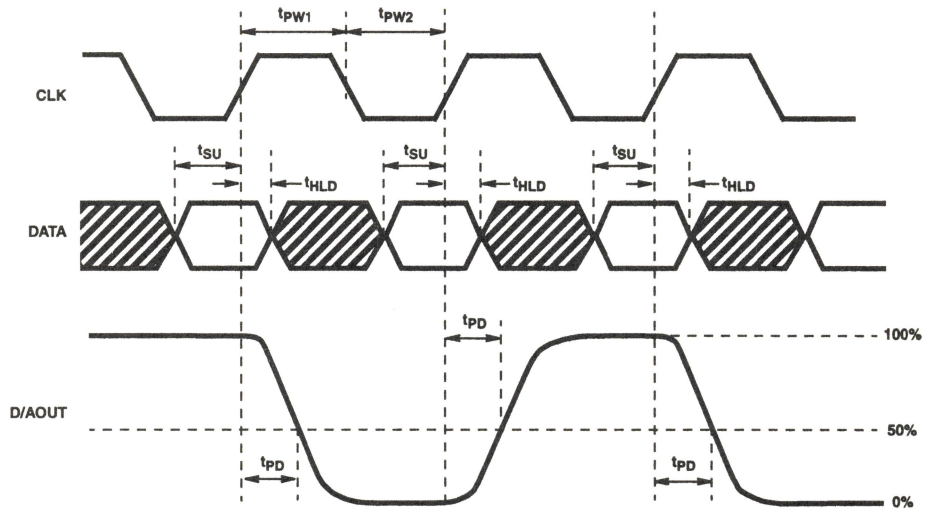


FIGURE 1.

Typical Performance Curves

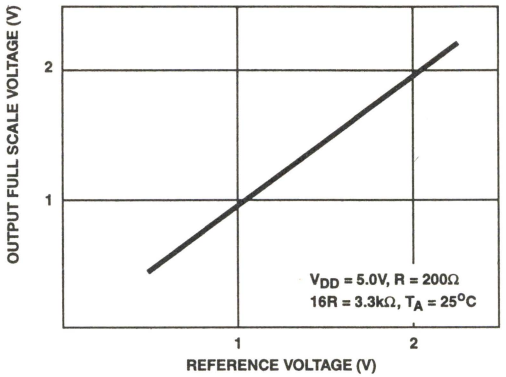


FIGURE 2. OUTPUT FULL SCALE VOLTAGE vs REFERENCE VOLTAGE

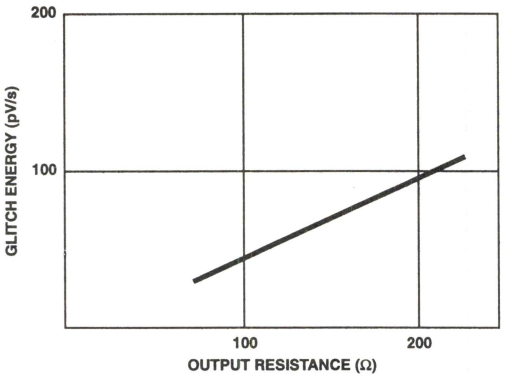


FIGURE 3. OUTPUT RESISTANCE vs GLITCH ENERGY

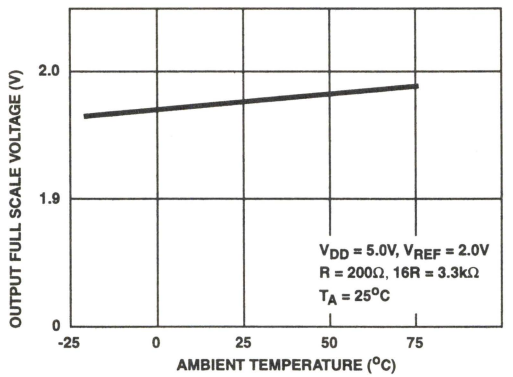


FIGURE 4. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

Pin Descriptions

24 PIN SOIC	PIN NAME	PIN DESCRIPTION
1-8	D0(LSB) thru D7(MSB)	Digital Data Bit 0, the Least Significant Bit thru Digital Data Bit 7, the Most Significant Bit.
9	BLNK	Blanking Line, used to clear the internal data register to the zero condition when High, normal operation when Low.
10, 13	DV_{SS}	Digital Ground.
11	VB	Voltage Bias, connect a 0.1µF capacitor to DV_{SS}.
12	CLK	Data Clock Pin 100kHz to 40MHz.
14	AV_{SS}	Analog Ground.
15	I_{REF}	Current Reference, used to set the current range. Connect a resistor to AV_{SS} that is 16 times greater than the resistor on I_{OUT1}. (See Typical Applications Circuit).
16	V_{REF}	Input Reference Voltage used to set the output full scale range.

Pin Descriptions (Continued)

24 PIN SOIC	PIN NAME	PIN DESCRIPTION
17	VG	Voltage Ground, connect a 0.1µF capacitor to AV_{DD}.
18, 19, 22	AV_{DD}	Analog Supply 4.75V to 7V.
20	I_{OUT1}	Current Output Pin.
21	I_{OUT2}	Current Output pin used for a virtual ground connection. Usually connected to AV_{SS}.
23, 24	DV_{DD}	Digital Supply 4.75V to 7V.

Detailed Description

The HI1171 is an 8-bit, current out D/A converter. The DAC can convert at 40MHz and run on a single +5V supply. The architecture is an encoded, switched current cell arrangement.

Voltage Output Mode

The output current of the HI1171 can be converted into a voltage by connecting an external resistor to I_{OUT1}. To calculate the output resistor use the following equation:

$R_{OUT} = V_{FS} / I_{FS}$,

where V_{FS} can range from +0.5V to +2.0V and I_{FS} can range from 0mA to 15mA.

In setting the output current the I_{REF} pin should have a resistor connected to it that is 16 times greater than the output resistor:

$R_{REF} = 16 \times R_{OUT}$

As the values of both R_{OUT} and R_{REF} increase, power consumption is decreased, but glitch energy and output settling time is increased.

Clock Phase Relationship

The internal latch is closed when the clock line is high. The latch can be cleared by the BLNK line. When BLNK is set (HIGH) the contents of the internal data latch will be cleared. When BLNK is low data is updated by the CLK.

Noise Reduction

To reduce power supply noise separate analog and digital power supplies should be used with 0.1µF ceramic capacitors placed as close to the body of the HI1171 as possible. The analog (AV_{SS}) and digital (DV_{SS}) ground returns should be connected together back at the power supply to ensure proper operation from power up.

Test Circuits

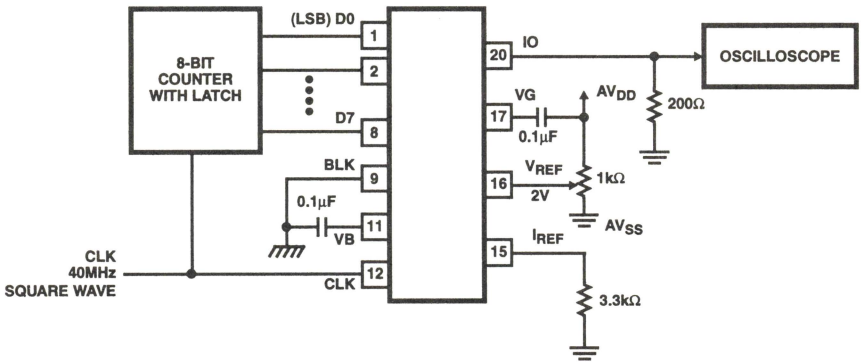


FIGURE 5. MAXIMUM CONVERSION SPEED TEST CIRCUIT

Test Circuits (Continued)

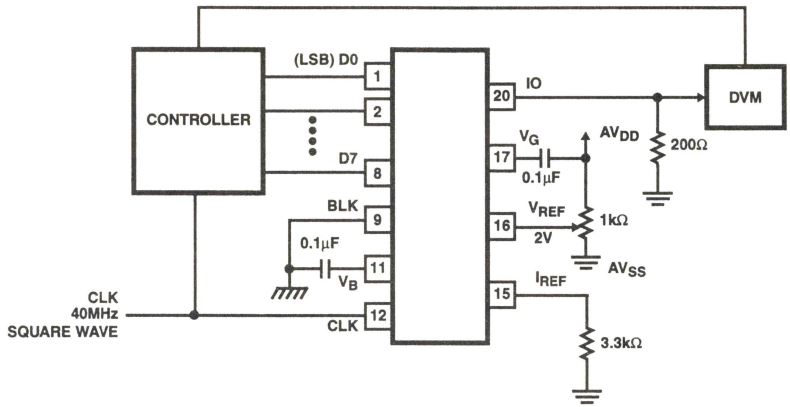


FIGURE 6. DC CHARACTERISTICS TEST CIRCUIT

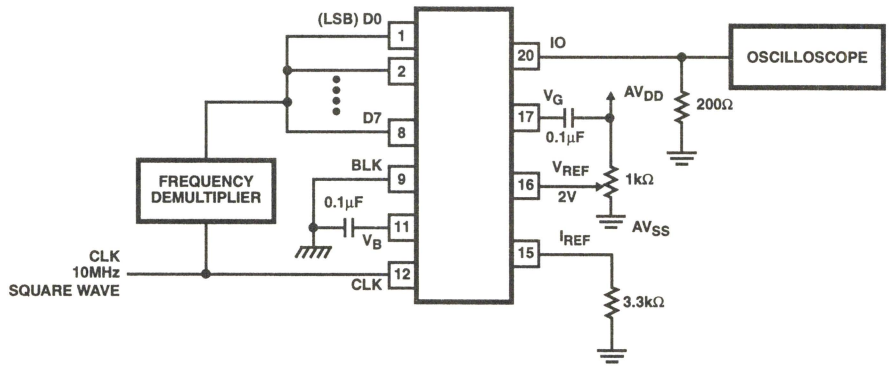


FIGURE 7. PROPAGATION DELAY TIME TEST CIRCUIT

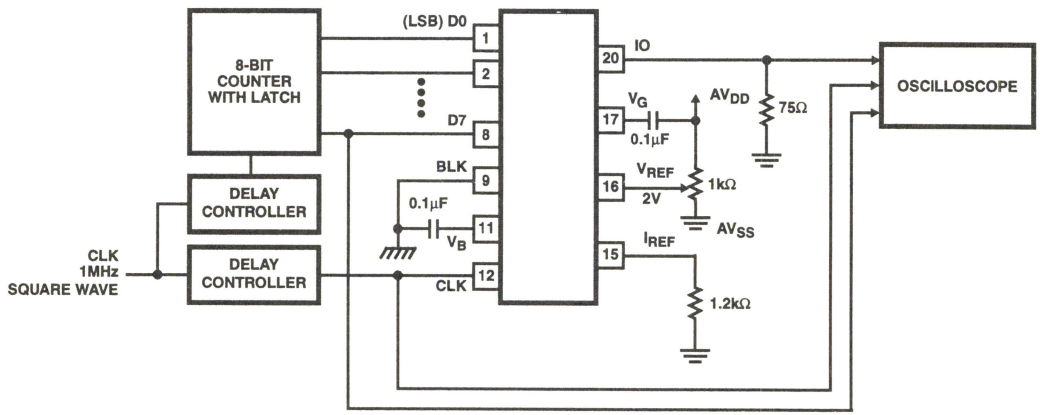


FIGURE 8. SET UP HOLD TIME AND GLITCH ENERGY TEST CIRCUIT

HARRIS SEMICONDUCTOR

HI1177

8-Bit, 40 MSPS, 2-Channel D/A Converter

August 1997

Features

- Resolution 8-Bit
- Maximum Conversion Speed 40MHz
- YC 2-Channel Input/Output
- Differential Linearity Error ..... ±0.3 LSB
- Low Power Consumption .....160mW (200Ω Load for $2V_{P-P}$ Output)
- Power Supply .....+5V Single
- Power-Down Mode
- Low Glitch Noise
- Direct Replacment for Sony CXD1177

Applications

- I/Q Modulation
- YC Video
- Digital TV
- Wireless Transmitters

Description

The HI1177 is a dual 8-bit CMOS digital-to-analog converter. It has input/output equivalent to 2 channels of Y and C for video use or I and Q for modulators.

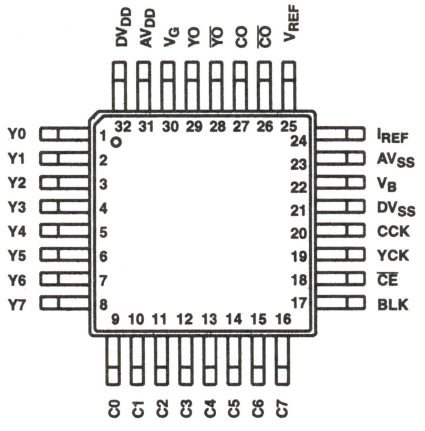
The HI1177 is available in the industrial temperature range and is supplied in a 32 lead plastic metric quad flatpack (MQFP) package.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1177JCQ	-40 to 85	32 Ld MQFP	Q32.7x7-S

Pinout

HI1177
(MQFP)
TOP VIEW



10 D/A CONVERTERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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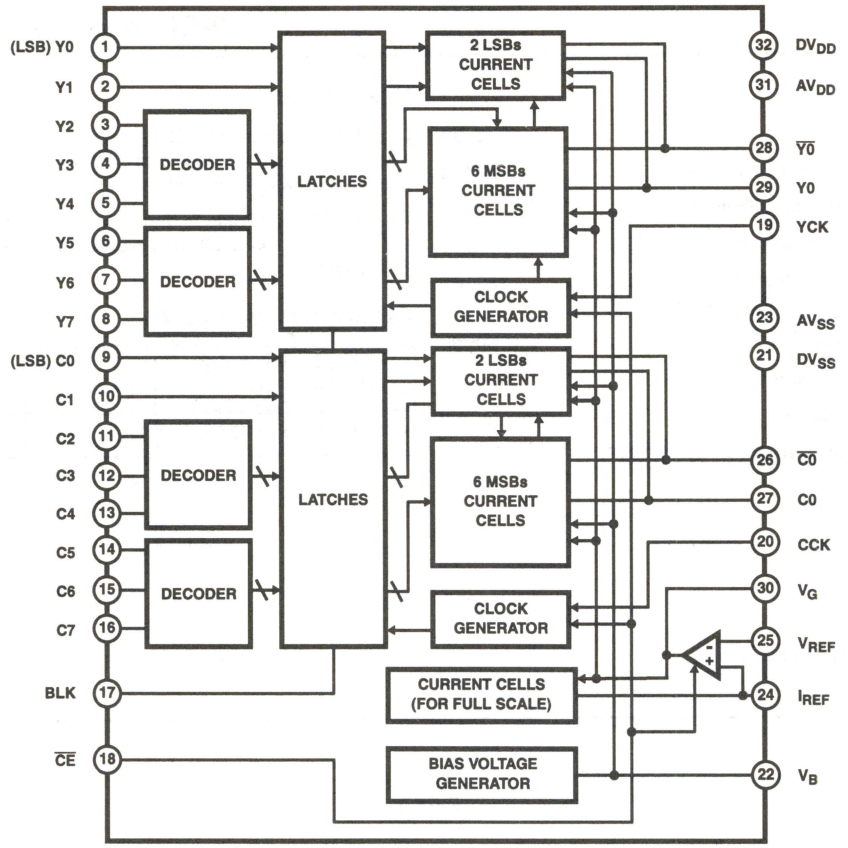
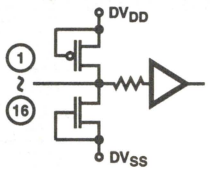
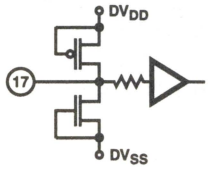
File Number 4114.1

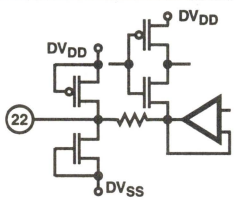
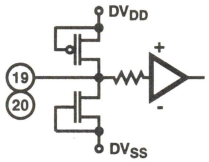
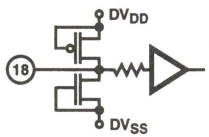
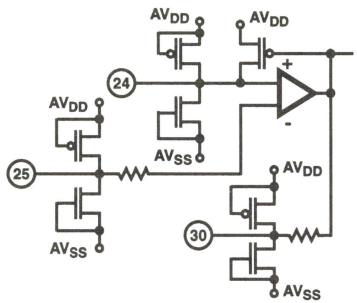
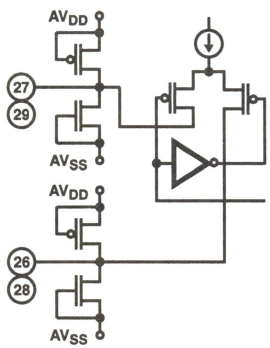
Functional Block Diagram



Pin Descriptions

NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 8	Y0 to Y7		Digital Input.
9 to 16	C0 to C7		
17	BLK		Blanking pin. No signal at "H" (Output 0V). Output condition at "L".

Pin Descriptions (Continued)

NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
22	V_B		Connect a capacitor of about 0.1µF.
19	YCK		Clock pin. Moreover all input pins are TTL-CMOS compatible.
20	CLK		
21	DV_{SS}		Digital GND.
23	AV_{SS}		Analog GND.
18	$\overline{CE}$		Chip enable pin. No signal (Output 0V) at "H" and minimizes power consumption.
24	I_{REF}		Connect a resistance 16 times "16R" that of output resistance value "R".
25	V_{REF}		Set full scale output value.
30	V_G		Connect a capacitor of about 0.1µF.
31	AV_{DD}		Analog V_{DD}.
27	CO		Current output pin. Voltage output can be obtained by connecting a resistance.
29	YO		
26	$\overline{CO}$		Inverted current output pin. Normally dropped to analog GND.
28	$\overline{YO}$		
32	DV_{DD}		Digital V_{DD}.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, V_{DD} 7V
Input Voltage, V_{IN} . . . . . V_{DD} to V_{SS}
Output Current (For Each Channel), I_{OUT} . . . . . .0mA to 15mA

Operating Conditions

Supply Voltage
AV_{DD}, AV_{SS} . . . . . .4.75V to 5.25V
DV_{DD}, DV_{SS} . . . . . .4.75V to 5.25V
Reference Input Voltage, V_{REF} 2.0V
Clock Pulse Width
t_{PW1} . . . . . 12.5ns (Min)
t_{PW0} . . . . . 12.5ns (Min)
Temperature Range, T_{OPR} . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 7) θ_{JA} ($^oC/W$)
MQFP Package 122
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $f_{CLK} = 40MHz$, $V_{DD} = 5V$, $R_{OUT} = 200\Omega$, $V_{REF} = 2.0V$, $T_A = 25^oC$

PARAMETER		SYMBOL	TEST CONDITIONS	TEST LEVEL OR NOTES	PART NUMBER OR GRADE MIN	TYP	MAX	UNITS
Resolution		n			-	8	-	bit
Maximum Conversion Speed		f_{MAX}			40	-	-	MHz
Linearity Error		E_L			-2.5	-	2.5	LSB
Differential Linearity Error		E_D			-0.3	-	0.3	LSB
Full Scale Output Voltage		V_{FS}			1.9	2.0	2.2	V
Full Scale Output Ratio		F_{SR}		Note 1	0	1.5	3	%
Full Scale Output Current		I_{FS}			-	10	15	mA
Offset Output Voltage		V_{OS}			-	-	1	mV
Power Supply Current		I_{DD}	14.3MHz, at Color Bar Data Input		-	-	32	mA
Digital Input Current	High Level	I_{IH}			-	-	5	µA
	Low Level	I_{IL}			-5	-	-	µA
Setup Time		t_S			5	-	-	ns
Hold Time		t_H			10	-	-	ns
Propagation Delay Time		t_{PD}			-	10	-	ns
Glitch Energy		GE	$R_{OUT} = 75\Omega$		-	30	-	pV-s
Cross Talk		CT	1MHz Sin Wave Output		-	57	-	dB

NOTE:

1. Full scale output ratio = $\left|\frac{\text{Full-scale voltage of channel}}{\text{Average of the full-scale voltage of the channels}}(-1)\right| \times 100(\%)$.

I/O Correspondence Table (Output Full Scale Voltage: 2V)

INPUT CODE								OUTPUT VOLTAGE
MSB							LSB	
1	1	1	1	1	1	1	1	2.0V
⋮								
1	0	0	0	0	0	0	0	1.0V
⋮								
0	0	0	0	0	0	0	0	0V

Timing Diagram

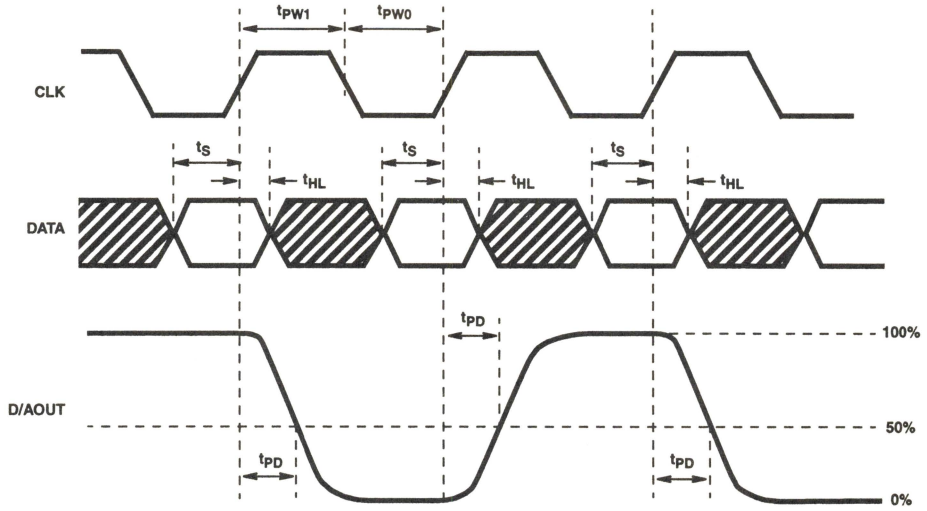


FIGURE 1.

Test Circuits

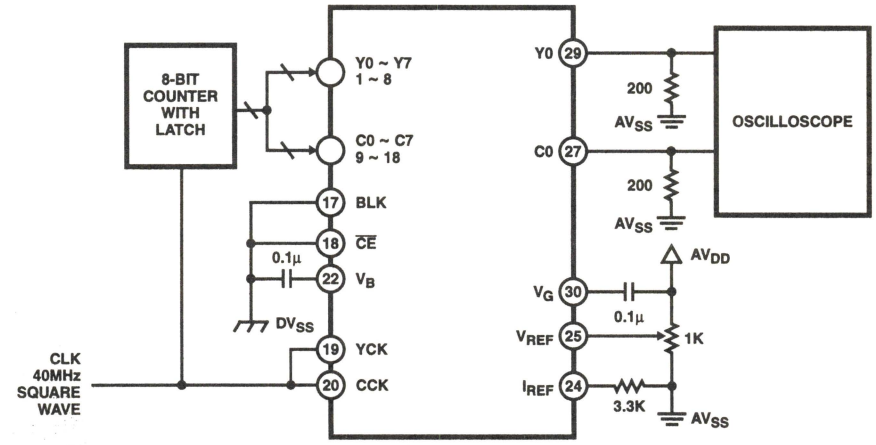


FIGURE 2. MAXIMUM CONVERSION

Test Circuits (Continued)

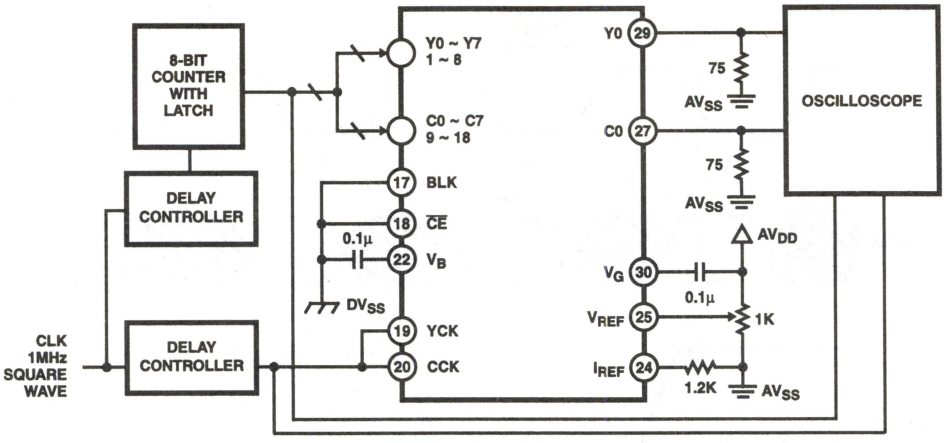


FIGURE 3. SETUP HOLD TIME AND GLITCH ENERGY

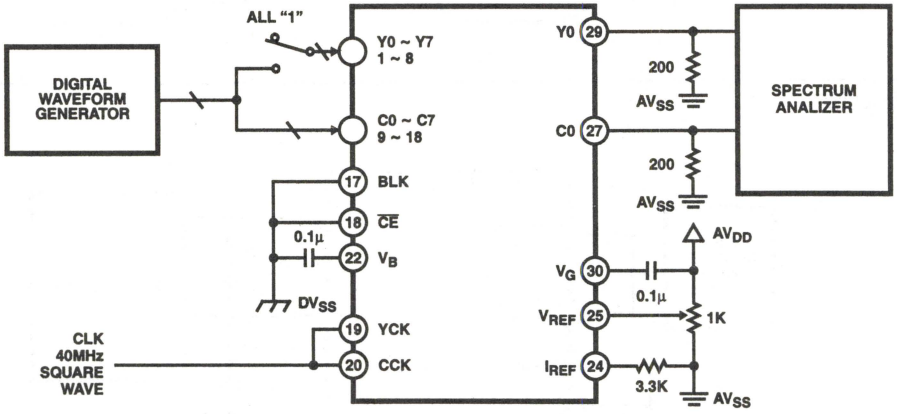


FIGURE 4. CROSSTALK

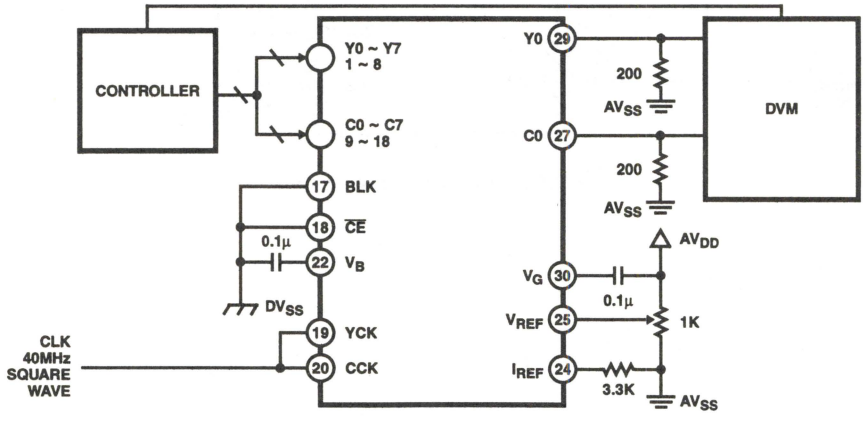


FIGURE 5. DC CHARACTERISTICS

Test Circuits (Continued)

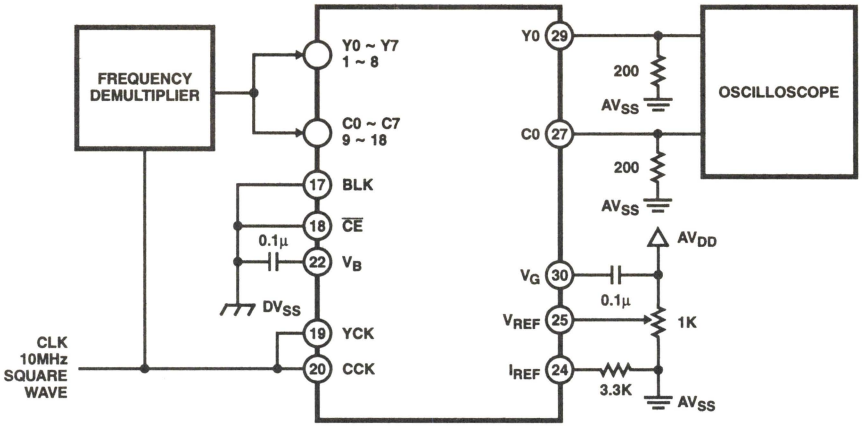


FIGURE 6. PROPAGATION DELAY TIME

Typical Performance Curves

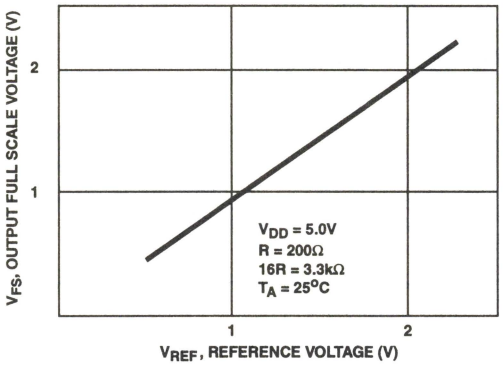


FIGURE 7. OUTPUT FULL SCALE VOLTAGE vs REFERENCE VOLTAGE

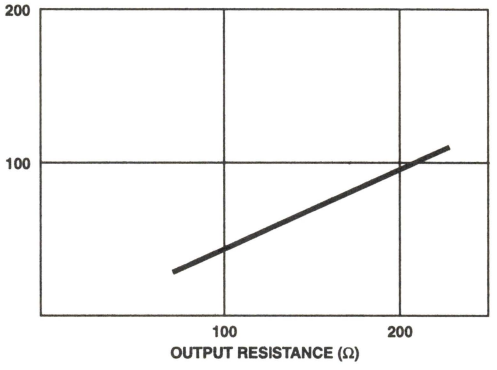


FIGURE 8. GLITCH ENERGY vs OUTPUT RESISTANCE

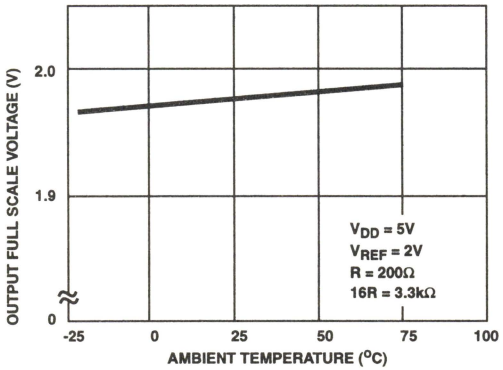


FIGURE 9. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

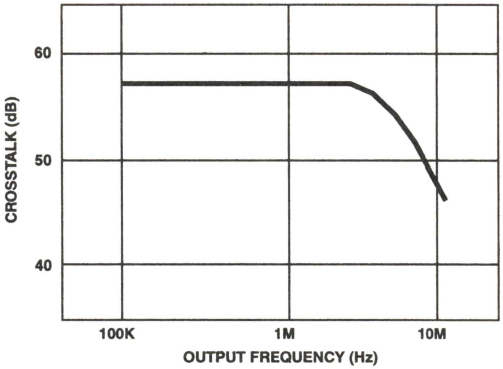
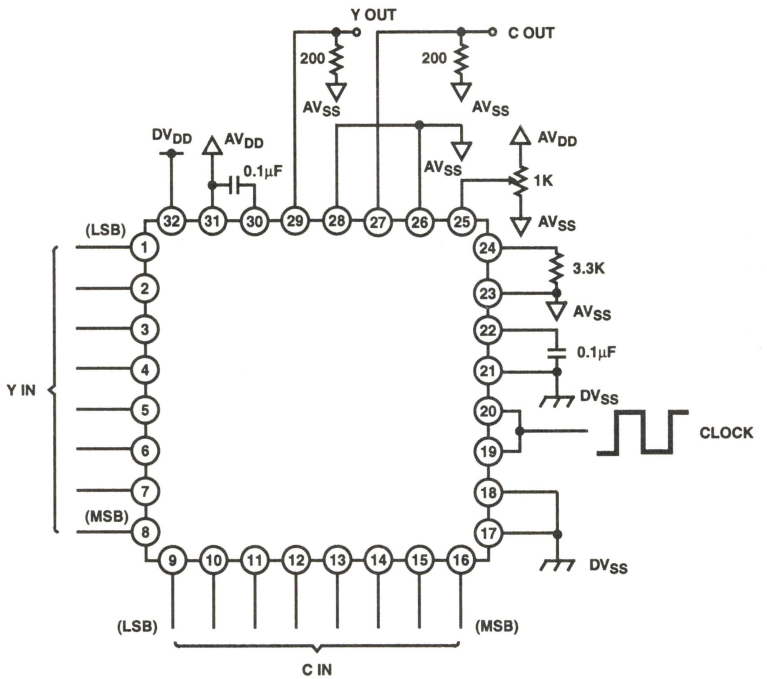


FIGURE 10. CROSSTALK vs OUTPUT FREQUENCY

Application Circuit



NOTE: Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

FIGURE 11.

Operation

- How to select the output resistance:
  - The HI1177 is a D/A converter of the current output type. To obtain the output voltage connect the resistance to IO pin (Y0, C0). For specifications we have:

Output full scale voltage	V_{FS} = less than 2V
Output full scale current	I_{FS} = less than 15mA

  - Calculate the output resistance value from the relation of $V_{FS} = I_{FS} \times R$. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF}. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS} = V_{REF} \times 16R/R'$. R is the resistance connected to IO while R' is connected to I_{REF}. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.
- Phase relation between data and clock:
  - To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the set up time (t_S) and hold time (t_H) as stipulated in the Electrical Characteristics.
- V_{DD}, V_{SS}:
  - To reduce noise effects separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of about 0.1µF, as close as possible to the pin.

HARRIS SEMICONDUCTOR

HI1178

Triple 8-Bit, 40 MSPS, RGB, 3-Channel D/A Converter

August 1997

Features

- Resolution ..... Triple 8-Bit
- Maximum Conversion Speed 40MHz
- RGB 3-Channel Input/Output
- Differential Linearity Error ..... +0.3 LSB
- Low Power Consumption ..... 240mW (200Ω Load for $2V_{P-P}$ Output)
- Single Power Supply ..... +5V
- Low Glitch Noise
- Direct Replacement for Sony CXD1178

Applications

- Digital TV
- Graphics Display
- High Resolution Color Graphics
- Video Reconstruction
- Instrumentation
- Image Processing
- I/Q Modulation

Description

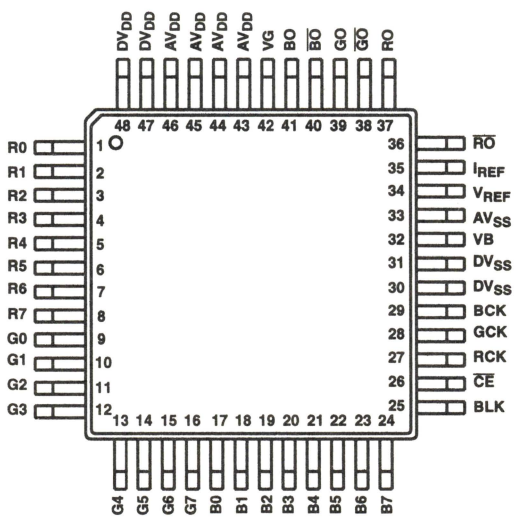
The HI1178 is a triple 8-bit, high-speed, CMOS D/A converter designed for video band use. It has three separate, 8-bit, pixel inputs, one each for red, green, and blue video data. A single 5.0V power supply and pixel clock input is all that is required to make the device operational. A bias voltage generator is internal. Each channel clock input can be controlled individually, or connected together as one. The HI1178 also has BLANK video control signal. Refer to the HI2304 for 3.3V operation.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1178JCQ	-40 to 85	48 Ld MQFP	Q48.12x12-S

Pinout

HI1178
(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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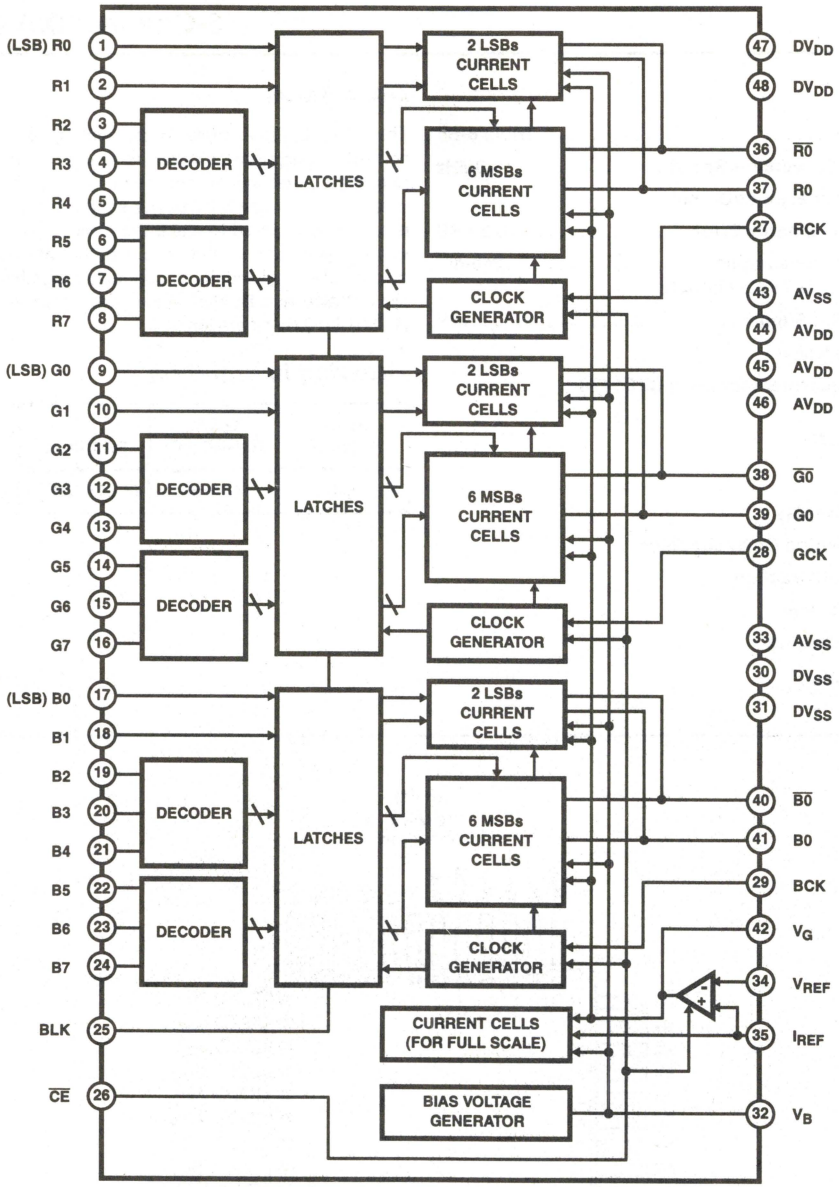
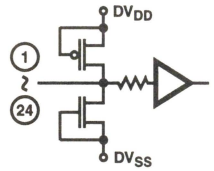
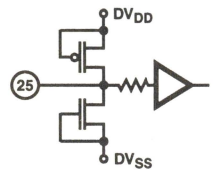
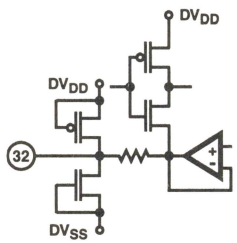
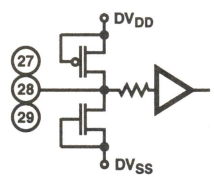
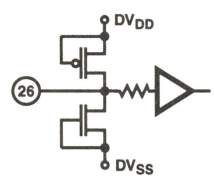
File Number 4115.1

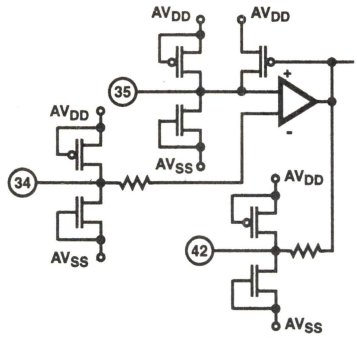
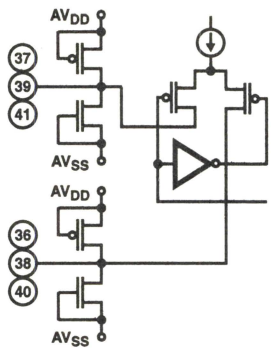
Functional Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 8	R0 to R7		Digital input.
9 to 16	G0 to G7		
17 to 24	B0 to B7		
25	BLK		Blanking pin. No signal at "H" (Output 0V). Output condition at "L".
32	V_B		Connect a capacitor of about 0.1µF.
27	RCK		Clock pin. Moreover all input pins are TTL-CMOS compatible.
28	CLK		
29	BCK		
30, 31	DV_{SS}		Digital GND.
33	AV_{SS}		Analog GND.
26	$\overline{CE}$		Chip enable pin. No signal (Output 0V) at "H" and minimizes power consumption.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
35	I_{REF}		Connect a resistance 16 times "16R" that of output resistance value "R".
34	V_{REF}		Set full scale output value.
42	V_G		Connect a capacitor of about 0.1µF.
43 to 46	AV_{DD}		Analog V_{DD}.
37	RO		Current output pin. Voltage output can be obtained by connecting a resistance.
29	GO		
41	BO		
36	$\overline{RO}$		Inverted current output pin. Normally dropped to analog GND.
38	$\overline{GO}$		
40	$\overline{BO}$		
47, 48	DV_{DD}		Digital V_{DD}.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Input Voltage (V_{IN}) . . . . . V_{DD} to V_{SS}
Output Current (I_{OUT}) . . . . . V_{DD} to V_{SS}
Digital Input Voltage (CLK) . . . . . 0mA to 15mA
(Every Each Channel)

Operating Conditions

Temperature Range (T_{OPR}) . . . . . -40^oC to 85^oC
Supply Voltage
AV_{DD}, AV_{SS} . . . . . 4.75V to 5.25V
DV_{DD}, DV_{SS} . . . . . 4.75V to 5.25V
Reference Input Voltage (V_{REF}) 2V
Clock Pulse Width
t_{PW1} . . . . . 12.5ns (Min)
t_{PW0} . . . . . 12.5ns (Min)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	94

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range (T_{STG}) . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $f_{CLK} = 40MHz$, $V_{DD} = 5V$, $R_{OUT} = 200\Omega$, $V_{REF} = 2.0V$, $T_A = 25^oC$

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		n		-	8	-	bit
Maximum Conversion Speed		f_{MAX}		40	-	-	MSPS
Linearity Error		E_L		-2.5	-	2.5	LSB
Differential Linearity Error		E_D		-0.3	-	0.3	LSB
Full Scale Output Voltage		V_{FS}		1.8	2.0	2.2	V
Full Scale Output Ratio (Note 1)		F_{SR}		0	1.5	3	%
Full Scale Output Current		I_{FS}		-	10	15	mA
Offset Output Voltage		V_{OS}		-	-	1	mV
Power Supply Current		I_{DD}	14.3MHz, at Color Bar Data Input	-	-	48	mA
Digital Input Current	H Level	I_{IH}		-	-	5	µA
	L Level	I_{IL}		-5	-	-	µA
Set Up Time		t_S		5	-	-	ns
Hold Time		t_H		10	-	-	ns
Propagation Delay Time		t_{PD}		-	10	-	ns
Glitch Energy		GE	$R_{OUT} = 75\Omega$	-	30	-	pV/s
Crosstalk		CT	1MHz Sin Wave Output	-	57	-	dB

NOTE:
1. Full scale output ratio = $\left| \frac{\text{Full Scale Voltage of Channel}}{\text{Average of the Full Scale Voltage of the Channels}} - 1 \right| \times 100(\%)$

I/O Chart (When Full Scale Output Voltage at 2.00V)

INPUT CODE								OUTPUT CODE
MSB							LSB	
1	1	1	1	1	1	1	1	2.0V
•								
•								
•								
1	0	0	0	0	0	0	0	1.0V
•								
•								
•								
0	0	0	0	0	0	0	0	0V

Timing Diagram

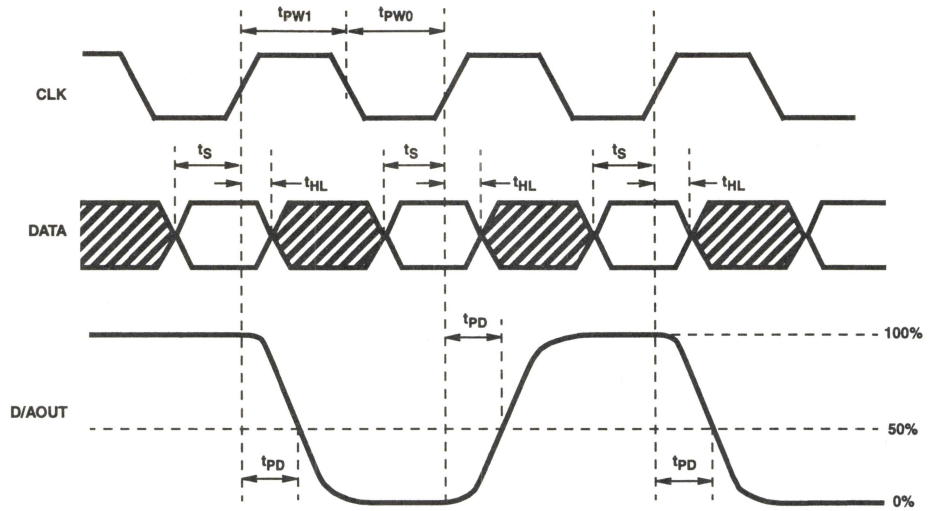


FIGURE 1.

Test Circuits

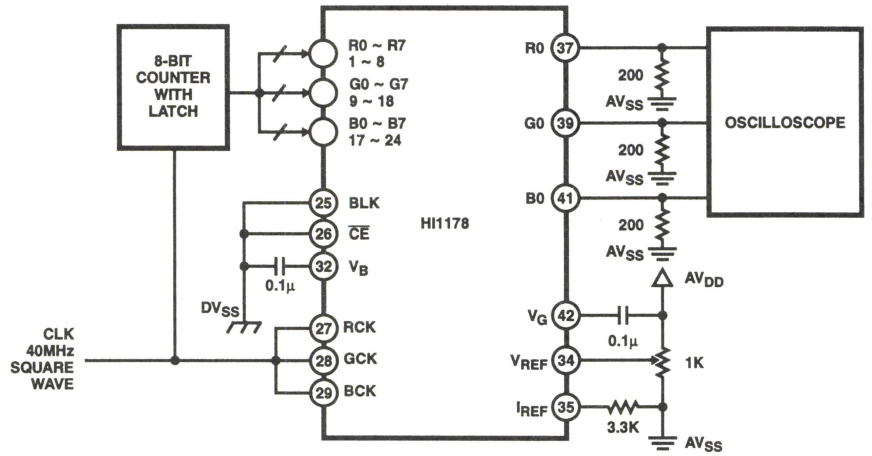


FIGURE 2. MAXIMUM CONVERSION RATE TEST CIRCUIT

Test Circuits (Continued)

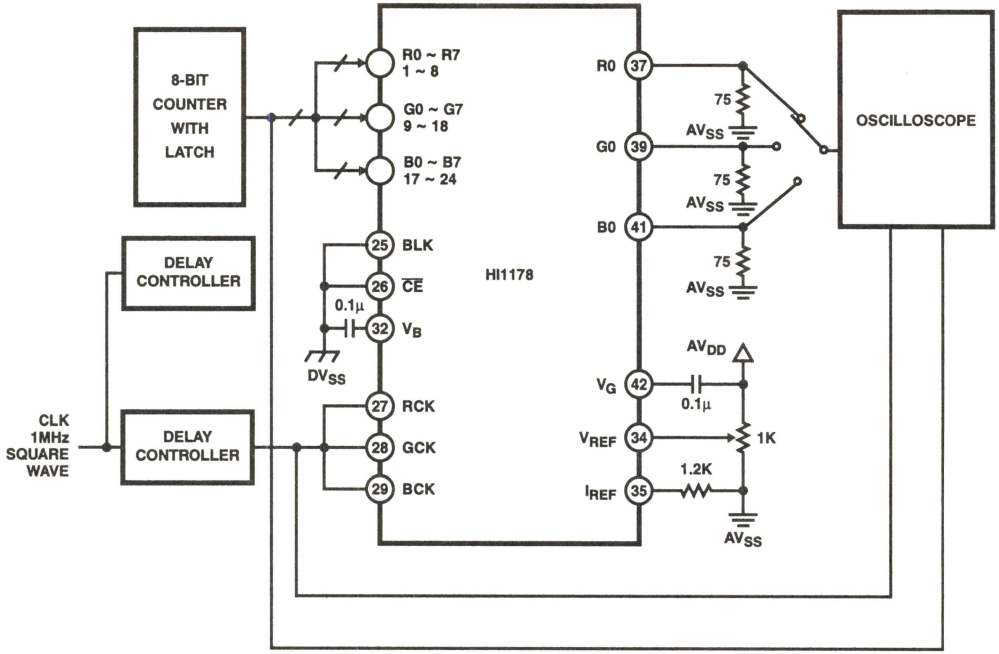


FIGURE 3. SETUP HOLD TIME AND GLITCH ENERGY TEST CIRCUIT

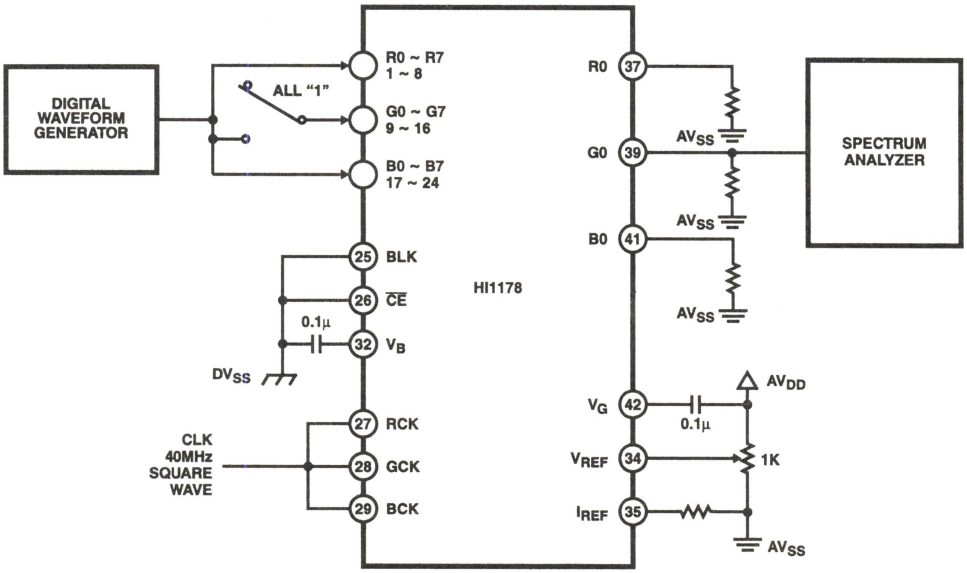


FIGURE 4. CROSSTALK TEST CIRCUIT

Test Circuits (Continued)

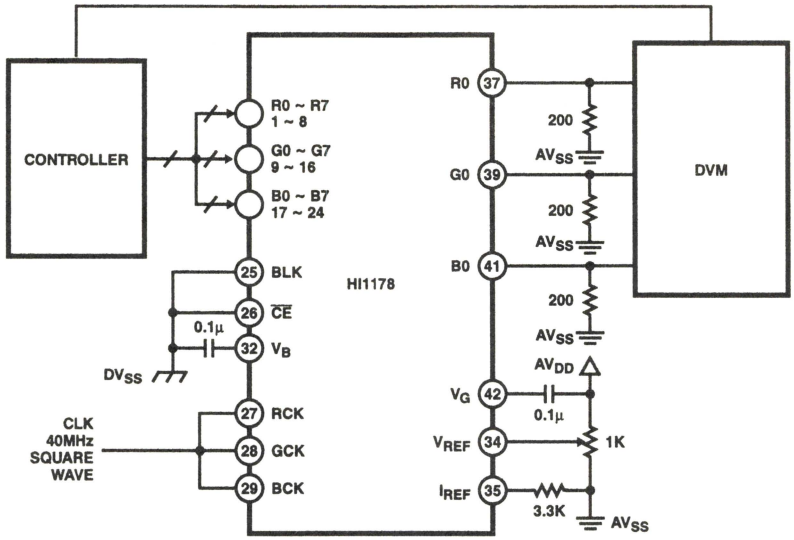


FIGURE 5. DC CHARACTERISTICS TEST CIRCUIT

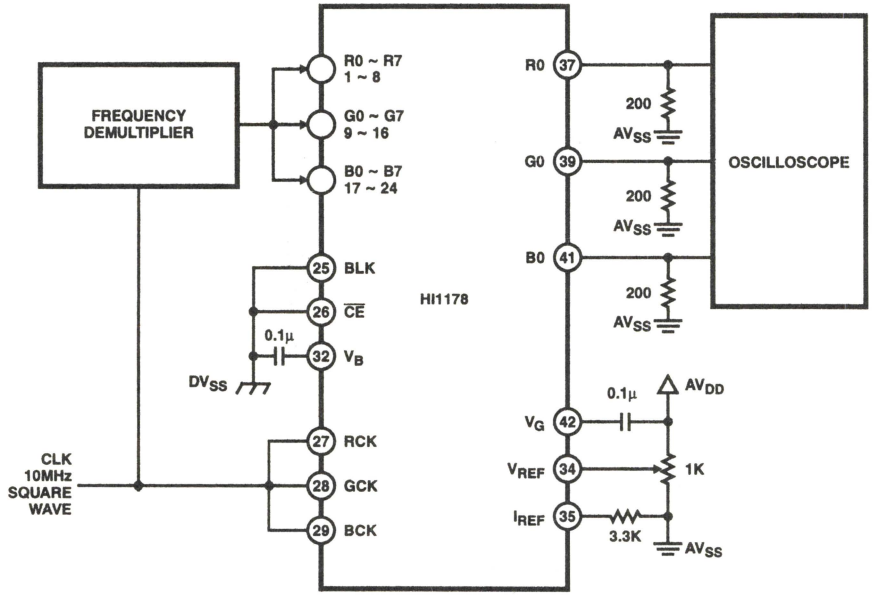


FIGURE 6. PROPAGATION DELAY TIME TEST CIRCUIT

Typical Performance Curves

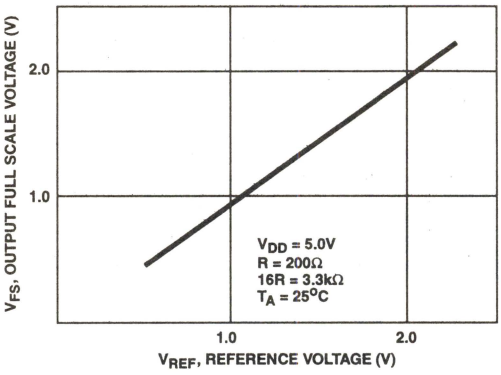


FIGURE 7. OUTPUT FULL SCALE VOLTAGE vs REFERENCE VOLTATE

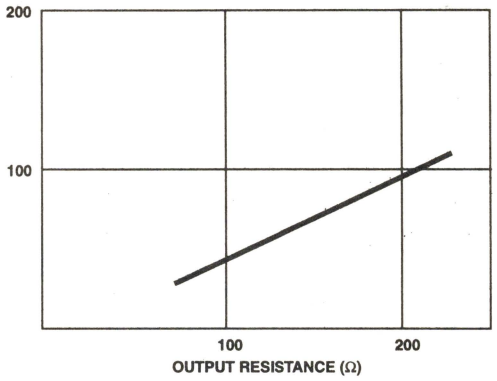


FIGURE 8. GLITCH ENERGY vs OUTPUT RESISTANCE

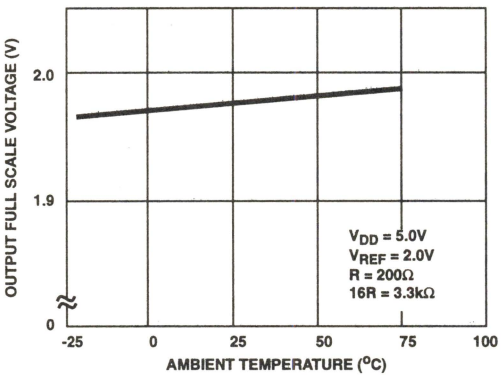


FIGURE 9. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

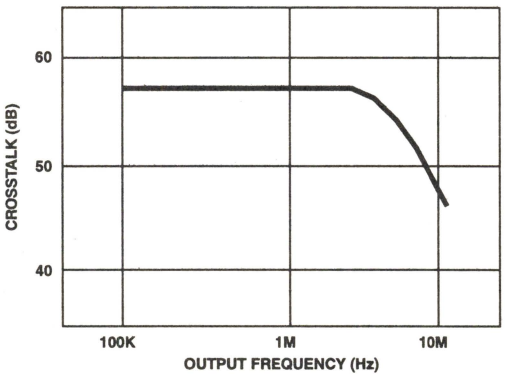


FIGURE 10. CROSSTALK vs OUTPUT FREQUENCY

Application Circuit

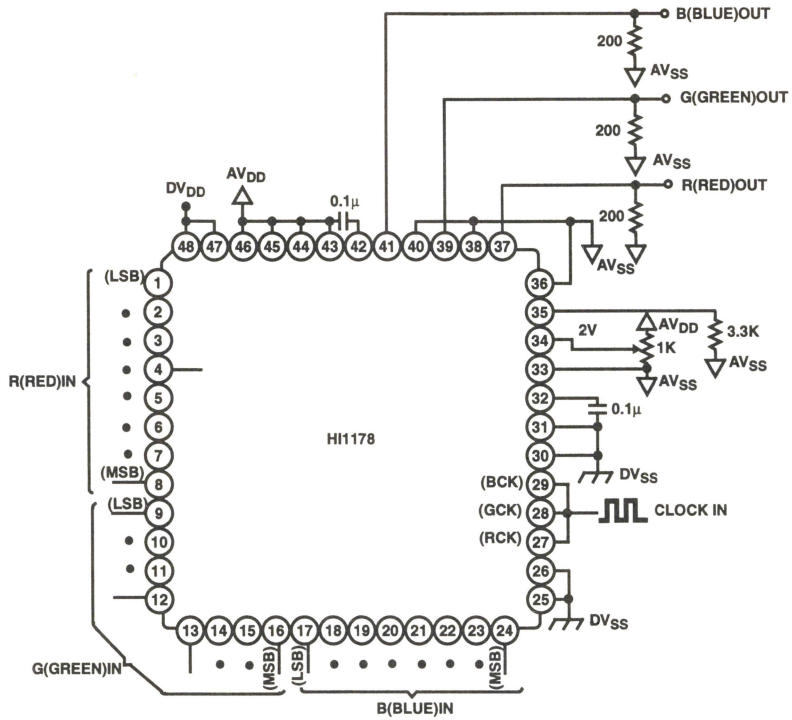


FIGURE 11.

Notes On Operation

- How to select the output resistance

  The HI1178 is a current-output D/A converter. To obtain the output voltage, connect the resistance to IO pin (RO, GO, BO). For specifications we have:

  Output Full Scale Voltage V_{FS} = less than 2.0 [V]

  Output Full Scale Current I_{FS} = less than 15 [mA]

  Calculate the output resistance value from the relation of $V_{FS} = I_{FS}$ X R. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF}. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS} = V_{REF}$ X 16R/R'. R is the resistance connected to IO while R' is connected to I_{REF}. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase Relation Between Data and Clock

  To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the set up time (t_S) and hold time (t_H) as stipulated in the Electrical Characteristics.

- V_{DD}, V_{SS}

  To reduce noise effects separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of 0.1µF, as close as possible to the pin.

HARRIS SEMICONDUCTOR

HI1260

Triple 8-Bit, 35 MSPS, RGB, 3-Channel D/A Converter

August 1997

NOT RECOMMENDED FOR NEW DESIGNS
See HI1178

Features

- Resolution ..... Triple 8-Bit
- Maximum Conversion Speed 35MHz
- RGB 3-Channel Input/Output
- Differential Linearity Error ..... ±0.5 LSB
- Digital Input Voltage ..... TTL Level
- Output Voltage Full Scale (Typ) ..... $1V_{P-P}$
- Low Power Consumption (Typ) 360mW
- Direct Replacement for Sony CXA1260

Applications

- Digital TV
- Graphics Display
- High Resolution Color Graphics
- Video Reconstruction
- Instrumentation
- Image Processing
- I/Q Modulation

Description

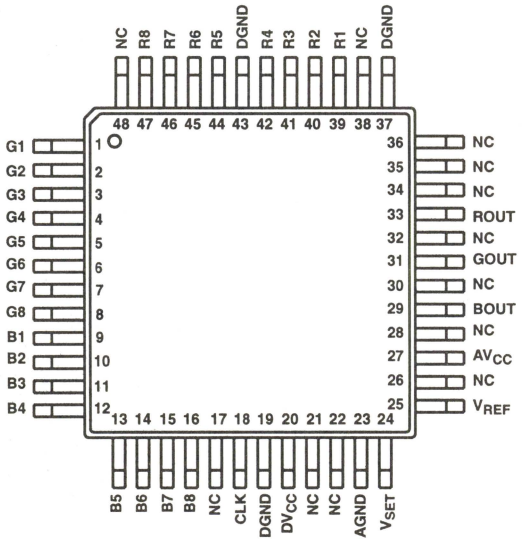
The HI1260 is a triple 8-bit, high-speed, bipolar D/A converter designed for video band use. It has three separate, 8-bit pixel inputs, one each for red, green, and blue video data. A single 5.0V power supply and pixel clock input is all that is required to make the device operational. A bias voltage generator is internal. For lower CMOS power consumption, refer to the HI1178.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI1260JCQ	-20 to 75	48 Ld MQFP	Q48.12 x 12-S

Pinout

HI1260
(MQFP)
TOP VIEW



10 D/A CONVERTERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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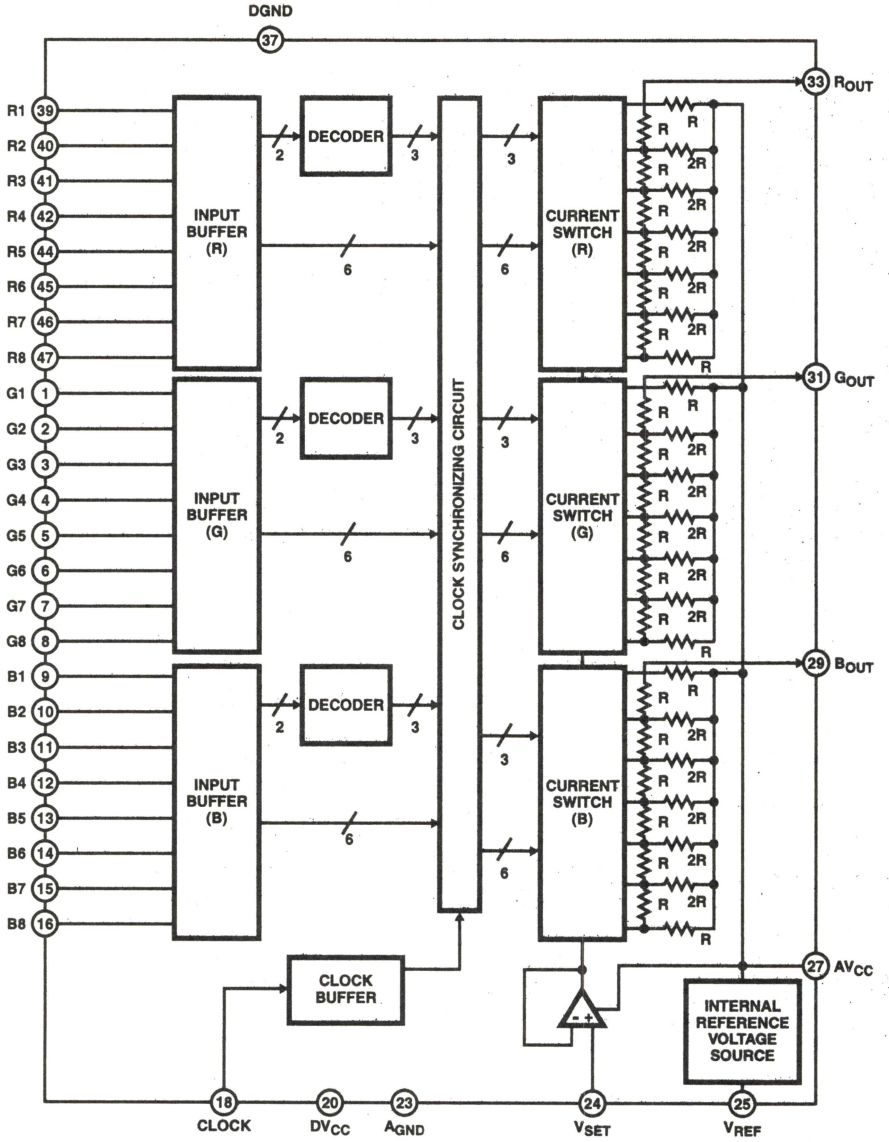
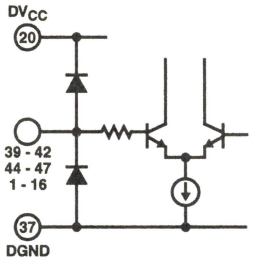
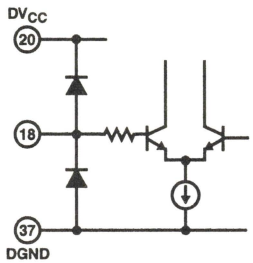
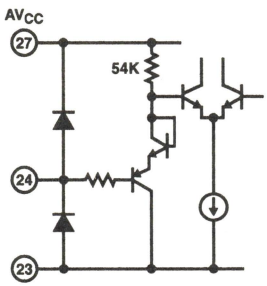
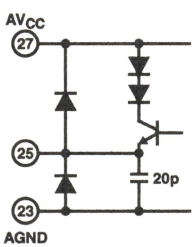
File Number **4112.1**

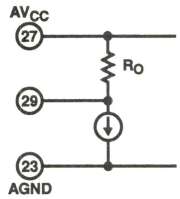
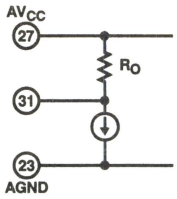
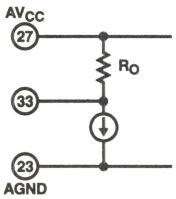
Functional Block Diagram



Pin Descriptions

NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 16 39 to 42 44 to 47	R1 to R8 G1 to G8 B1 to B8		Digital Input pin. From pins 39 to 42 and from 44 to 47 are for RED. R1 is MSB and R8 is LSB. From pins 1 to 8 are for GREEN. G1 is MSB and G8 is LSB. From pins 9 to 16 are for BLUE. B1 is MSB and B8 is LSB.
18	CLK		Clock Input pin.
20	DV_{CC}		Digital V_{CC}.
17 21 to 22	NC		Vacant pin (no connection).
23	AGND		Analog GND.
24	V_{SET}		Bias Input pin. Normally, apply 0.87V. See "Note on use."
25	V_{REF}		Internal Reference Voltage Out pin, 1.2V (Typ). A pull-down resistor is necessary externally. See "Notes on use."

Pin Descriptions (Continued)

NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
26	NC		Vacant pin (no connection).
27	AV_{CC}		Analog V_{CC}.
28	NC		Vacant pin but connect to AV_{CC} (Note 1).
29	B_{OUT}		Analog Output pin for BLUE.
30	NC		Vacant pin but connect to AV_{CC} (Note 1).
31	G_{OUT}		Analog Output pin for GREEN.
32	NC		Vacant pin but connect to AV_{CC} (Note 1).
33	R_{OUT}		Analog Output pin for RED.
34 To 36	NC		Vacant pin but connect to AV_{CC} (Note 1).
19, 37, 43	DGND		Digital GND.
48	NC		Vacant pin (no connection).

NOTE:

1. Pins 30, 32, 34 and 36 are vacant, but in order to reduce interference between the individual RGB outputs, connect them to AV_{CC}.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, V_{CC} . . . . . 0V to 7V
Input Voltage (Digital)
V_I . . . . . -0.3V to V_{CC}
V_{CLK} . . . . . -0.3V to V_{CC}
Input Voltage (V_{SET} Pin), V_{SET} . . . . . -0.3V to V_{CC}
Output Voltage (Analog), V_{OUT} . . . . . V_{CC} -2.1V to V_{CC}
Output Current (Analog), I_{OUT} . . . . . -3mA to 10mA
(V_{REF} Pin), I_{REF} . . . . . -5mA to 0mA
Allowable Power Dissipation, P_D 0.7W

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
MQFP Package	85

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -55^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

Recommended Operating Conditions

Temperature Range . . . . . -20^oC to 75^oC
Supply Voltage
AV_{CC}, DV_{CC} . . . . . 4.5V to 5.5V
AV_{CC} - DV_{CC} . . . . . -0.2V to 0.2V
AGND - DGND . . . . . -0.05V to 0.05V
Digital Input Voltage
H Level, V_{IH}, V_{CLKH} . . . . . 2.0V to DV_{CC}
L Level, V_{IL}, V_{CLKL} . . . . . DGND to 0.8V
V_{SET} Input Voltage, V_{SET} . . . . . 0.7V to 1.0V
V_{REF} Pin Current, I_{REF} . . . . . -3mA to 0.4mA
Clock Pule Width
t_{PW1} 15ns
t_{PW0} 10ns

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, $AV_{CC} = DV_{CC} = 5.0V$, AGND = DGND = 0.0V

PARAMETER			SYMBOL	TEST CONDITIONS	NOTES	MIN	TYP	MAX	UNITS
Resolution			RSL			-	8	-	Bit
Monotony			MNT			-	Guar-antee	-	-
Differential Linearity Error			DLE	V_{SET} - AGND = 0.87V $R_L > 10k\Omega$ FS = Full Scale		-0.5	-	0.5	LSB
Integral Linearity Error			ILE			-0.4	-	4	% of FS
Maximum Conversion Speed			f_{MAX}	V_{SET} - AGND = 0.87V $R_L > 10k\Omega$ $C_L < 20pF$		35	-	-	MSPS
Full Scale Output Voltage			V_{OFS}		Note 3	0.85	1.0	1.15	V_{P-P}
RGB Output Voltage Full Scale Ratio			FSR		Note 4	0	4	8	%
Output Zero Offset Voltage			V_{OFFSET}			-40	-6	0	mV
Output Resistance			R_O			270	340	420	Ω
Consumption Current			I_D	V_{SET} - AGND = 0.87V $R_L > 10k\Omega$ I_{REF} = -400µA		54	72	90	mA
Digital Data Input Current	H Level	Upper 2 Bits	$I_{IH(U)}$	$V_I = DV_{CC}$		-	1.2	20	µA
		Lower 6 Bits	$I_{IH(L)}$			-	0.6	10	µA
	L Level	Upper 2 Bits	$I_{IL(U)}$	V_I = DGND		-10	0	10	µA
		Lower 6 Bits	$I_{IL(L)}$			-10	0	10	µA
Clock Input Current		H Level	I_{CLKH}	$V_{CLK} = DV_{CC}$		-	3	30	µA
		L Level	I_{CLKL}	V_{CLK} = DGND		-10	0	10	µA
V_{SET} Input Current			I_{SET}	V_{SET} = AGND = 0.87V		-5	-0.3	0	µA
Internal Reference Voltage			V_{REF}	I_{REF} = -400µA		1.08	1.20	1.32	V
Set-Up Time			t_S			12	-	-	ns
Hold Time			t_H			3	-	-	ns

NOTES:

3. AV_{CC} - V_O.
4. Maximum value among $100 \times \left|\frac{V_{OFS(R)}}{V_{OFS(G)}} - 1\right|$, $100 \times \left|\frac{V_{OFS(G)}}{V_{OFS(B)}} - 1\right|$, or $100 \times \left|\frac{V_{OFS(B)}}{V_{OFS(R)}} - 1\right|$.

TABLE 1. INPUT CORRESPONDING TABLE

INPUT CODE								OUTPUT VOLTAGE
MSB							LSB	
1	1	1	1	1	1	1	1	$V_{CC} + V_{OFFSET}$
			•					•
			•					•
			•					•
1	0	0	0	0	0	0	0	$V_{CC} + V_{OFFSET}$ -0.5V
			•					•
			•					•
			•					•
0	0	0	0	0	0	0	0	$V_{CC} + V_{OFFSET}$ -1.0V

Standard Circuit Design Data $T_A = 25^oC$, $AV_{CC} = DV_{CC} = 5.0V$, AGND = DGND = 0.0V

PARAMETER	SYMBOL	TEST CONDITIONS	NOTES	MIN	TYP	MAX	UNITS
Crosstalk Among R, G and B	CT	D/A OUT: $1V_{P-P}$ $R_L > 10k\Omega$ $C_L < 20pF$ $f_{DATA} = 7MHz$ $f_{CLK} = 14MHz$ See Figure 5		-	-40	-35	dB
Glitch Energy	GE	$V_{SET} - AGND = 0.87V$ $R_L > 10k\Omega$ $f_{CLK} = 1MHz$ Digital Ramp Output See Figure 6	Note 5	-	30	-	pV/s
Rise Time	t_r	V_{SET} -AGND = 0.87V See Figure 4	Note 6	-	5.5	-	ns
Fall Time	t_f		Note 6	-	5.0	-	ns
Settling Time	t_{SET}			-	1.6	-	ns

NOTE:

5. Observe the glitch which is generated when the digital input varies as follows:

0	0	1	1	1	1	1	1	–	0	1	0	0	0	0	0	0
0	1	1	1	1	1	1	1	–	1	0	0	0	0	0	0	0
1	0	1	1	1	1	1	1	–	1	1	0	0	0	0	0	0

6. The time required for the D/A OUT to arrive at 90% of its final value from 10%.

Test Circuits and Waveforms

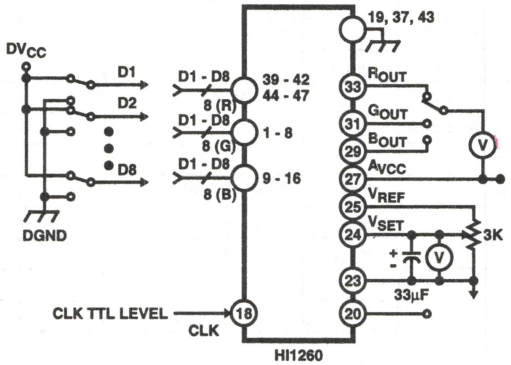


FIGURE 1. DIFFERENTIAL LINEARITY AND INTEGRAL LINEARITY TEST CIRCUIT

Test Circuits and Waveforms (Continued)

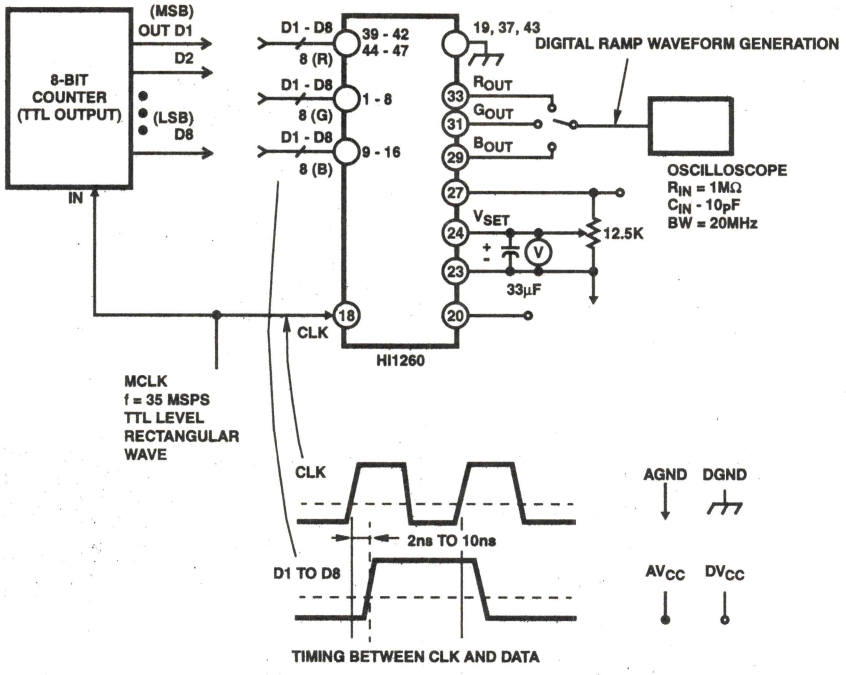


FIGURE 2. MAXIMUM CONVERSION RATE TEST CIRCUIT

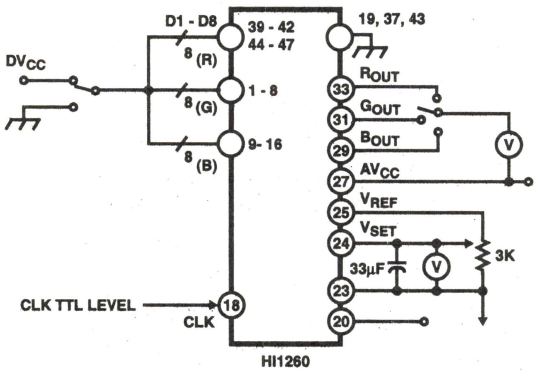


FIGURE 3. OUTPUT VOLTAGE FULL SCALE PRECISION, RGB OUTPUT VOLTAGE FULL SCALE RATIO, AND OUTPUT ZERO OFFSET VOLTAGE TEST CIRCUITS

Test Circuits and Waveforms (Continued)

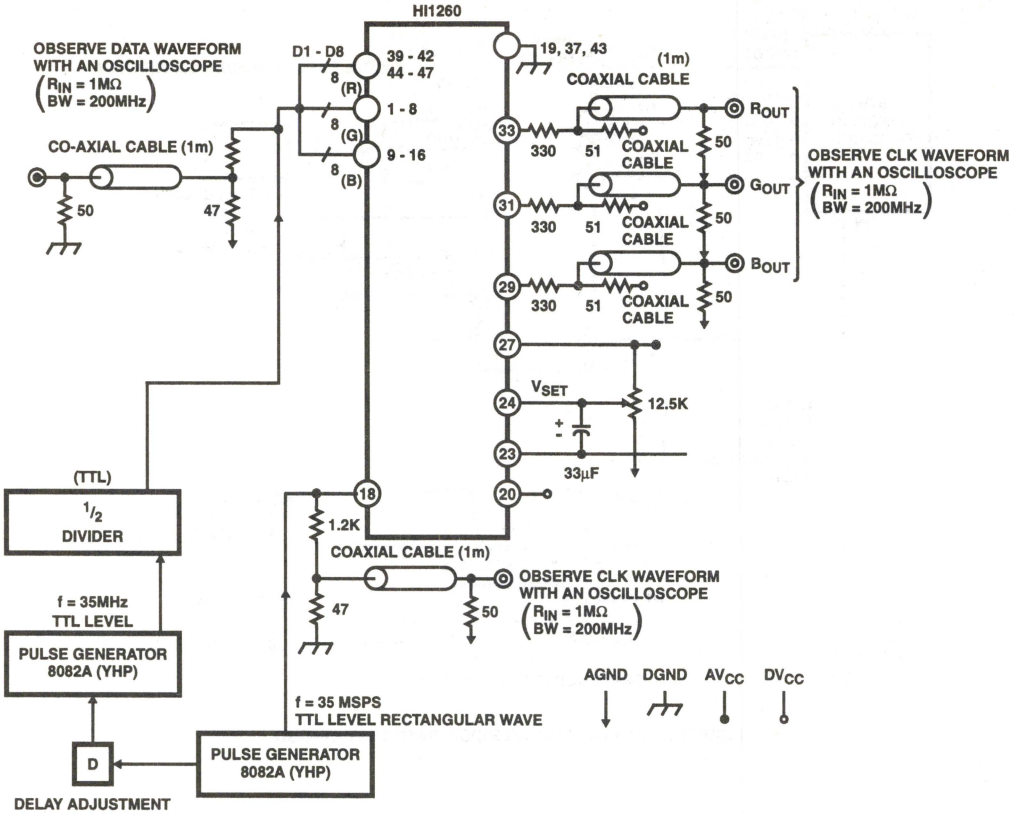
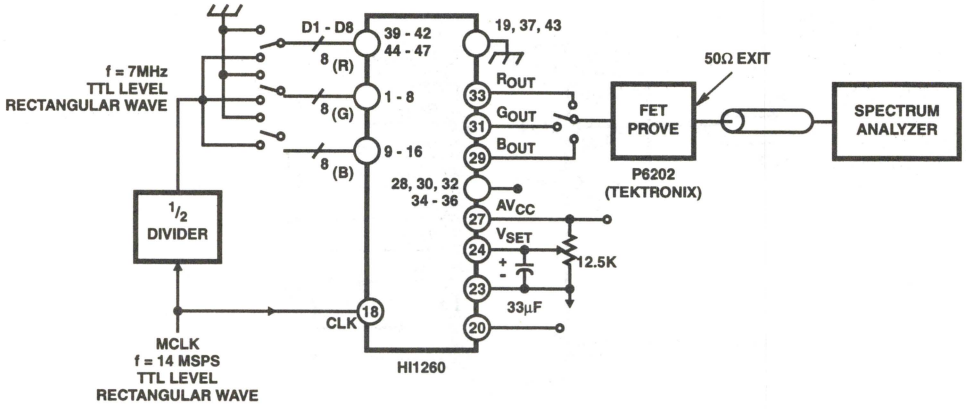


FIGURE 4. SETUP TIME, HOLD TIME, AND RISE AND FALL TIME TEST CIRCUITS



NOTES: The following notes cover the measurement methods in case the measuring crosstalk of G → R:

7. Apply the data to G only and measure the power of the frequency component of the data at R_{OUT}.
8. Apply the data to R only and measure the power of the frequency component of the data at R_{OUT}.
9. Take the difference of the above two powers. The unit is in dB.

FIGURE 5. CROSSTALK AMONG R, G AND B TEST CIRCUIT

Test Circuits and Waveforms (Continued)

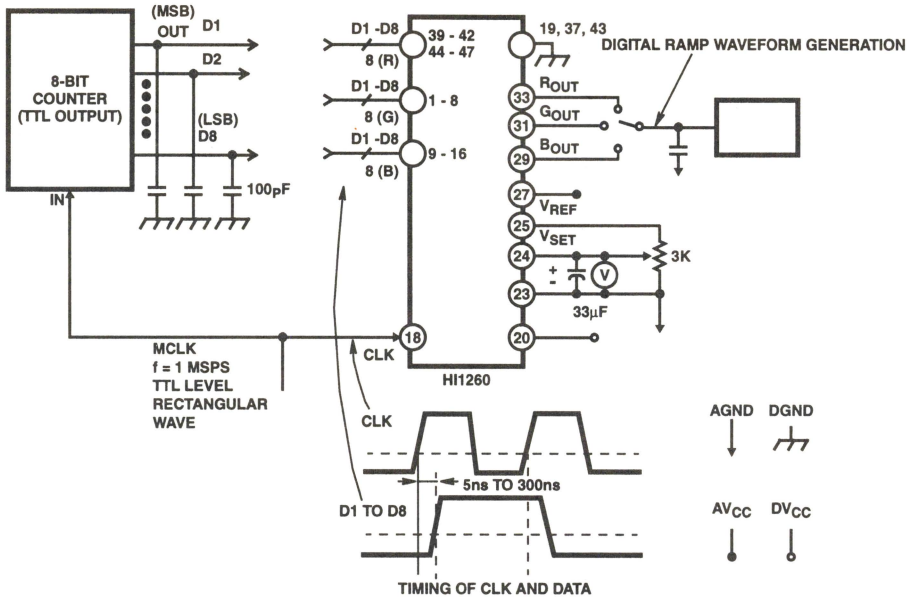
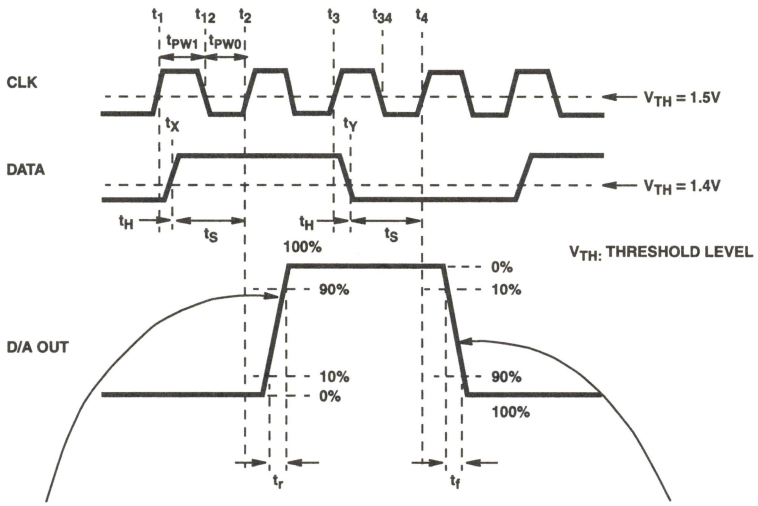


FIGURE 6. GLITCH ENERGY TEST CIRCUIT

Timing Diagram



At the time $t = t_X$, the data of individual bits are switched and thereafter, when the CLK becomes L → H at $t = t_2$, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK. (In this case, fetching of the data is carried out at the fall of the CLK (at the time when $t = T_{12}$).)

At the time $t = T_Y$, the data of individual bits are switched and thereafter, when the CLK becomes L → H at $t = t_4$, the D/A OUT is synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK. (In this case, fetching of the data is carried out at the fall of CLK (at the time when $t = t_4$).)

FIGURE 7.

Typical Performance Curves

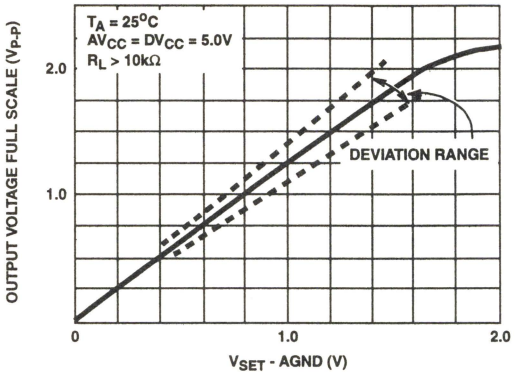


FIGURE 8. OUTPUT VOLTAGE FULL SCALE vs V_{SET} - AGND

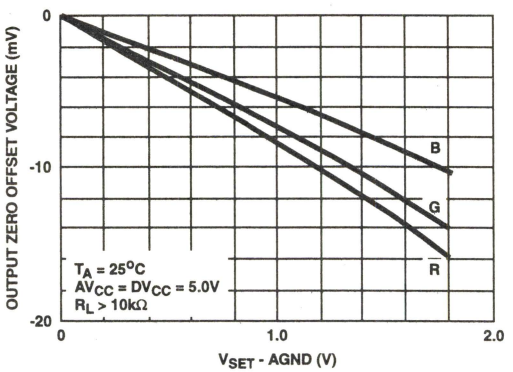


FIGURE 9. OUTPUT ZERO OFFSET VOLTAGE vs V_{SET} - AGND

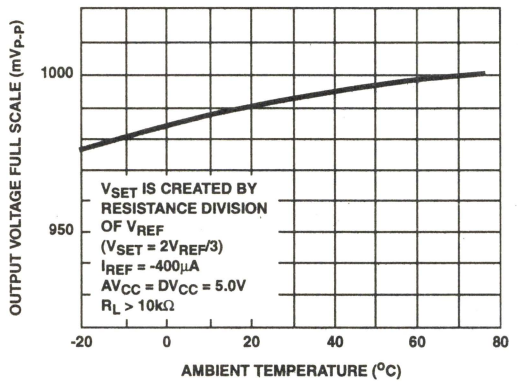


FIGURE 10. OUTPUT VOLTAGE FULL SCALE vs AMBIENT TEMPERATURE

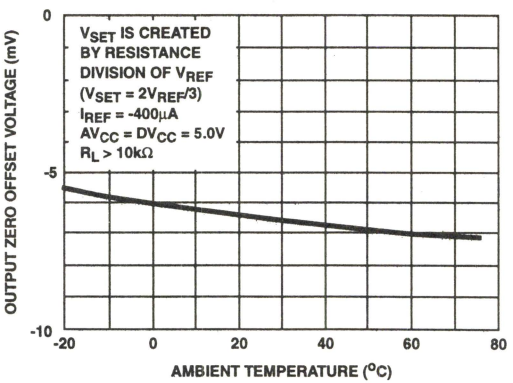


FIGURE 11. OUTPUT ZERO OFFSET VOLTAGE vs AMBIENT TEMPERATURE

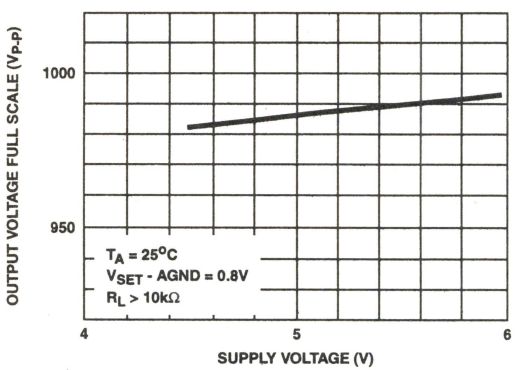


FIGURE 12. OUTPUT VOLTAGE FULL SCALE vs SUPPLY VOLTAGE

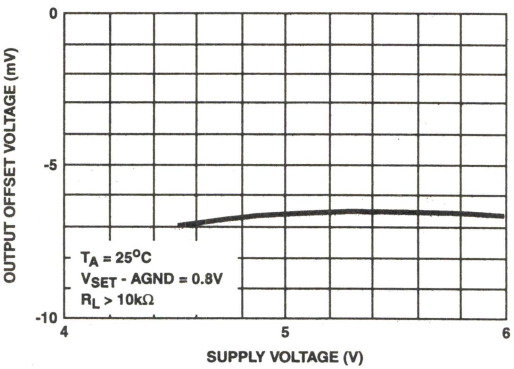


FIGURE 13. OUTPUT ZERO OFFSET VOLTAGE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

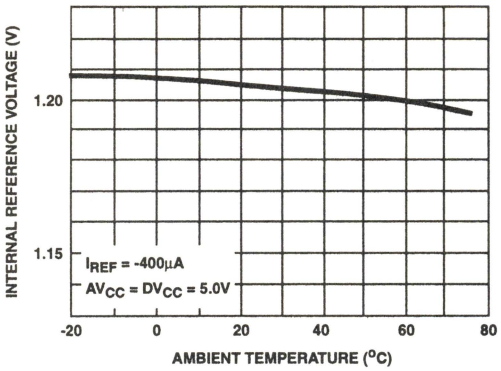


FIGURE 14. INTERNAL REFERENCE VOLTAGE vs AMBIENT TEMPERATURE

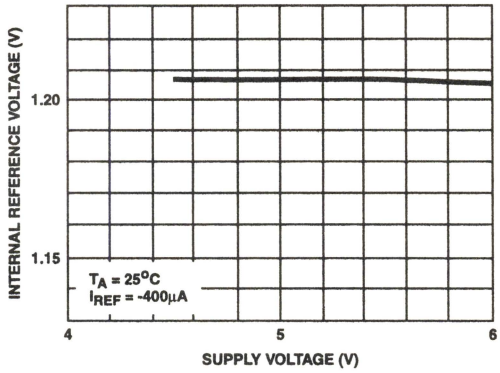


FIGURE 15. INTERNAL REFERENCE VOLTAGE vs SUPPLY VOLTAGE

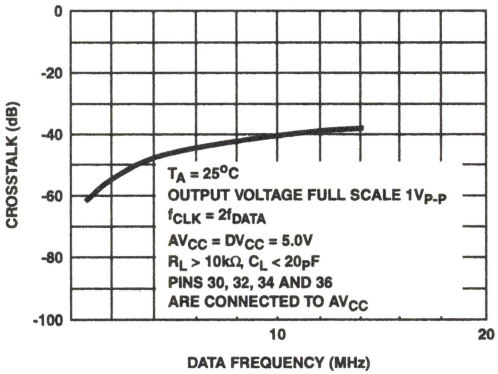


FIGURE 16. CROSSTALK AMONG R, G AND B vs DATA FREQUENCY

Typical Application Circuit

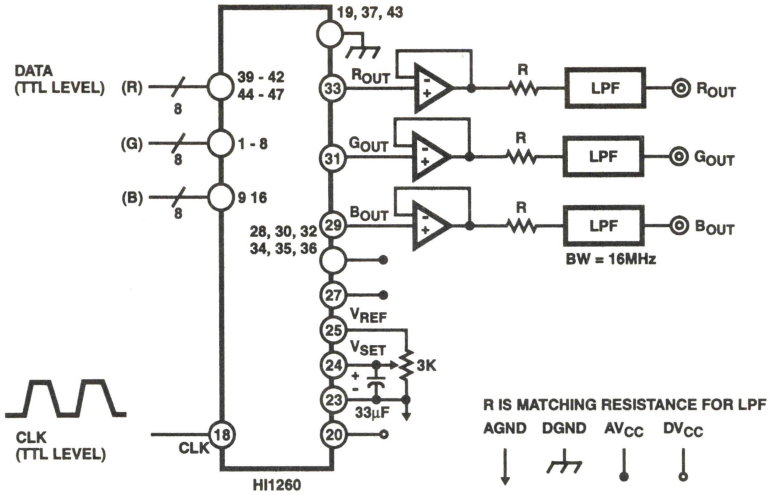


FIGURE 17.

Notes On Use

- Setting of Pin 24 (V_{SET})

  The full scale of the D/A output voltage changes by applying voltage to pin 24 (V_{SET}). When load is connected to pin 25 (V_{REF}), DC voltage of 1.2V is issued and the said voltage is dropped to 0.87V by resistance division.

  When the 0.87V is applied to pin 24 (V_{SET}), the D/A output of $1V_{P-P}$ can be obtained.

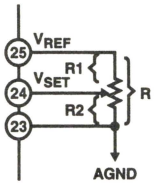


FIGURE 18. EXAMPLE OF USE

Adjustment Method

The resistance R is determined in accordance with the recommended operating condition of I_{REF} (Current flowing through resistance R).

See R vs I_{REF} of Figure 19. The calculation expression is as follows: $R = V_{REF}/I_{REF}$.

Adjust the volume so that the RGB output voltage full scale becomes 1.0V. (At this point, it becomes R1:R2 = 2:5).

- **Phase Relationship Between Data and Clock**

  In order to obtain the desired characteristics as a D/A converter, it is necessary to set the phase relationship correctly between the externally applied data and clock.

  Satisfy the standard of the setup time (t_S) and hold time (t_H) indicated in the electrical characteristics. As to the reaming of t_S and t_H, see the timing chart.

  Moreover, the clock pulse width is desired to be as indicated in the recommended operating condition.

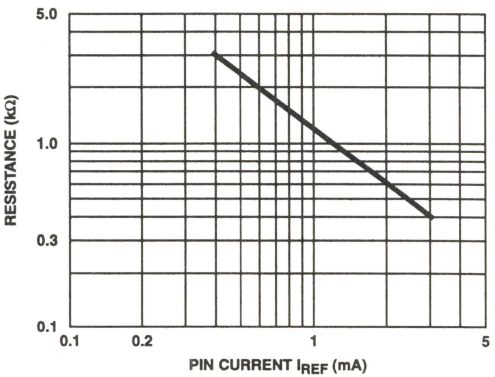


FIGURE 19. RESISTANCE vs V_{REF} PIN CURRENT

- **Regarding the Load of D/A Output Pin**

  Receive the D/A output of the next stage with high impedance. In other words, perform so that it becomes as follows:

  $R_L > 10k\Omega$
  $C_L < 20pF$

  The temperature characteristics indicated in the characteristics diagram has been measured under this condition.

However, when it is made to $R_L \leq 10k\Omega$ the temperature characteristics may change considerably. In addition, when it is made to $C_L \leq 20pF$, the rise and fall of the D/A output become slow and will not operate at high speed.

- **Noise Reduction Measures**

  As the D/A output voltage is a minute voltage of approximately 4mV per one step, ingenuity is required in reducing the noise entering from the outside of the IC as much as possible. Therefore, use the items given below as reference.

  When mounting onto the printed board, allow as much space as possible to the ground surface and the V_{CC} surface on the board and reduce the parasitic inductance and resistance.

  It is desirable that the AGND and DGND be separated in the pattern on the board. It is similar with AV_{CC} and DV_{CC}. As shown in the diagram below, for example, it is recommended that the wiring to the electric supply of AGND and DGND as also AV_{CC} and DV_{CC} be conducted separately, and then making AGND and DGND as also AV_{CC} and DV_{CC} in common right near the power supply respectively.

  Inset in parallel a 47µF tantalum capacitor and a 100pF ceramic capacitor between the V_{CC} surface on the printed board and the nearmost ground surface (A of diagram below). It is also desirable to insert the above between the V_{CC} surface near the pin of the IC and the ground surface (B of diagram below). They are bypass capacitors to prevent bad effects from occurring to the characteristics when the power supply voltage fluctuates due to the clock, etc.

It is recommended to reduce noise which overlaps the D/A output by inserting a capacitor of over 0.1µF between pin 23 (AGND) and pin 24 (V_{SET}).

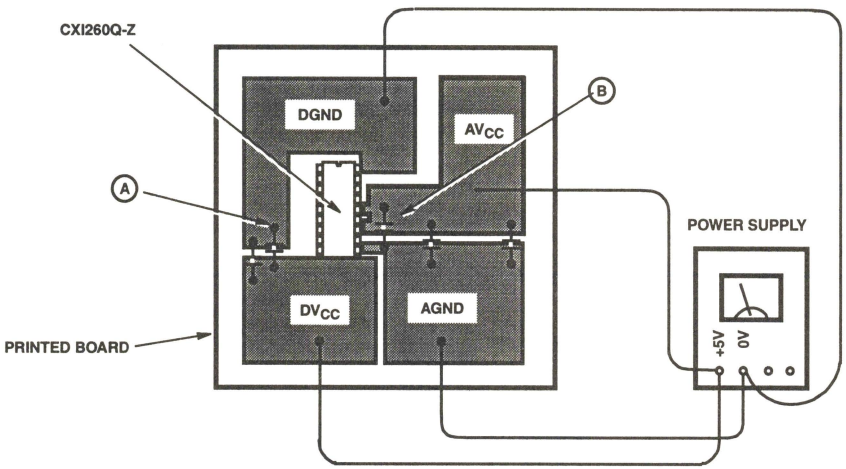


FIGURE 20.

HARRIS SEMICONDUCTOR

HI20201

10-Bit, 160 MSPS, Ultra-High-Speed D/A Converter

August 1997

Features

- Throughput Rate 160MHz
- Resolution (HI20201) 10-Bit
- Differential Linearity Error ..... 0.5 LSB
- Low Glitch Noise
- Analog Multiplying Function
- Low Power Consumption 420mW
- Evaluation Board Available
- Direct Replacement for Sony CX20201-1, CX20202-1

Applications

- Wireless Communications
- Signal Reconstruction
- Direct Digital Synthesis
- High Definition Video Systems
- Digital Measurement Systems
- Radar

Description

The HI20201 is a 160MHz ultra high speed D/A converter. The converter is based on an R/2R switched current source architecture that includes an input data register with a complement feature and is Emitter Coupled Logic (ECL) compatible.

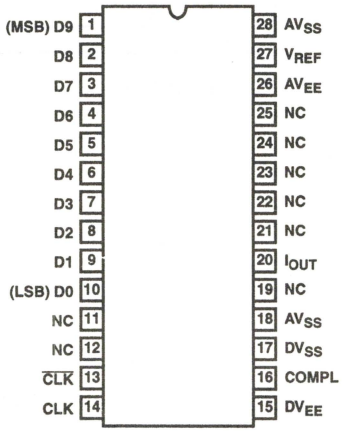
The HI20201 is available in a commercial temperature range and offered in a 28 lead plastic SOIC (300 mil) and a 28 lead plastic DIP package.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI20201JCB	-20 to 75	28 Ld SOIC	M28.3A-S
HI20201JCP	-20 to 75	28 Ld PDIP	E28.6A-S
HI20201-EV	25	Evaluation Kit	

Pinout

HI20201
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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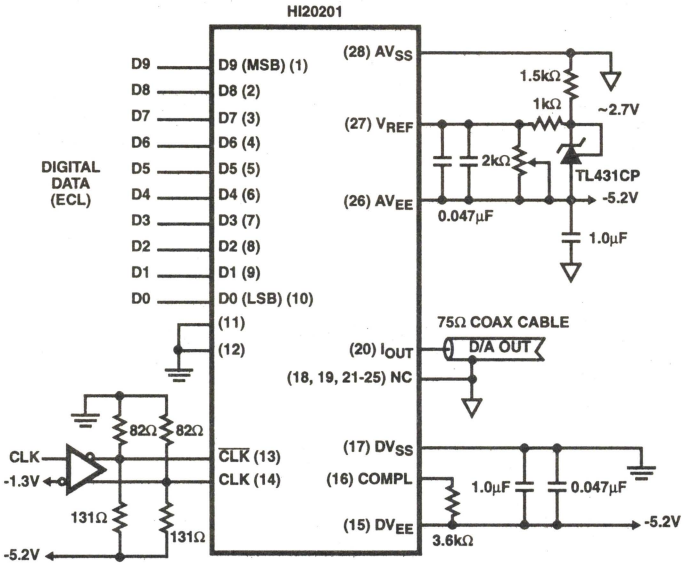
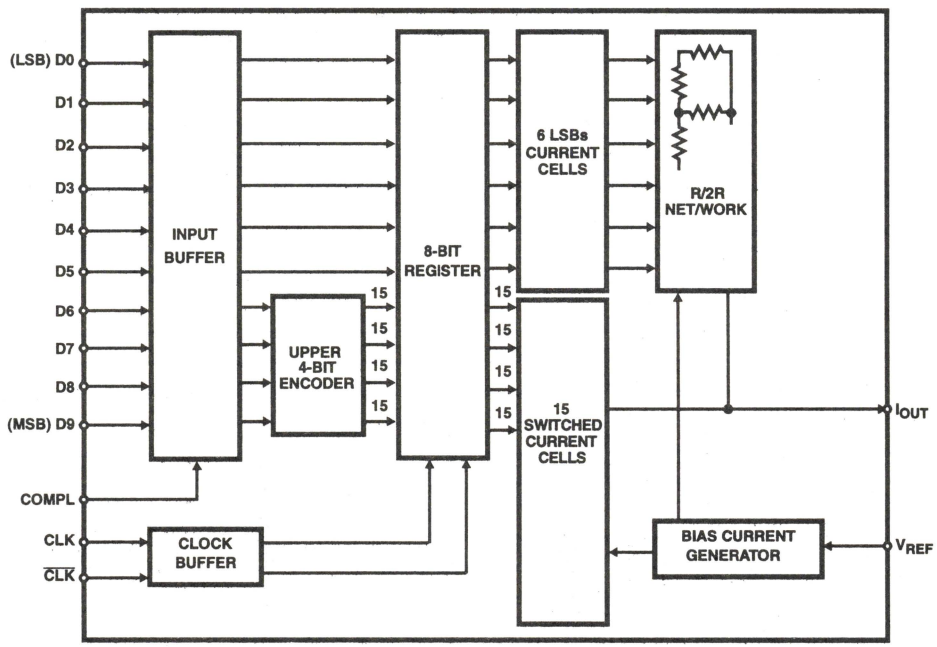
File Number **3581.5**

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings

Digital Supply Voltage DV_{EE} to DV_{SS} . . . . . -7.0V
Analog Supply Voltage AV_{DD} to AV_{SS} . . . . . -7.0V
Digital Input Voltage . . . . . +0.3 to DV_{EE} V
Reference Input Voltage . . . . . +0.3 to AV_{EE} V
Output Current 20mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	67
PDIP Package	58

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Recommended Operating Conditions

Supply Voltage
AV_{EE}, DV_{EE} . . . . . -4.75V to -5.45V
AV_{EE} - DV_{EE} . . . . . -0.05V to +0.05V
Digital Input Voltage
V_{IH} . . . . . -1.0V to -0.7V
V_{IL} . . . . . -1.9V to -1.6V

Reference Input Voltage, V_{REF} . . . . . V_{EE} + 0.5V to V_{EE} + 1.4V
Load Resistance, R_L . . . . . ≥75Ω
Output Voltage, V_{OUT} . . . . . 0.8V to 1.2V
Temperature Range . . . . . -20°C to 75°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = 25°C, AV_{EE} = DV_{EE} = -5.2V, AGND = DGND = 0V, R_L = ∞, V_{OUT} = -1V

PARAMETER	TEST CONDITIONS	HI20201JCB/JCP			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	f_S = 160MHz (End Point)	-	-	±1.0	LSB
Differential Linearity Error, DNL	f_S = 160MHz	-	-	±0.50	LSB
Offset Error, V_{OS} (Adjustable to Zero)	(Note 3)	-	7	-	LSB
Full Scale Error, FSE (Adjustable to Zero)	(Note 3)	-	-	±102	LSB
Full Scale Output Current, I_{FS}		-	-	20	mA
DYNAMIC CHARACTERISTICS					
Throughput Rate	See Figure 11	160	-	-	MHz
Glitch Energy, GE	R_{OUT} = 75Ω	-	15	-	pV/s
REFERENCE INPUT					
Voltage Reference Input Range	With Respect to AV_{EE}	+0.5	-	+1.4	V
Reference Input Current	V_{REF} = -4.58V	-0.1	-0.4	-3.0	µA
Voltage Reference to Output Small Signal Bandwidth	-3dB point $1V_{P-P}$ Input	-	14.0	-	MHz
Output Rise Time, t_r	R_{LOAD} = 75Ω	-	1.5	-	ns
Output Fall Time, t_f	R_{LOAD} = 75Ω	-	1.5	-	ns
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}	(Note 2)	-1.0	-0.89		V
Input Logic Low Voltage, V_{IL}	(Note 2)		-1.75	-1.6	V
Input Logic Current, I_{IL}, I_{IH} (For D9 thru D6, COMPL)	V_{IH} = -0.89V, V_{IL} = -1.75V (Note 2)	0.1	1.5	6.0	µA
Input Logic Current, I_{IL}, I_{IH} (For D5 thru D0)	V_{IH} = -0.89V, V_{IL} = -1.75V (Note 2)	0.1	0.75	3.0	µA
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 11	5	-	-	ns
Data Hold Time, t_{HLD}	See Figure 11	1	-	-	ns
Propagation Delay Time, t_{PD}	See Figure 11	-	3.8	-	ns
Settling Time, t_{SET} (to $^1/_2$ LSB)	See Figure 11	-	5.2	-	ns

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, AGND = DGND = 0V, $R_L = \infty$, $V_{OUT} = -1V$ **(Continued)**

PARAMETER	TEST CONDITIONS	HI20201JCB/JCP			UNITS
		MIN	TYP	MAX	
POWER SUPPLY CHARACTERISITICS					
I_{EE}		-60	-75	-90	mA
Power Dissipation	75Ω load	-	420	470	mW

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. Excludes error due to reference drift.
4. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagram

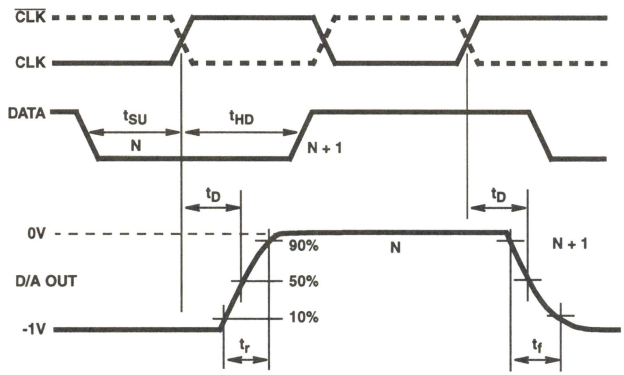


FIGURE 1. LADDER SETTLING TIME FULL POWER BANDWIDTH (LS)

Pin Descriptions

28 PIN SOIC	PIN NAME	PIN DESCRIPTION
1-10	D0 (LSB)-D9 (MSB)	Digital Data Bit 0, the Least Significant Bit thru Digital Data Bit 9, the Most Significant Bit.
11, 12, 19, 21- 25	NC	No Connect, not used.
13	$\overline{CLK}$	Negative Differential Clock Input.
14	CLK	Positive Differential Clock Input
15	DV_{EE}	Digital (ECL) Power Supply -4.75V to -7V.
16	COMPL	Data Complement Pin. When set to a (ECL) logic High the input data is complemented in the input buffer. When cleared to a (ECL) logic Low the input data is not complemented.
17	DV_{SS}	Digital Ground.
18	AV_{SS}	Analog Ground.
20	I_{OUT}	Current Output Pin.
26	AV_{EE}	Analog Supply -4.75V to -7V.
27	V_{REF}	Input Reference Voltage used to set the output full scale range.
28	AV_{SS}	Analog Ground.

Typical Performance Curves

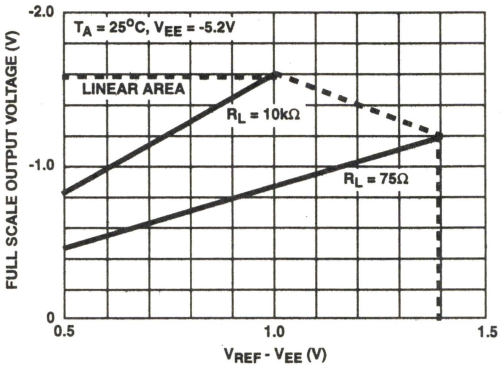


FIGURE 2. $V_{O(FS)}$ RATIO vs (V_{REF} - V_{EE})

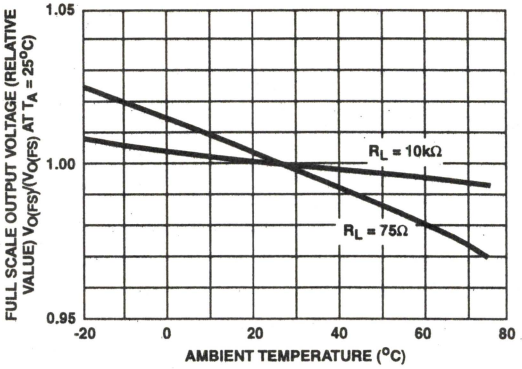


FIGURE 3. FULL SCALE OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

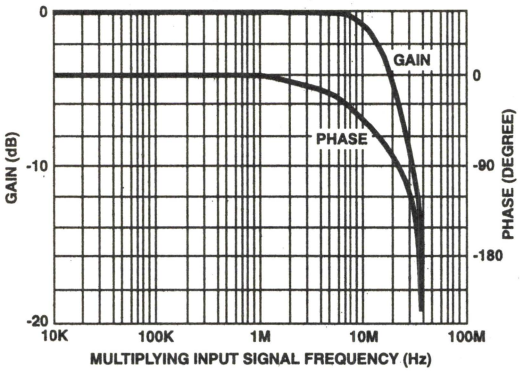


FIGURE 4. OUTPUT CHARACTERISTICS vs MULTIPLYING INPUT SIGNAL FREQUENCY

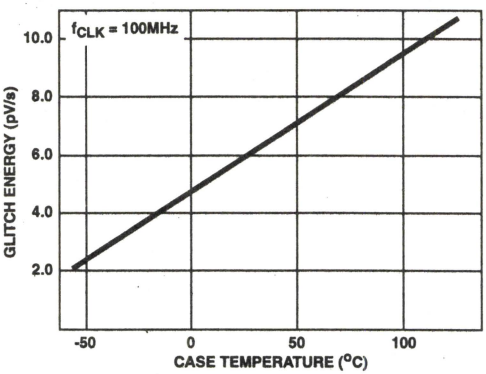


FIGURE 5. GLITCH ENERGY vs CASE TEMPERATURE (FULL SCALE - 1023mV)

Detailed Description

The HI20201 is a 10-bit, current output D/A converter. The DAC can run at 160MHz and is ECL compatible. The architecture is segmented/R2R combination to reduce glitch and improve linearity.

Architecture

The HI20201 is a combined R2R/segmented current source design. The 6 least significant bits of the converter are derived by a traditional R2R network to binary weight the 1mA current sources. The upper 4 most significant bits are implemented as segmented or thermometer encoded current sources. The encoder converts the incoming 4 bits to 15 control lines to enable the most significant current sources. The thermometer encoder will convert binary to individual control lines. See Table 1.

TABLE 1. THERMOMETER ENCODER

MSB	BIT 8	BIT 7	BIT 6	THERMOMETER CODE 1 = ON, 0 = OFF, I_{15} - I_0
0	0	0	0	000 0000 0000 0000
0	0	0	1	000 0000 0000 0001
0	0	1	0	000 0000 0000 0011
0	0	1	1	000 0000 0000 0111
0	1	0	0	000 0000 0000 1111
0	1	0	1	000 0000 0001 1111
0	1	1	0	000 0000 0011 1111
0	1	1	1	000 0000 0111 1111
1	0	0	0	000 0000 1111 1111
1	0	0	1	000 0001 1111 1111
1	0	1	0	000 0011 1111 1111
1	0	1	1	000 0111 1111 1111
1	1	0	0	000 1111 1111 1111
1	1	0	1	001 1111 1111 1111
1	1	1	0	011 1111 1111 1111
1	1	1	1	111 1111 1111 1111

The architecture of the HI20201 is designed to minimize glitch while providing a manufacturable 10-bit design that does not require laser trimming to achieve good linearity.

Glitch

Glitch is caused by the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). In an ECL system where the logic levels switch from one non-saturated level to another, the switching times can be considered close to symmetrical. This helps to reduce glitch in the D/A. Unequal delay paths through the device can also cause one current source to change before another. To minimize this the Harris HI20201 employs an internal register, just prior to the current sources, that is updated on the clock edge. Lastly the worst case glitch usually happens at the major transition i.e., 01 1111 1111 to 10 0000 0000. But in the HI20201 the glitch is moved to the 00 0001 1111 to 11 1110 0000 transition. This is achieved by the split R2R/segmented current source architecture. This decreases the amount of current switching at any one time and makes the glitch practically constant over the entire output range. By making the glitch a constant size over the entire output range this effectively integrates this error out of the end application.

In measuring the output glitch of the HI20201 the output is terminated into a 75Ω load. The glitch is measured at the major carry's throughout the DAC's output range.

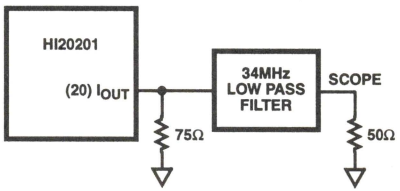


FIGURE 6. HI20201 GLITCH TEST CIRCUIT

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 7 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt/seconds (pV/s).

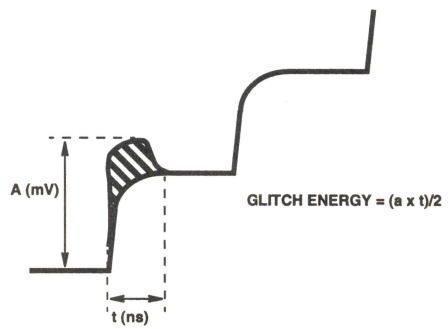


FIGURE 7. GLITCH ENERGY

Setting Full Scale

The full scale output voltage is set by the Voltage Reference pin (27). The output voltage performance will vary as shown in Figure 2.

The output structure of the HI20201 can handle down to a 75Ω load effectively. To drive a 50Ω load Figure 8 is suggested. Note the equivalent output load is ~75Ω.

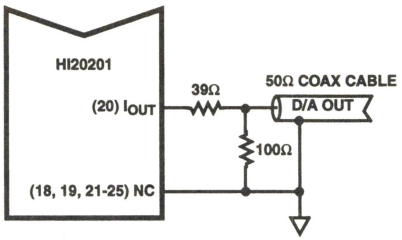


FIGURE 8. HI20201 DRIVING A 50Ω LOAD

Variable Attenuator Capability

The HI20201 can be used in a multiplying mode with a variable frequency input on the V_{REF} pin. In order for the part to operate correctly a DC bias must be applied and the incoming AC signal should be coupled to the V_{REF} pin. See Figure 13 for the application circuit. The user must first adjust the DC reference voltage. The incoming signal must be attenuated so as not to exceed the maximum (+1.4V) and minimum (+0.5V) reference input. The typical output Small Signal Bandwidth is 14MHz.

Integral Linearity

The Integral Linearity is measured using the End Point method. In the End Point method the gain is adjusted. A line is then established from the zero point to the end point or Full Scale of the converter. All codes along the transfer curve must fall within an error band of 1 LSB of the line. Figure 10 shows the linearity test circuit.

Differential Linearity

The Differential Linearity is the difference from the ideal step. To guarantee monotonicity a maximum of 1 LSB differential error is allowed. When more than 1 LSB is specified the converter is considered to be missing codes. Figure 10 shows the linearity test circuit.

Clock Phase Relationship

The HI20201 is designed to be operated at very high speed (i.e., 160MHz). The clock lines should be driven with ECL100K logic for full performance. Any external data drivers and clock drivers should be terminated with 50Ω to minimize reflections and ringing.

Internal Data Register

The HI20201 incorporates a data register as shown in the Functional Block Diagram. This register is updated on the rising edge of the CLK line. The state of the Complement bit (COMPL) will determine the data coding. See Table 2.

TABLE 2. INPUT CODING TABLE

INPUT CODE	OUTPUT CODE	
	COMPL = 1	COMPL = 0
00 0000 0000	0	-1
10 0000 0000	-0.5	-0.5
11 1111 1111	-1	0

Thermal Considerations

The temperature coefficient of the full scale output voltage and zero offset voltage depend on the load resistance connected to I_{OUT}. The larger the load resistor, the better (i.e., smaller) the temperature coefficient of the D/A. See Figure 3 in the performance curves section.

Noise Reduction

Digital switching noise must be minimized to guarantee system specifications. Since 1 LSB corresponds to 1mV for 10-bit resolution, care must be taken in the layout of a circuit board.

Separate ground planes should be used for DV_{SS} and AV_{SS}. They should be connected back at the power supply.

Separate power planes should be used for DV_{EE} and AV_{EE}. They should be decoupled with a 1µF tantalum capacitor and a ceramic 0.047µF capacitor positioned as close to the body of the IC as possible.

Test Circuits

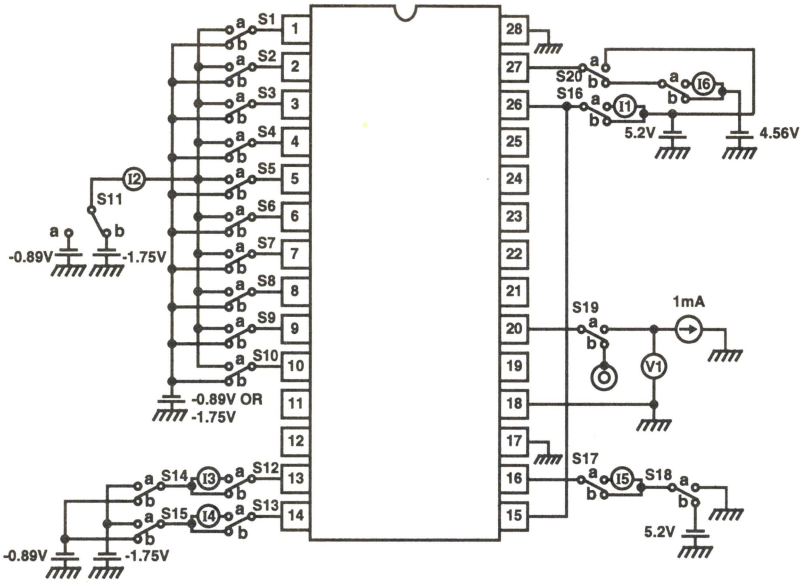
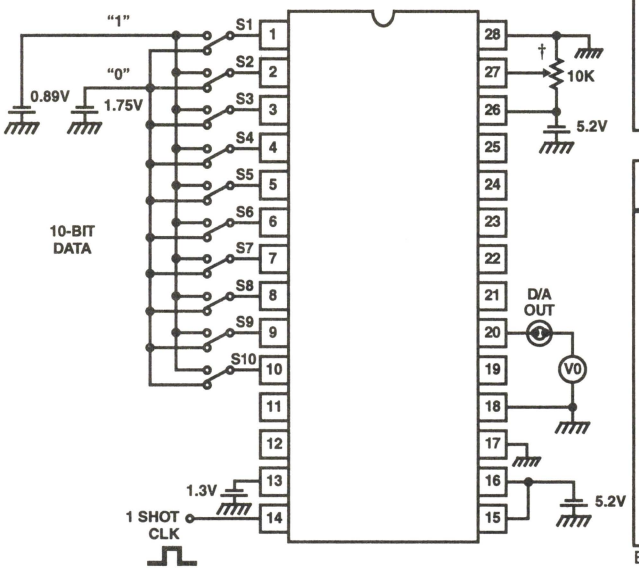


FIGURE 9. CURRENT CONSUMPTION, INPUT CURRENT AND OUTPUT RESISTANCE



† Adjust so that the full scale of DC voltage at pin 20 becomes 1.023V, that is, to satisfy $V_O - V_{1023} = 1.023V$.

LINEARITY ERRORS ARE MEASURED AS FOLLOWS						
S1	S2	S3	••••	S9	S10	D/A OUT
0	0	0	••••	0	0	V_0
0	0	0	••••	0	1	V_1
0	0	0	••••	1	0	V_2
			⋮			⋮
1	1	1	••••	1	1	V_{1023}

INTEGRAL LINEARITY ERROR	DIFFERENTIAL LINEARITY ERROR
V_0	
V_1	$V_1 - V_0$
V_2	$V_2 - V_1$
V_4	$V_4 - V_3$
V_8	$V_8 - V_7$
V_{16}	$V_{16} - V_{15}$
V_{32}	$V_{32} - V_{31}$
V_{64}	$V_{64} - V_{63}$
V_{128}	$V_{128} - V_{127}$
V_{192}	$V_{192} - V_{191}$
⋮	⋮
V_{960}	$V_{960} - V_{959}$
V_{1023}	

Error at individual measurement points are calculated according to the following definition.

$(V_{1023} - V_0)/1023 = V_{0(FS)}/1023 \equiv 1$ LSB.

FIGURE 10. DIFFERENTIAL LINEARITY ERROR AND LINEARITY ERROR

Test Circuits (Continued)

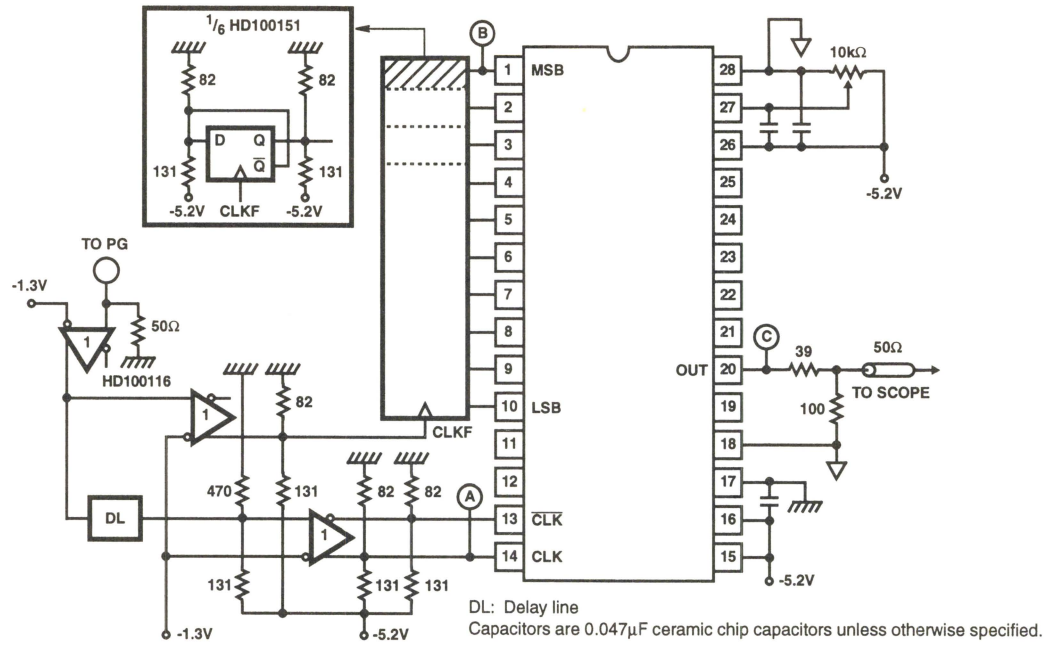


FIGURE 11. MAXIMUM CONVERSION RATE, RISE TIME, FALL TIME, PROPAGATION DELAY, SETUP TIME, HOLD TIME AND SETTLING TIME CIRCUIT

Measuring Settling Time

Settling time is measured as follows. The relationship between V and $V_{0(FS)}$ as shown in the D/A output waveform in Figure 12 is expressed as

$$V = V_{0(FS)} (1 - e^{-t\tau}).$$

The settling time for respective accuracy of 10, 9 and 8-bit is specified as

$V = 0.9995\ V_{0(FS)}$
$V = 0.999\ V_{0(FS)}$
$V = 0.999\ V_{0(FS)}$

which results in the following:

$t_S = 7.60\tau$ for 10-bit,
$t_S = 6.93\tau$ for 9-bit, and
$t_S = 6.24\tau$ for 8-bit,

Rise time (t_r) and fall time (t_f) are defined as the time interval to slew from 10% to 90% of full scale voltage ($V_{0(FS)}$):

$V = 0.1\ V_{0(FS)}$
$V = 0.9\ V_{0(FS)}$

and calculated as $t_r = t_f = 2.20\tau$.

The settling time is obtained by combining these expressions:

$t_S = 3.45t_r$ for 10-bit,
$t_S = 3.15t_r$ for 9-bit, and
$t_S = 6.24t_r$ for 8-bit

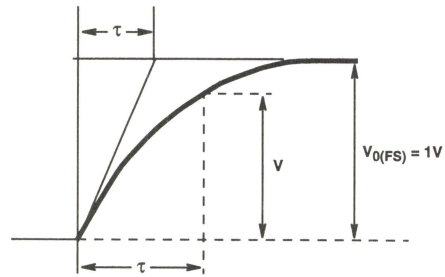


FIGURE 12. D/A OUTPUT WAVEFORM

Test Circuits (Continued)

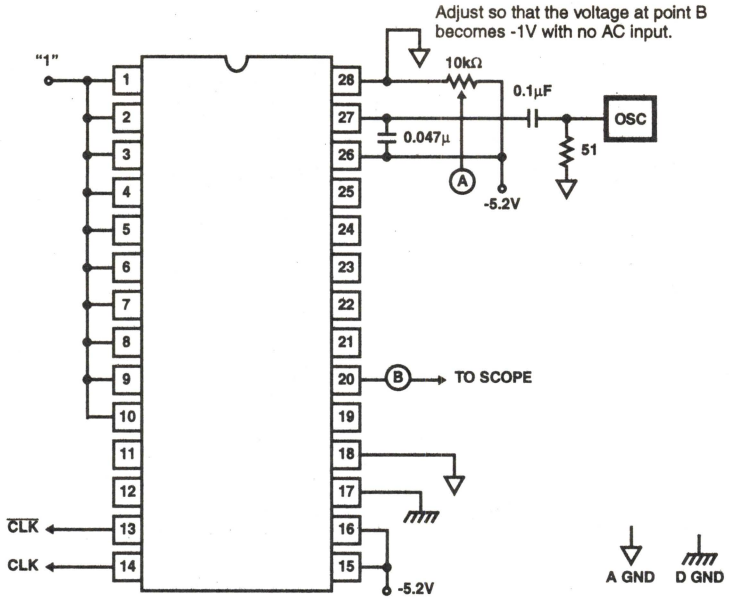


FIGURE 13A.

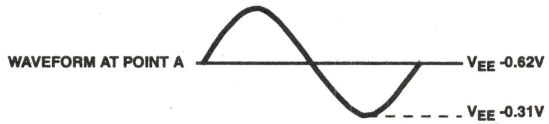


FIGURE 13B.

FIGURE 13C.

FIGURE 13. MULTIPLYING BANDWIDTH

HARRIS SEMICONDUCTOR

HI20203

8-Bit, 160 MSPS, Ultra High-Speed D/A Converter

August 1997

Features

- Throughput Rate 160MHz
- 8-Bit (HI20203) Resolution
- Differential Linearity Error ..... 0.5 LSB
- Low Glitch Noise
- Analog Multiplying Function
- Low Power Consumption 420mW
- Evaluation Board Available
- Direct Replacement for the Sony CX20201-3, CX20202-3

Applications

- Wireless Communications
- Signal Reconstruction
- Direct Digital Synthesis
- High Definition Video Systems
- Digital Measurement Systems
- Radar

Description

The HI20203 is an 8-bit, 160MHz ultra high speed D/A converter. The converter is based on an R2R switched current source architecture that includes an input data register with a complement feature and is Emitter Coupled Logic (ECL) compatible.

The HI20203 is an 8-bit accurate D/A with a linearity error of 0.5 LSB.

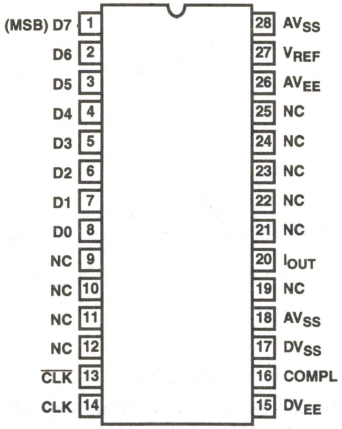
For 10-bit resolution, please refer to the HI20201 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI20203JCB	-20 to 75	28 Ld SOIC	M28.3A-S
HI20203JCP	-20 to 75	28 Ld PDIP	E28.6A-S

Pinout

HI20203
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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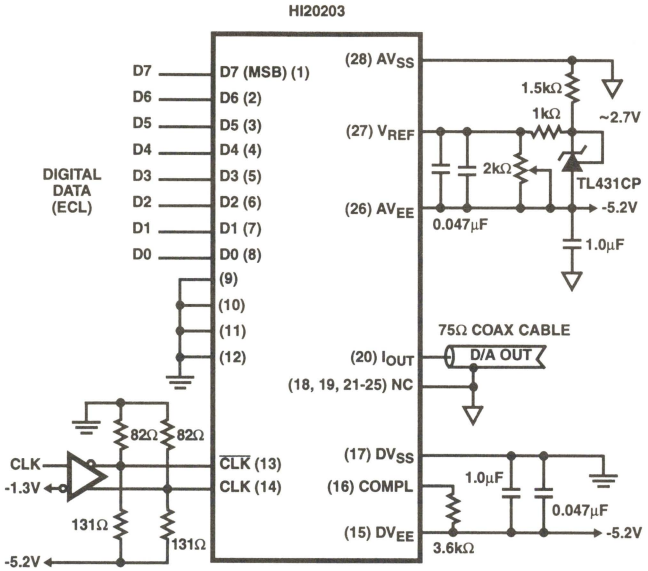
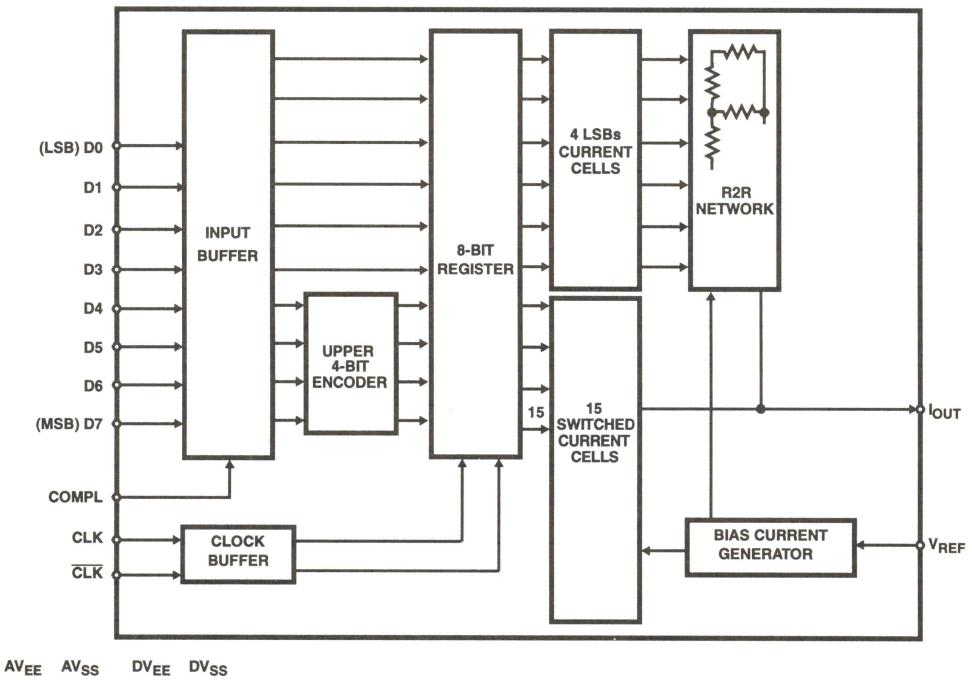
File Number 4096.1

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Digital Supply Voltage DV_{EE} to DV_{SS} ..... -7.0V
Analog Supply Voltage AV_{DD} to AV_{SS} ..... -7.0V
Digital Input Voltage ..... +0.3 to DV_{EE} V
Reference Input Voltage ..... +0.3 to AV_{EE} V
Output Current 20mA

Thermal Information

Thermal Resistance (Typical, Note 5) θ_{JA} ($^oC/W$)
SOIC Package 67
PDIP Package 58
Maximum Junction Temperature ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(SOIC - Lead Tips Only)

Operating Conditions

Supply Voltage
AV_{EE}, DV_{EE} ..... -4.75V to -5.45V
AV_{EE} - DV_{EE} ..... -0.05V to +0.05V
Digital Input Voltage
V_{IH} ..... -1.0V to -0.7V
V_{IL} ..... -1.9V to -1.6V

Reference Input Voltage, V_{REE} ..... V_{EE} + 0.5V to V_{EE} + 1.4V
Load Resistance, R_L ..... Above 75Ω
Output Voltage, $V_{O(FS)}$ ..... 0.8V to 1.2V
Temperature Range ..... -20^oC to 75^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications AV_{EE} = -5.2V, DV_{EE} = -5.2V, AGND = 0V, DGND = 0V, $R_L = \infty$, V_{OUT} = -1V, $T_A = 25^oC$

PARAMETER	TEST CONDITION	HI20203JCB/JCP			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		8	-	-	Bits
Integral Linearity Error, INL	f_S = 160MHz (End Point)	-	-	±0.5	LSB
Differential Linearity Error, DNL	f_S = 160MHz	-	-	±0.50	LSB
Offset Error, V_{OS} (Adjustable to Zero)	(Note 3)	-	1.8	-	LSB
Full Scale Error, FSE (Adjustable to Zero)	(Note 3)	-	-	±26	LSB
Full Scale Output Current, I_{FS}		-	-	20	mA
DYNAMIC CHARACTERISTICS					
Throughput Rate	See Figure 11	160	-	-	MHz
Glitch Energy, GE	R_{OUT} = 75Ω	-	15	-	pV/s
REFERENCE INPUT					
Voltage Reference Input Range	With respect to AV_{EE}	+0.5	-	+1.4	V
Reference Input Current	V_{REF} = -4.58V	-0.1	-0.4	-3.0	µA
Voltage Reference to Output Small Signal Bandwidth	-3dB point $1V_{P-P}$ Input	-	14.0	-	MHz
Output Rise Time, t_r	R_{LOAD} = 75Ω	-	1.5	-	ns
Output Fall Time, t_f	R_{LOAD} = 75Ω	-	1.5	-	ns
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}	(Note 2)	-1.0	-0.89		V
Input Logic Low Voltage, V_{IL}	(Note 2)		-1.75	-1.6	V

Electrical Specifications AV_{EE} = -5.2V, DV_{EE} = -5.2V, AGND = 0V, DGND = 0V, R_L = ∞, V_{OUT} = -1V, T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITION	HI20203JCB/JCP			UNITS
		MIN	TYP	MAX	
Input Logic Current, I_{IL}, I_{IH} (For D9 thru D6, COMPL)	V_{IH} = -0.89V, V_{IL} = -1.75V (Note 2)	0.1	1.5	6.0	µA
Input Logic Current, I_{IL}, I_{IH} (For D5 thru D0)	V_{IH} = -0.89V, V_{IL} = -1.75V (Note 2)	0.1	0.75	3.0	µA
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 11	5	-	-	ns
Data Hold Time, t_{HLD}	See Figure 11	1	-	-	ns
Propagation Delay Time, t_{PD}	See Figure 11	-	3.8	-	ns
Settling Time, t_{SET} (to $^1/_2$ LSB)	See Figure 11	-	4.3	-	ns
POWER SUPPLY CHARACTERISITICS					
I_{EE}		-60	-75	-90	mA
Power Dissipation	75Ω load	-	420	470	mW

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. Excludes error due to reference drift.
4. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagram

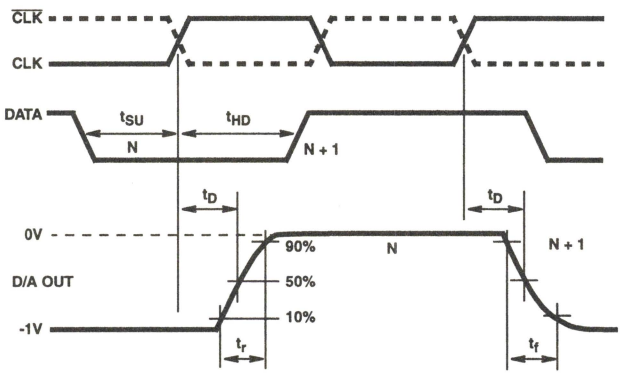


FIGURE 1. LADDER SETTLING TIME FULL POWER BANDWIDTH (LS)

Typical Performance Curves

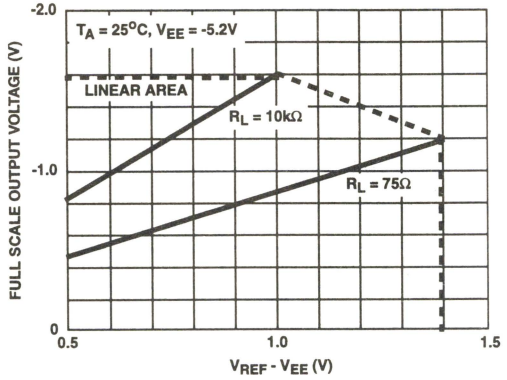


FIGURE 2. $V_{O(FS)}$ RATIO vs (V_{REF} - V_{EE})

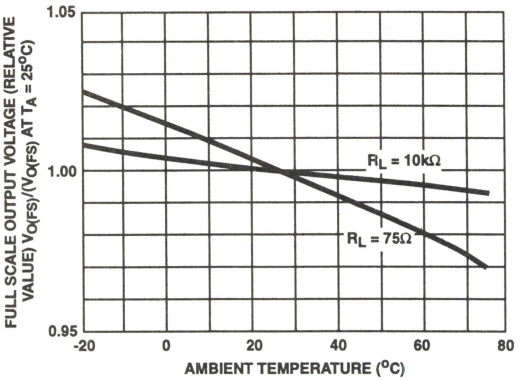


FIGURE 3. FULL SCALE OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

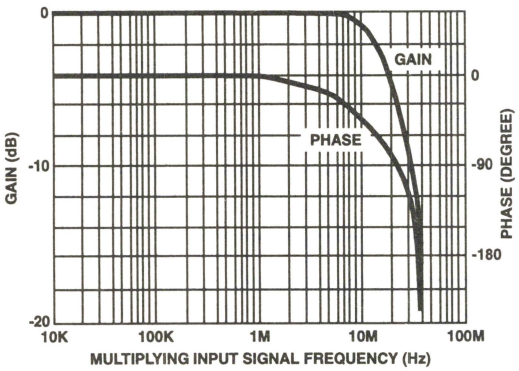


FIGURE 4. OUTPUT CHARACTERISTICS vs MULTIPLYING INPUT SIGNAL FREQUENCY

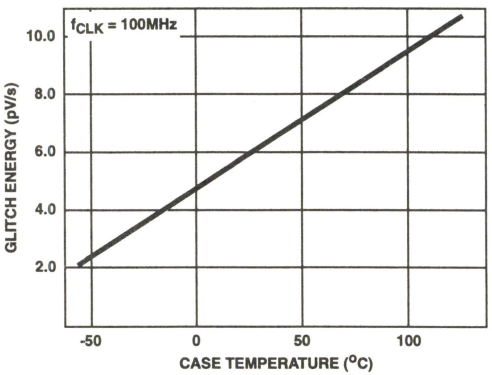


FIGURE 5. GLITCH ENERGY vs CASE TEMPERATURE (FULL SCALE - 1023mV)

Pin Descriptions

28 PIN SOIC	PIN NAME	PIN DESCRIPTION
1-8	D0 (LSB) - D7 (MSB)	Digital Data Bit 0, the Least Significant Bit thru Digital Data Bit 7, the Most Significant Bit.
11, 12, 19, 21-25	NC	No connect, not used.
13	$\overline{CLK}$	Negative Differential Clock Input.
14	CLK	Positive Differential Clock Input
15	DV_{EE}	Digital (ECL) Power Supply -4.75V to -7V.
16	COMPL	Data Complement Pin. When set to a (ECL) logic High the input data is complemented in the input buffer. When cleared to a (ECL) logic Low the input data is not complemented.
17	DV_{SS}	Digital Ground.
18	AV_{SS}	Analog Ground.
20	I_{OUT}	Current Output Pin.
26	AV_{EE}	Analog Supply -4.75V to -7V.
27	V_{REF}	Input Reference Voltage used to set the output full scale range.
28	AV_{SS}	Analog Ground

Detailed Description

The HI20203 is an 8-bit, current-output D/A converter. The converter has 10 data bits but yields 8-bit performance.

Architecture

The HI20203 is a combined R2R/segmented current source design. The 6 least significant bits of the converter are derived by a traditional R2R network to binary weight the 1mA current sources. The upper 4 most significant bits are implemented as segmented or thermometer encoded current sources. The encoder converts the incoming 4 bits to 15 control lines to enable the most significant current sources. The thermometer encoder will convert binary to individual control lines. See Table 1.

TABLE 1. THERMOMETER ENCODER

MSB	BIT 6	BIT 5	BIT 4	THERMOMETER CODE 1 = ON, 0 = OFF I_{15} - I_0
0	0	0	0	000 0000 0000 0000
0	0	0	1	000 0000 0000 0001
0	0	1	0	000 0000 0000 0011
0	0	1	1	000 0000 0000 0111
0	1	0	0	000 0000 0000 1111
0	1	0	1	000 0000 0001 1111
0	1	1	0	000 0000 0011 1111
0	1	1	1	000 0000 0111 1111
1	0	0	0	000 0000 1111 1111
1	0	0	1	000 0001 1111 1111
1	0	1	0	000 0011 1111 1111
1	0	1	1	000 0111 1111 1111
1	1	0	0	000 1111 1111 1111
1	1	0	1	001 1111 1111 1111
1	1	1	0	011 1111 1111 1111
1	1	1	1	111 1111 1111 1111

The architecture of the HI20203 is designed to minimize glitch while providing a manufacturable 10-bit design that does not require laser trimming to achieve good linearity.

Glitch

Glitch is caused by the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). In an ECL system where the logic levels switch from one non-saturated level to another, the switching times can be considered close to symmetrical. This helps to reduce glitch in the D/A. Unequal delay paths through the device can also cause one current source to change before another. To minimize this the Harris HI20203 employs an internal register, just prior to the current sources, that is updated on the clock edge. Lastly the worst case glitch usually happens at the major transition i.e., 01 1111 1111 to 10 0000 0000. But in the HI20203 the glitch is moved to the 00 0001 1111 to 11 1110 0000 transition. This is achieved by the split R2R/segmented current source architecture. This decreases the amount of current switching at any one time and makes the glitch practically constant over the entire output range. By making the glitch a constant size over the entire output range this effectively integrates this error out of the end application.

In measuring the output glitch of the HI20203 the output is terminated into a 75Ω load. The glitch is measured at the major carry's throughout the DACs output range.

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 7 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt/seconds (pV/s).

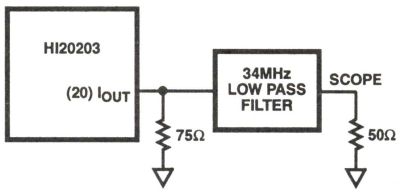


FIGURE 6. HI20203 GLITCH TEST CIRCUIT

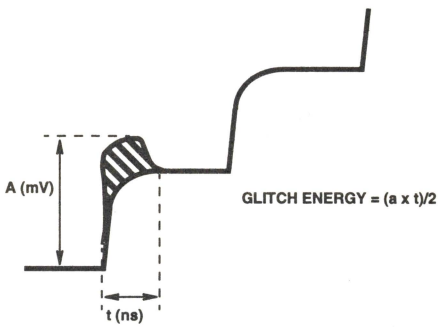


FIGURE 7. GLITCH ENERGY

Setting Full Scale

The Full Scale output voltage is set by the Voltage Reference pin (27). The output voltage performance will vary as shown in Figure 2.

The output structure of the HI20203 can handle down to a 75Ω load effectively. To drive a 50Ω load Figure 8 is suggested. Note the equivalent output load is ~75Ω.

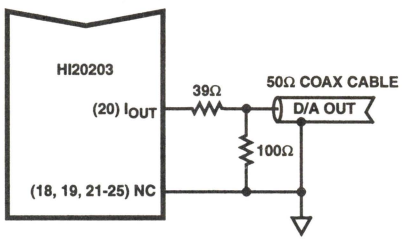


FIGURE 8. HI20203 DRIVING A 50Ω LOAD

Variable Attenuator Capability

The HI20203 can be used in a multiplying mode with a variable frequency input on the V_{REF} pin. In order for the part to operate correctly a DC bias must be applied and the incoming AC signal should be coupled to the V_{REF} pin. See Figure 13 for the application circuit. The user must first adjust the DC reference voltage. The incoming signal must be attenuated so as not to exceed the maximum (+1.4V) and minimum (+0.5V) reference input. The typical output Small Signal Bandwidth is 14MHz.

Integral Linearity

The Integral Linearity is measured using the End Point method. In the End Point method the gain is adjusted. A line is then established from the zero point to the end point or Full Scale of the converter. All codes along the transfer curve must fall within an error band of 1 LSB of the line. Figure 10 shows the linearity test circuit.

Differential Linearity

The Differential Linearity is the difference from the ideal step. To guarantee monotonicity a maximum of 1 LSB differential error is allowed. When more than 1 LSB is specified the converter is considered to be missing codes. Figure 10 shows the linearity test circuit.

Clock Phase Relationship

The HI20203 is designed to be operated at very high speed (i.e., 160MHz). The clock lines should be driven with ECL100K logic for full performance. Any external data drivers and clock drivers should be terminated with 50Ω to minimize reflections and ringing.

Internal Data Register

The HI20203 incorporates a data register as shown in the Functional Block Diagram. This register is updated on the rising edge of the CLK line. The state of the Complement bit (COMPL) will determine the data coding. See Table 2.

TABLE 2. INPUT CODING TABLE

INPUT CODE	OUTPUT CODE	
	COMPL = 1	COMPL = 0
00 0000 0000	0	-1
10 0000 0000	-0.5	-0.5
11 1111 1111	-1	0

Thermal Considerations

The temperature coefficient of the full scale output voltage and zero offset voltage depend on the load resistance connected to I_{OUT}. The larger the load resistor the better (i.e., smaller) the temperature coefficient of the D/A. See Figure 3 in the performance curves section.

Noise Reduction

Digital switching noise must be minimized to guarantee system specifications. Since 1 LSB corresponds to 1mV for 10-bit resolution, care must be taken in the layout of a circuit board.

Separate ground planes should be used for DV_{SS} and AV_{SS}. They should be connected back at the power supply.

Separate power planes should be used for DV_{EE} and AV_{EE}. They should be decoupled with a 1µF tantalum capacitor and a ceramic 0.047µF capacitor positioned as close to the body of the IC as possible.

Test Circuits and Waveforms

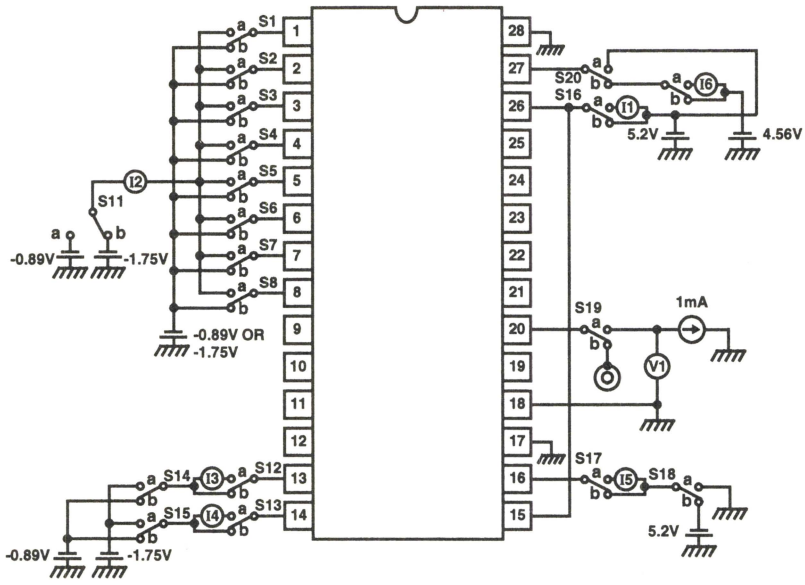
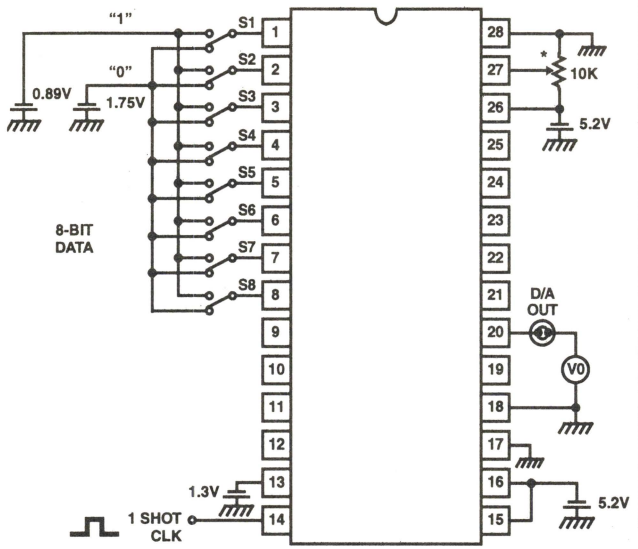


FIGURE 9. CURRENT CONSUMPTION, INPUT CURRENT AND OUTPUT RESISTANCE

Test Circuits and Waveforms (Continued)

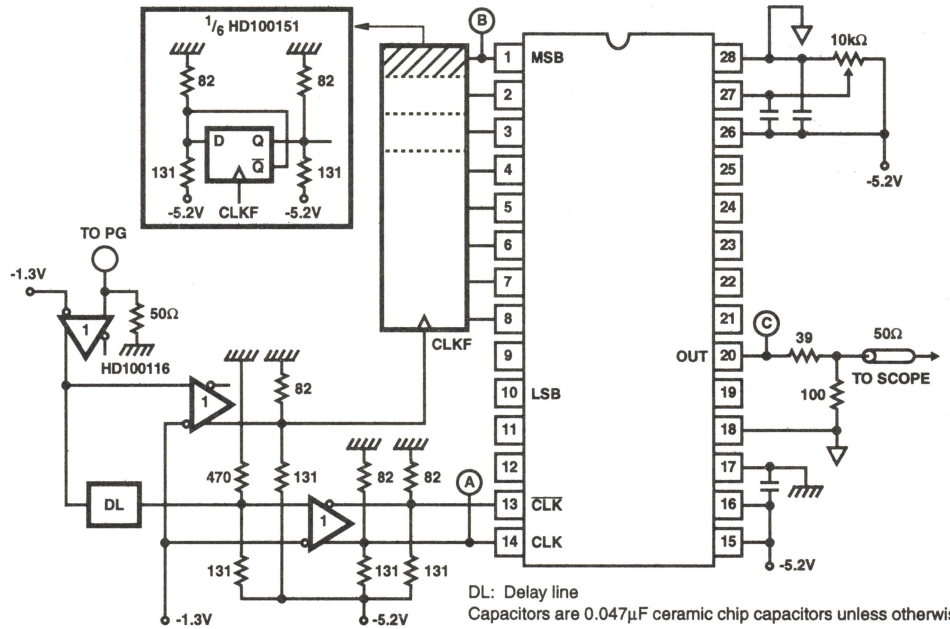


LINEARITY ERRORS ARE MEASURED AS FOLLOWS						
S1	S2	S3	••••	S7	S8	D/A OUT
0	0	0	••••	0	0	V_0
0	0	0	••••	0	1	V_1
0	0	0	••••	1	0	V_2
			⋮			⋮
1	1	1	••••	1	1	V_{255}

INTEGRAL LINEARITY ERROR	DIFFERENTIAL LINEARITY ERROR
V_0	
V_1	$V_1 - V_0$
V_2	$V_2 - V_1$
V_4	$V_4 - V_3$
V_8	$V_8 - V_7$
V_{16}	$V_{16} - V_{15}$
V_{32}	$V_{32} - V_{31}$
V_{64}	$V_{64} - V_{63}$
V_{128}	$V_{128} - V_{127}$
⋮	⋮
V_{255}	

Error at individual measurement points are calculated according to the following definition.
$(V_{255} - V_0)/1023 = V_{0(FS)}/255 \equiv 1$ LSB.

FIGURE 10. DIFFERENTIAL LINEARITY ERROR AND LINEARITY ERROR



DL: Delay line
Capacitors are 0.047µF ceramic chip capacitors unless otherwise specified.

FIGURE 11. MAXIMUM CONVERSION RATE, RISE TIME, FALL TIME, PROPAGATION DELAY, SETUP TIME, HOLD TIME AND SETTLING TIME

Test Circuits and Waveforms (Continued)

Measuring Settling Time

Settling time is measured as follows. The relationship between V and $V_{0(FS)}$ as shown in the D/A output waveform in Figure 12 is expressed as

$$V = V_{0(FS)} (1 - e^{-t\tau}).$$

The settling time for respective accuracy of 10, 9 and 8-bit is specified as

$V = 0.9995\ V_{0(FS)}$
$V = 0.999\ V_{0(FS)}$
$V = 0.999\ V_{0(FS)}$

which results in the following:

$t_S = 7.60\tau$ for 10-bit,
$t_S = 6.93\tau$ for 9-bit, and
$t_S = 6.24\tau$ for 8-bit,

Rise time (t_r) and fall time (t_f) are defined as the time interval to slew from 10% to 90% of full scale voltage ($V_{0(FS)}$):

$V = 0.1\ V_{0(FS)}$
$V = 0.9\ V_{0(FS)}$

and calculated as $t_r = t_f = 2.20\tau$.

The settling time is obtained by combining these expressions:

$t_S = 3.45t_r$ for 10-bit,
$t_S = 3.15t_r$ for 9-bit, and
$t_S = 6.24t_r$ for 8-bit

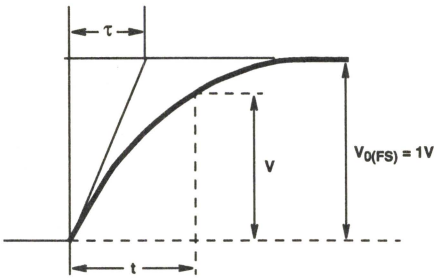


FIGURE 12. D/A OUTPUT WAVEFORM

Test Circuits and Waveforms (Continued)

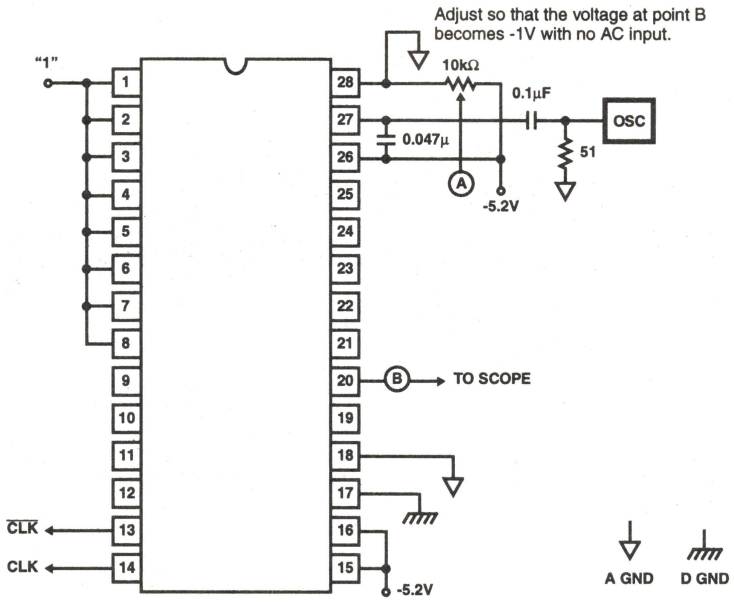


FIGURE 13A.

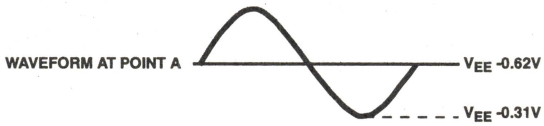


FIGURE 13B.

FIGURE 13C.

FIGURE 13. MULTIPLYING BANDWIDTH

HARRIS SEMICONDUCTOR

HI20206

NOT RECOMMENDED FOR NEW DESIGNS
See HI1178

August 1997

Triple 8-Bit, 35 MSPS, RGB, 3-Channel D/A Converter

Features

- Resolution ..... Triple 8-Bit
- Maximum Conversion Speed 35MHz
- RGB 3-Channel Input/Output
- Differential Linearity Error ..... $\pm 1/2$ LSB
- Digital Input Voltage ..... TTL Level
- Output Voltage Full-Scale ..... $1V_{P-P}$ (Typ)
- Low Power Consumption ..... 360mW (Typ)
- +5V Single Power Supply
- Direct Replacement for Sony CX20206

Applications

- Digital TV
- Graphics Display
- High Resolution Color Graphics
- Video Reconstruction
- Instrumentation
- Image Processing
- I/Q Modulation

Description

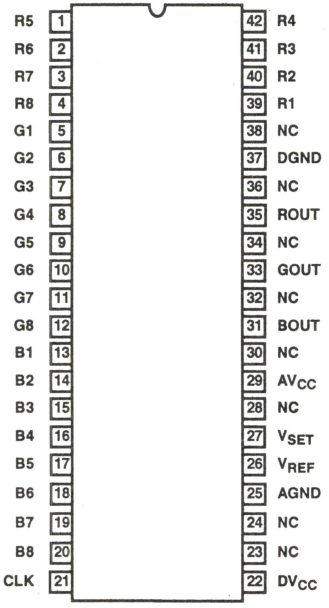
The HI20206 is a triple 8-bit, high-speed, bipolar D/A converter designed for video band use. It has three separate, 8-bit pixel inputs, one each for red, green, and blue video data. A single 5.0V power supply and pixel clock input is all that is required to make the device operational. A bias voltage generator is internal. For lower CMOS power consumption, refer to the HI1178.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI20206JCP	-20 to 75	42 Ld PDIP	E42.6B-S

Pinout

HI20206 (PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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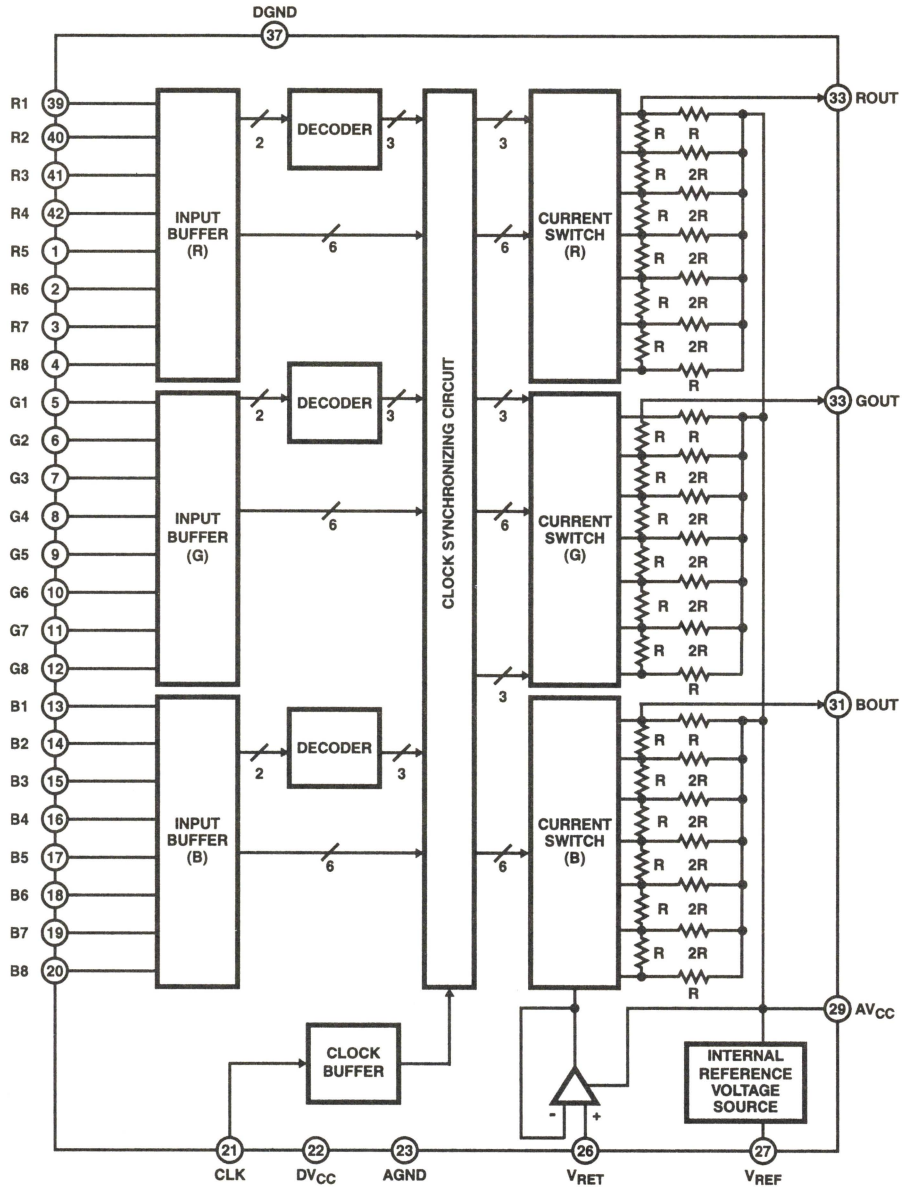
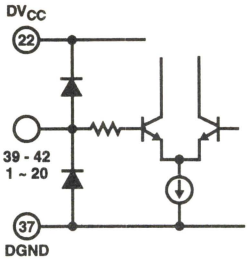
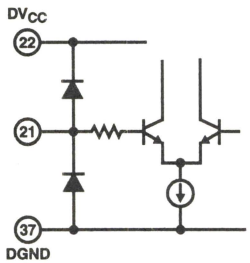
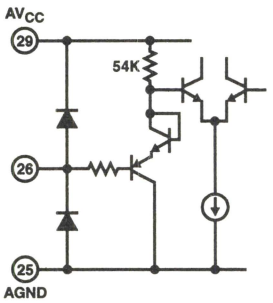
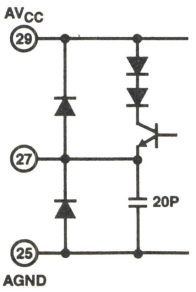
File Number **4111.1**

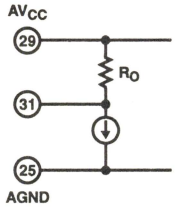
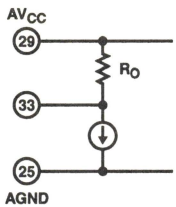
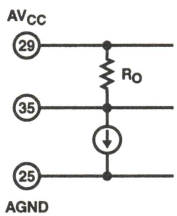
Functional Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 To 20 39 To 42	R1 To R8 G1 To G8 B1 To B8		Digital Input pin. From pins 39 to 42 and from 1 to 4 are for RED. R1 is MSB and R8 is LSB. From pins 5 to 12 are for GREEN. G1 is MSB and G8 is LSB. From pins 13 to 20 are for BLUE. B1 is MSB and B8 is LSB.
21	CLK		Clock Input pin.
22	DV_{CC}		Digital V_{CC}.
23 24	NC		No Connect.
25	AGND		Analog GND.
26	V_{SET}		Bias Input pin. Normally, apply 0.8V.
27	V_{REF}		Internal Reference Voltage Output pin 1.2V (Typ). A pulldown resistance is necessary externally.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
28	NC		No Connect.
29	AV_{CC}		Analog V_{CC}.
30	NC		Vacant pin but connect to AV_{CC} (Note 1).
31	BOUT		Analog Output pin for BLUE.
32	NC		Vacant pin but connect to AV_{CC} (Note 1).
33	GOUT		Analog Output pin for GREEN.
34	NC		Vacant pin but connect to AV_{CC} (Note 1).
35	ROUT		Analog Output pin for RED.
36	NC		Vacant pin but connect to AV_{CC} (Note 1).
37	DGND		Digital GND.
38	NC		No Connect.

NOTE:

1. Pins 30, 32, 34 and 36 are vacant, but in order to reduce interference between the individual RGB outputs, connect them to AV_{CC}.

Absolute Maximum Ratings

Supply Voltage (V_{CC}) . . . . . .0V to 7V
Input Voltage (Digital) (V_I, V_{CLK}) . . . . . -0.3V to V_{CC}
Output Voltage (Analog) (V_{SET}) . . . . . V_{CC} -2.1V to V_{CC}
Output Current
  Analog (I_{OUT}) . . . . . -3mA to 10mA
  V_{REF} Pin (I_{REF}) . . . . . -5mA to 0mA
Supply Voltage Range (Typ) . . . . . 5V to 10V

Recommended Operating Conditions

Supply Voltage
  AV_{CC}, DV_{CC} . . . . . .4.5V to 5.5V
  AV_{CC}-DV_{CC} . . . . . -0.2V to 0.2V
  AGND-DGND . . . . . -0.05V to 0.05V
Digital Input Voltage
  H Level (V_{IH}, V_{CLKH}) . . . . . .2.0V to DV_{CC}
  L Level (V_{IL}, V_{CLKL}) . . . . . DGND to 0.8V
V_{SET} Input Voltage (V_{SET}) . . . . . .0.7V to 0.9V
V_{REF} Pin Current (I_{REF}) . . . . . -3mA to -0.4mA
Clock Pulse Width
  t_{PW1} 15ns
  t_{PW0} 10ns
Temperature Range (T_{OPR}) . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	70

Maximum Storage Temperature Range (T_{STG}) . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = 25°C, AV_{CC} = DV_{CC} = 5V, AGND = DGND = 0V

PARAMETER			SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution			RSL		-	8	-	Bit
Monotonic			MNT		-	Guarantee	-	-
Differential Linearity Error			DLE	V_{SET} - AGND = 0.8V, R_L > 10kΩ	-0.5	-	0.5	LSB
Integral Linearity Error			ILE		-0.4	-	0.4	% of Full Scale
Maximum Conversion Speed			f_{MAX}	V_{SET} - AGND = 0.8V, R_L > 10kΩ, C_L < 20pF	35	-	-	MHz
Full Scale Output Voltage (Note 3)			V_{OFS}		0.85	1.0	1.15	V_{P-P}
RGB Output Voltage Full Scale Ratio (Note 4)			FSR		0	4	8	%
Output Zero Offset Voltage			V_{OFFSET}		-40	-6	0	mV
Output Resistance			R_O		270	340	420	Ω
Dissipation Current			I_D	V_{SET} - AGND = 0.8V, R_L > 10kΩ, I_{REF} = -400µA	54	72	90	mA
Digital Data Input Current	H Level	Upper 2 Bits	$I_{IH(U)}$	V_I = DV_{CC}	-	1.2	20	µA
		Lower 6 Bits	$I_{IH(L)}$		-	0.6	10	µA
	L Level	Upper 2 Bits	$I_{IL(U)}$	V_I = DGND	-10	0	10	µA
		Lower 6 Bits	$I_{IL(U)}$		-10	0	10	µA
Clock Input Current		H Level	I_{CLKH}	V_{CLK} = DV_{CC}	-	3	30	µA
		L Level	I_{CLKL}	V_{CLK} = DGND	-10	0	10	µA
V_{SET} Input Current			I_{SET}	V_{SET} - AGND = 0.8V	-5	-0.3	0	µA
Internal Reference Voltage			V_{REF}	I_{REF} = -400µA	1.08	1.20	1.32	V
Set-Up Time			t_S		12	-	-	ns
Hold Time			t_H		3	-	-	ns
Crosstalk Among R, G and B			CT	D/A OUT: 1V_{P-P}, R_L>10kΩ, C_L<20pF, f_{DATA} = 7MHz, f_{CLK} = 14MHz, See Figure 5	-	-40	-33	dB

Electrical Specifications $T_A = 25^oC$, $AV_{CC} = DV_{CC} = 5V$, AGND = DGND = 0V **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Glitch Energy	GE	V_{SET} - AGND = 0.8V, R_L>10kΩ, f_{CLK} = 1MHz, Digital Ramp Output, See Figure 6 (Note 5)	-	160	-	pV/s
Rise Time (Note 6)	t_r	V_{SET} - AGND = 0.8V See Figure 4	-	5.5	-	ns
Fall Time (Note 6)	t_f		-	5.0	-	ns
Settling Time	t_{SET}		-	16	-	ns

NOTES:

3. AV_{CC} - V_O.
4. Maximum value among $100 \times \left|\frac{V_{OFS(R)}}{V_{OFS(G)}} - 1\right|$, $100 \times \left|\frac{V_{OFS(G)}}{V_{OFS(B)}} - 1\right|$, or $100 \times \left|\frac{V_{OFS(B)}}{V_{OFS(R)}} - 1\right|$.
5. Observe the glitch which is generated when the digital input varies as follows:
   0 0 1 1 1 1 1 1 — 0 1 0 0 0 0 0 0
   01 1 1 1 1 1 1 1 — 1 0 0 0 0 0 0 0
   10 1 1 1 1 1 1 1 — 1 1 0 0 0 0 0 0
6. The time required for the D/A OUT to arrive at 90% of its final value from 10%.

INPUT CORRESPONDING TABLE

INPUT CODE (MSB … LSB)	OUTPUT VOLTAGE
11111111	$V_{CC} + V_{OFFSET}$
•	•
•	•
•	•
10000000	$V_{CC} + V_{OFFSET}$ -0.5V
•	•
•	•
•	•
00000000	$V_{CC} + V_{OFFSET}$ -1.0V

NOTE: In case the output voltage full scale is 1V (1 LSB = 3.92mV).

Test Circuits

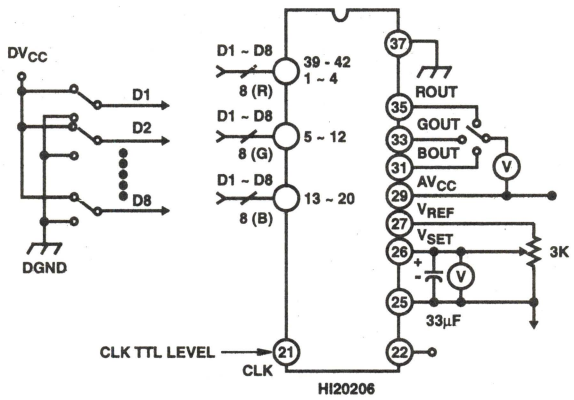


FIGURE 1. DIFFERENTIAL LINEARITY AND INTEGRAL LINEARITY TEST CIRCUITS

Test Circuits (Continued)

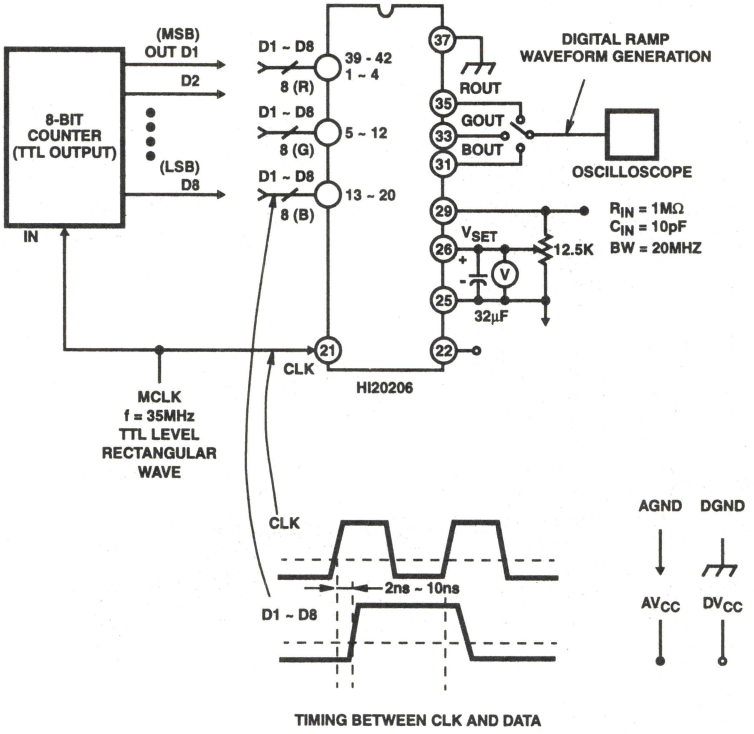


FIGURE 2. MAXIMUM CONVERSION RATE TEST CIRCUIT

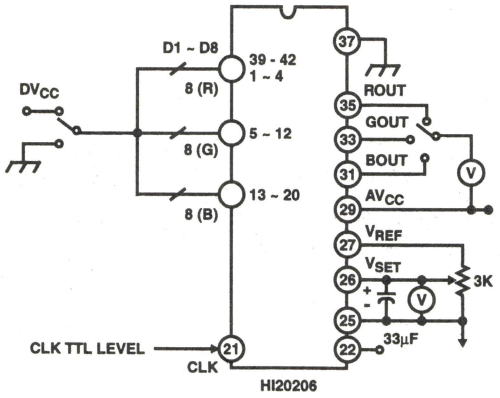


FIGURE 3. OUTPUT VOLTAGE FULL SCALE PRECISION, RGB OUTPUT VOLTAGE FULL SCALE RATIO, AND OUTPUT ZERO OFFSET VOLTAGE TEST CIRCUITS

Test Circuits (Continued)

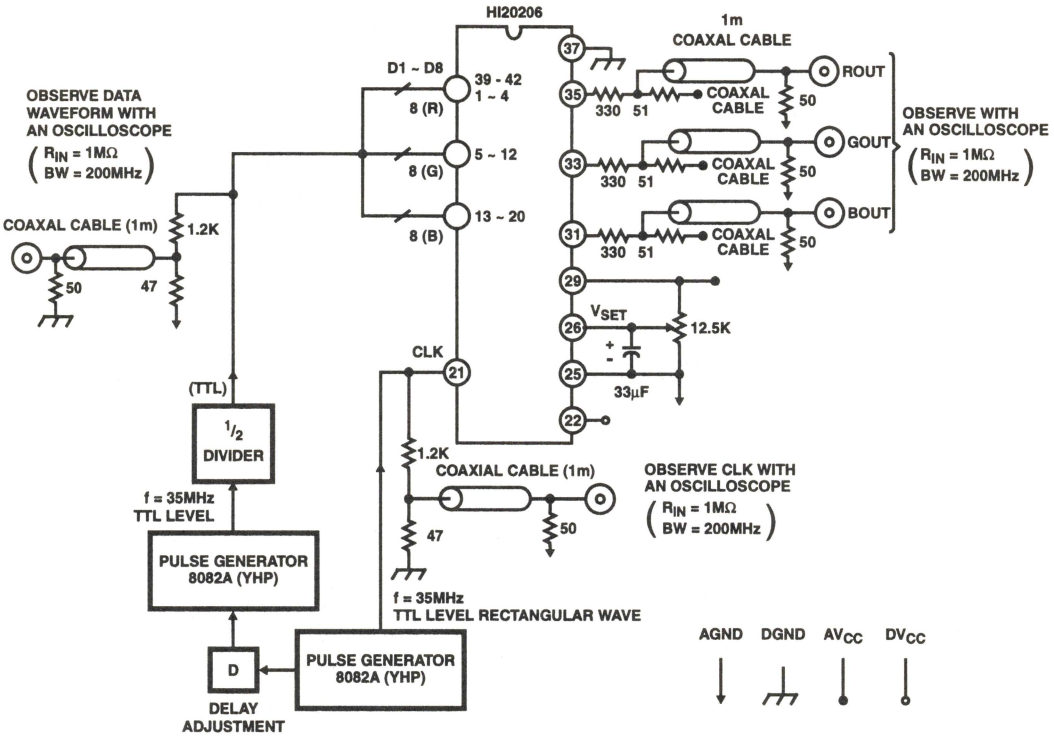
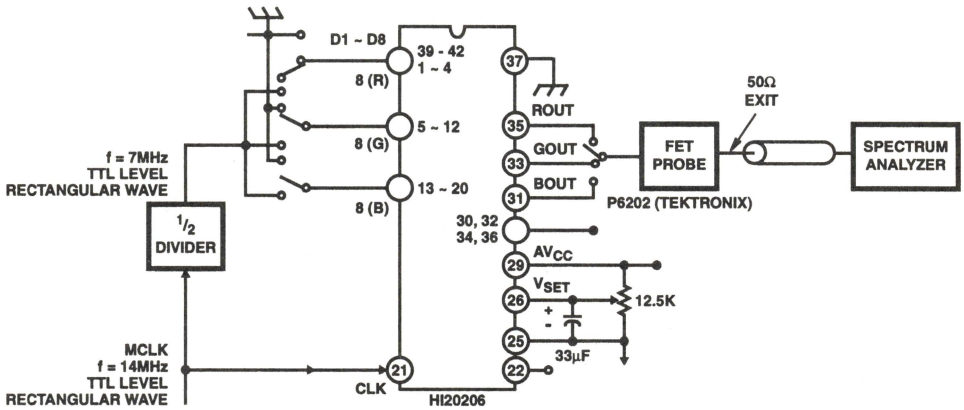


FIGURE 4. SET-UP TIME, HOLD TIME, AND RISE AND FALL TIME TEST CIRCUITS



Measuring Method, in case the measuring crosstalk of G → R:

1. Apply the data to G only, and measure the power of the frequency component of the data at R_{OUT}.
2. Apply the data to R only, and measure the power of the frequency component of the data at R_{OUT}.
3. Take the difference of the above two powers; the unit is in dB.

FIGURE 5. CROSSTALK AMONG R, G, AND B TEST CIRCUIT

Test Circuits (Continued)

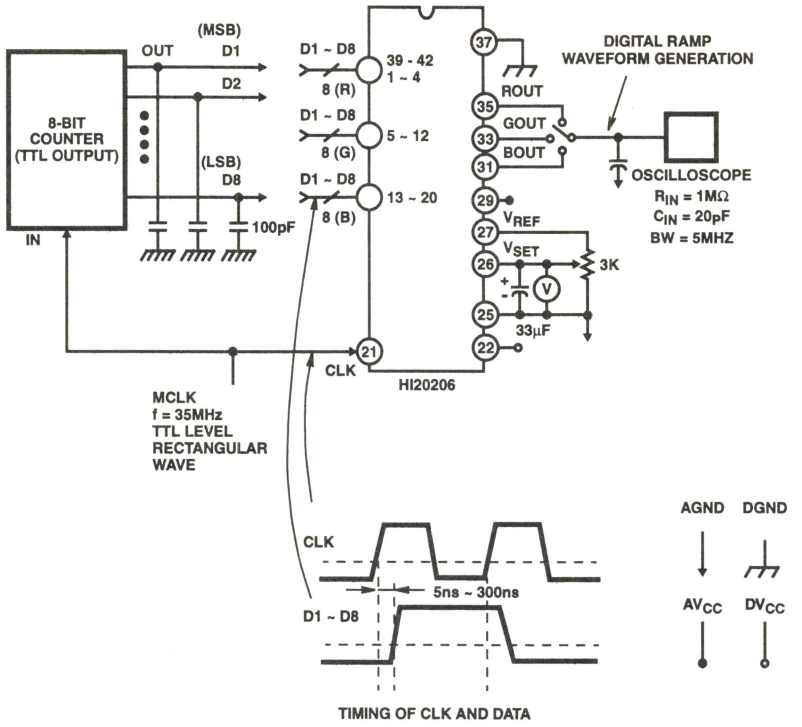
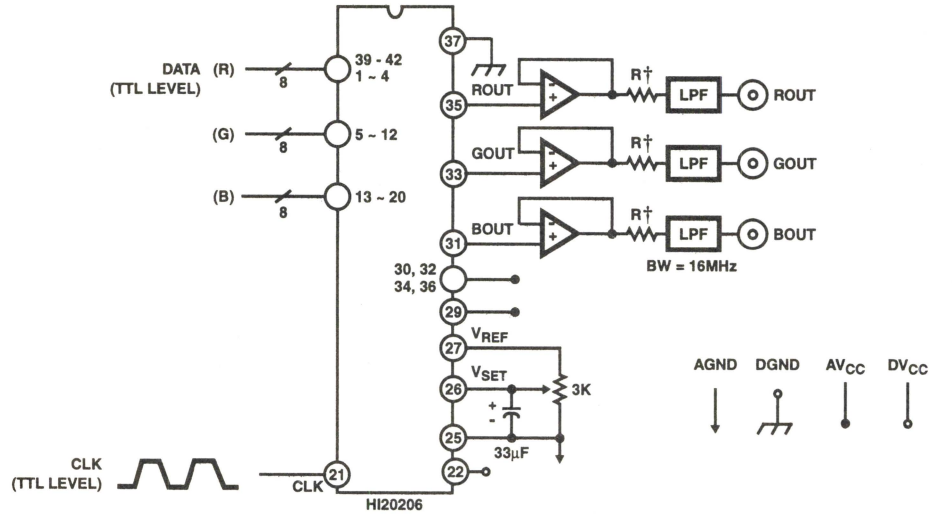


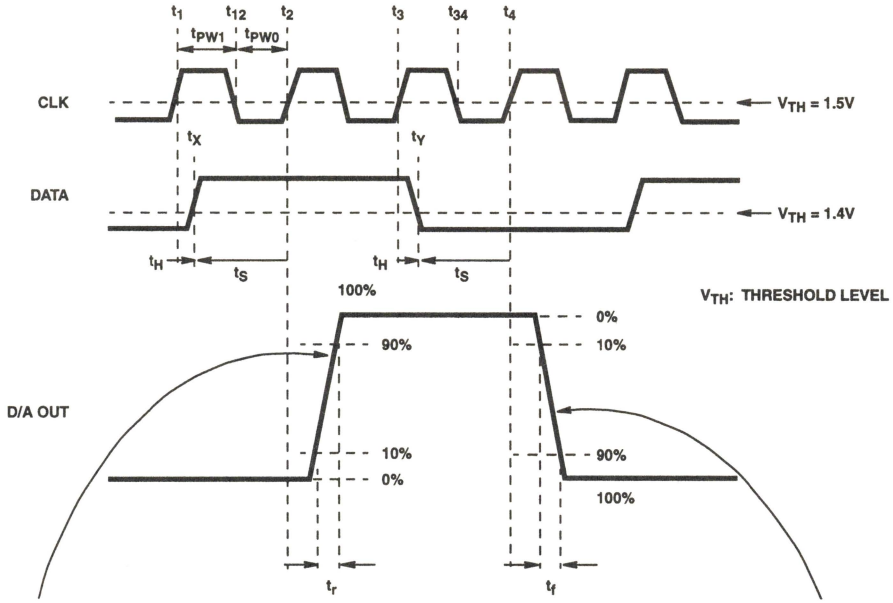
FIGURE 6. GLITCH ENERGY TEST CIRCUIT



†R is matching resistance for LPF.

FIGURE 7. APPLIED CIRCUIT EXAMPLE

Timing Diagram



NOTE: At the time $t = t_X$, the data of individual bits are switched and thereafter, when the CLK becomes L → H at $t = t_2$, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK. [In this case, fetching of the data is carried out at the fall of the CLK (at the time when $t = t_{12}$)].

NOTE: At the time $t = t_Y$, the data of individual bits are switched and thereafter when the CLK becomes L → H at $t = t_4$, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK. [In this case, fetching of the data is carried out at the fall of the CLK (at the time when $t = t_4$)].

FIGURE 8. TIMING CHART

Notes On Use

(1) Setting of pin 26 (V_{SET})

The full scale of the D/A output voltage changes by applying voltage to pin 26 (V_{SET}). When load is connected to pin 27 (V_{REF}), DC voltage of 1.2V is issued and the said voltage is dropped to 0.8V by resistance division.

When the 0.8V is applied to pin 26 (V_{SET}), the D/A output of $1V_{P-P}$ can be obtained.

(Example of use):

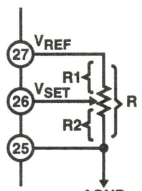


FIGURE 9.

(Adjustment Method)

1. The resistance R is determined in accordance with the recommended operating condition of I_{REF}, (current flowing through resistance R).
   See R vs I_{REF} of Figure 14. The calculation expression is as follows:
   $R = V_{REF}/I_{REF}$.
2. Adjust the volume so that the RGB output voltage full scale becomes 1V.
   (At this point, it becomes R1: R2 = 1:2).

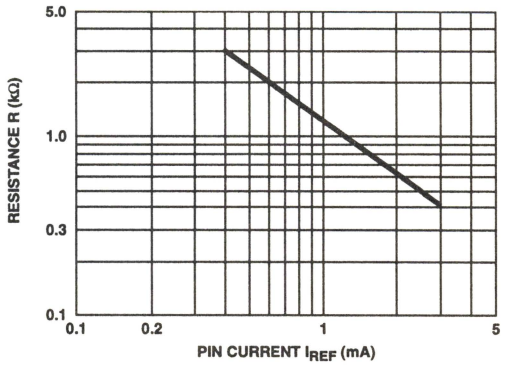


FIGURE 10. RESISTANCE vs V_{REF} PIN CURRENT

(2) Phase Relationship Between Data and Clock

In order to obtain the desired characteristics as a D/A converter, it is necessary to set the phase relationship correctly between the externally applied data and clock.

Satisfy the standard of the set-up time (t_S) and hold time (t_H) indicated in the electrical characteristics. As to the meaning of t_S and t_H, see the timing chart.

Moreover, the clock pulse width is desired to be as indicated in the recommended operating condition.

(3) Regarding the Load of D/A Output Pin

Receive the D/A output of the next stage with high impedance. In other words perform so that it becomes as follows:

$R_L > 10k\Omega$
$C_L < 20pF$.

The temperature characteristics indicated in the characteristics diagram has been measured under this condition.

However, when it is made $R_L \leq 10k\Omega$ the temperature characteristics may change considerably. In addition, when it is made to $C_L \geq 20pF$, the rise and fall of the D/A output become slow and will not operate at high speed.

(4) Noise Reduction Measures

As the D/A output voltage is a minute voltage of approximately 4mV per one step, ingenuity is required in reducing the noise entering from the outside of the IC as much as possible. Therefore, use the items given below as reference.

- When mounting onto the printed board, allow as much space as possible to the ground surface and the V_{CC} surface on the board and reduce the parasitic inductance and resistance.
- It is desirable that the AGND and DGND be separated in the pattern on the board. It is similar with AV_{CC} and DV_{CC}. As shown in the diagram below, for example, it is recommended that the wiring to the electric supply of AGND and DGND as also AV_{CC} and DV_{CC} be conducted separately, and then making AGND and DGND as also AV_{CC} and DV_{CC} in common right near the power supply respectively.
- Insert in parallel a 47µF tantalum capacitor and a 100pF ceramic capacitor between the V_{CC} surface on the printed board and the nearmost ground surface. (A of diagram below). It is also desirable to insert the above between the V_{CC} surface near the pin of the IC and the ground surface (see Figure 11). They are bypass capacitors to prevent bad effects from occurring to the characteristics when the power supply voltage fluctuates due to the clock, etc.

  It is recommended to reduce noise which overlaps the D/A output by inserting a capacitor of over 0.1µF between pin 25 (AGND) and pin 26 (V_{SET}).

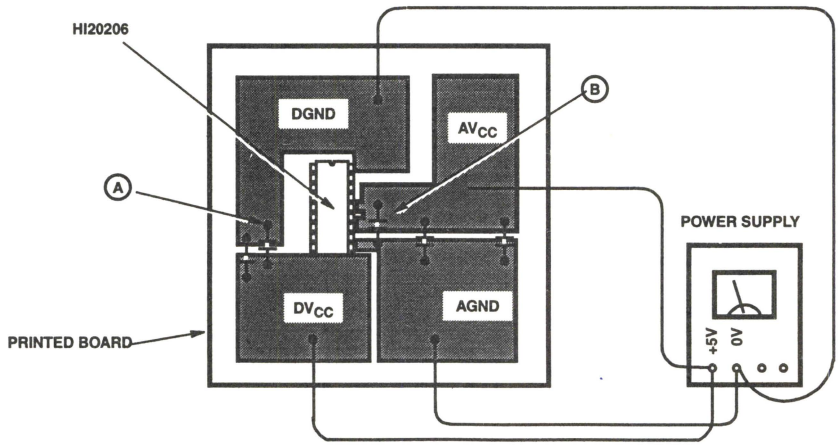


FIGURE 11.

Typical Performance Curves

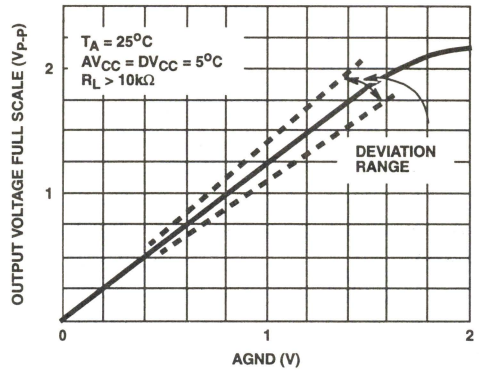


FIGURE 12. OUTPUT VOLTAGE FULL SCALE vs V_{SET} - AGND

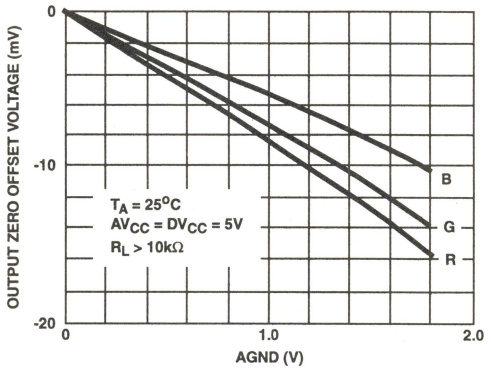


FIGURE 13. OUTPUT ZERO OFFSET VOLTAGE vs V_{SET} - AGND

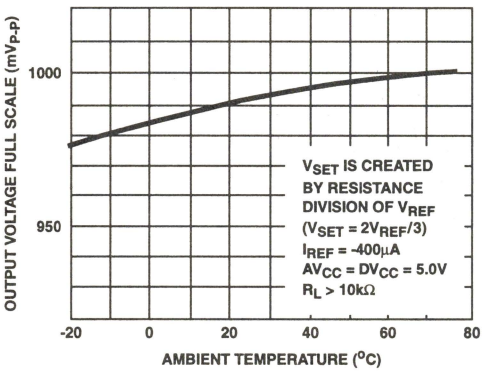


FIGURE 14. OUTPUT VOLTAGE FULL SCALE vs AMBIENT TEMPERATURE

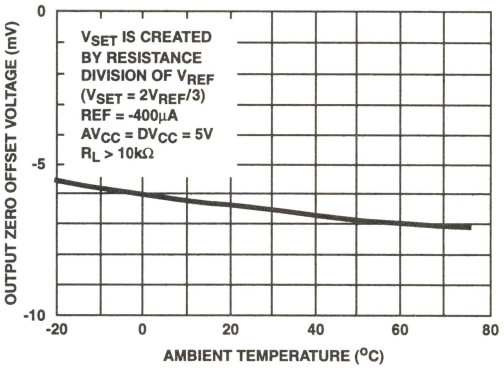


FIGURE 15. OUTPUT ZERO OFFSET vs AMBIENT TEMPERATURE

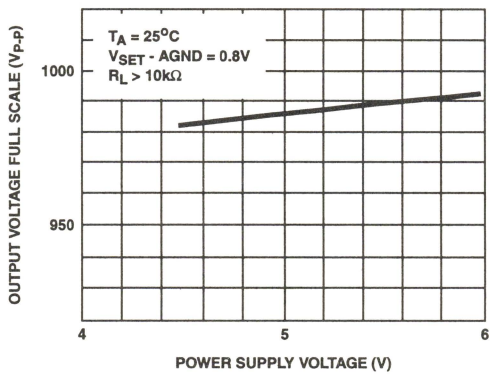


FIGURE 16. OUTPUT VOLTAGE FULL SCALE vs POWER SUPPLY VOLTAGE

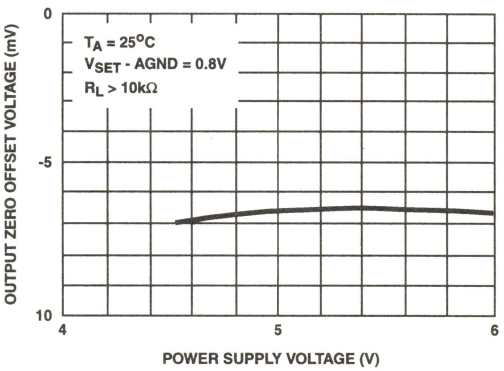


FIGURE 17. OUTPUT ZERO OFFSET VOLTAGE vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

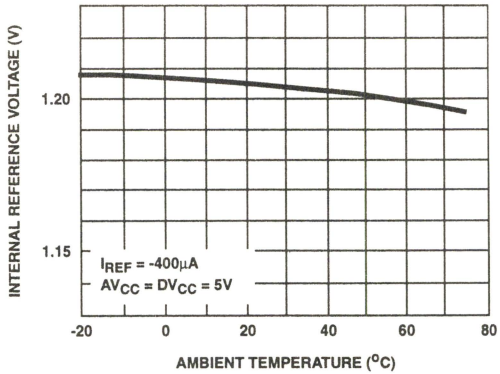


FIGURE 18. INTERNAL REFERENCE VOLTAGE vs AMBIENT TEMPERATURE

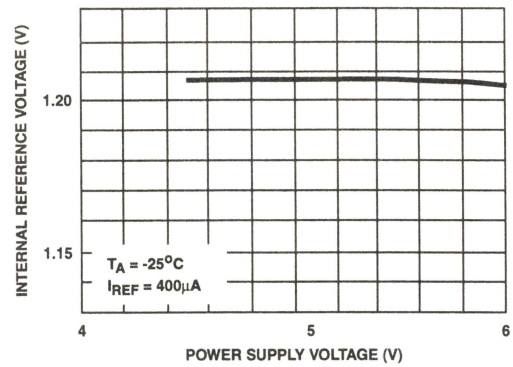


FIGURE 19. INTERNAL REFERENCE VOLTAGE vs POWER SUPPLY VOLTAGE

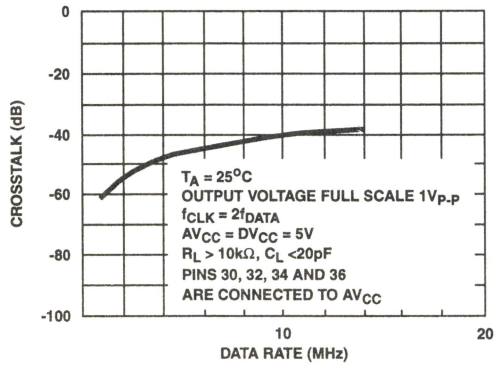


FIGURE 20. CROSSTALK AMONG R, G, AND B vs DATA RATE

HARRIS SEMICONDUCTOR

HI2304

August 1997

NOT RECOMMENDED FOR NEW DESIGNS
See HI1178

Triple 8-Bit, 20 MSPS, RGB, 3-Channel D/A Converter

Features

- Resolution ..... Triple 8-Bit
- Maximum Conversion Speed 20MHz
- RGB 3-Channel Input/Output
- Differential Linearity Error ..... ±0.5 LSB
- Low Power Consumption 50mW
  (330Ω Load for 1.2V_{P-P} Output)
- Single Power Supply ..... +3.3V
- Low Glitch Noise
- Direct Replacement for Sony CXD2304

Applications

- Digital TV
- Graphics Display
- High Resolution Color Graphics
- Video Reconstruction
- Instrumentation
- Image Processing
- I/Q Modulation

Description

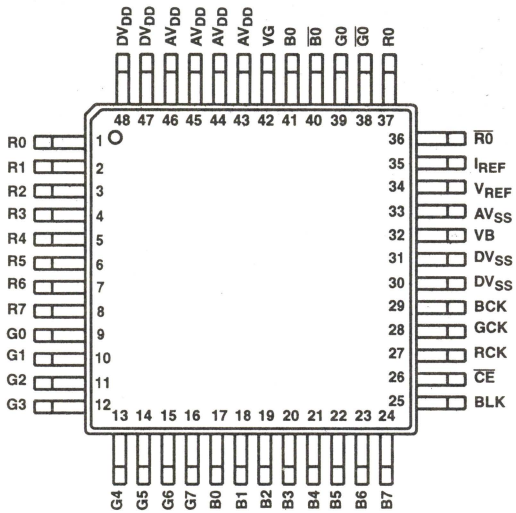
The HI2304 is a triple 8-bit, high-speed, CMOS D/A converter designed for video band use. It has three separate, 8-bit, pixel inputs, one each for red, green, and blue video data. A single 3.3V power supply and pixel clock input can be controlled individually, or connected together as one. The HI2304 also has BLANK video control signal. For faster speed and 5.0V operation, refer to the HI1178.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI2304JCQ	-20 to 75	48 Ld MQFP	Q48.7x7-S

Pinout

HI2304
(MQFP)
TOP VIEW



10 D/A CONVERTERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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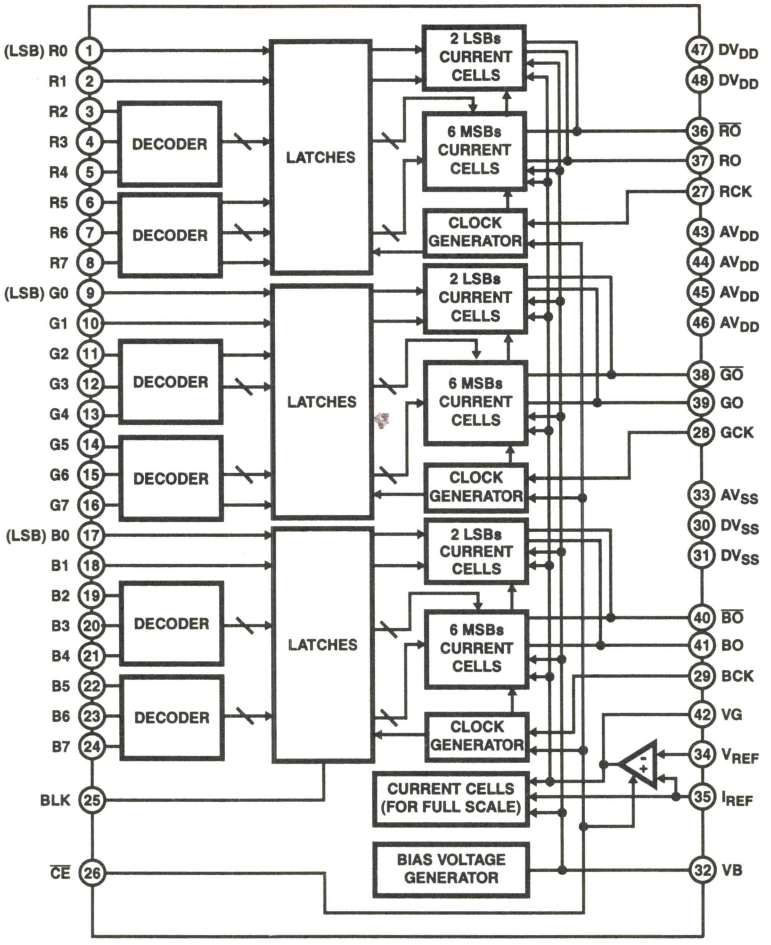
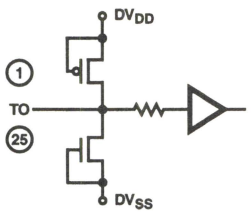
File Number 4116.1

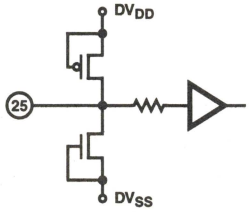
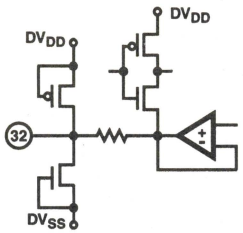
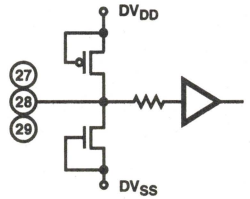
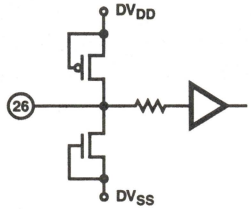
Functional Block Diagram



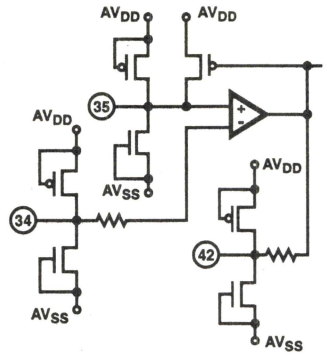
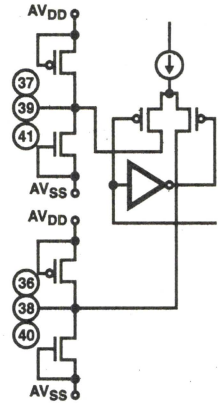
Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 8	R0 to R7		Digital Input.
9 to 16	G0 to G7		
17 to 24	B0 to B7		

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
25	BLK		Blanking pin. No signal at "H" (Output 0V) Output condition at "L".
32	VB		Connect a capacitor of about 0.1μF.
27	RCK		Clock Pin.
28	GCK		
29	BCK		
30, 31	DV_{SS}		Digital GND.
33	AV_{SS}		Analog GND.
26	$\overline{CE}$		Chip Enable Pin. No signal (Output 0V) at "H" and minimizes power consumption.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
35	I_{REF}		Connect a resistance 16 times "16R" that of output resistance value "R".
34	V_{REF}		Set full scale output value.
42	VG		Connect a capacitor of about 0.1µF.
43 to 46	AV_{DD}		Analog V_{DD}.
37	RO		Current output pin. Voltage output can be obtained by connecting a resistance.
39	GO		
41	BO		
36	$\overline{RO}$		Inverted current output pin. Normally dropped to analog GND.
38	$\overline{GO}$		
40	$\overline{BO}$		
47, 48	DV_{DD}		Digital V_{DD}.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Input Voltage (V_{IN}) . . . . . V_{DD} to V_{SS}
Output Current (I_{OUT}) . . . . . .0mA to 15mA
(Every Each Channel)

Operating Conditions

Temperature Range (T_{OPR}) . . . . . -20°C to 75°C
Supply Voltage
AV_{DD}, AV_{SS} . . . . . .3.0V to 3.6V
DV_{DD}, DV_{SS} . . . . . .3.0V to 3.6V
Reference Input Voltage (V_{REF}) 1.2V
Clock Pulse Width
t_{PW1} . . . . . 25ns (Min)
t_{PW0} . . . . . 25ns (Min)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
MQFP Package	104

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature (T_{STG}) . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications f_{CLK} = 20MHz, V_{DD} = 3.3V, R_{OUT} = 330Ω, V_{REF} = 1.2V, R_{IRF} = 5.1kΩ, T_A = 25°C

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		n		-	8	-	Bit
Maximum Conversion Speed		f_{MAX}		20	-	-	MHz
Linearity Error		INL		-2.5	-	2.5	LSB
Differential Linearity Error		DNL		-0.5	-	0.5	LSB
Full Scale Output Voltage		V_{FS}		1.12	1.24	1.36	V
Full Scale Output Ratio (Note 1)		F_{SR}		0	1.5	3	%
Full Scale Output Current		I_{FS}		-	3.8	-	mA
Offset Output Voltage		V_{OS}		-	-	1	mV
Power supply Current		I_{DD}	14.3MHz, at Color Bar Data input	-	15	-	mA
Digital Input Current	H Level	I_{IH}		-	-	5	µA
	L Level	I_{IL}		-5	-	-	µA
Set Up Time		t_S		7	-	-	ns
Hold Time		t_H		3	-	-	ns
Propagation Delay Time		t_{PD}		-	20	-	ns
Glitch Energy		GE		-	150	-	pV/s
Crosstalk		CT	1MHz Sine Wave Output	-	53	-	dB

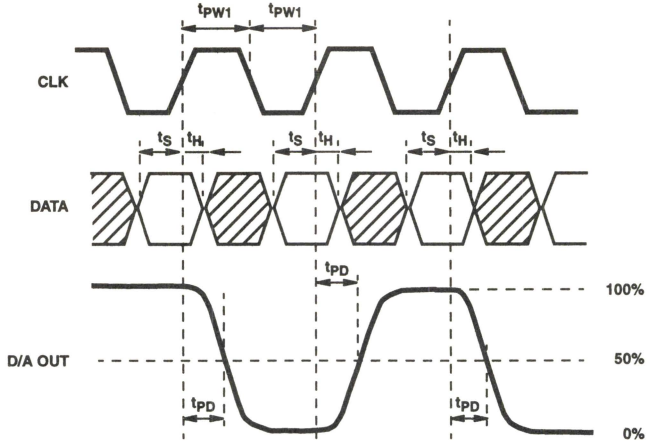
NOTE:

2. Full Scale Output Ratio = $\left| \frac{\text{Full scale voltage of channel}}{\text{Average of the full-scale voltage of the channels}} - 1 \right| \times 100(\%)$.

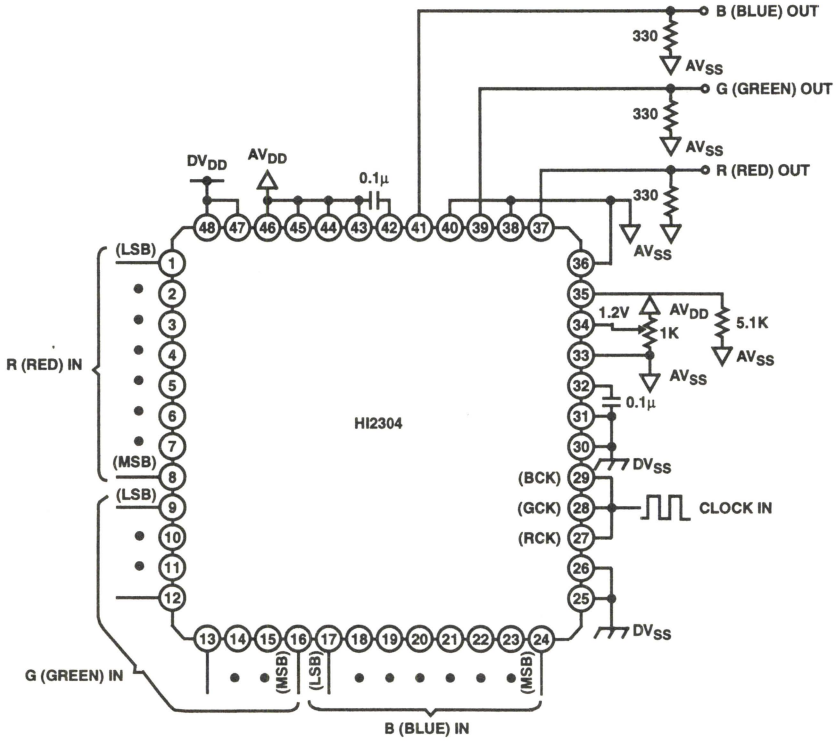
I/O Chart (When Full Scale Output Voltage at 2.00V)

INPUT CODE								OUTPUT VOLTAGE
MSB							LSB	
1	1	1	1	1	1	1	1	1.2V
			•					
			•					
			•					
1	0	0	0	0	0	0	0	0.6V
			•					
			•					
			•					
0	0	0	0	0	0	0	0	0V

Timing Diagram



Typical Application Circuit



Notes On Operation

- How to Select the Output Resistance

The HI2304 is a current output D/A converter. To obtain the output voltage, connect the resistance to IO pin (RO, GO, BO). For specifications we have:

Output Full Scale Voltage V_{FS} = 1.2 [V].

Output Full Scale Current I_{FS} = 3.8 [mA].

Calculate the output resistance value from the relation of $V_{FS} = I_{FS} \times R$. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF}. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here, please note that V_{FS} becomes $V_{FS} = V_{REF} \times 16R/R$. R is the resistance connected to IO while R is connected to I_{REF}. Increasing the resistance value can curb power consumption. On the other hand, glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase Relation Between Data and Clock

To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock, applied from the exterior. Be sure to satisfy the provisions of the set up time (t_S) and hold time (t_H) as stipulated in the Electrical Characteristics.

- V_{DD}, V_{SS}

To reduce noise effects, separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of about 0.1µF, as close as possible to the pin.

Test Circuits

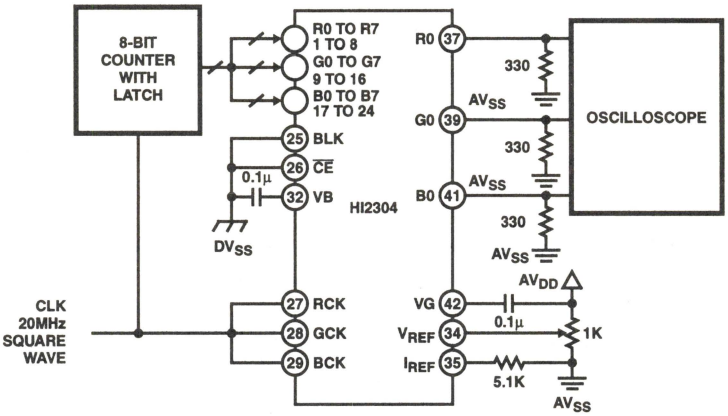


FIGURE 1. MAXIMUM CONVERSION RATE TEST CIRCUIT

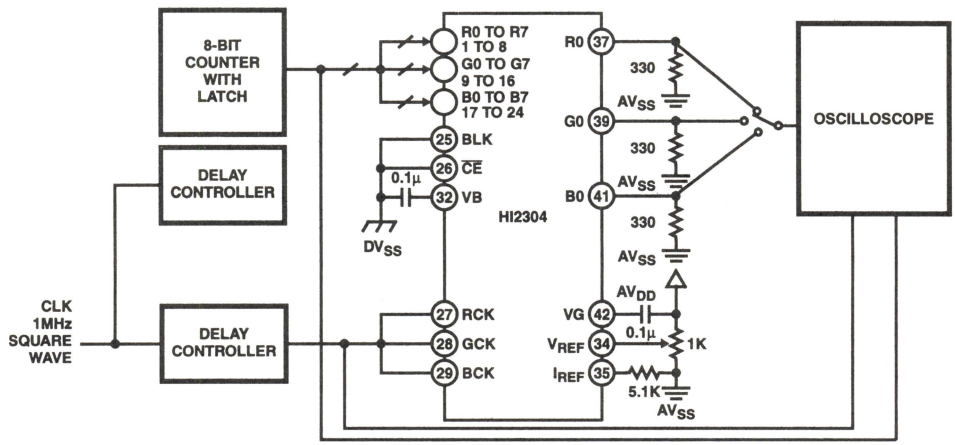


FIGURE 2. SET-UP HOLD TIME GLITCH ENERGY TEST CIRCUIT

Test Circuits (Continued)

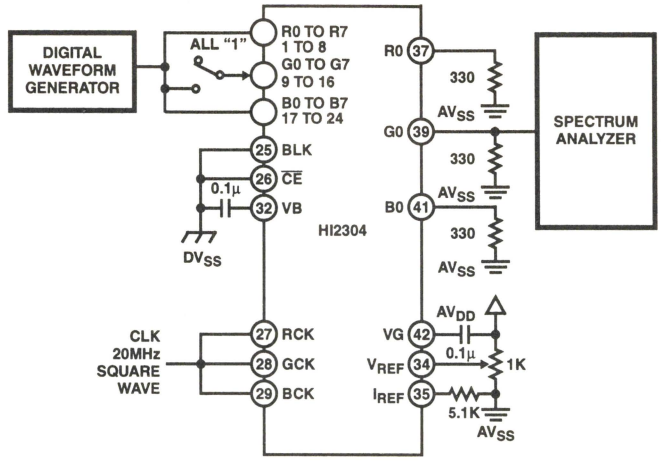


FIGURE 3. CROSSTALK TEST CIRCUIT (See Figure 7)

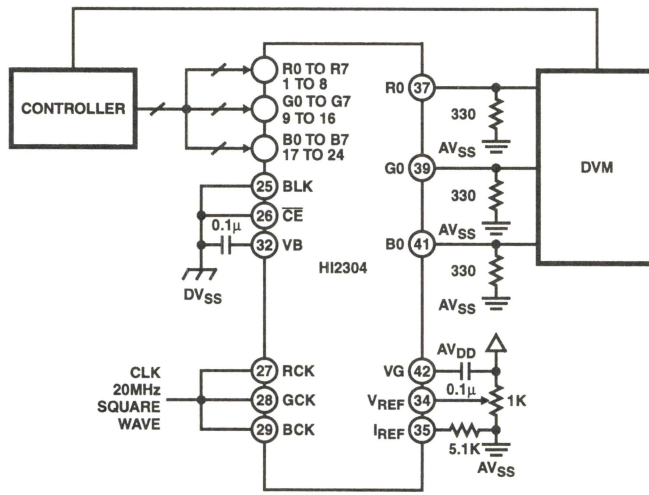


FIGURE 4. DC CHARACTERISTICS TEST CIRCUIT

Test Circuits (Continued)

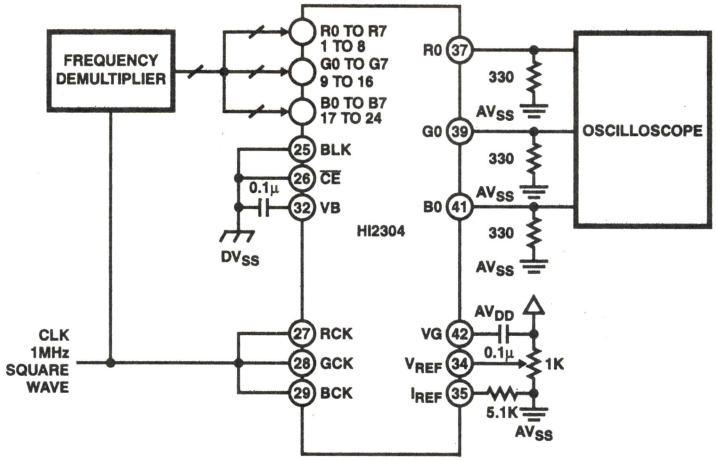
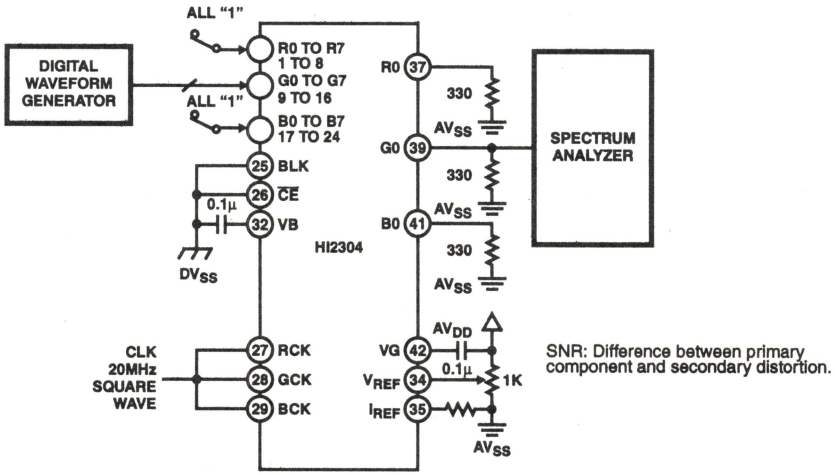


FIGURE 5. PROPAGATION DELAY TIME TEST CIRCUIT



SNR: Difference between primary component and secondary distortion.

FIGURE 6. SNR TEST CIRCUIT (See Figure 8)

Typical Performance Curves

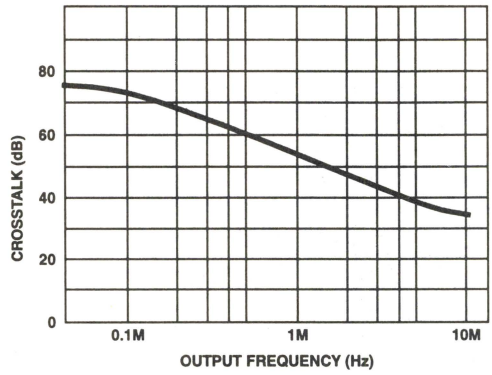


FIGURE 7. CROSSTALK

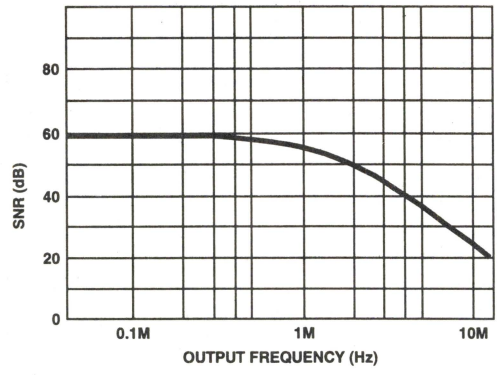


FIGURE 8. SNR (DIFFERENCE BETWEEN PRIMARY COMPONENT AND SECONDARY DISTORTION)

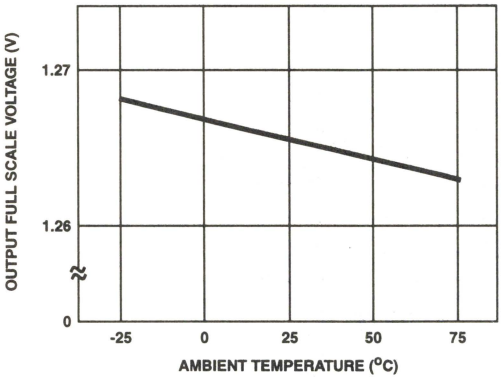


FIGURE 9. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

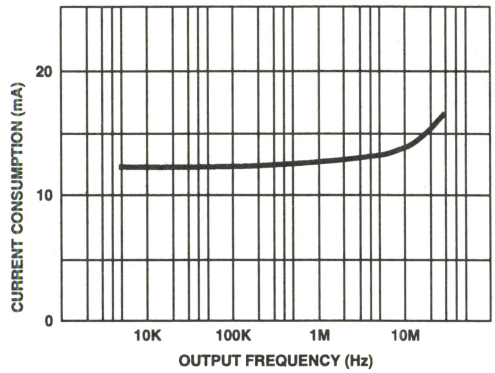


FIGURE 10. OUTPUT FREQUENCY vs CURRENT CONSUMPTION

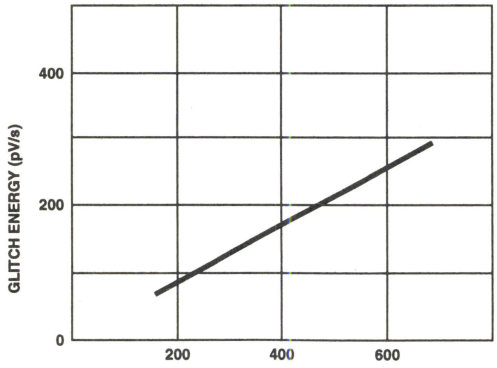


FIGURE 11. OUTPUT RESISTANCE vs GLITCH ENERGY

Reference Measurement Condition and Description

AV_{DD} = 3.3V.

DV_{DD} = 3.3V.

V_{REF} = 1.2V.

R_{IRF} = 5.1kΩ.

T_A = 25°C.

Figure 7 and Figure 8 refer to the measurement circuit.

Figure 9 is input data = all 1.

Figure 10 is input data = output of incremental counter, current consumption is total of 3ch.

HARRIS SEMICONDUCTOR

HI2307

NOT RECOMMENDED FOR NEW DESIGNS
See HI3050

August 1997

Triple 10-Bit, 50 MSPS, RGB, 3-Channel D/A Converter

Features

- Resolution ..... Triple 10-Bit
- Maximum Conversion Speed 50MHz
- RGB 3-Channel Input/Output
- Differential Linearity Error ..... ±0.5 LSB
- Low Power Consumption ..... 300mW (Max)
- Single Power Supply ..... +5V
- Low Glitch
- Direct Replacement for Sony CXD2307

Applications

- Digital TV
- Graphics Display
- High Resolution Color Graphics
- Video Reconstruction
- Instrumentation
- Image Processing
- I/Q Modulation

Description

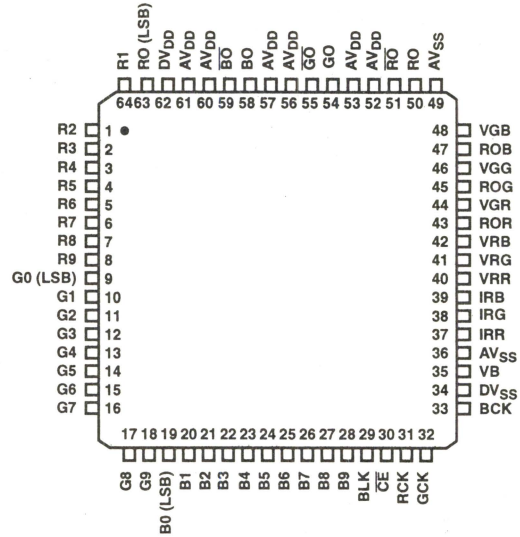
The HI2307 is a triple 10-bit, high-speed, CMOS D/A converter designed for video band use. It has three separate, 10-bit, pixel inputs, one each for red, green, and blue video data. A single 5.0V power supply and pixel clock input is all that is required to make the device operational. A bias voltage generator is internal. Each channel clock input can be controlled individually, or connected together as one. The HI2307 also has BLANK video control signal.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI2307JCQ	-20 to 75	64 Ld MQFP	Q64.10x10-S

Pinout

HI2307
(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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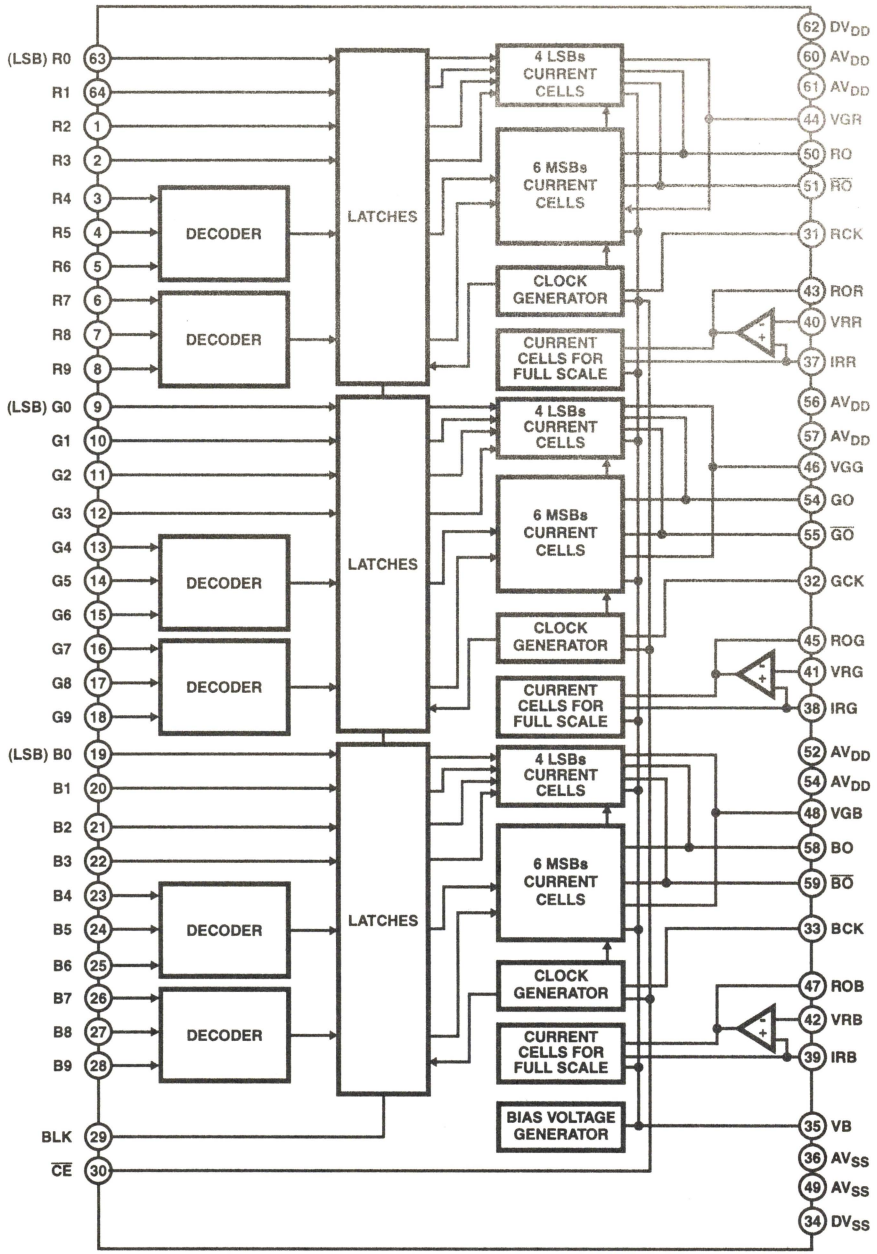
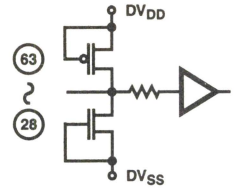
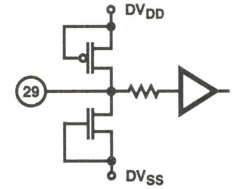
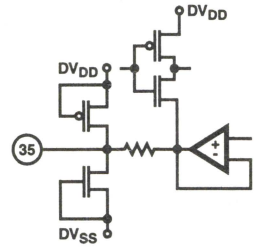
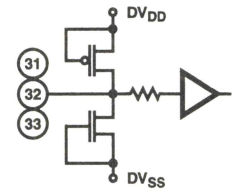
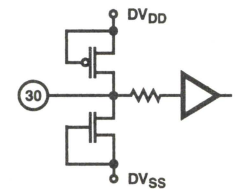
File Number 4117.1

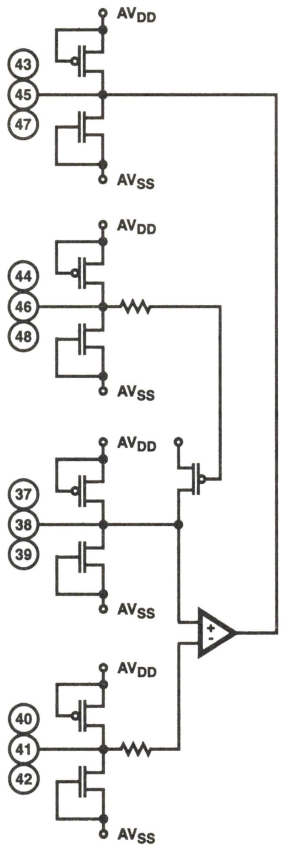
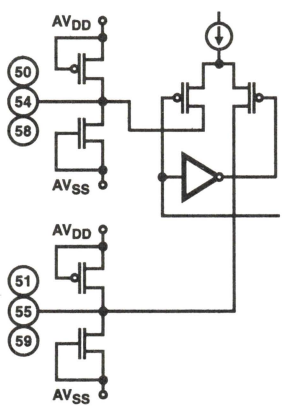
Functional Block Diagram



Pin Descriptions

NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
63 to 8 9 to 18 19 to 28	R0 to R9 G0 to G9 B0 to B9		Digital Input.
29	BLK		Blanking pin. No signal for High (0V output). Output generated for Low.
35	VB		Connect to DV_{SS} with a capacitor of approximately 0.1µF.
31 32 33	RCK GCK BCK		Clock pins. All input pins are TTL compatible.
34	DV_{SS}		Digital GND.
36, 49	AV_{SS}		Analog GND.
30	$\overline{CE}$		Chip Enable pin. No signal for High (0V output) to minimize power consumption.
52, 53, 56, 57, 60, 61	AV_{DD}		Analog V_{DD}.

Pin Descriptions (Continued)

NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
43 45 47	ROR ROG ROB		Connect to VGR, VGG, and VGB with the control method of output amplitude. See Application Circuit.
44 46 48	VGR VGG VGB		Connect a capacitor of approximately 0.1µF.
37 38 39	IRR IRG IRB		Connect to AV_{SS} with a resistance of 3.3kΩ.
40 41 42	VRR VRG VRB		Set output fullscale value (2.0V).
50 54 58	RO GO BO		Current output pins. Output can be retrieved by connecting a resistance of 200Ω to AV_{SS}.
51 55 59	$\overline{RO}$ $\overline{GO}$ $\overline{BO}$		Reverse current output pins. Normally connect to AV_{SS}.
62	DV_{DD}		Digital V_{DD}.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, V_{DD} 7.0V
Input Voltage, V_{IN} . . . . . V_{DD} to V_{SS}
Output Current (for Each Channel), I_{OUT} . . . . . 0 to 15mA

Operating Conditions

Supply Voltage
AV_{DD}, AV_{SS} . . . . . 4.75V to 5.25V
DV_{DD}, DV_{SS} . . . . . 4.75V to 5.25V
Reference Input Voltage, V_{REF} . . . . . 0.5V to 2.0V
Clock Pulse Width
t_{PW1} . . . . . 10ns (Min)
t_{PW0} . . . . . 10ns (Min)
Temperature Range, T_{OPR} . . . . . -20^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 7)	θ_{JA} ($^oC/W$)
MQFP Package	93

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, $f_{CLK} = 50MHz$, $V_{DD} = 5V$, $R_{OUT} = 200\Omega$, $V_{REF} = 2.0V$

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		n		-	10	-	Bit
Maximum Conversion Speed		f_{MAX}		50	-	-	MHz
Linearity Error		E_L		-2.0	-	2.0	LSB
Differential Linearity Error		E_D		-0.5	-	0.5	LSB
Output Full Scale Voltage		V_{FS}		1.8	1.9	2.0	V
Output Full Scale Ratio (Note 8)		F_{SR}	For the Equal Gain	0	1.5	3	%
Output Full Scale Current		I_{FS}		-	9.5	10	mA
Output Offset Voltage		V_{OS}		-	-	1	mV
Supply Current		I_{DD}		-	55	60	mA
Digital Input Current	High Level	I_{IH}		-	-	5	µA
	Low Level	I_{IL}		-5	-	-	µA
Precision Guaranteed Output Voltage Range		V_{OC}		1.8	1.9	2.0	V
Setup Time		t_S		-	5	7	ns
Hold Time		t_H		-	1	3	ns
Propagation Delay Time		t_{PD}		-	10	-	ns
Glitch Energy		GE		-	100	-	pV-s
Cross Talk		CT	For 10MHz Sinewave Output	-	54	-	dB

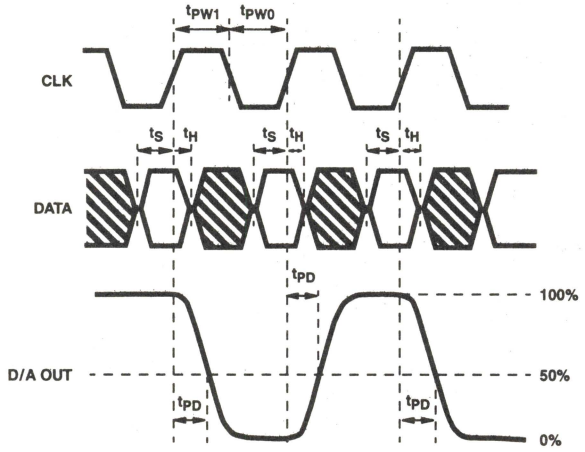
NOTE:

2. Output Full Scale Ratio = $\left|\frac{\text{Full scale voltage of channel}}{\text{Average of the full scale voltage of the channels}}(-1)\right| \times 100(\%)$.

I/O Correspondence Table (Output Full Scale Voltage: 2.0V)

INPUT CODE	OUTPUT VOLTAGE
MSB LSB	
1 1 1 1 1 1 1 1 1 1	2.0V
⋮	
1 0 0 0 0 0 0 0 0 0	1.0V
⋮	
0 0 0 0 0 0 0 0 0 0	0V

Timing Diagram



Test Circuits

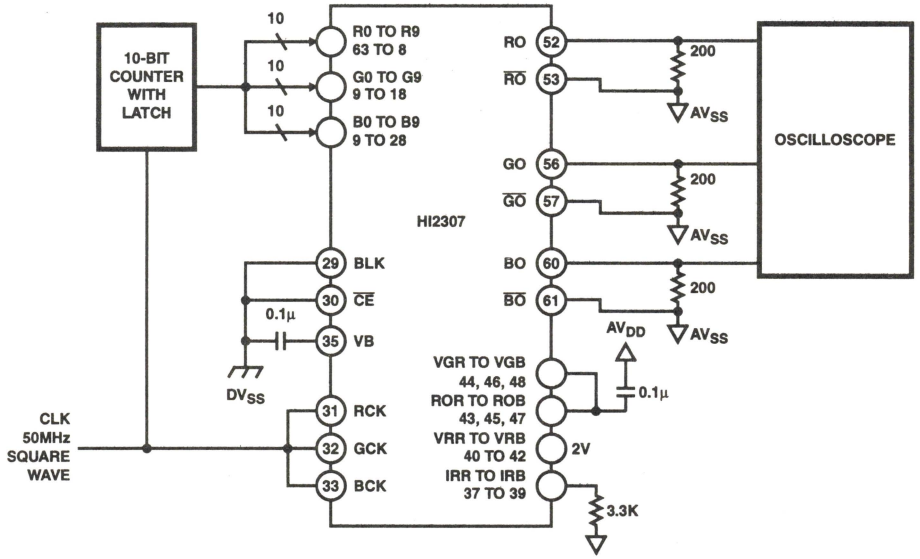


FIGURE 1. MAXIMUM CONVERSION RATE

Test Circuits (Continued)

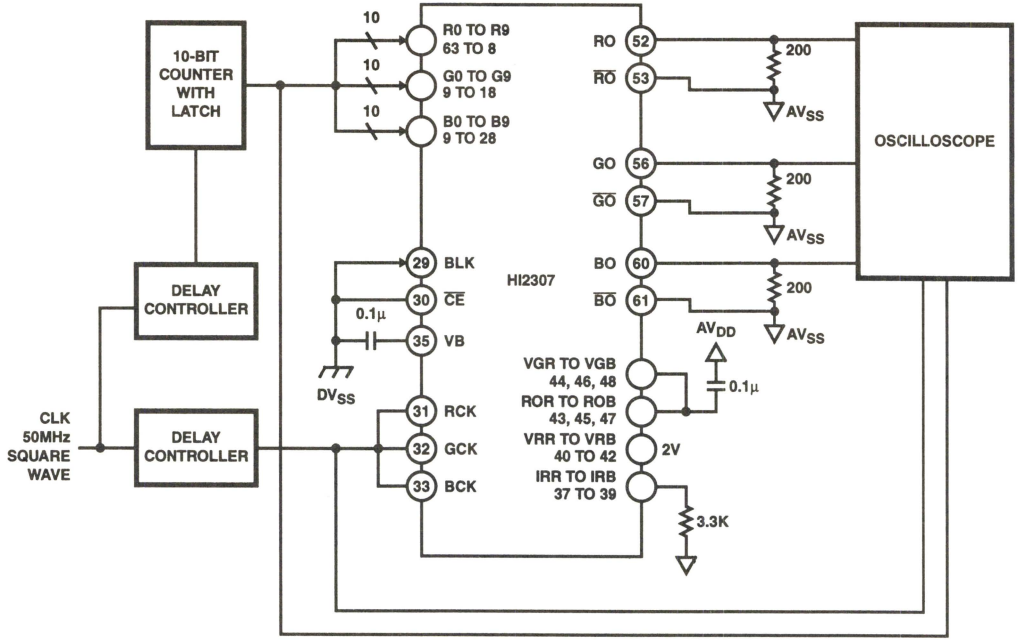


FIGURE 2. SETUP HOLD TIME AND GLITCH ENERGY TEST CIRCUIT

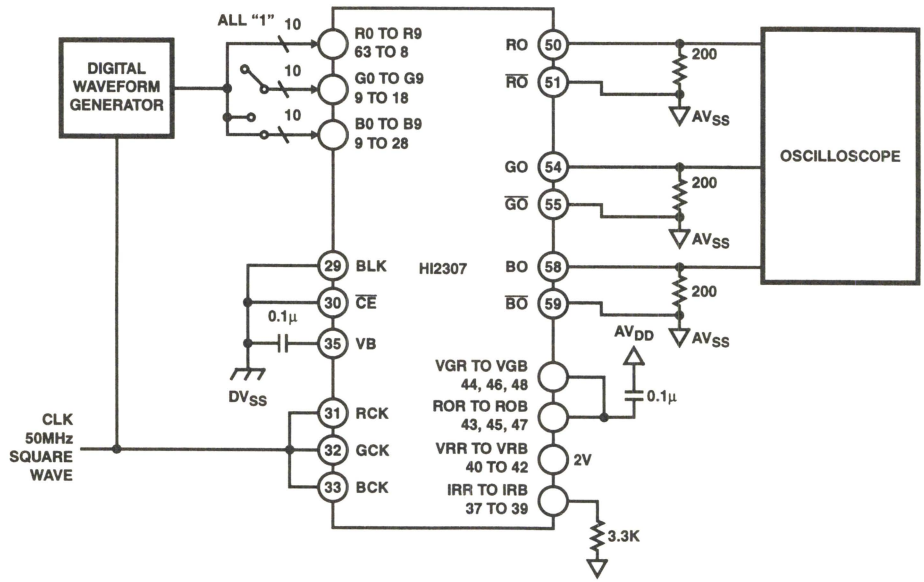


FIGURE 3. CROSS TALK TEST CIRCUIT

Typical Performance Curves

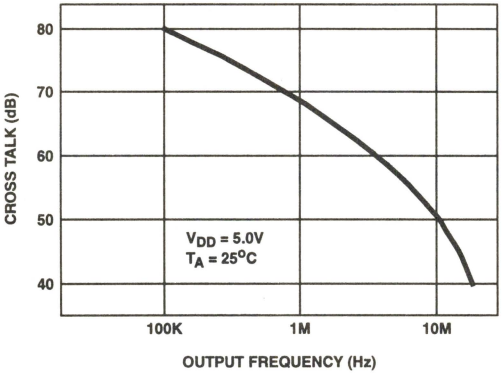


FIGURE 4. OUTPUT FREQUENCY vs CROSS TALK

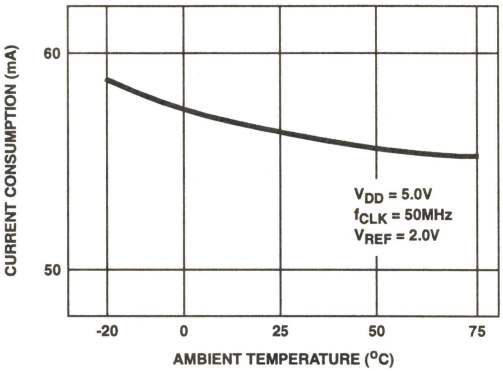


FIGURE 5. CURRENT CONSUMPTION vs AMBIENT TEMPERATURE

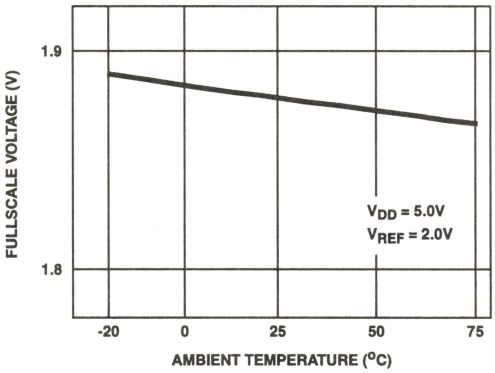


FIGURE 6. FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

Application Circuits

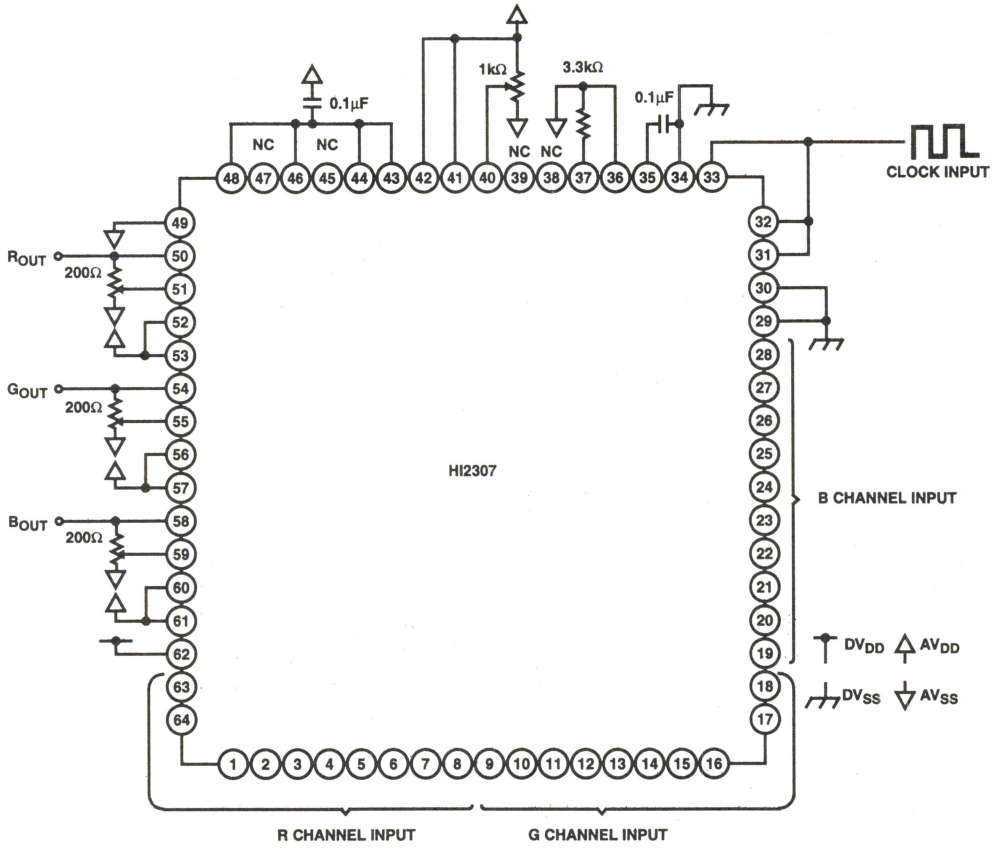


FIGURE 7. GAIN EQUAL

Application Circuits (Continued)

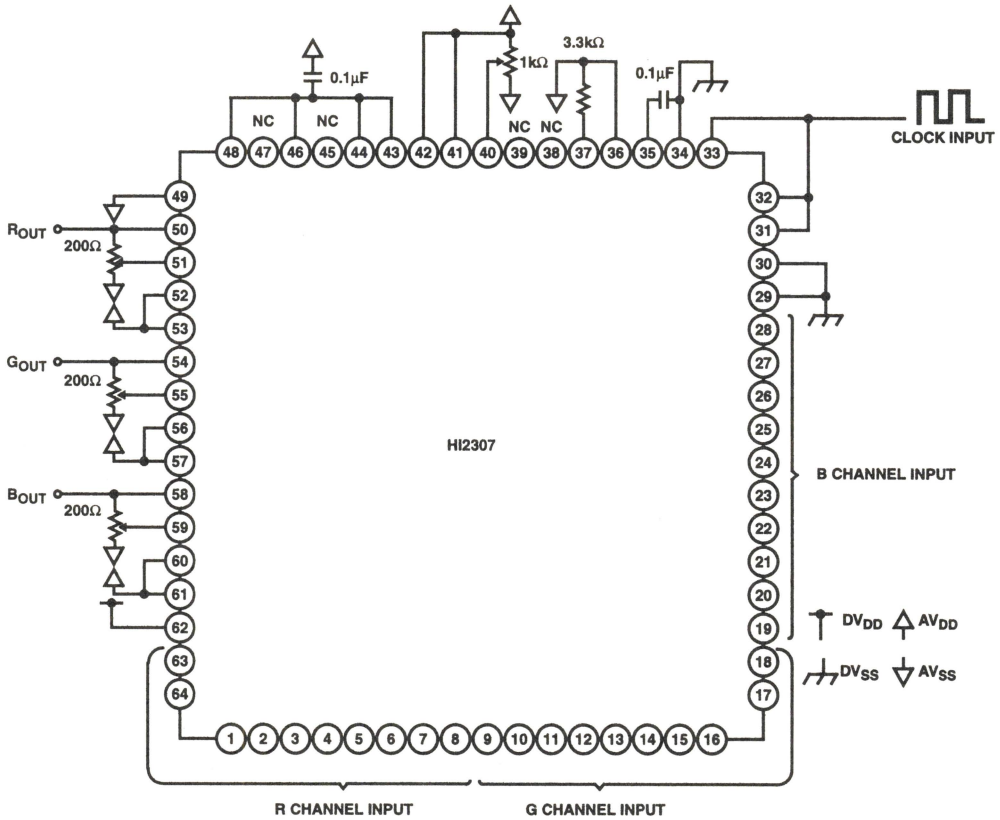


FIGURE 8. GAIN INDEPENDENTLY

HARRIS SEMICONDUCTOR

HI2309

Triple 10-Bit, 50 MSPS, 3-Channel D/A Converter

August 1997

Features

- Resolution ..... Triple 10-Bit
- Maximum Conversion Speed 50MHz
- RGB 3-Channel Input/Output
- Differential Linearity Error ..... ±0.5 LSB
- Low Power Consumption ..... 200mW (200Ω Load for $2V_{P-P}$ Output)
- Power Supply ..... +5V Single
- Low Glitch
- Direct Replacement for Sony CXD2309

Applications

- Digital TV
- Graphics Display
- High Resolution Color Graphics
- Video Reconstruction
- Instrumentation
- Image Processing
- I/Q Modulation

Description

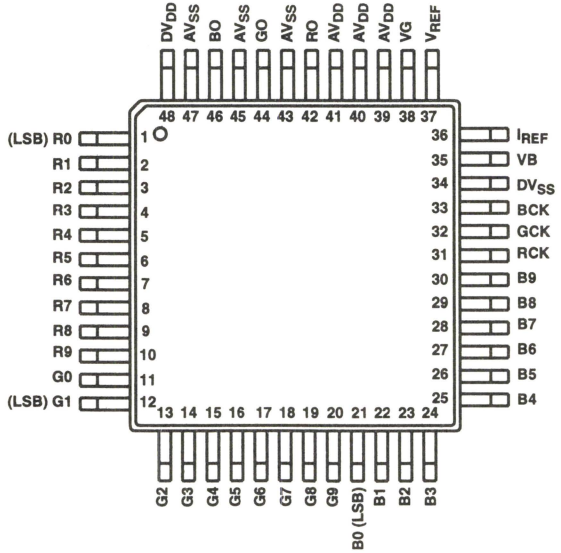
The HI2309 is a triple 10-bit, high-speed, CMOS D/A converter designed for video band use. It has three separate, 10-bit, pixel inputs, one each for red, green, and blue video data. A single 5.0V power supply and pixel clock input is all that is required to make the device operational. A bias voltage generator is internal. Each channel clock input can be controlled individually, or connected together as one. The HI2309 also has BLANK video control signal.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI2309JCQ	-20 to 75	48 Ld MQFP	Q48.12x12-S

Pinout

HI2309 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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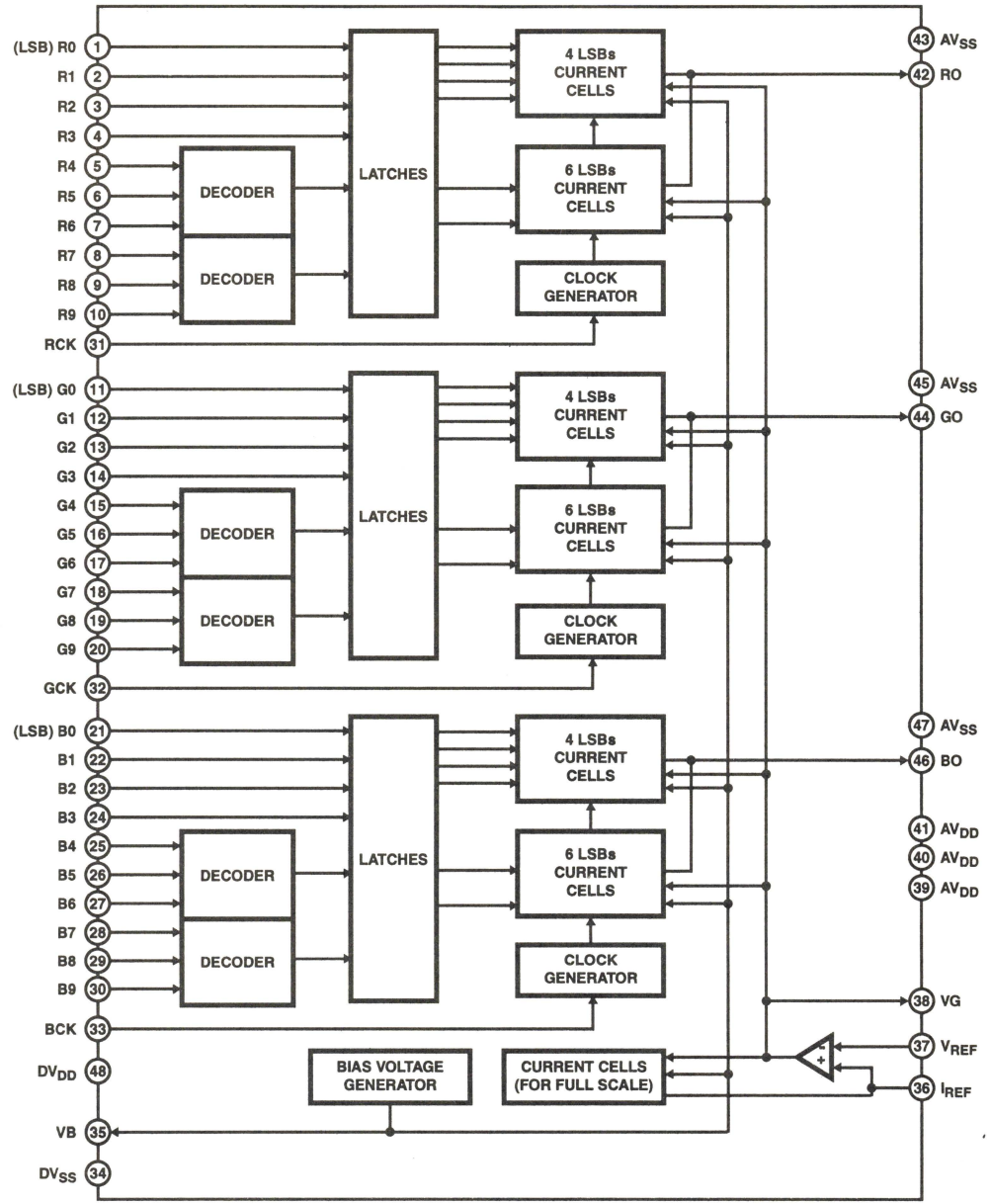
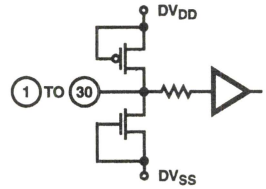
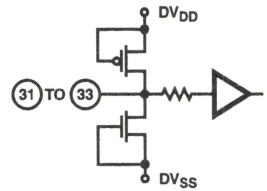
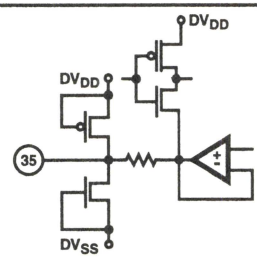
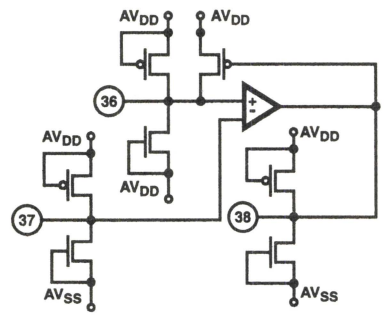
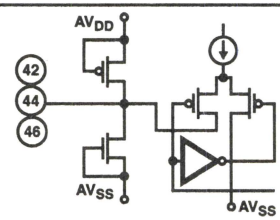
File Number **4118.1**

Functional Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 10	R0 to R9		Digital Input.
11 to 20	G0 to G9		
21 to 30	B0 to B9		
31	RCLK		Clock pin.
32	GCLK		
33	BCLK		
34	DV_{SS}		Digital GND.
35	VB		Connect an approximately 0.1µF capacitor.
36	I_{REF}		Connect a "16R" resistor which is 16 times the output resistance "R".
37	V_{REF}		Sets an output full scale value.
38	VG		Connect an approximately 0.1µF capacitor.
39 to 41	AV_{DD}		Analog V_{DD}.
42	RO		Current Output. Output can be obtained by connecting a resistor (200Ω typical).
44	GO		
46	BO		
43, 45, 47	AV_{DD}		Analog GND.
47, 48	DV_{DD}		Digital V_{DD}.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Input Voltage (V_{IN}) . . . . . V_{DD} to V_{SS}
Output Current (I_{OUT}) . . . . . .0mA to 15mA
Storage Temperature . . . . . -55°C 150°C

Operating Conditions

Supply Voltage
AV_{DD}, AV_{SS} . . . . . 4.75V to 5.25V
DV_{DD}, DV_{SS} . . . . . 4.75V to 5.25V
Reference Input Voltage (V_{REF}) . . . . . .0.5V to 2.0V
Clock Pulse Width
t_{PW1} . . . . . 10ns (Min)
t_{PW0} . . . . . 10ns (Min)
Temperature Range (T_{OPR}) . . . . . -20°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
MQFP Package	94

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $f_{CLK} = 50MHz$, $V_{DD} = 5V$, $R = 200\Omega$, $V_{REF} = 2.0V$, $T_A = 25^oC$

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		n		-	10	-	Bit
Maximum Conversion Speed		f_{MAX}		50	-	-	MHz
Linearity Error		E_L		-2.0	-	2.0	LSB
Differential Linearity Error		E_D		-0.5	-	0.5	LSB
Output Full Scale Voltage		V_{FS}		1.8	1.92	2.0	V
Output Full Scale Current		I_{FS}		9.0	9.6	10	mA
Output Offset Voltage		V_{OS}		-	-	1	mV
Supply Current		I_{DD}		-	40	50	mA
Digital Input Current	High Level	I_{IH}		-	-	5	µA
	Low Level	I_{IL}		-5	-	-	µA
Digital Input Voltage	High Level	V_{IH}	DV_{DD} = 4.75 to 5.25V	2.15	-	-	V
	Low Level	V_{IL}	DV_{DD} - 4.75 to 5.25V	-	-	0.85	V
Precision Guaranteed Output Voltage Range		V_{OC}		1.8	1.92	2.0	V
Setup Time		t_S		6	-	-	ns
Hold Time		t_H		3	-	-	ns
Propagation Delay Time		t_{PD}		-	14	-	ns
Glitch Energy		GE	For $R_{OUT} = 100\Omega$, $1V_{P-P}$ Output	-	50	-	pV/s
Cross Talk		CT	For 10MHz Sine Wave Output	40	42	-	dB
SNR		SNR	For 1MHz Sine Wave Output	50	55	-	dB

NOTE:

2. Output full scale ratio = $\left| \frac{\text{Full scale voltage for each channel}}{\text{Average of full scale voltage for each channel}} - 1 \right| \times 100\%$.

Test Circuits

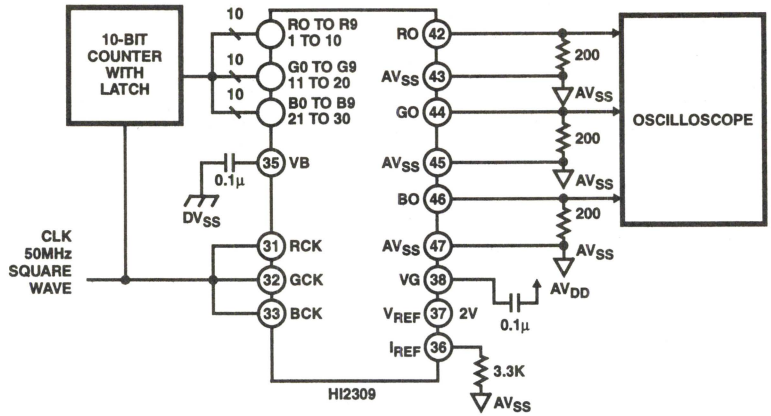


FIGURE 1. MAXIMUM CONVERSION RATE TEST CIRCUIT

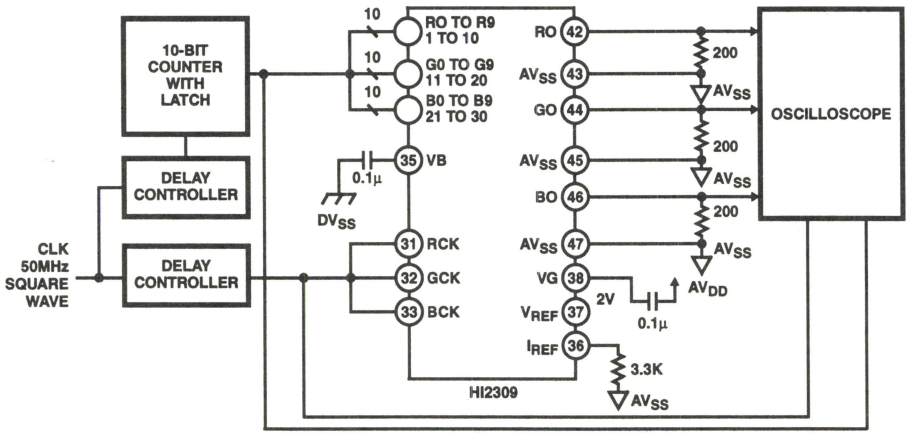


FIGURE 2. SETUP HOLD TIME GLITCH ENERGY TEST CIRCUIT

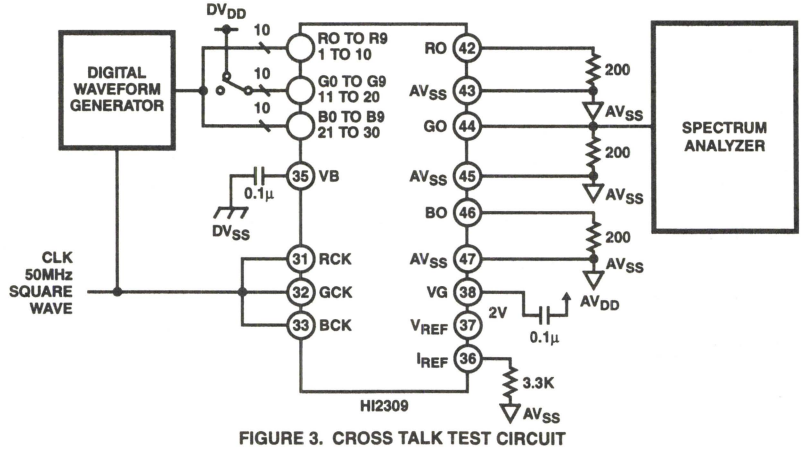


FIGURE 3. CROSS TALK TEST CIRCUIT

Test Circuits (Continued)

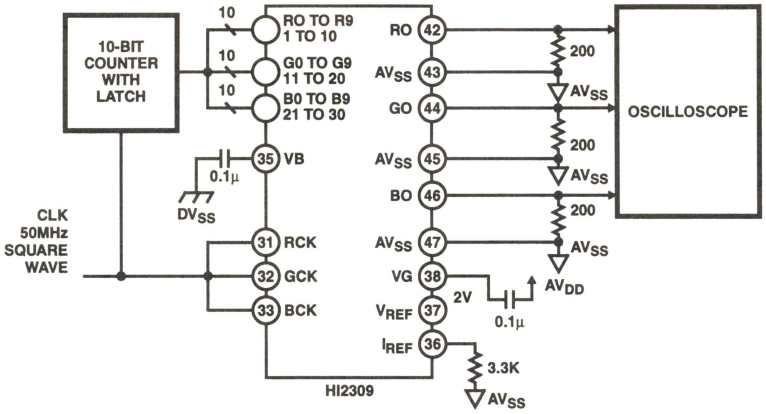


FIGURE 4. DC CHARACTERISTICS TEST CIRCUIT

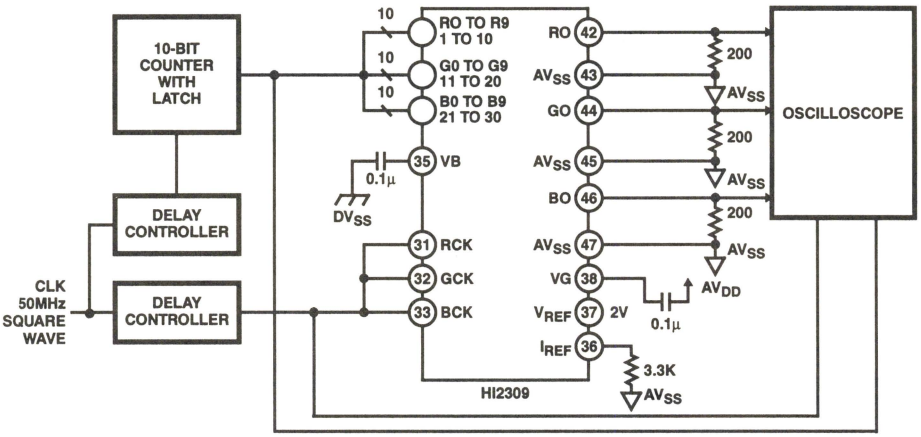


FIGURE 5. PROPAGATION DELAY TIME TEST CIRCUIT

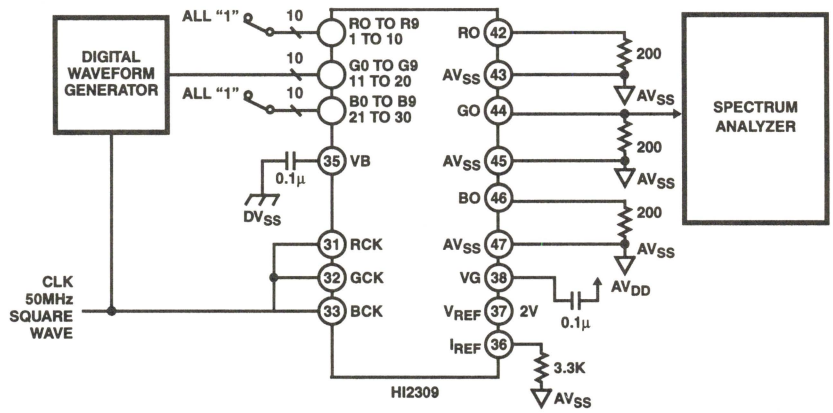
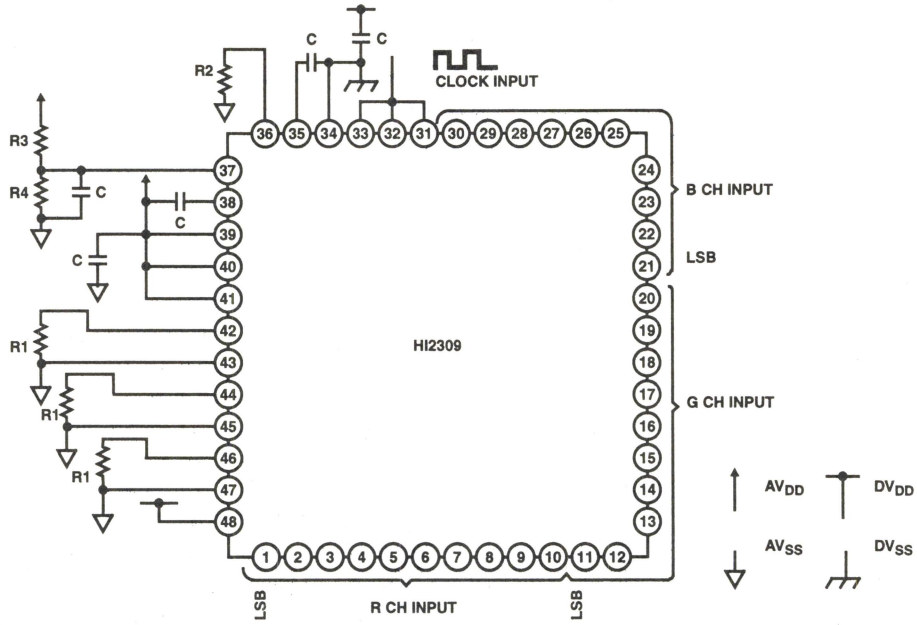


FIGURE 6. SNR TEST CIRCUIT

Application Circuit



- When the power supply (AV_{DD} and DV_{DD} is 5.0.
- R1 - 200Ω.
- R2 = 3.3kΩ.
- R3 = 3.0kΩ.
- R4 = 2.0kΩ.
- C = 0.1µF.

Application circuits shown are typical examples illustrating the operation of the devices. Harris cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Typical Performance Curves

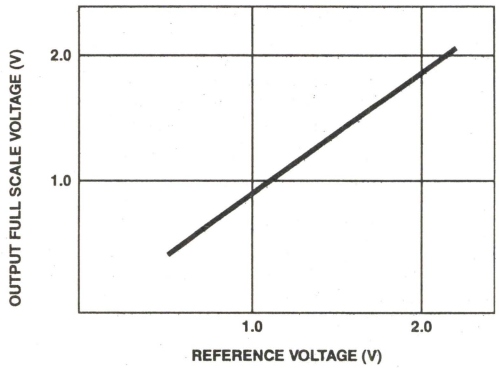


FIGURE 7. OUTPUT FULL SCALE VOLTAGE vs REFERENCE VOLTAGE

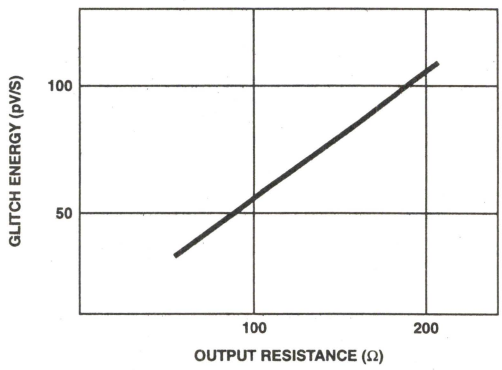


FIGURE 8. OUTPUT RESISTANCE vs GLITCH ENERGY

Typical Performance Curves (Continued)

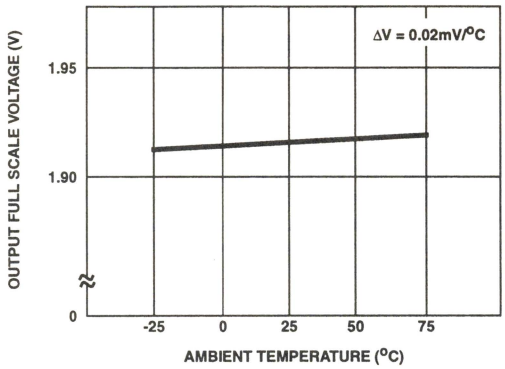


FIGURE 9. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

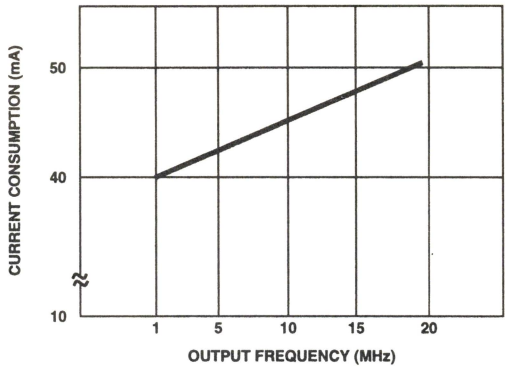


FIGURE 10. OUTPUT FREQUENCY vs CURRENT CONSUMPTION

Standard Measurement Conditions and Description

V_{DD} = 5.0V.

V_{REF} = 2.0V.

R = 200Ω.

16R = 3.3kΩ.

T_A = 25°C.

V_{REF} in Figure 9 is fixed to $2V_{DC}$ without resistor dividing.

Input data in Figure 10 = all "0" and "1" of rectangular wave, clock frequency = 50MHz for a total value of three channels.

Notes On Operation

Selecting the Output Resistance:

HI2309 is a current output type D/A converter. To create the output voltage, connect the resistor to the current output pin.

Specifications:

Output full scale voltage V_{FS} Max = 2.0 [V].

Output full scale current I_{FS} Max = 10 [mA].

Calculate the output resistance from $V_{FS} = I_{FS} \times R$. Connect a resistance sixteen times the output resistance to the reference current pin I_{REF}. In some cases, this value may not exist, a similar value can be used instead.

Note that the V_{FS} will be the following:

$V_{FS} = V_{REF} \times 16\ R/R'$.

R is the resistor to be connected to the IO and R' is the resistor to be connected to the I_{REF}. Power consumption can be reduced by increasing the resistance, but this will on the contrary, increase the glitch energy and data setting time. Set the best values according to the purpose of use.

Correlation Between Data and Clock:

For HI2309 to display the desired performance as a D/A converter, the data transmitted from outside and the clock must be synchronized properly. Adjust the setup time (t_S) and hold time (t_H) as specified in "Electrical Characteristics."

V_{DD}, V_{SS}:

Separate the analog and digital signals around the device to reduce noise effects. Bypass the V_{DD} pin to each GND with a 0.1µF ceramic capacitor as near as possible to the pin for both digital and analog signals.

Latch Up:

The AV_{DD} and DV_{DD} pins must be able to share the same power supply of the board. This is to prevent latch up caused by potential difference between the two pins when the power is turned on.

I_{REF} Pin:

The I_{REF} pin is very sensitive to improve the AC Characteristics. Pay attention for capacitance component not to attach to this pin because its output may become unstable.

VG Pin:

It is recommended to use a 1µF capacitor to improve the AC Characteristics, though the typical capacitance value externally connected to the V_G Pin is 0.1µF.

HARRIS SEMICONDUCTOR

HI2315

10-Bit, 80 MSPS D/A Converter (Ultra-Low Glitch Version)

August 1997

Features

- Throughput Rate 80MHz
- Low Power 150mW
- Single Power Supply .....+5V
- Differential Linearity Error ..... ±0.5 LSB
- TTL/CMOS Compatible Inputs
- Built in Bandgap Voltage Reference
- Power Down and Blanking Control Pins
- Low Glitch
- Pin Compatible with Sony CXD2306
- Direct Replacement for Sony CXD2315Q

Applications

- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Test Equipment
- High Resolution Imaging and Graphics Systems

Description

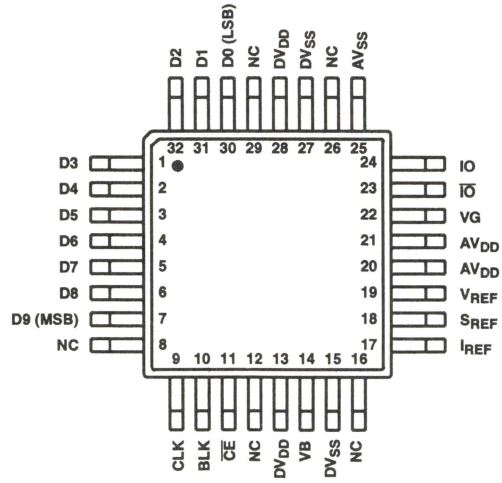
The HI2315 is a 10-bit, 80MHz, high speed, low power CMOS D/A converter. The converter incorporates a 10-bit input data register with current outputs. The HI2315 includes a power down feature that reduces power consumption and a blanking control. The on-chip bandgap reference can be used to set the output current range of the D/A.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI2315JCQ	-20 to 75	32 Ld MQFP	Q32.7x7-S

Pinout

HI2315
(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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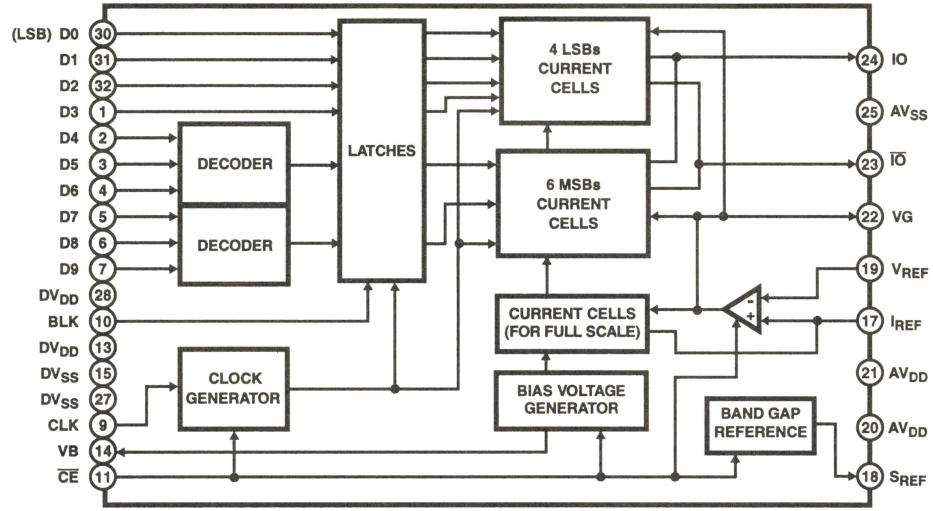
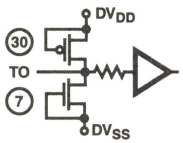
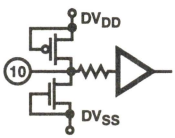
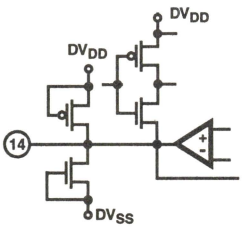
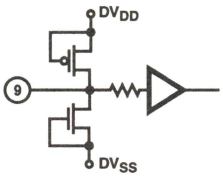
File Number 4119.1

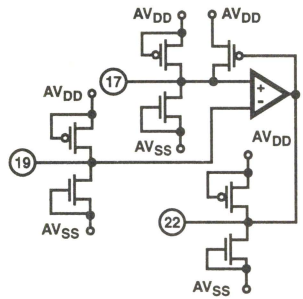
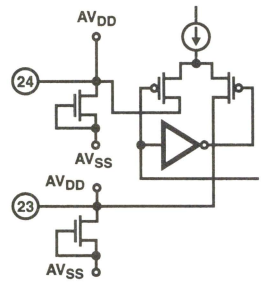
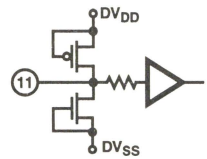
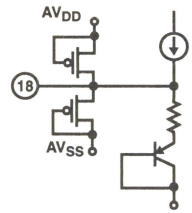
Functional Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
30 to 32 1 to 7	D0 to D9		Digital Input.
10	BLK		Blanking pin. No signal (0V output) at high and output state at low.
14	VB		Connect a capacitor of approximately 0.1µF.
9	CLK		Clock pin.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
15, 27	DV_{SS}		Digital GND.
25	AV_{SS}		Analog GND.
17	I_{REF}		Connect resistance "16R" which is 16 times output resistance "R".
19	V_{REF}		Sets output full scale value.
22	VG		Connect a capacitor of approximately 0.1µF.
20, 21	AV_{DD}		Analog V_{DD}.
24	IO		Current Output pin. Output can be retrieved by connecting resistance. The standard is 200Ω.
23	$\overline{IO}$		Inverted Current Output pin. Connect to GND normally.
13, 28	DV_{DD}		Digital V_{DD}.
11	$\overline{CE}$		Chip Enable pin. No signal (0V output) at high makes power consumption minimum.
18	S_{REF}		Independent Constant-Voltage Source Output pin using band gap reference. Stable voltage independent of the fluctuation for supply voltage can be obtained by connecting to V_{REF}. See Application Circuit 2 for details.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Input Voltage (V_{IN}) . . . . . V_{SS} -0.5V to V_{DD} + 0.5V
Output Voltage (I_{OUT}) . . . . . .0mA to 15mA

Operating Conditions

Supply Voltage
AV_{DD}, AV_{SS} . . . . . 5.0V ±0.25V
DV_{DD}, DV_{SS} . . . . . .5.0V ±0.25V
Reference Input Voltage (V_{REF}) . . . . . .0.5V to 2.0V
Clock Pulse Width (t_{PW1}, t_{PW0}) . . . . . 6.25ns (Min)
Temperature Range (T_{OPR}) . . . . . -20^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP Package 122
Maximum Junction Temperature (MQFP Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, f_{CLK} = 80MHz, V_{DD} = 5V, R = 200Ω, V_{REF} = 2.0V, 16R = 3.3kΩ

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		n		-	10	-	Bit
Maximum Conversion Rate		f_{MAX}		80	-	-	MHz
Linearity Error		EL		-1.5	-	1.5	LSB
Differential Linearity Error		ED		-0.5	-	0.5	LSB
Output Full-Scale Voltage		V_{FS}		1.8	1.94	2.0	V
Output Full-Scale Current		I_{FS}		9.0	9.7	10	mA
Output Off-Set Voltage		V_{OS}		-	-	1	mV
Output Impedance				-	300	-	kΩ
Supply Current		I_{DD}		-	-	30	mA
Digital Input Current	High Level	I_{IH}		-	-	5	µA
	Low Level	I_{IL}		-5	-	-	µA
Digital Input Voltage	High Level	V_{IH}		2.45	-	-	V
	Low Level	V_{IL}		-	-	0.85	V
Accuracy Guarantee Output Voltage Range		V_{OC}		1.8	1.94	2.0	V
Setup Time		t_S		3.0	-	-	ns
Hold Time		t_H		3.0	-	-	ns
Rise Time		t_r		5.0	-	-	ns
Propagation Delay Time		t_{PD}		-	5	-	ns
Glitch Energy		GE	R_{OUT} = 200Ω, $2V_{P-P}$	-	-	30	pV/s
Differential Gain		DG		-	-	1.0	%
Differential Phase		DP		-	-	1.0	Degrees
S_{REF} Output Voltage		S_{REF}	$T_A = 25^oC$	1.0	1.2	1.4	V

Test Circuits

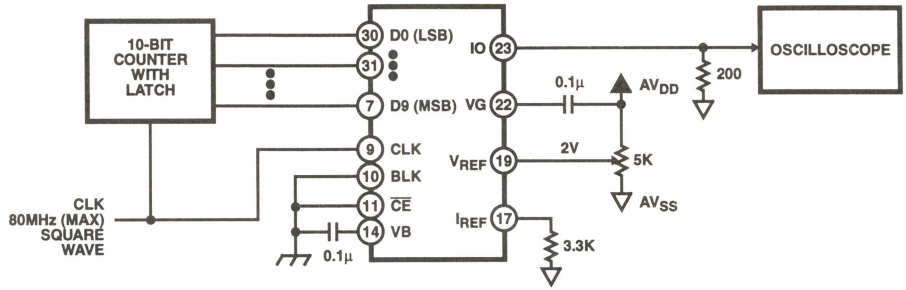


FIGURE 1. MAXIMUM CONVERSION RATE TEST CIRCUIT

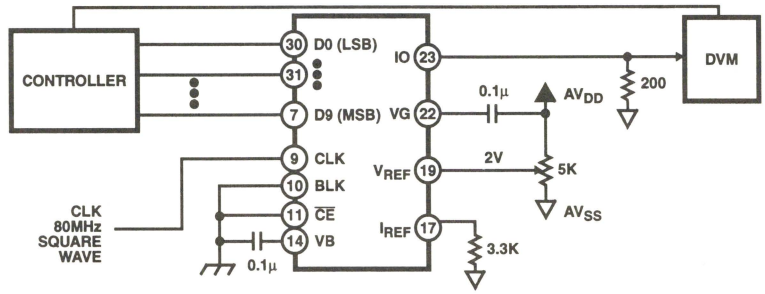


FIGURE 2. DC CHARACTERISTICS TEST CIRCUIT

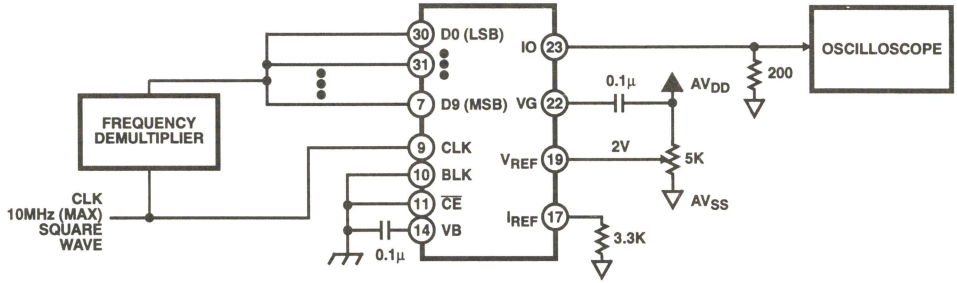


FIGURE 3. PROPAGATION DELAY TIME TEST CIRCUIT

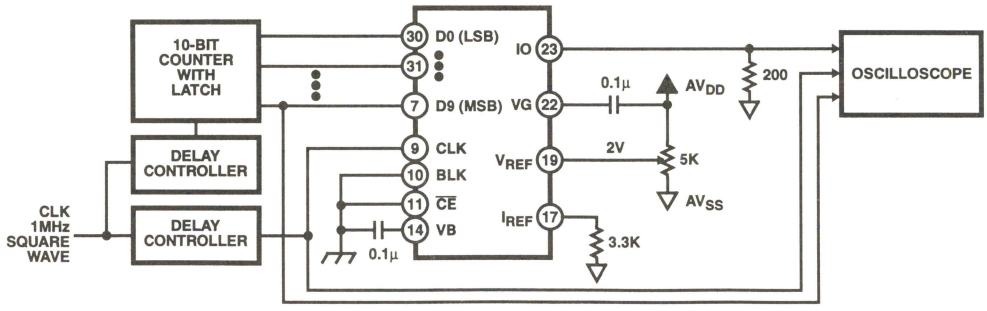


FIGURE 4. SETUP HOLD TIME AND GLITCH ENERGY TEST CIRCUIT

Timing Diagram

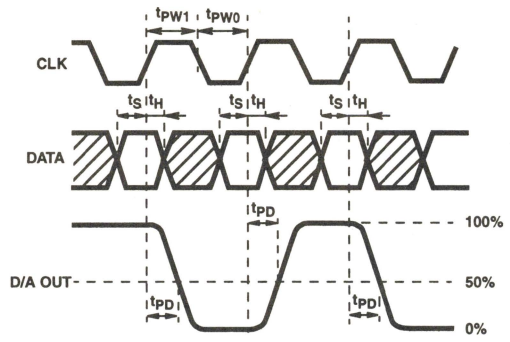
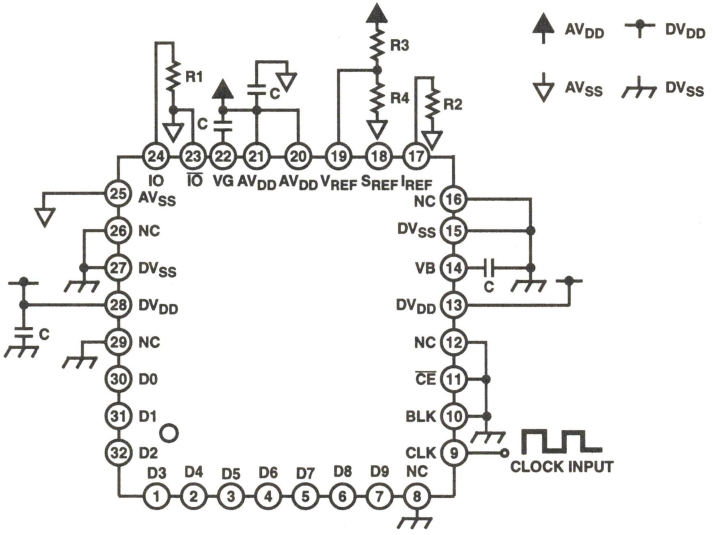


TABLE 1. I/O CORRESPONDENCE TABLE
(2.00V Output Full Scale Voltage)

INPUT CODE	OUTPUT VOLTAGE
MSB LSB	
1 1 1 1 1 1 1 1 1 1	2.0V
⋮	
1 0 0 0 0 0 0 0 0 0	1.0V
⋮	
0 0 0 0 0 0 0 0 0 0	0V

Typical Application Circuits

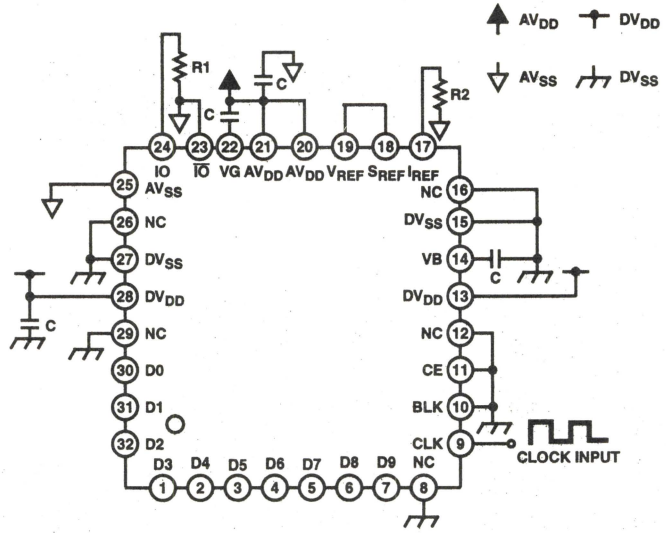


NOTE:

2. When 5.0V supply voltage (DV_{DD} and AV_{DD}). Digital input from pins 30 to 32 and pins 1 to 7. Pin 18 is Left Open When Using Normally. R1 = 200Ω, R2 = 3.3Ω (Resistance 16 Times R1), R3 = 3.0kΩ, R4 = 2.0kΩ, C = 0.1μF.

FIGURE 5. APPLICATION CIRCUIT 1

Typical Application Circuits (Continued)



NOTE:

3. When 5.0V supply voltage (DV_{DD} and AV_{DD}). Digital input from pins 30 to 32 and pins 1 to 7. R1 = 200Ω, R2 = 2.0kΩ, C = 0.1µF.

FIGURE 6. APPLICATION CIRCUIT 2

Typical Performance Curves

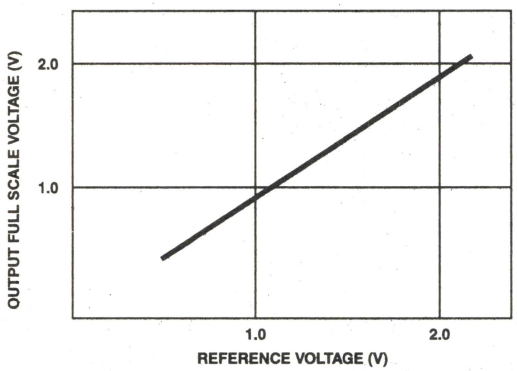


FIGURE 7. OUTPUT FULL SCALE VOLTAGE (V_{FS}) vs REFERENCE VOLTAGE (V_{REF})

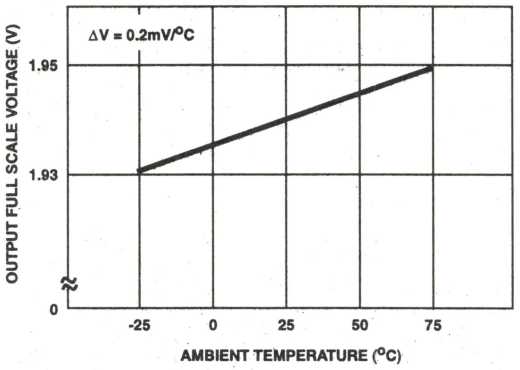


FIGURE 8. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

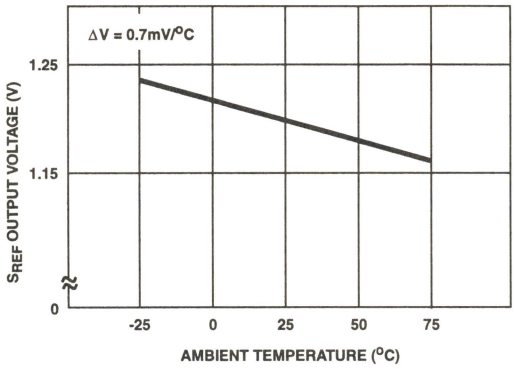


FIGURE 9. S_{REF} vs AMBIENT TEMPERATURE

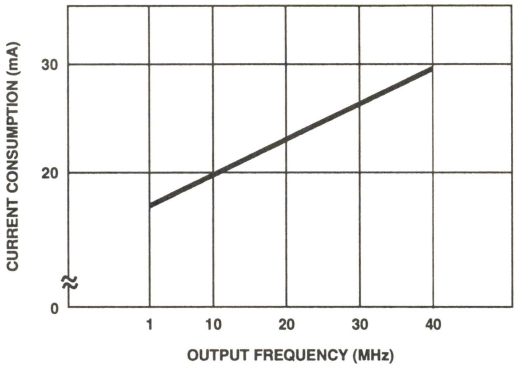


FIGURE 10. OUTPUT FREQUENCY vs CURRENT CONSUMPTION

NOTE:

4. Standard Measurement Conditions and Description: V_{DD} = 5.0V, V_{REF} = 2.0V, R = 200Ω, 16R - 3.3kΩ, T_A = 25°C. The temperature characteristics of external input data in Figure 10 = all "0" and "1" of rectangular wave; clock frequency = 80MHz.

GE (Glitch Energy)

GE, as described in the HI2315, is a spike noise which appears synchronizing with the clock falling edge when the input data (for 1 to 1024 input) changes to 128, 256, 384, 512, 640, 768, 896, and 1024. Figure 11 shows the change state of GE for the staircase wave output, and Figure 12 shows the repetitive output waveform where the GE appears. These figures exhibit the difference of this IC from the convention device.

The HI2315 reduces the GE as shown in Figures 11 and 12.

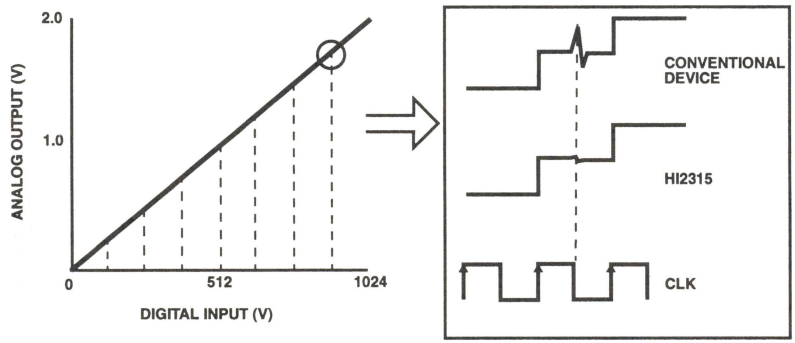


FIGURE 11. CHANGE OF GE FOR STAIRCASE WAVE OUTPUT

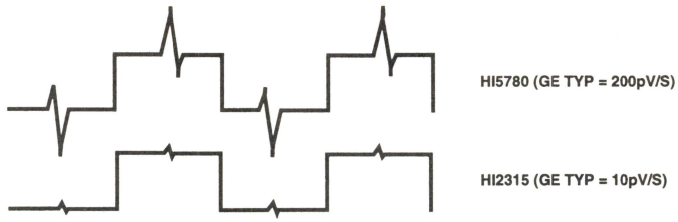


FIGURE 12. REPETITIVE OUTPUT WAVEFORM WHERE GE APPEARS (FOR 200Ω, $2V_{P-P}$ OUTPUT)

Notes On Operation

- Selecting the Output Resistance
  - HI2315 is a current output type D/A converter. To create the output voltage, connect the resistor to the current output pin.

    Specifications:
    Output full-scale voltage V_{FS} (Max) = 2.0V
    Output full-scale current I_{FS} (Max) = 10mA
  - Calculate the output resistance from $V_{FS} = I_{FS} \times R$. Connect a resistance sixteen times the output resistance to the reference current pin I_{REF}. In some cases, as this value may not exist, a similar value can be used instead.

    Note that the V_{FS} will be the following:

    $V_{FS} = V_{REF} \times 16\ R/R'$.
  - R is the resistor to be connected to the IO and R' is the resistor to be connected to the I_{REF}. Power consumption can be reduced by increasing the resistance, but this will on the contrary increase the glitch energy and data settling time. Set the best values according to the purpose of use.
- Correlation between Data and Clock
  - For the HI2315 to display the desired performance as a D/A converter, the data transmitted form outside and the clock must be synchronized properly. Adjust the setup time (t_S) and hold time (t_H) as specified in "Electrical Characteristics."
- V_{DD}, V_{SS}
  - Separate the analog and digital signals around the device to reduce noise effects. By-pass the V_{DD} pin to each GND with a 0.1µF ceramics capacitor as near to the pin as possible for both the digital and analog signals.
- Latch up
  - The AV_{DD} and DV_{DD} pins must be able to share the same power supply of the board. This is prevent latch up caused by potential difference between the two pins when the power is turned on.
- I_{REF} pin
  - The I_{REF} pin is very sensitive to improve the AC characteristics. Pay attention for capacitance component not to attach to this pin because its output may become unstable.
- VG Pin
  - It is recommended to use a 1µF capacitor to improve the AC characteristics though the typical capacitance value externally connected to the VG pin is 0.1µF.
- S_{REF}
  - The S_{REF} is independent regulated current source. By connecting it to the V_{REF}, stable output amplitudes that do not depend on fluctuations in the power supply can be obtained.
  - In this case, as $V_{FS} = S_{REF} \times 16R/R'$, set the V_{FS} according to R'.
  - Do not use this pin as a reference power supply for other ICs because this is dedicated for the D/A converter.

HARRIS SEMICONDUCTOR

HI3050

Triple 10-Bit, 50 MSPS, High Speed, 3-Channel D/A Converter

August 1997

Features

- Resolution ..... Triple 10-Bit
- Throughput Rate 50MHz
- 3-Channel, RGB, I/O
- RS-343A/RS-170 Compatible Outputs
- Low Power Consumption (Typ) 500mW
- Differential Linearity Error ..... ±0.5 LSB
- Low Glitch Energy
- CMOS Compatible Inputs
- Direct Replacement for Sony CXD2308

Applications

- NTSC, PAL, SECAM Displays
- High Definition Television (HDTV)
- Presentation and Broadcast Video
- Image Processing
- Graphics Displays

Description

The HI3050 is a triple, 10-bit D/A converter, fabricated in a silicon gate CMOS process, ideally suited for RGB video applications.

The converter incorporates three 10-bit input data registers with a common blanking capability, forcing all outputs to 0mA. The HI3050 features low glitch, high impedance current outputs and single 5V supply operation. Low current inputs accept standard TTL/CMOS levels. The architecture is a current cell arrangement providing low differential and integral linearity errors.

The HI3050 requires a 2V external reference and a set resistor to control the output current. The HI3050 also features a chip enable/disable pin for reducing power consumption (<5mW) when the part is not in use.

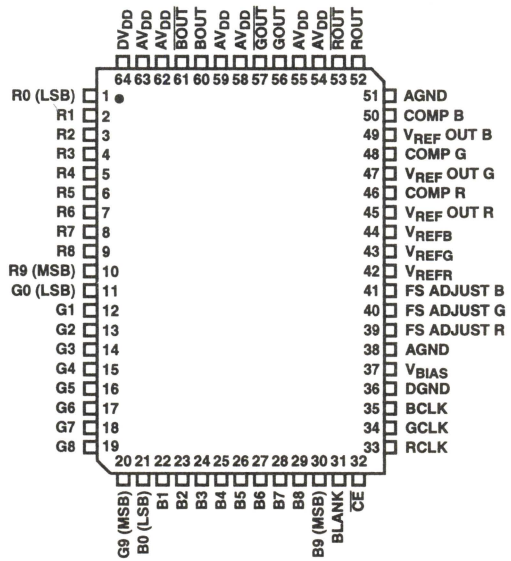
The HI3050 can generate RS-343A and RS-170 compatible video signals into doubly terminated and singly terminated 75Ω loads.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3050JCQ	-20 to 75	64 Ld MQFP	Q64.14x20-S

Pinout

HI3050 (MQFP)
TOP VIEW



10 D/A CONVERTERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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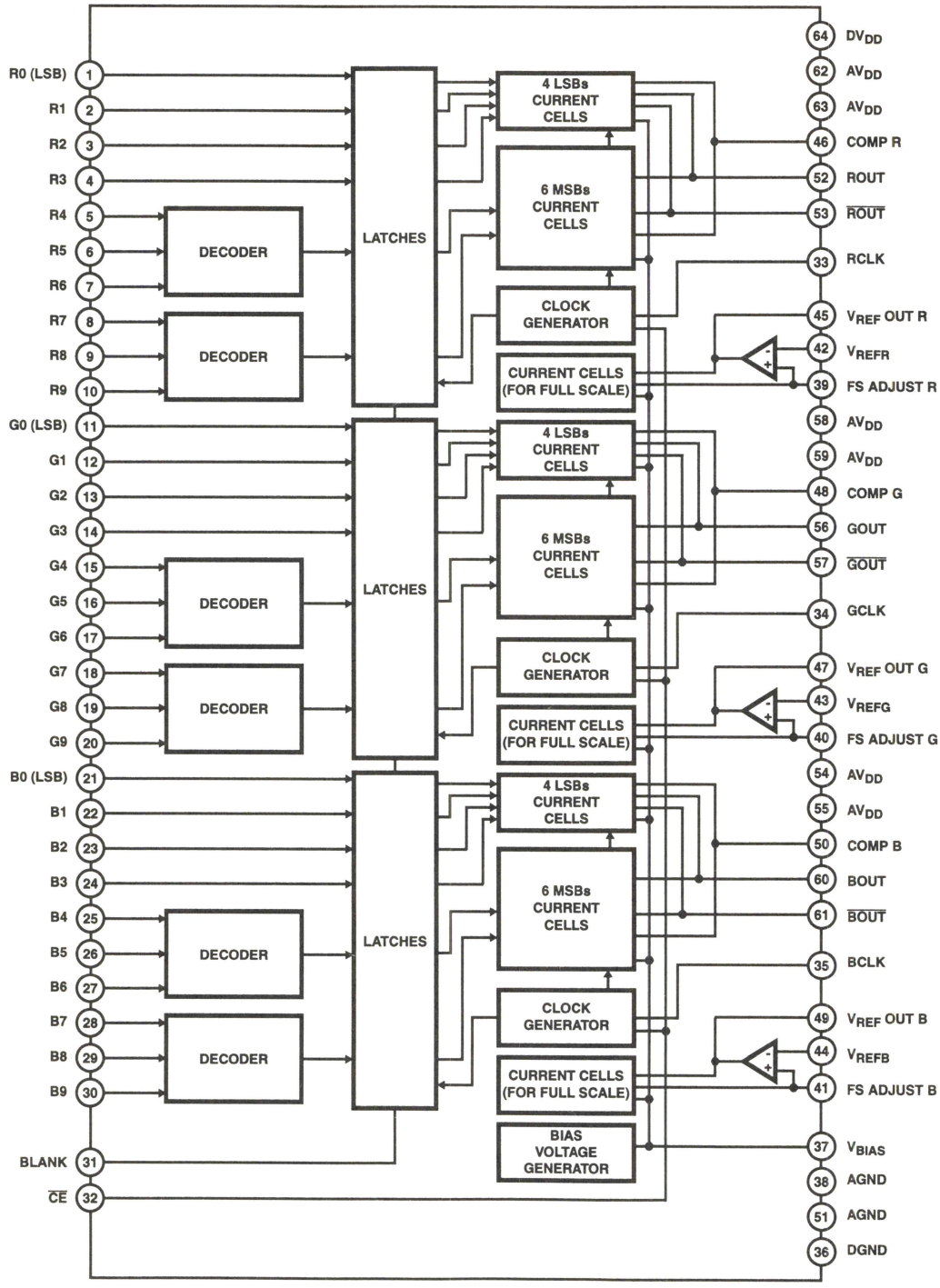
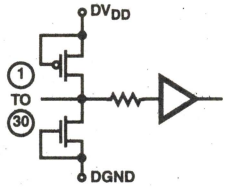
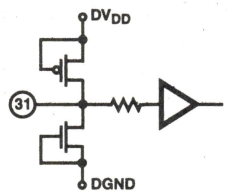
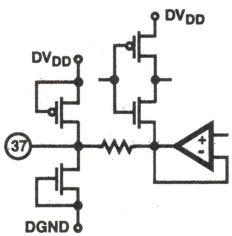
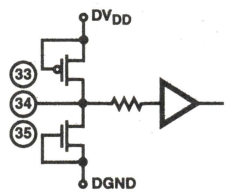
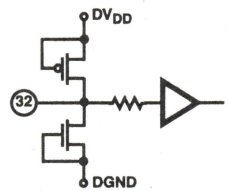
File Number 3936.2

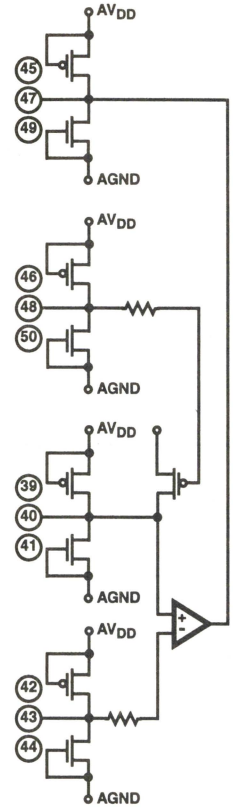
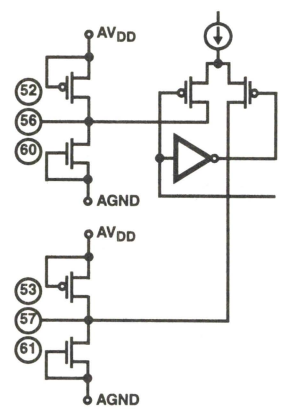
Functional Block Diagram



Pin Descriptions and Equivalent Circuits

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 - 10	R0 - R9		Digital Inputs.
11 - 20	G0 - G9		
21 - 30	B0 - B9		
31	BLANK		Output Blanking Input. High: Outputs Set to 0mA. Low: Normal Output Operation.
37	V_{BIAS}		Internal Bias Decoupling. Connect a 0.1µF decoupling capacitor to DGND.
33	RCLK		Clock Inputs. All input pins are TTL/CMOS compatible.
34	GCLK		
35	BCLK		
36	DGND		Digital Ground.
38, 51	AGND		Analog Ground.
32	$\overline{CE}$		Chip Enable pin. High: Part Disabled Low: Part Enabled
54, 55, 58, 59, 62, 63	AV_{DD}		Analog Power Supply.

Pin Descriptions and Equivalent Circuits (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
45	V_{REF} OUT R		Reference Output. Typically connected to the Reference Decoupling inputs (COMP R, COMP G, COMP B). See Figures 11 and 12 for various configurations.
47	V_{REF} OUT G		
49	V_{REF} OUT B		
46	COMP R		Reference Decoupling. Connect a decoupling capacitor (0.1µF) to reduce noise on reference to AV_{DD}.
48	COMP G		
50	COMP B		
39	FS ADJUST R		Full Scale Adjust. Typically connect a 1.2kΩ resistor, R_{SET}, to AGND. R_{SET} is used to determine full scale output current.
40	FS ADJUST G		
41	FS ADJUST B		
42	V_{REFR}		Voltage Reference Input. Typically set to 2V and determines full scale output current. $I_{OUT}(\text{Full Scale}) = \frac{V_{REF}}{R_{SET}} \times 16$
43	V_{REFG}		
44	V_{REFB}		
52	ROUT		Current Outputs.
56	GOUT		
60	BOUT		
53	$\overline{\text{ROUT}}$		Inverted Current Outputs.
57	$\overline{\text{GOUT}}$		
61	$\overline{\text{BOUT}}$		
64	DV_{DD}		Digital Power Supply.

Absolute Maximum Ratings $T_A = 25^oC$

Digital Supply Voltage, DV_{DD} to DGND . . . . . +7V
Analog Supply Voltage, AV_{DD} to AGND . . . . . +7V
Digital Input Voltages . . . . . DV_{DD} to DGND
Analog Output Current (I_{OUT}) 30mA

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP Package 80
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP - Lead Tips Only)

Operating Conditions

Supply Voltage, AV_{DD}, AV_{SS} . . . . . 4.75V to 5.25V
DV_{DD}, DV_{SS} . . . . . 4.75V to 5.25V
Clock Pulse Width (t_{PW1}, t_{PW0}) . . . . . 10ns (Min)
Temperature Range (T_{OPR}) . . . . . -20^oC to 75^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $AV_{DD} = +5V$, $DV_{DD} = +5V$, $f_{CLK} = 50MHz$, $R_L = 75\Omega$, $V_{REF} = 2V$, $R_{SET} = 1.2k\Omega$, $T_A = 25^oC$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		-	10	-	Bits
Maximum Conversion Speed		50	-	-	MSPS
Integral Linearity Error, INL	"Best Fit" Straight Line	-2.0	-	2.0	LSB
Differential Linearity Error, DNL		-0.5	-	0.5	LSB
Output Offset Voltage, V_{OS}		-	-	1	mV
Output Full Scale Ratio Error, F_{SRE}	(Note 2)	0	1.5	3	%
Full Scale Output Current, I_{FS}		-	27	30	mA
Full Scale Output Voltage, V_{FS}		1.8	1.9	2.0	V
Output Voltage Compliance Range		-	2.5	-	V
DYNAMIC CHARACTERISTICS					
Glitch Energy, GE		-	50	-	pV/s
Settling Time	$I_{OUT} = 13.5mA$	-	40	-	ns
Crosstalk	10MHz Output Sine Wave	-	50	-	dB
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic Current, I_{IH}		-	-	5	µA
Input Logic Current, I_{IL}		-5	-	-	µA
Digital Input Capacitance, C_{IN}		-	10	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 1	-	5	7	ns
Data Hold Time, t_{HLD}	See Figure 1	-	1	3	ns
Propagation Delay Time, t_{PD}	See Figure 1	-	10	-	ns
Clock Pulse Width, t_{PW1}, t_{PW0}	See Figure 1	10	-	-	ns
POWER SUPPLY CHARACTERISITICS					
Total Supply Current, $AI_{DD} + DI_{DD}$		-	100	110	mA
Analog Supply Current, AI_{DD}		-	92	-	mA
Digital Supply Current, DI_{DD}		-	8	-	mA
Power Dissipation		-	500	550	mW

NOTE:

2. Configured for Common Reference.

$$F_{SRE} = \left| \frac{\text{Full Scale Voltage of Channel}}{\text{Average Full Scale Voltage of All Channels}} - 1 \right| \times 100\%$$

Timing Diagram

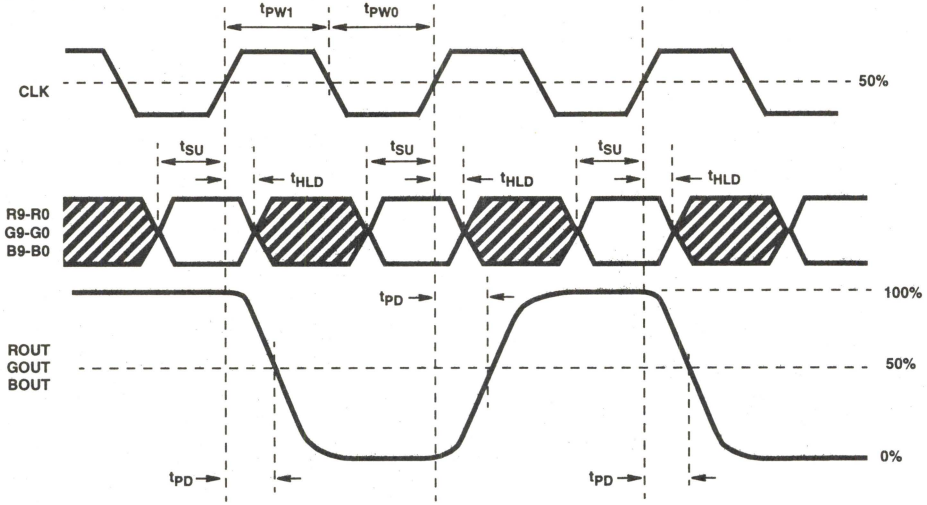


FIGURE 1. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Typical Performance Curves

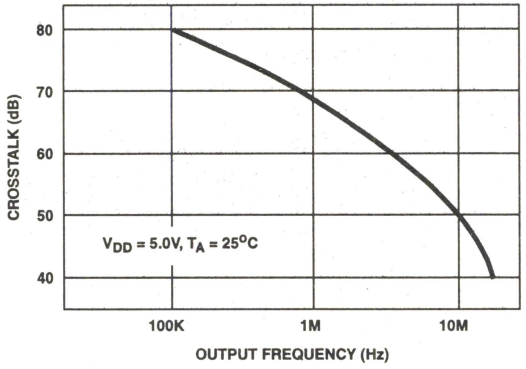


FIGURE 2. CROSSTALK vs OUTPUT FREQUENCY

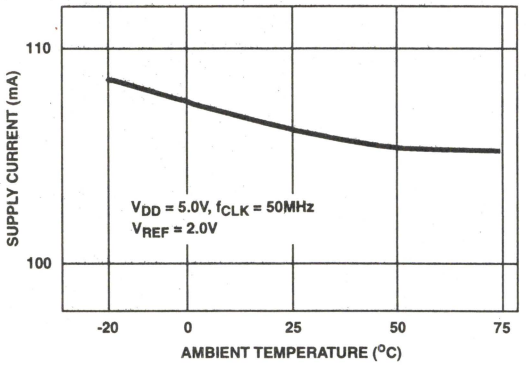


FIGURE 3. SUPPLY CURRENT vs AMBIENT TEMPERATURE

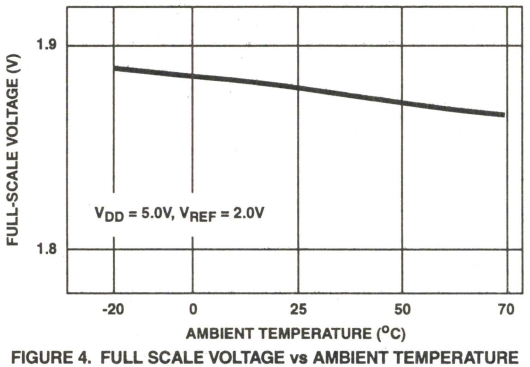


FIGURE 4. FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

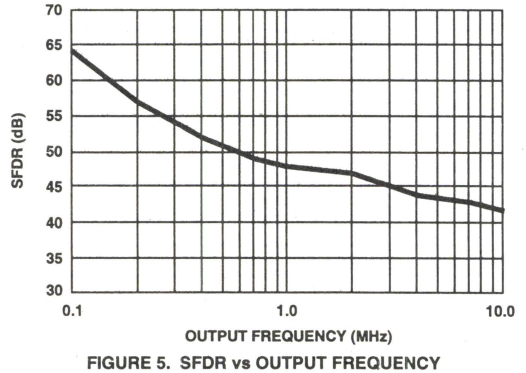


FIGURE 5. SFDR vs OUTPUT FREQUENCY

DAC INPUT/OUTPUT CODE TABLE (NOTE 1)

INPUT CODE										
MSB D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0	OUTPUT VOLTAGE
1	1	1	1	1	1	1	1	1	1	2.0V
				•						
				•						
				•						
1	0	0	0	0	0	0	0	0	0	1.0V
				•						
				•						
				•						
0	0	0	0	0	0	0	0	0	0	0V

NOTE:

1. V_{REF} = 2.0V, R_{SET} = 1.2K, R_{LOAD} = 75Ω.

Detailed Description

The HI3050 contains three matched, individual, 10 bit current output digital-to-analog converters. The DACs can convert at 50MHz and run on +5V for both the analog and digital supplies. The architecture is a current cell arrangement. 10-bit linearity is obtained without laser trimming due to an internal calibration.

Digital Inputs

The digital inputs to the HI3050 have TTL level thresholds. Due to the low input currents CMOS logic can be used as well. The digital inputs are latched on the rising edge of the clock.

To reduce switching noise from the digital data inputs, a series termination resistor is the best solution. Using a 50Ω to 130Ω resistor in series with the data lines, the edge rates are slowed. Slower edge rates reduce the amount of overshoot and undershoot that directly couples through the lead frame of the device. TTL drivers such as the 74ALS or 74F series or CMOS logic series drivers, ACT, AC, or FCT, are excellent for driving the TTL/CMOS inputs of the converter.

Clocks and Termination

The HI3050 clock rate can run to 50MHz, therefore, to minimize reflections and clock noise into the part, proper termination should be considered. In PCB layout clock traces should be kept short and have a minimum of loads. To guarantee consistent results from board to board controlled impedance traces should be used with a characteristic line impedance.

To terminate the clock line, a shunt terminator to an AC ground is the most effective type at a 50MHz clock rate. Shunt termination is best used at the receiving end of the transmission line or as close to the HI3050 CLK pin as possible.

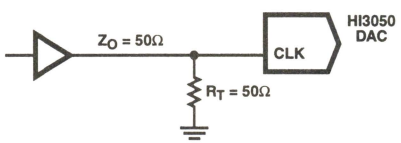


FIGURE 6. AC TERMINATION OF THE HI3050 CLOCK LINE

Rise and fall times and propagation delay of the line will be affected by the Shunt Terminator. The terminator can be connected to DGND.

Power Supplies

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1µF and 0.01µF ceramic capacitors placed as close to the body of the HI3050 as possible on the analog (AV_{DD}) and digital (DV_{DD}) supplies. The analog and digital ground returns should be connected together at the device to ensure proper operation on power up.

Reference

The HI3050 DACs have their own references and can be set individually, see Figure 13. The three references can also share a common reference voltage, see Figure 12. A shared reference gives DAC to DAC matching of 1.5%, typically.

The HI3050 requires an external reference voltage to set the full scale output current. The external reference voltage is connected to the V_{REF} inputs (V_{REFR}, V_{REFG}, and VREFB). The Full Scale Adjust input (FS ADJUST R, FS ADJUST G, FS ADJUST B) should be connected to AGND through a 1.2kΩ resistor, R_{SET}. The reference outputs (V_{REF} OUT R, V_{REF} OUT G, V_{REF} OUT B) should be connected to the decoupling input (COMP R, COMP G, COMP B) and decoupled to AV_{DD} with a 0.1µF capacitor. This improves settling time by decoupling switching noise from the reference output of the HI3050.

The full scale output current is controlled by the voltage reference pin and the set resistor (R_{SET}). The ratio is:

I_{OUT} (Full Scale) = (V_{REF}/R_{SET}) x 16, I_{OUT} is in mA (EQ.1)

Blanking Input

The BLANK input, when pulled high, will force the outputs of all three DACs to 0mA.

Chip Enable

The chip enable input, $\overline{CE}$, will shut down the HI3050 causing the outputs to go to 0mA. The analog and digital supply current will decrease to less than 1mA, reducing power for low power applications.

Outputs

The HI3050 DAC outputs are complementary current outputs. Current is steered to either I_{OUT} or $I_{\overline{OUT}}$ in proportion to the digital input code. The current output can be converted to a voltage by using a resistor load or I/V converting op amp. If only one output of a converter is being used, the unused output can be connected to ground or to a load equal to the used output. The output voltage when using a resistor load is:

$$V_{OUT} = I_{OUT} \times R_{OUT} \quad \text{(EQ. 2)}$$

The compliance range of the outputs is from 0V to +2.5V.

To convert the output current of the D/A converter to a voltage a load resistor followed by a buffer amplifier can be used as shown in Figure 5. The DAC needs a 75Ω termination resistor on the I_{OUT} pin to ensure proper settling.

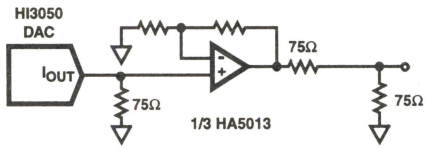


FIGURE 7. HIGH SPEED CURRENT TO VOLTAGE CONVERSION

Glitch

The output glitch of the HI3050 is measured by summing the area under the switching transients after an update of the DAC. Glitch is caused by the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). Unequal delay paths through the device can also cause one current source to change before another. To minimize this, the Harris HI3050 employs an internal register, just prior to the current sources, that is updated on the clock edge.

In measuring the output glitch of the HI3050, the output is terminated into a 75Ω load. The glitch is measured at the major carries throughout the DACs output range.

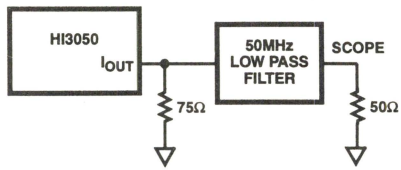
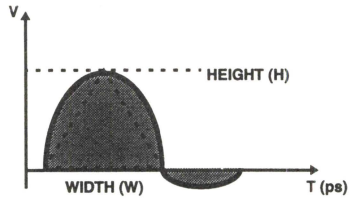


FIGURE 8. GLITCH TEST CIRCUIT

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 9 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt/seconds (pV/s).



GLITCH AREA = $^1/_2$ (H X W)

FIGURE 9. GLITCH ENERGY

Test Circuits

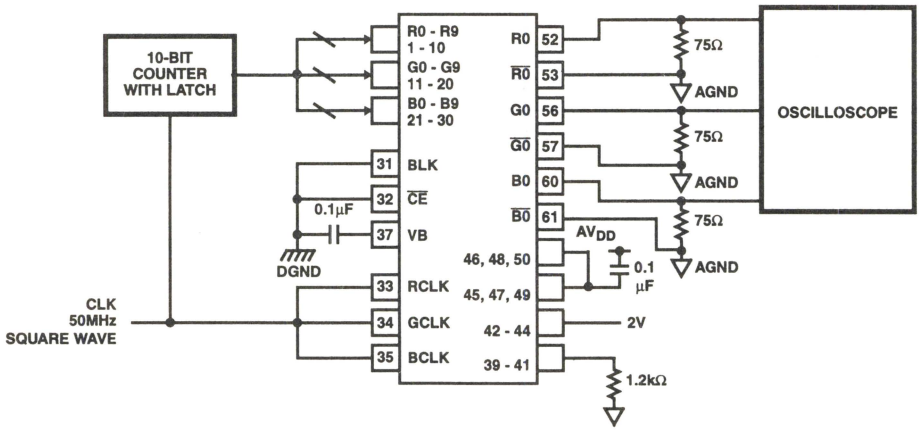


FIGURE 10. MAXIMUM CONVERSION SPEED TEST CIRCUIT

Test Circuits (Continued)

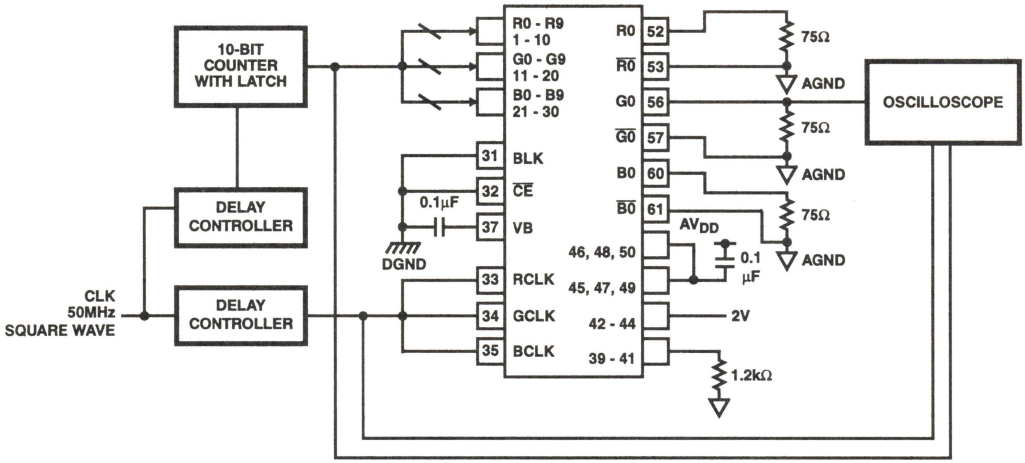


FIGURE 11. SETUP HOLD TIME AND GLITCH ENERGY TEST CIRCUIT

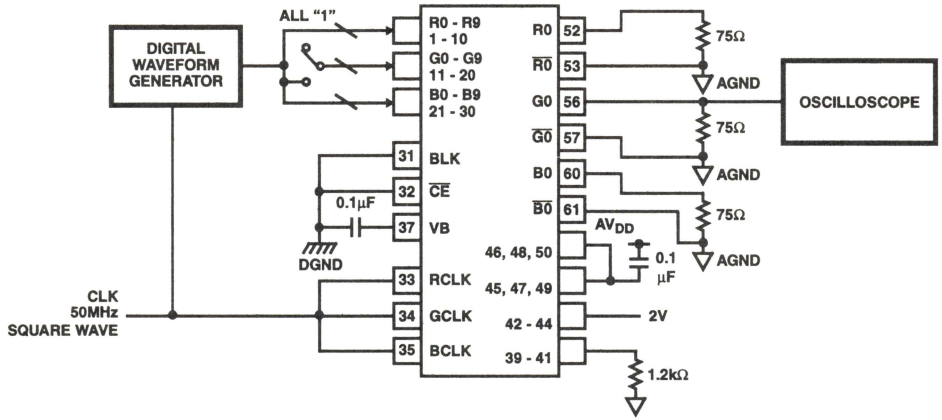


FIGURE 12. CROSSTALK TEST CIRCUIT

Applications Circuits

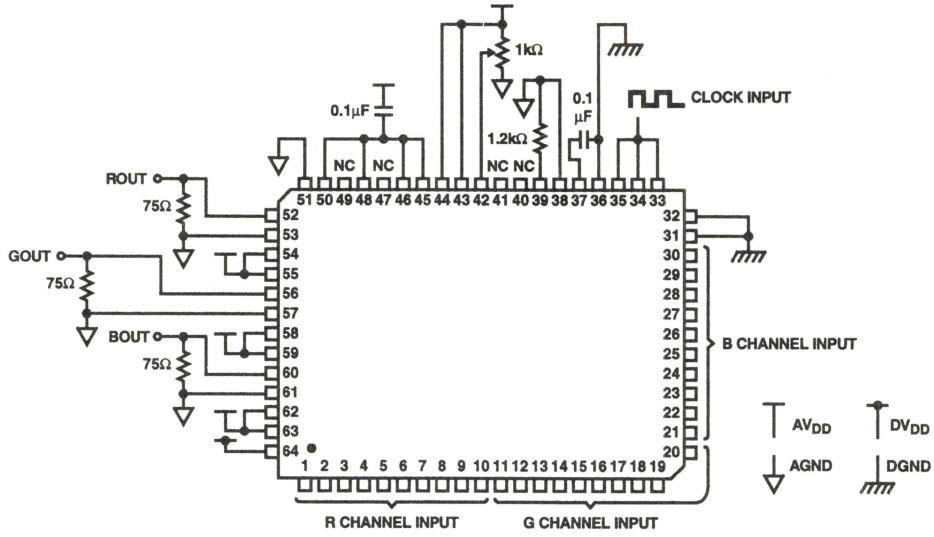


FIGURE 13. COMMON VOLTAGE REFERENCE

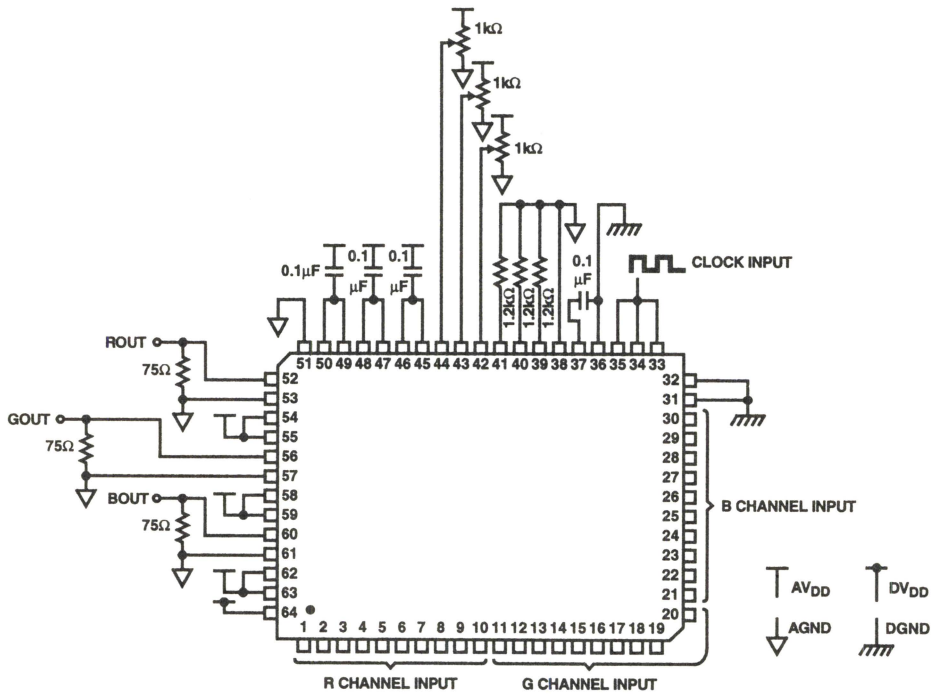


FIGURE 14. INDEPENDENT REFERENCES

Definition of Specifications

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Crosstalk, is the undesirable signal coupling from one channel to another.

Feedthrough, is the measure of the undesirable switching noise coupled to the output.

Output Voltage Full Scale Settling Time, is the time required from the 50% point on the clock input for a full scale step to settle within an $^1/_2$ LSB error band.

Output Voltage Small Scale Settling Time, is the time required from the 50% point on the clock input for a 100mV step to settle within an $^1/_2$ LSB error band. This is used by applications reconstructing highly correlated signals such as sine waves with more than 5 points per cycle.

Glitch Energy, GE, is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a Volt-Time specification.

Differential Gain, DG, is the peak difference in chrominance amplitude (in percent) at two different DC levels.

Differential Phase, DP, is the peak difference in chrominance phase (in degrees) at two different DC levels.

Signal to Noise Ratio, SNR, is the ratio of a fundamental to the noise floor of the analog output. The first 5 harmonics are ignored, and an output filter of $^1/_2$ the clock frequency is used to eliminate alias products.

Total Harmonic Distortion, THD, is the ratio of the DAC output fundamental to the RMS sum of the harmonics. The first 5 harmonics are included, and an output filter of $^1/_2$ the clock frequency is used to eliminate alias products.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at $^1/_2$ the clock frequency to eliminate noise from clocking alias terms.

Intermodulation Distortion, IMD, is the measure of the sum and difference products produced when a two tone input is driven into the D/A. The distortion products created will arise at sum and difference frequencies of the two tones. IMD is:

$$IMD = \frac{20\ Log\ (RMS\ of\ Sum\ and\ Difference\ Distortion\ Products)}{(RMS\ Amplitude\ of\ the\ Fundamental)}$$

HARRIS SEMICONDUCTOR

HI3197

PRELIMINARY

August 1997

10-Bit, 125 MSPS D/A Converter

Features

- Maximum Conversion Rate . . . . . 125 MSPS
- Low Glitch Energy . . . . . .1.5pV•s
- Low Power Consumption . . . . . .400mW (Typ)
- Differential Linearity Error . . . . . ±0.5 LSB or Less
- Integral Linearity Error . . . . . ±1.0 LSB or Less
- Data Input Level . . . . . .TTL
- Clock, Reset Input Level: TTL and PECL Compatible
- 2:1 Multiplexed Input Function
- $^1/_2$ Frequency-Divided Clock Output Possible by the Built-In Clock Frequency Divider Circuit
- Voltage Output (50Ω Load Drive Possible)
- Single Power Supply or ±Dual Power Supplies
- Polarity Switching Function of Reset Signal

Applications

- LCD
- DDS
- HDTV
- Communications (QPSK, QAM)
- Measuring Devices

Description

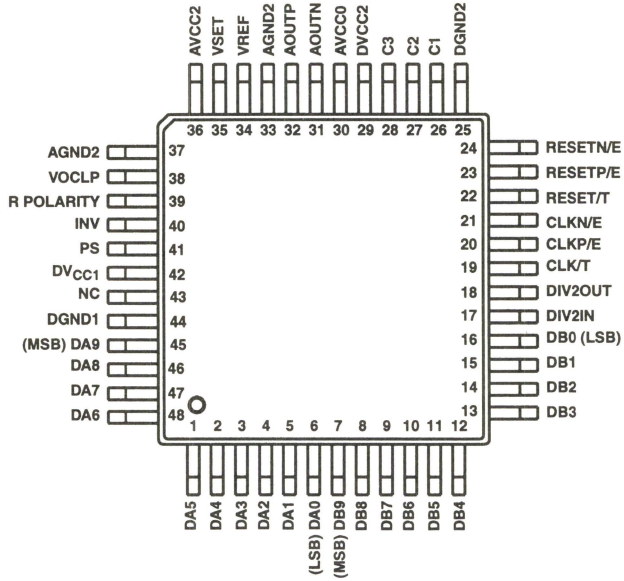
The HI3197 is a high-speed D/A converter which can perform the multiplexed input of the two system 10-bit data. The maximum conversion rate achieves 125 MSPS. The multiplexed operation is possible by the 1/2 frequency-divided clock or by halving the frequency of the clock with the clock frequency divider circuit having the reset pin in the IC. The data input is TTL; the clock input pin and reset input pin can select either TTL or PECL according to the application.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
TBD			

Pinout

HI3197 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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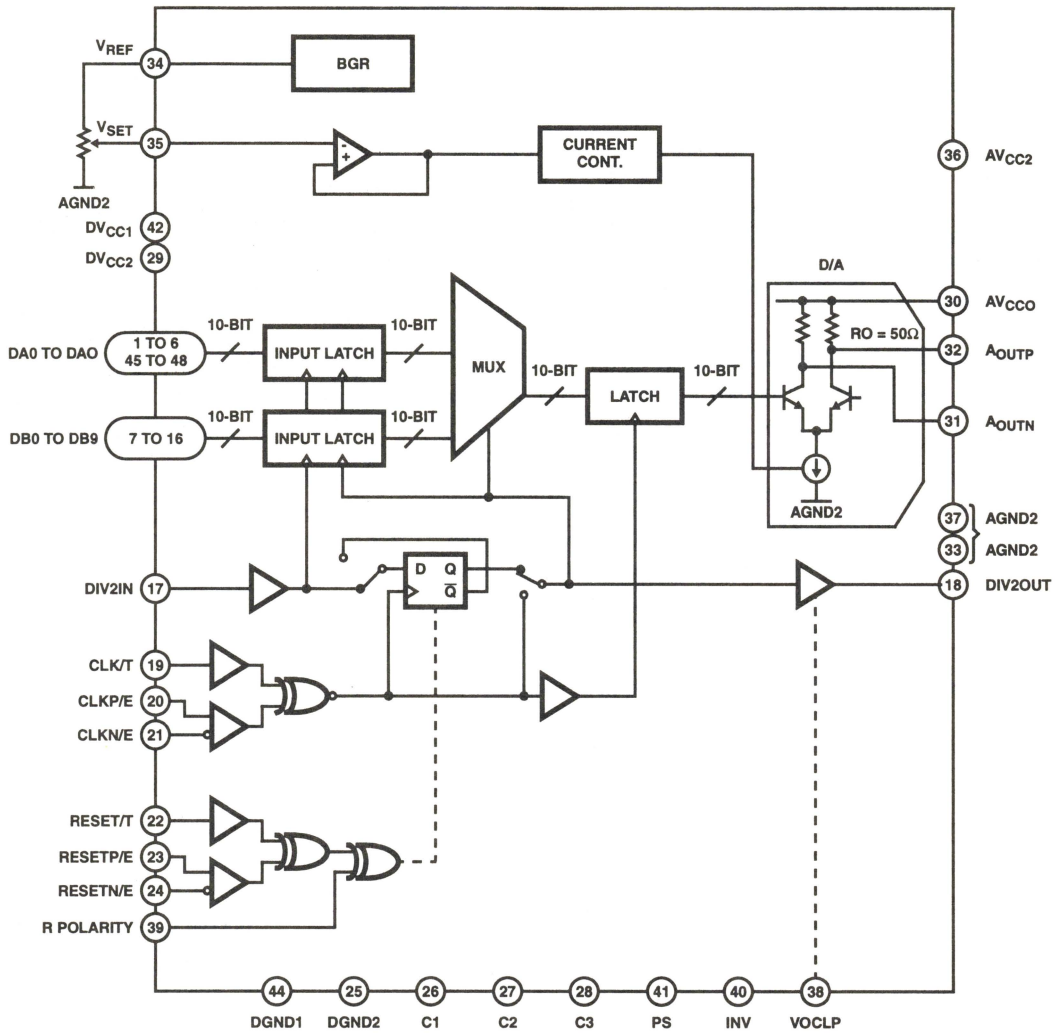
File Number 4356

Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{CC0}, AV_{CC2}, DV_{CC2}) . . . . . -0.5 to +7.0V
AGND2, DGND2 . . . . . -7.0 to +0.5V
DV_{CC1} . . . . . -0.5 to +7.0V
AV_{CC2} - AGND2 . . . . . -0.5 to +7.0V
AV_{CC0} - AGND2 . . . . . -0.5 to +7.0V
DV_{CC2} - DGND2 . . . . . -0.5 to +7.0V
Input Voltage
V_{SET}, AGND2 . . . . . -05 to AV_{CC2} + 0.5V
TTL Pin . . . . . DGND1 -0.5 to DV_{CC1} + 0.5V
PECL Pin, ... DGND1 -0.5 to DV_{CC1} + 0.5V
PS . . . . . DGND1 -0.5 to DV_{CC1} + 0.5V
(Others), VOCLP . . . . . DGND1 -0.5 to DV_{CC1} + 5V
Power Dissipation, P_D 1.4W
(When mounted on a glass fabric base epoxy board with 76mm x 114mm, 1.6mm thick)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	TBD

Maximum Junction Temperature (Hermetic Package or Die) . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range, T_{STG} . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Recommended Operating Conditions

SINGLE POWER SUPPLY	MIN	TYP	MAX	DUAL POWER SUPPLY	MIN	TYP	MAX
AV_{CC0}	4.75V	5.0V	5.25V	AV_{CC0}	-0.05V	0V	0.05V
AV_{CC2}	4.75V	5.0V	5.25V	AV_{CC2}	-0.05V	0V	0.05V
AGND2	-0.05V	0V	0.05V	AGND2	-5.50V	-5.0V	-4.75V
DV_{CC1}	4.75V	5.0V	5.25V	DV_{CC1}	4.75V	5.0V	5.25V
DGND1	-0.05V	0V	0.05V	DGND1	-0.05V	0V	0.05V
DV_{CC2}	-4.75V	5.0V	5.25V	DV_{CC2}	-0.05V	0V	0.05V
DGND2	-0.05V	0V	0.05V	DGND2	-5.50V	-5.0V	-4.75V

INPUT VOLTAGE		SYMBOL	MIN	TYP	MAX	UNITS
Analog	V_{SET}	-	AGND2 + 0.7	-	AGND2 + 1.03	V
Digital	TTL Pin	V_{IH}	DGND1 + 2.0	-	-	V
		V_{IL}	-	-	-	V
	PECL Pin	V_{IH}	DGND1 + 2.6	-	DV_{CC1}	V
		V_{IL}	-	V_{IH} - 0.8	V_{IH} - 0.4	V
	PS	V_{IH}	DGND1 + 2.0	-	-	V
		V_{IL}	-	-	DGND1 + 0.8	V
Others	V_{OCLP}	-	DGND1 + 2.7	-	DV_{CC1}	V
CLK Pulse Width	t_{PW1}	-	4.0	-	-	ns
	t_{PW0}	-	4.0	-	-	ns
Maximum Conversion Rate		f_C	125	-	-	MSPS
Load Resistance		R_L	50	50	≥10K	Ω
Analog Output Full Scale Voltage	$R_L \geq 10k\Omega$	V_{FS}	1.5	2.0	2.2	V
	$R_L = 50\Omega$	V_{FS}	0.75	1.0	1.2	V
Operating Temperature		T_A	-20	-	75	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

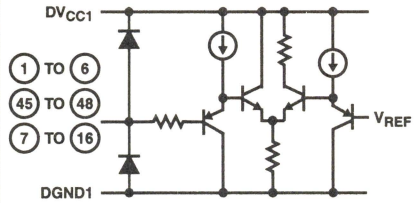
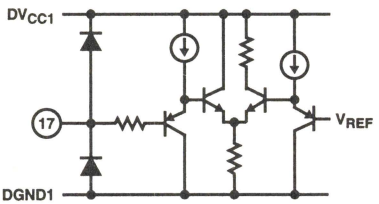
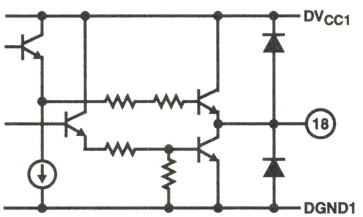
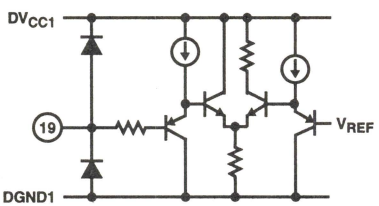
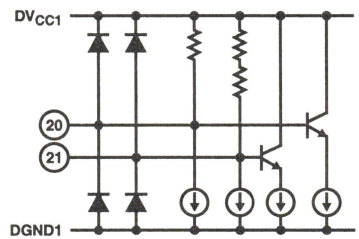
Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	n		-	10	-	Bit
Integral Linearity Error	INL	V_{FS} = 1V	-	-	±0.5	LSB
Differential Linearity Error	DNL		-	-	±1.0	LSB
Digital Input Current (TTL Pin)	I_{IH}	I_{IH} = 2.0V	-10	-	0	µA
	I_{IL}	I_{IL} = 0.8V	-10	-	0	µA
Digital Input Current (PECL Pin)	I_{IH}	$V_{IH} = DV_{CC1}$ -1.1	-	-	10	µA
	I_{IL}	$V_{IL} = DV_{CC1}$ -1.5	-	-	10	µA
Digital Input Current (PS)	I_{IH}	V_{IH} = 2.0V or more	5	-	60	µA
	I_{IL}	V_{IL} = 0.8V or less	0	-	-	µA
Clamp Pin Input Current (VOCLP)	I_O	$V = DV_{CC1}$	-	-	0	µA
	I_O	V = 2.7V	-10	-	-	µA
Digital Input Capacitance	C_{IN}		-	3	-	pF
Digital Output Voltage (DIV2OUT)	V_{OH}	I_{OH} = -2mA	2.4	-	-	V
	V_{OL}	I_{OL} = 1mA	-	-	0.5	V
V_{REF} Pin Voltage	V_{REF}	I_{REF} = 1mA	AGND2 +1.16	AGND2 +1.20	AGND2 +1.24	V
Analog Output Voltage	V_{FS}	$R_L = 50\Omega$	1.5	2.0	2.2	V
		$R_L \geq 10k\Omega$	0.75	1.0	1.2	V
Compliance Voltage	V_{OC}		-	-	-	V
Output Zero Offset Voltage	V_{OF}	$R_L = 50\Omega$	-	-	6	mV
		$R_L \geq 10k\Omega$	-	-	12	mV
Output Resistance	R_O		-	50	-	Ω
Output Capacitance	C_O		-	10	-	pF
Absolute Amplitude Error	EG	V_{FS} = 1V	-10	-	+10	% of FS
Absolute Amplitude Error Temperature Characteristics	TCG		-	-	-	% of FS/°C
Current Consumption	I_{CC}		70	85	100	mA
Maximum Conversion Rate	f_C		125	-	-	MSPS
Analog Output						
Rise Time	t_r	$R_L = 50\Omega$	-	1.0	1.2	ns
Fall Time	t_f		-	1.0	1.2	ns
Settling Time	t_{SET}		-	3.5	-	ns
Glitch Energy	GE		-	1.5	-	pV•S

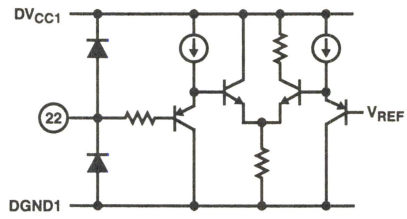
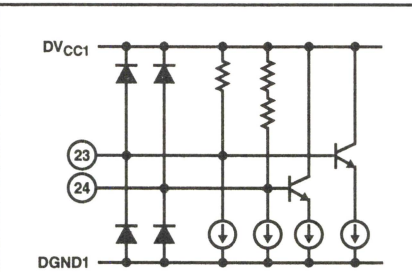
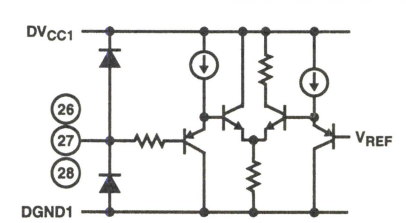
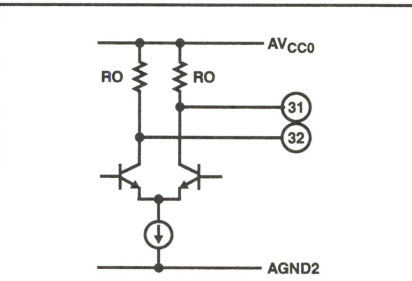
Pin Descriptions

PIN NO.	SYMBOL	LEVEL FOR A SINGLE POWER SUPPLY	LEVEL FOR DUAL POWER SUPPLIES	DESCRIPTION
1 to 6, 45 to 48	DA0 to DA9	TTL	TTL	Side A Data Input.
7 to 16	DB0 to DB9	TTL	TTL	Side B Data Input.
17	DIV2IN	TTL	TTL	$^1/_2$ Frequency-Divided Clock Input.
18	DIV2OUT	TTL	TTL	$^1/_2$ Frequency Divided Clock Output.
19	CLK/T	TTL	TTL	TTL Clock Input.
20	CLKP/E	PECL	PECL	PECL Clock Input.
21	CLKN/E	PECL	PECL	PECL Clock Input.
22	RESET/T	TTL	TTL	TTL Reset Input.
23	RESETP/E	PECL	PECL	PECL Reset Input.
24	RESETN/E	PECL	PECL	PECL Reset Input.
25	DGND2	0V	-5V	Digital Ground.
26	C1	TTL	TTL	Function Setting.
27	C2	TTL	TTL	Function Setting.
28	C3	TTL	TTL	Function Setting.
29	DV_{CC2}	5V	0V	Digital Power Supply.
30	AV_{CCO}	5V (Typ)	0V (Typ)	Analog Output Power Supply.
31	OUTN	AV_{CCO} - V_{FS}	AV_{CCO} - V_{FS}	D/A Negative Output.
32	AOUTP	AV_{CCO} - V_{FS}	AV_{CCO} - V_{FS}	D/A Positive Output.
33	AGND2	0V	-5V	Analog Ground.
34	V_{REF}	AGND2 + 1.2V	AGND2 + 1.2V	Analog reference voltage.
35	V_{SET}			Full scale adjustment.
36	AV_{CC2}	5V	0V	Analog Power Supply.
37	AGND2	0V	-5V	Analog Ground.
38	VOCLP	Clamp Voltage	Clamp Voltage	TTL High Level Clamp.
39	R POLARITY	TTL	TTL	Reset signal polarity switching.
40	INV	TTL	TTL	Analog output inversion.
41	PS	TTL	TTL	Power saving.
42	DV_{CC1}	5V	5V	Digital Power Supply.
43	NC			Not Connected.
44	DGND1	0V	0V	Digital Ground.

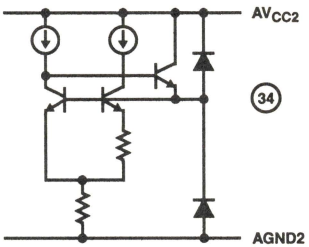
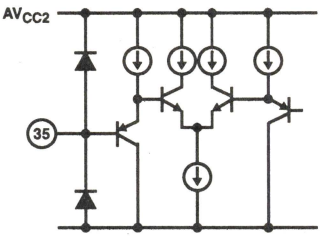
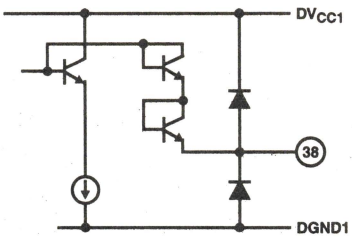
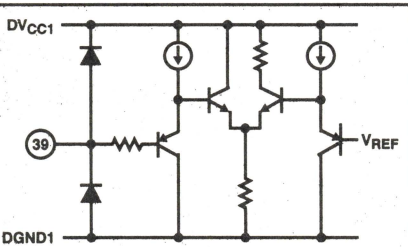
Pin Descriptions and I/O Pin Equivalent Circuits

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 6 45 to 48	DA0 to DA9	I	TTL		Side A Data Input.
7 to 16	DB0 to DA9	I	TTL		Side B Data Input.
17	DIV2IN	I	TTL		1/2 Frequency-Divided Clock Input. Use this pin for MUX.1A or MUX.2 mode. Leave open for other modes.
18	DIV2OUT	O	TTL		1/2 Frequency-Divided Clock Output. The signal with the 1/2 frequency divided clock (DIV2OUT) is output for MUX.1A mode. Leave open for other modes.
19	CLK/T	I	TTL		Clock Input. Use this pin when the clock is input in the TTL level. At this time, leave Pins 20 and 21 open.
20	CLKP/E	I	PECL		Clock Input. Use this pin when the clock is input in PECL level. At this time, leave Pin 19 open.
21	CLKN/E	I	PECL		CLKP/E Complementary Input. When left open, this pin goes to the threshold potential. Operation is possible only with CLKP/E, but complementary input is recommended to attain fast and stable operation.

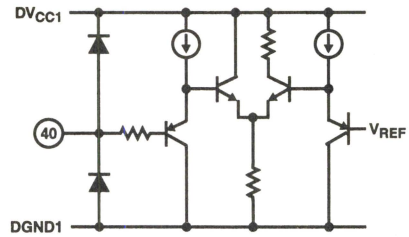
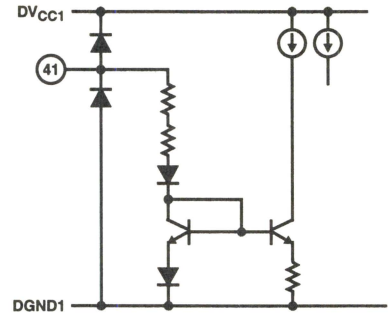
Pin Descriptions and I/O Pin Equivalent Circuits (Continued)

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
22	RESET/T	I	TTL		Reset signal input. When the multiple HI3197 are operated at a time for MUX.1A or MUX.1B mode, the start timing of the internal $^1/_2$ frequency divider circuits should be matched. At this time, the reset signal is used; when the reset signal is the TTL level, Pin 22 is used and Pins 23 and 24 are left open. When the reset signal is the PECL level, Pins 23 and 24 are used and Pin 22 is left open. For the PECL level, operation is possible only with RESETP/E as with the case for the clock. The reset signal polarity can be set by Pin 39 (RPOLARITY). Leave the reset pin open when the other modes are used.
23	RESETP/E	I	PECL		
24	RESETN/E	I	PECL		
25	DGND2		Single Power Supply: GND Dual Power Supplies: -5V		Digital Power Supply.
26	C1	I	TTL		Function setting.
27	C2	I	TTL		
28	C3	I	TTL		
29	DV_{CC2}		Single Power Supply: +5V Dual Power Supplies: GND		Digital Power Supply.
30	AV_{CC0}				Analog Output Power Supply.
31	OUTN	O	AV_{CC0} - V_{FS}		D/A Negative Output. The inversion of the D/A positive output pin is output. Terminate the inversion without pin with 50Ω when the inversion output is not used and the positive output is terminated with 50Ω.
32	AOUTP	O	AV_{CC0} - V_{FS}		D/A positive output.

Pin Descriptions and I/O Pin Equivalent Circuits (Continued)

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
33	AGND2		Single Power Supply: GND Dual Power Supplies: -5V		Analog Ground.
34	V_{REF}	O	AGND +1.2V		Analog Reference Voltage Output.
35	V_{SET}	I	AGND 2 + 0.7V to AGND2 + 1.03V		Full scale adjustment.
36	AV_{CC2}		Single Power Supply: +5V Dual Power Supplies: GND		Analog Power Supply.
37	AGND2		Single Power Supply: GND Dual Power Supplies: -5V		Analog Power Supply
38	VOCLP	I	Clamp Voltage		TTL Output High Level Clamp. The TTL level signal is output from the DIV2OUT pin for MUX.1A mode. The TTL high level voltage is clamped to the value approximately equivalent to the voltage supplied to this pin. Leave the VOCLP pin open for other modes.
39	P Polarity	I	TTL		Reset signal polarity switching. At high level, the reset polarity is active high; at low level, active low.

Pin Descriptions and I/O Pin Equivalent Circuits (Continued)

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
40	INV	I	TTL		Analog Output polarity inversion. The analog output is inverted at low level.
41	PS	I	TTL		Power saving. Power saving at low level. Normally pull up the PS pin to high level as this pin is open low.
42	DV_{CC1}		5V		Digital Power Supply.
43	NC				No connection.
44	DGND1		0V		Digital Ground.

Description of Operation

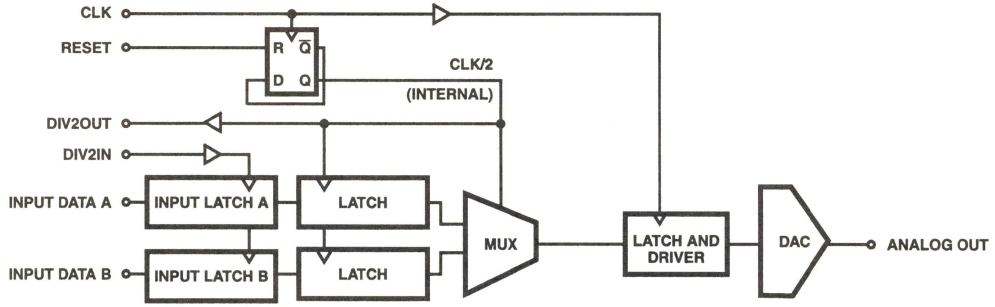


FIGURE 1A. BLOCK DIAGRAM (MUX.1A MODE)

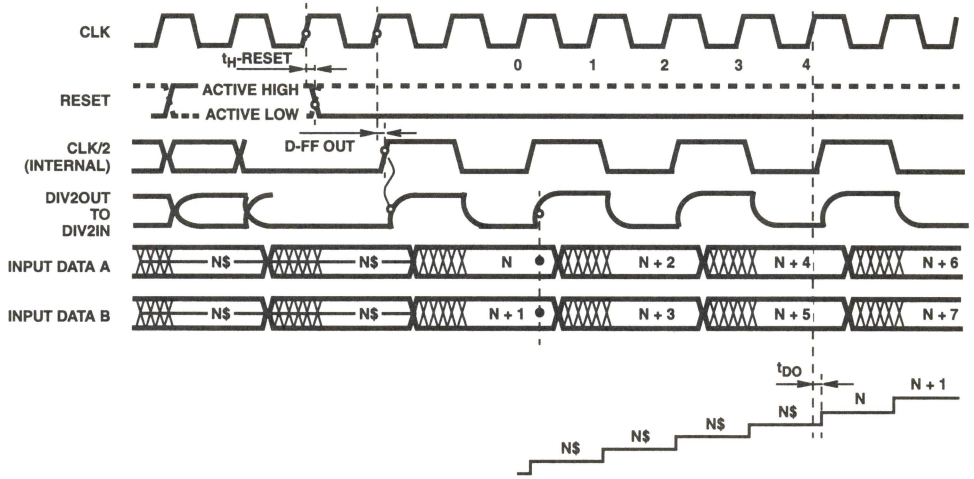


FIGURE 1B. TIMING CHART (MUX.1A MODE)

Description of Operation (Continued)

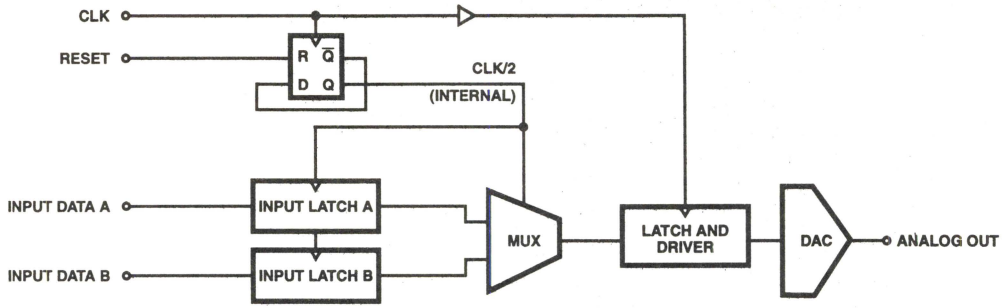


FIGURE 2A. BLOCK DIAGRAM (MUX.1B MODE)

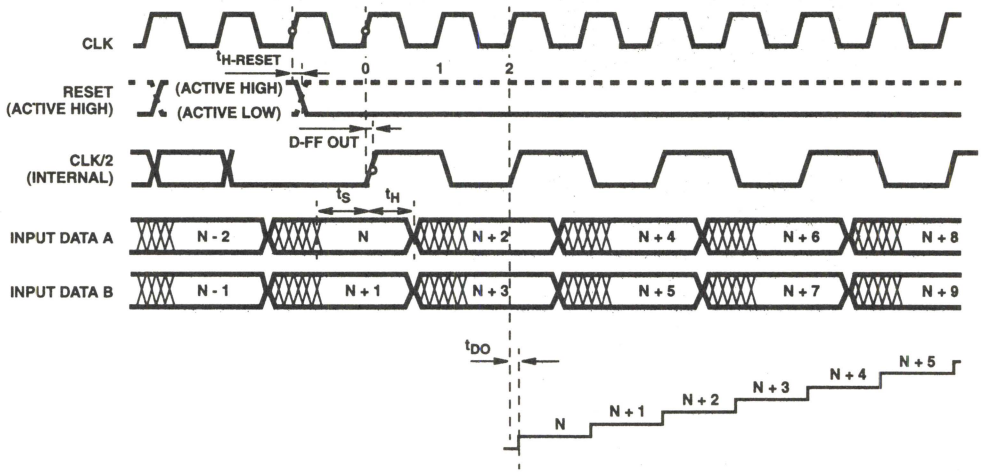


FIGURE 2B. TIMING CHART (MUX.1B MODE)

Description of Operation (Continued)

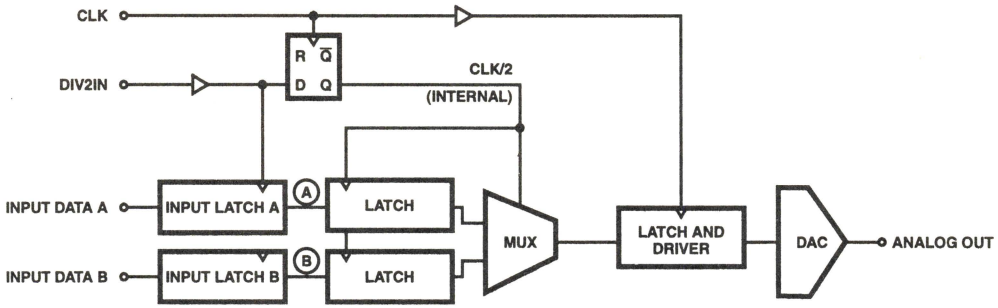


FIGURE 3A. BLOCK DIAGRAM (MUX.2 MODE)

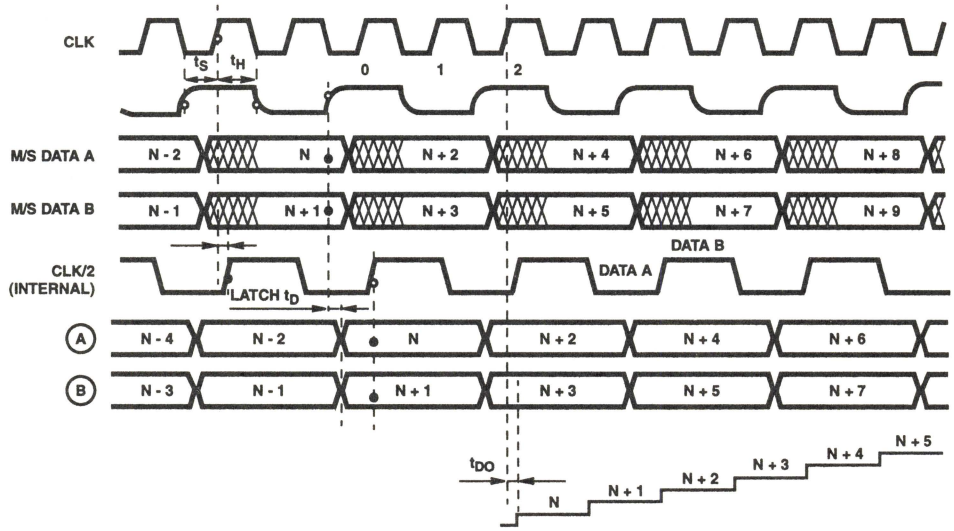


FIGURE 3B. TIMING MODE (MUX.2 MODE)

Description of Operation (Continued)

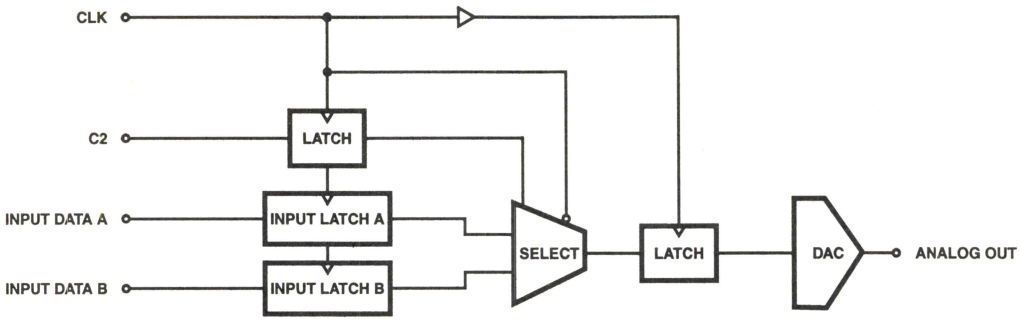


FIGURE 4A. BLOCK DIAGRAM (SELE.A SELE.B MODE)

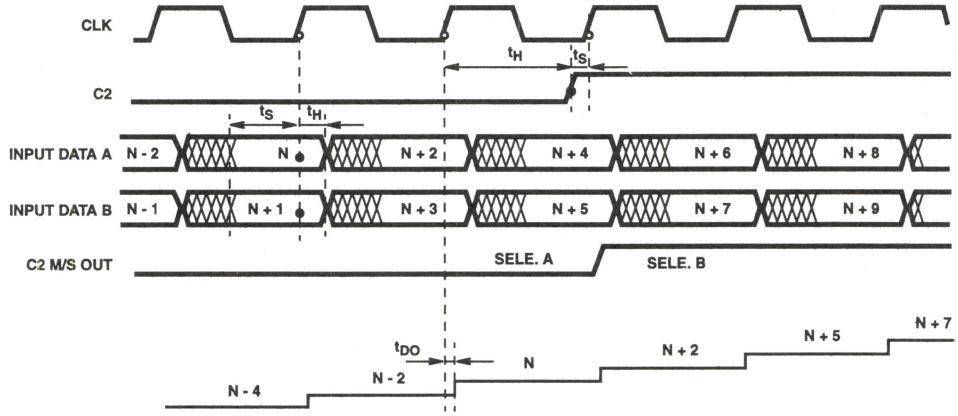


FIGURE 4B. TIMING CHART (SELE.A SELE.B MODE)

Application Circuit

The circuit shown below is the basic circuit when the analog output is terminated with the external resistance of 50Ω in the dual ±5V power supplies for MUX.2 mode.

The analog output full scale voltage V_{FS} is obtained with the following equation:

$$V_{FS} = \frac{V_{SET}}{375} \times \left(15 + \frac{63}{64}\right) \times R$$

$R = R_O // R_L$

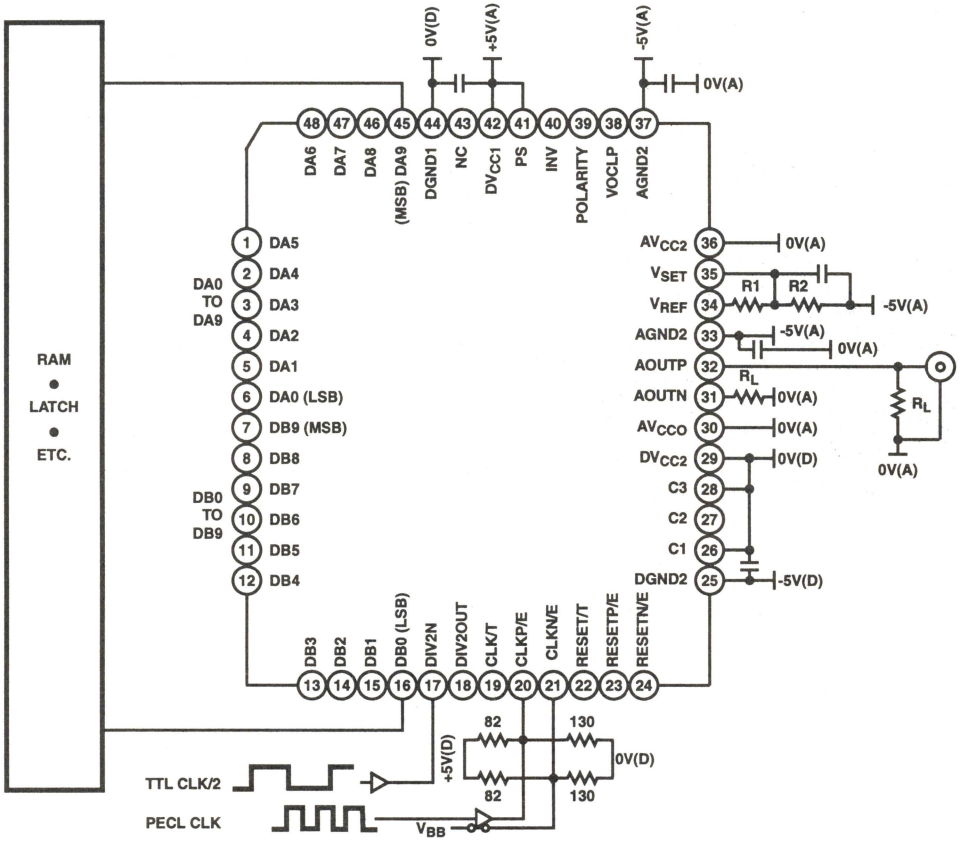
R_O = Output impedance = (50Ω)

R_L = External termination resistance

Here, $V_{SET} = \frac{R2}{R1 + R2} V_{REF}$

($V_{REF} \approx 1.2V$)

($R1 + R2 \geq 1.2k\Omega$)



HARRIS SEMICONDUCTOR

HI3338

August 1997

8-Bit, CMOS R2R D/A Converter

Features

- CMOS Low Power (Typ) 100mW
- R2R Output, Segmented for Low "Glitch"
- CMOS/TTL Compatible Inputs
- Fast Settling (Typ) . . . . . 20ns to $^1/_2$ LSB
- Feedthrough Latch for Clocked or Unclocked Use
- Accuracy (Typ) . . . . . ±0.5 LSB
- Data Complement Control
- High Update Rate (Typ) 50MHz
- Unipolar or Bipolar Operation
- Linearity (INL):
  - HI3338KIP . . . . . ±0.75 LSB
  - HI3338KIB . . . . . ±0.75 LSB

Applications

- TV/Video Display
- High Speed Oscilloscope Display
- Digital Waveform Generator
- Direct Digital Frequency Synthesis
- Wireless Communication

Description

The HI3338 family are CMOS high speed R2R voltage output digital-to-analog converters. They can operate from a single +5V supply, at video speeds, and can produce "rail-to-rail" output swings. Internal level shifters and a pin for an optional second supply provide for an output range below digital ground.

The data complement control allows the inversion of input data while the latch enable control provides either feedthrough or latched operation. Both ends of the R2R ladder network are available externally and may be modulated for gain or offset adjustments. In addition, "glitch" energy has been kept very low by segmenting and thermometer encoding of the upper 3 bits.

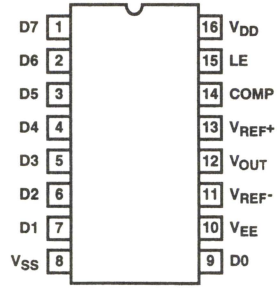
The HI3338 is manufactured to give low dynamic power dissipation, low output capacitance, and inherent latch-up resistance.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI3338KIP	-40 to 85	16 Ld PDIP	E16.3
HI3338KIB	-40 to 85	16 Ld SOIC	M16.3

Pinout

HI3338
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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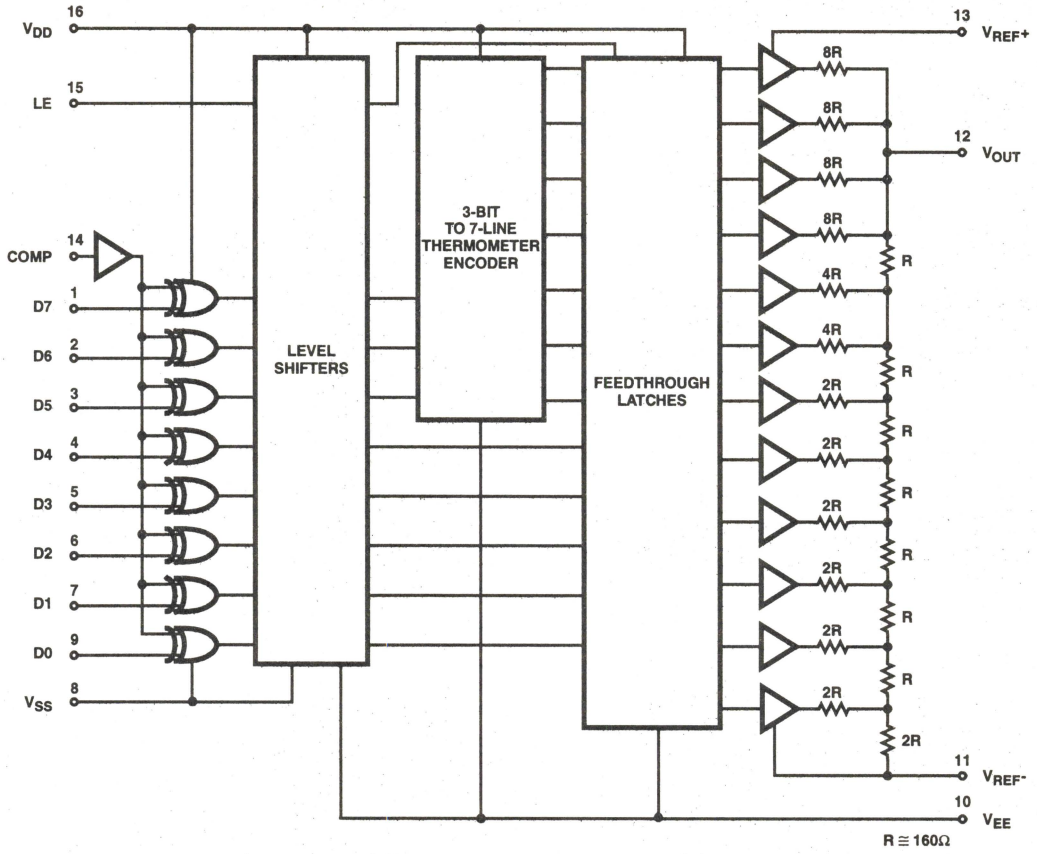
File Number **4134.1**

Functional Diagram



Die Characteristics

DIE DIMENSIONS:

2,740µm x 3,310µm x 530 ±50µm

METALLIZATION:

Type: Al with 0.8% Si
Thickness: 11kÅ ±1kÅ

GLASSIVATION:

Type: 3% PSG
Thickness: 13kÅ ±2.6kÅ

Absolute Maximum Ratings

DC Supply-Voltage Range . . . . . -0.5V to +8V
(V_{DD} - V_{SS} or V_{DD} - V_{EE}, Whichever Is Greater)
Input Voltage Range
Digital Inputs (LE, COMP D0 - D7) . . . . V_{SS} - 0.5V to V_{DD} + 0.5V
Analog Pins (V_{REF}+, V_{REF}-, V_{OUT}) . . . . V_{DD} - 8V to V_{DD} + 0.5V
DC Input Current
Digital Inputs (LE, COMP, D0 - D7) . . . . . ±20mA
Recommended Supply Voltage Range . . . . . .4.5V to 7.5V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package	100

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range, T_{STG} . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A) . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = 25°C, V_{DD} = 5V, V_{REF}+ = 4.608V, V_{SS} = V_{EE} = V_{REF}- = GND, LE clocked at 20MHz, $R_L \geq 1M\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		8	-	-	Bits
Integral Linearity Error	See Figure 4	-	-	±0.75	LSB
Differential Linearity Error	See Figure 4	-	-	±0.5	LSB
Gain Error	Input Code = FF_{HEX}, See Figure 3	-	-	±0.5	LSB
Offset Error	Input Code = 00_{HEX}, See Figure 3	-	-	±0.25	LSB
DIGITAL INPUT TIMING					
Update Rate	To Maintain $^1/_2$ LSB Settling	DC	50	-	MHz
Update Rate	V_{REF}- = V_{EE} = -2.5V, V_{REF}+ = +2.5V	DC	20	-	MHz
Set Up Time t_{SU1}	For Low Glitch	-	-2	-	ns
Set Up Time t_{SU2}	For Data Store	-	8	-	ns
Hold Time t_H	For Data Store	-	5	-	ns
Latch Pulse Width t_W	For Data Store	-	5	-	ns
Latch Pulse Width t_W	V_{REF}- = V_{EE} = -2.5V, V_{REF}+ = +2.5V	-	25	-	ns
OUTPUT PARAMETERS	R_L Adjusted for $1V_{P-P}$ Output				
Output Delay t_{D1}	From LE Edge	-	25	-	ns
Output Delay t_{D2}	From Data Changing	-	22	-	ns
Rise Time t_r	10% to 90% of Output	-	4	-	ns
Settling Time t_S	10% to Settling to $^1/_2$ LSB	-	20	-	ns
Output Impedance	V_{REF}+ = 6V, V_{DD} = 6V	120	160	200	Ω
Glitch Area		-	150	-	pV-s
Glitch Area	V_{REF}- = V_{EE} = -2.5V, V_{REF}+ = +2.5V	-	250	-	pV-s
REFERENCE VOLTAGE					
V_{REF}+ Range	(+) Full Scale (Note 1)	V_{REF}- + 3	-	V_{DD}	V
V_{REF}- Range	(-) Full Scale (Note 1)	V_{EE}	-	V_{REF}+ - 3	V

Electrical Specifications $T_A = 25^oC$, $V_{DD} = 5V$, $V_{REF}+ = 4.608V$, $V_{SS} = V_{EE} = V_{REF}- = GND$, LE clocked at 20MHz, $R_L \geq 1M\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{REF}+$ Input Current	$V_{REF}+ = 6V$, $V_{DD} = 6V$	-	40	50	mA
SUPPLY VOLTAGE					
Static I_{DD} or I_{EE}	LE = Low, D0 - D7 = High	-	100	220	µA
	LE = Low, D0 - D7 = Low	-	-	100	µA
Dynamic I_{DD} or I_{EE}	V_{OUT} = 10MHz, 0V to 5V Square Wave	-	20	-	mA
Dynamic I_{DD} or I_{EE}	V_{OUT} = 10MHz, ±2.5V Square Wave	-	25	-	mA
V_{DD} Rejection	50kHz Sine Wave Applied	-	3	-	mV/V
V_{EE} Rejection	50kHz Sine Wave Applied	-	1	-	mV/V
DIGITAL INPUTS D0 - D7, LE, COMP					
High Level Input Voltage	Note 1	2	-	-	V
Low Level Input Voltage	Note 1	-	-	0.8	V
Leakage Current		-	±1	±5	µA
Capacitance		-	5	-	pF
TEMPERATURE COEFFICIENTS					
Output Impedance		-	200	-	ppm/^{o}C

NOTE:

1. Parameter not tested, but guaranteed by design or characterization.

Timing Diagrams

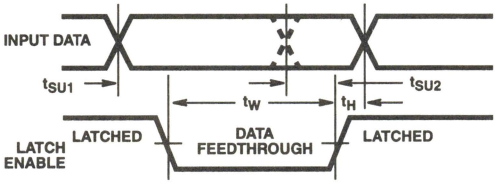


FIGURE 1. DATA TO LATCH ENABLE TIMING

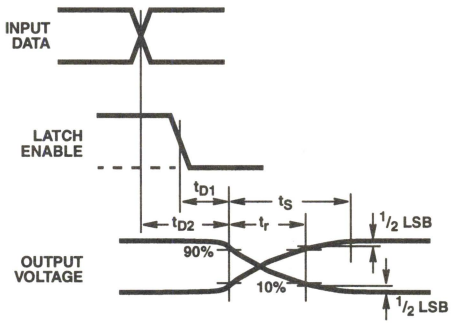


FIGURE 2. DATA AND LATCH ENABLE TO OUTPUT TIMING

Pin Descriptions

PIN	NAME	DESCRIPTION
1	D7	Most Significant Bit.
2	D6	Input
3	D5	Data
4	D4	Bits
5	D3	(High = True)
6	D2	
7	D1	
8	V_{SS}	Digital Ground.
9	D0	Least Significant Bit. Input Data Bit.
10	V_{EE}	Analog Ground.
11	V_{REF}-	Reference Voltage Negative Input.
12	V_{OUT}	Analog Output.
13	V_{REF}+	Reference Voltage Positive Input.
14	COMP	Data Complement Control input. Active High.
15	LE	Latch Enable Input. Active Low.
16	V_{DD}	Digital Power Supply, +5V.

Digital Signal Path

The digital inputs (LE, COMP, and D0 - D7) are of TTL compatible HCT High Speed CMOS design: the loading is essentially capacitive and the logic threshold is typically 1.5V.

The 8 data bits, D0 (weighted 2^0) through D7 (weighted 2^7), are applied to Exclusive OR gates (see Functional Diagram). The COMP (data complement) control provides the second input to the gates: if COMP is high, the data bits will be inverted as they pass through.

The input data and the LE (latch enable) signals are next applied to a level shifter. The inputs, operating between the levels of V_{DD} and V_{SS}, are shifted to operate between V_{DD} and V_{EE}. V_{EE} optionally at ground or at a negative voltage, will be discussed under bipolar operation. All further logic elements except the output drivers operate from the V_{DD} and V_{EE} supplies.

The upper 3 bits of data, D5 through D7, are input to a 3-to-7 line bar graph encoder. The encoder outputs and D0 through D4 are applied to a feedthrough latch, which is controlled by LE (latch enable).

Latch Operation

Data is fed from input to output while LE is low: LE should be tied low for non-clocked operation.

Non-clocked operation or changing data while LE is low is not recommended for applications requiring low output "glitch" energy: there is no guarantee of the simultaneous changing of input data or the equal propagation delay of all bits through the converter. Several parameters are given if the converter is to be used in either of these modes: t_{D2} gives the delay from the input changing to the output changing (10%), while t_{SU2} and t_H give the set up and hold times (referred to LE rising edge) needed to latch data. See Figures 1 and 2.

Clocked operation is needed for low "glitch" energy use. Data must meet the given t_{SU1} set up time to the LE falling edge, and the t_H hold time from the LE rising edge. The delay to the output changing, t_{D1}, is now referred to the LE falling edge.

There is no need for a square wave LE clock; LE must only meet the minimum t_W pulse width for successful latch operation. Generally, output timing (desired accuracy of settling) sets the upper limit of usable clock frequency.

Output Structure

The latches feed data to a row of high current CMOS drivers, which in turn feed a modified R2R ladder network.

The "N" channel (pull down) transistor of each driver plus the bottom "2R" resistor are returned to V_{REF}- this is the (-) full-scale reference. The "P" channel (pull up) transistor of each driver is returned to V_{REF}+, the (+) full-scale reference.

In unipolar operation, V_{REF}- would typically be returned to analog ground, but may be raised above ground (see specifications). There is substantial code dependent current that flows from V_{REF}+ to V_{REF}- (see V_{REF}+ input current in specifications), so V_{REF}- should have a low impedance path to ground.

In bipolar operation, V_{REF}- would be returned to a negative voltage (the maximum voltage rating to V_{DD} must be observed). V_{EE}, which supplies the gate potential for the output drivers, must be returned to a point at least as negative as V_{REF}-. Note that the maximum clocking speed decreases when the bipolar mode is used.

Static Characteristics

The ideal 8-bit D/A would have an output equal to V_{REF}- with an input code of 00_{HEX} (zero scale output), and an output equal to 255/256 of V_{REF}+ (referred to V_{REF}-) with an input code of FF_{HEX} (full scale output). The difference between the ideal and actual values of these two parameters are the OFFSET and GAIN errors, respectively; see Figure 3.

If the code into an 8-bit D/A is changed by 1 count, the output should change by 1/255 (full-scale output-zero scale output). A deviation from this step size is a differential linearity error, see Figure 4. Note that the error is expressed in fractions of the ideal step size (usually called an LSB). Also note that if the (-) differential linearity error is less (in

absolute numbers) than 1 LSB, the device is monotonic. (The output will always increase for increasing code or decrease for decreasing code).

If the code into an 8-bit D/A is at any value, say "N", the output voltage should be N/255 of the full-scale output (referred to the zero-scale output). Any deviation from that output is an integral linearity error, usually expressed in LSBs. See Figure 4.

Note that OFFSET and GAIN errors do not affect integral linearity, as the linearity is referenced to actual zero and full scale outputs, not ideal. Absolute accuracy would have to also take these errors into account.

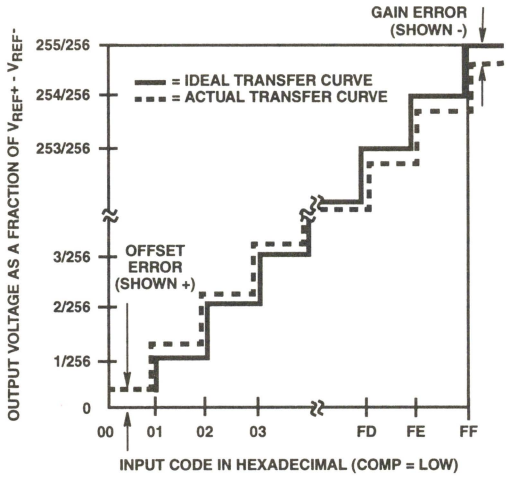


FIGURE 3. D/A OFFSET AND GAIN ERROR

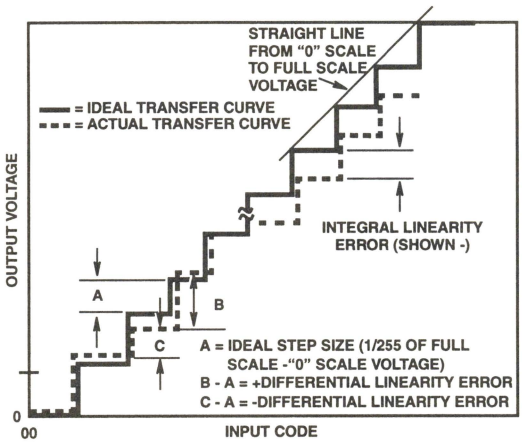


FIGURE 4. D/A INTEGRAL AND DIFFERENTIAL LINEARITY ERROR

Dynamic Characteristics

Keeping the full-scale range (V_{REF}+ - V_{REF}-) as high as possible gives the best linearity and lowest "glitch" energy (referred to 1V). This provides the best "P" and "N" channel gate drives (hence saturation resistance) and propagation delays. The V_{REF}+ (and V_{REF}- if bipolar) terminal should be well bypassed as near the chip as possible.

"Glitch" energy is defined as a spurious voltage that occurs as the output is changed from one voltage to another. In a binary input converter, it is usually highest at the most significant bit transition ($7F_{HEX}$ to 80_{HEX} for an 8-bit device), and can be measured by displaying the output as the input code alternates around that point. The "glitch" energy is the area between the actual output display and an ideal one LSB step voltage (subtracting negative area from positive), at either the positive or negative-going step. It is usually expressed in pV-s.

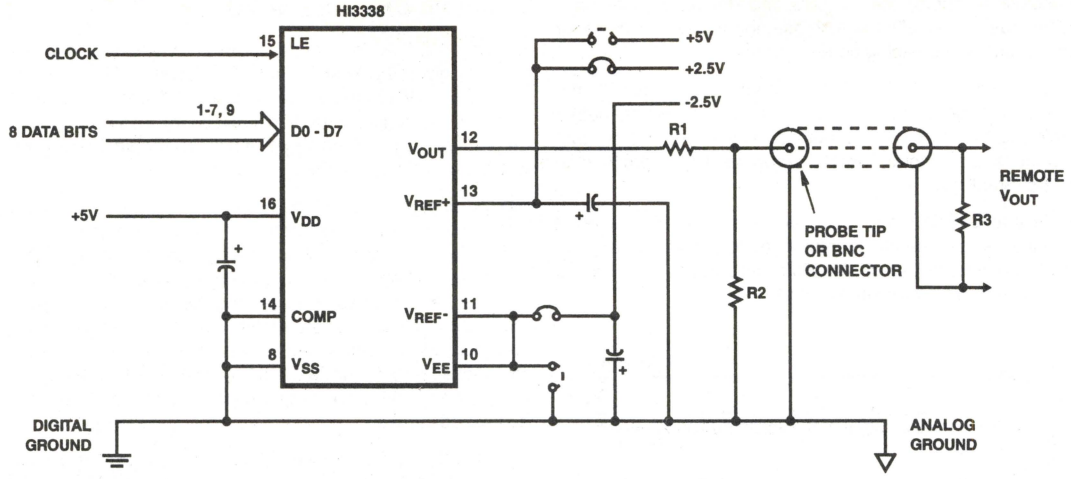
The HI3338 uses a modified R2R ladder, where the 3 most significant bits drive a bar graph decoder and 7 equally weighted resistors. This makes the "glitch" energy at each $^1/_8$ scale transition ($1F_{HEX}$ to 20_{HEX}, $3F_{HEX}$ to 40_{HEX}, etc.) essentially equal, and far less than the MSB transition would otherwise display.

For the purpose of comparison to other converters, the output should be resistively divided to 1V full scale. Figure 5 shows a typical hook-up for checking "glitch" energy or settling time.

The settling time of the A/D is mainly a function of the output resistance (approximately 160Ω in parallel with the load resistance) and the load plus internal chip capacitance. Both "glitch" energy and settling time measurements require very good circuit and probe grounding: a probe tip connector such as Tektronix part number 131-0258-00 is recommended.

TABLE 1. OUTPUT VOLTAGE vs INPUT CODE AND V_{REF}

V_{REF}+ V_{REF}- STEP SIZE	5.12V 0 0.0200V	5.00V 0 0.0195V	4.608V 0 0.0180V	2.56V -2.56V 0.0200V	2.50V -2.50V 0.0195V
Input Code					
$11111112 = FF_{HEX}$	5.1000V	4.9805V	4.5900V	2.5400V	2.4805V
$11111102 = FE_{HEX}$	5.0800	4.9610	4.5720	2.5200	2.4610
•					
•					
•					
$10000001_2 = 81_{HEX}$	2.5800	2.5195	2.3220	0.0200	0.0195
$10000000_2 = 80_{HEX}$	2.5600	2.5000	2.3040	0.0000	0.0000
$01111111_2 = 7F_{HEX}$	2.5400	2.4805	2.2860	- 0.0200	-0.0195
•					
•					
•					
$00000001_2 = 01_{HEX}$	0.0200	0.0195	0.0180	-2.5400	-2.4805
$00000000_2 = 00_{HEX}$	0.0000	0.0000	0.0000	-2.5600	-2.5000

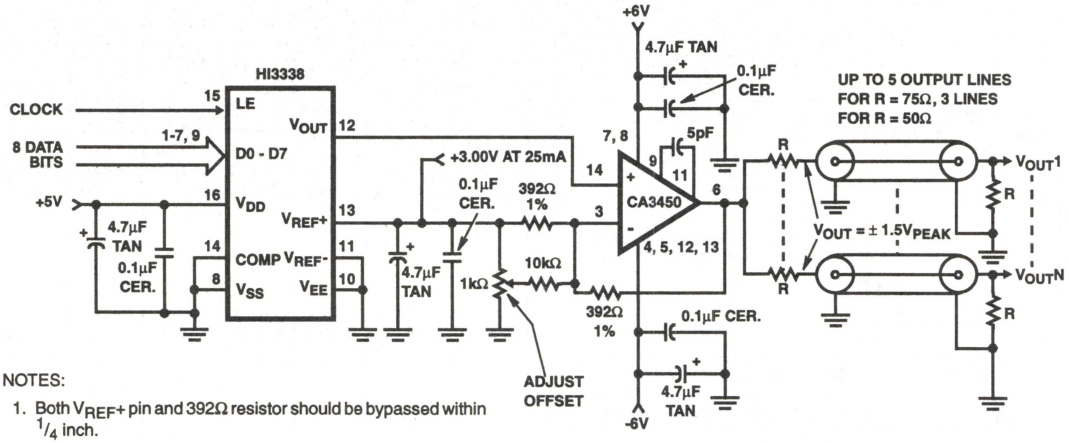


FUNCTION	CONNECTOR	R1	R2	R3	$V_{OUT(P-P)}$
Oscilloscope Display	Probe Tip	82Ω	62Ω	N/C	1V
Match 93Ω Cable	BNC	75	160	93	1V
Match 75Ω Cable	BNC	18	130	75	1V
Match 50Ω Cable	BNC	Short	75	50	0.79V

NOTES:

1. $V_{OUT(P-P)}$ is approximate, and will vary as R_{OUT} of D/A varies.
2. All drawn capacitors are 0.1µF multilayer ceramic/4.7µF tantalum.
3. Dashed connections are for unipolar operation. Solid connection are for bipolar operation.

FIGURE 5. HI3338 DYNAMIC TEST CIRCUIT



NOTES:

1. Both V_{REF+} pin and 392Ω resistor should be bypassed within $^1/_4$ inch.
2. Keep nodal capacitance at CA3450 pin 3 as low as possible.
3. V_{OUT} Range = ±3V at CA3450.

FIGURE 6. HI3338 AND CA3450 FOR DRIVING MULTIPLE COAXIAL LINES

Applications

The output of the HI3338 can be resistively divided to match a doubly terminated 50Ω or 75Ω line, although peak-to-peak swings of less than 1V may result. The output magnitude will also vary with the converter's output impedance. Figure 5 shows such an application. Note that because of the HCT input structure, the HI3338 could be operated up to +7.5V V_{DD} and V_{REF}+ supplies and still accept 0V to 5V CMOS input voltages.

If larger voltage swings or better accuracy is desired, a high speed output buffer, such as the HA-5033, HA-2542, or CA3450, can be employed. Figure 6 shows a typical application, with the output capable of driving ±2V into multiple 50Ω terminated lines.

Operating and Handling Considerations

HANDLING

All inputs and outputs of CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in AN6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

OPERATING

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause the absolute maximum ratings to be exceeded.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 20mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or GND, whichever is appropriate.

HARRIS SEMICONDUCTOR

HI5721

10-Bit, 125 MSPS, High Speed D/A Converter

August 1997

Features

- Throughput Rate ..... 125 MSPS
- Low Power 700mW
- Integral Linearity Error ..... 1.5 LSB
- Low Glitch Energy .....1.5pV•s
- TTL/CMOS Compatible Inputs
- Improved Hold Time 0.5ns
- Excellent Spurious Free Dynamic Range
- Improved Second Source for the AD9721

Applications

- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- HDTV
- Test Equipment
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

Description

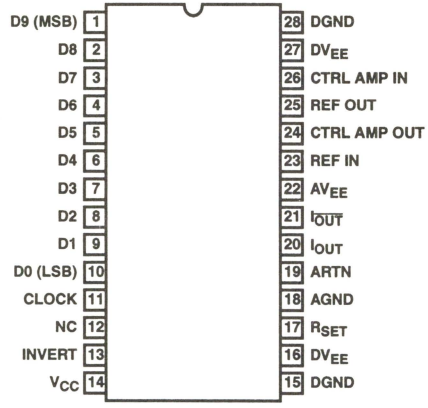
The HI5721 is a 10-bit, 125 MSPS, high speed D/A converter. The converter incorporates a 10-bit, input data register with quadrature data logic capability and current outputs. The HI5721 features low glitch energy and excellent frequency domain specifications.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5721BIP	-40 to 85	28 Ld PDIP	E28.6
HI5721BIB	-40 to 85	28 Ld SOIC (W)	M28.3
HI5721-EVP	25	Evaluation Board (PDIP)	
HI5721-EVS	25	Evaluation Board (SOIC)	

Pinout

HI5721
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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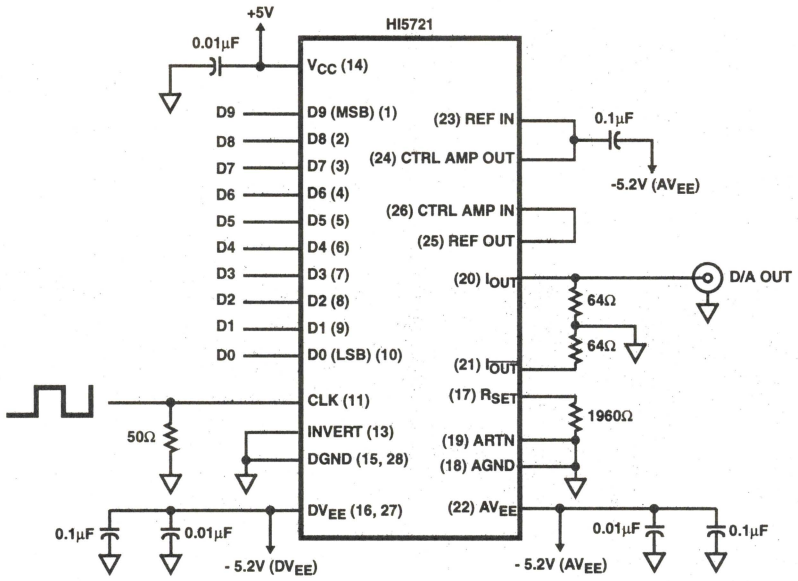
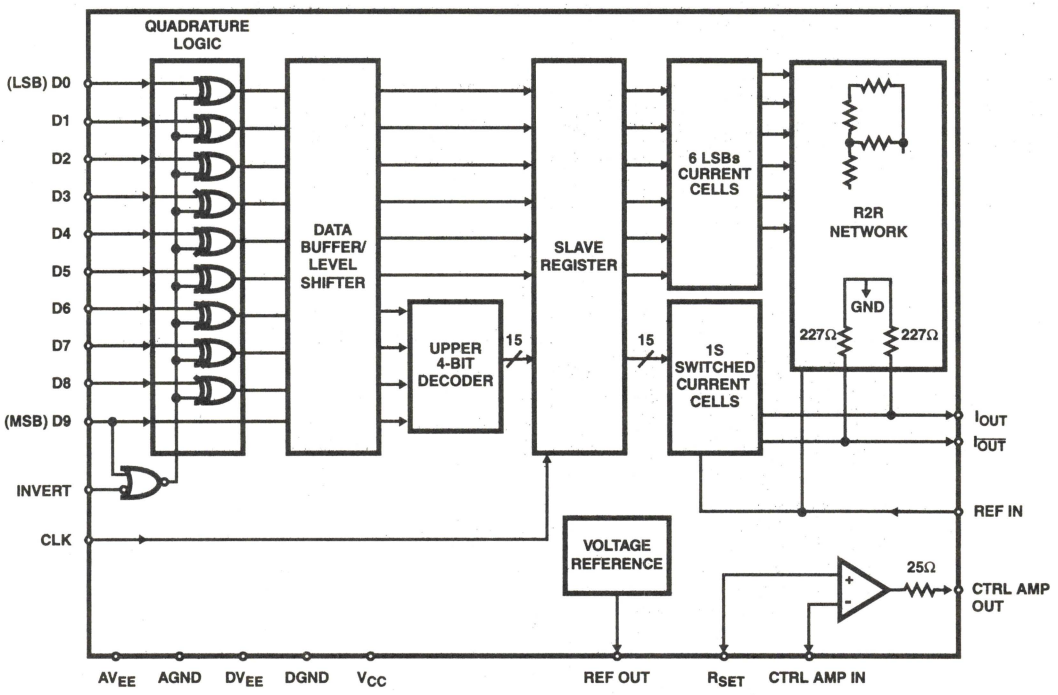
File Number **3949.5**

Typical Applications Circuit



Functional Block Diagram



Absolute Maximum Ratings

Digital Supply Voltage V_{CC} to DGND . . . . . +5.5V
Negative Digital Supply Voltage DV_{EE} to DGND . . . . . -5.5V
Negative Analog Supply Voltage AV_{EE} to AGND, ARTN . . . . . -5.5V
Digital Input Voltages (D9-D0, CLK, INVERT) . . . . . V_{CC} to -0.5 V
Internal Reference Output Current 500µA
Control Amplifier Input Voltage Range . . . . . AGND to -4.0V
Control Amplifier Output Current . . . . . ±2.5mA
Reference Input Voltage Range . . . . . -3.7 V to AV_{EE}
Analog Output Current (I_{OUT}) 30mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}(°C/W)
PDIP Package	55
SOIC Package	70

Maximum Power Dissipation
HI5721BIx 750mW
Maximum Junction Temperature
HI5721BIx . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, CTRL AMP IN = REF OUT, T_A = 25°C for All Typical Values

PARAMETER	TEST CONDITIONS	HI5721BI T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	(Note 4) ("Best Fit" Straight Line)	-	±0.5	±1.5	LSB
Differential Linearity Error, DNL	(Note 4)	-	±0.5	±1.0	LSB
Offset Error, I_{OS}	(Note 4)	-	16	75	µA
Full Scale Gain Error, FSE	(Notes 2, 4)	-	2	10	%
Offset Drift Coefficient	(Note 3)	-	0.1	-	µA/°C
Full Scale Output Current, I_{FS}		-	-20.48	-	mA
Output Voltage Compliance Range	(Notes 3, 5)	-1.5	-	+3.0	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	(Note 3)	125.0	-	-	MSPS
Output Voltage Full Scale Step Settling Time, $t_{SETT\ FS}$	To ±0.5 LSB Error Band R_L = 50Ω (Note 3)	-	4.5	-	ns
Output Voltage Small Step Settling Time, $t_{SETT\ SM}$	100mV Step to ±0.5 LSB Error Band, R_L = 50Ω (Note 3)	-	3.5	-	ns
Singlet Glitch Area, GE (Peak Glitch)	R_L = 50Ω (Note 3)	-	3.5	-	pV•s
Doublet Glitch Area, (Net Glitch)		-	1.5	-	pV•s
Output Slew Rate	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	1,000	-	V/µs
Output Rise Time	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	675	-	ps
Output Fall Time	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	470	-	ps

Electrical Specifications AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, CTRL AMP IN = REF OUT, T_A = 25°C for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	HI5721BI T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
Spurious Free Dynamic Range, SFDR to Nyquist	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, 62.5MHz Span (Notes 3, 5)	-	-59	-	dBc
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz, 62.5MHz Span (Notes 3, 5)	-	-53	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, 50MHz Span (Notes 3, 5)	-	-59	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz, 50MHz Span (Notes 3, 5)	-	-51	-	dBc
Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, 2MHz Span (Notes 3, 5)	-	-75	-	dBc
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz, 2MHz Span (Notes 3, 5)	-	-70	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, 2MHz Span (Notes 3, 5)	-	-75	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz, 2MHz Span (Notes 3, 5)	-	-72	-	dBc
Signal to Noise Ratio (SNR) to Nyquist (Ignoring the First 5 Harmonics)	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 5)	-	54	-	dB
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz (Notes 3, 5)	-	51.5	-	dB
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 5)	-	54.5	-	dB
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz (Notes 3, 5)	-	50.3	-	dB
Signal to Noise Ratio + Distortion (SINAD) to Nyquist	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 5)	-	52.4	-	dB
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz (Notes 3, 5)	-	49.2	-	dB
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 5)	-	52.7	-	dB
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz (Notes 3, 5)	-	47.6	-	dB
Total Harmonic Distortion (THD) to Nyquist	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 5)	-	-57.8	-	dBc
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz (Notes 3, 5)	-	-53.3	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 5)	-	-57.9	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz (Notes 3, 5)	-	-51	-	dBc
Intermodulation Distortion (IMD) to Nyquist	f_{CLK} = 125 MSPS, f_{OUT1} = 800kHz, f_{OUT2} = 900kHz (Notes 3, 5)	-	57.3	-	dB
	f_{CLK} = 100 MSPS, f_{OUT1} = 800kHz, f_{OUT2} = 900kHz (Notes 3, 5)	-	57.2	-	dB

Electrical Specifications AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, CTRL AMP IN = REF OUT, T_A = 25°C for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	HI5721BI T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
REFERENCE/CONTROL AMPLIFIER					
Internal Reference Voltage, REF OUT	(Note 4)	-1.15	-1.25	-1.35	V
Internal Reference Voltage Drift	(Note 3)	-	100	-	µV/°C
Internal Reference Output Current Sink/Source Capability	(Note 3)	-50	-	+500	µA
Amplifier Input Impedance	(Note 3)	-	10	-	MΩ
Amplifier Large Signal Bandwidth	4.0V_{P-P} Sine Wave Input, to Slew Rate Limited (Note 3)	-	1	-	MHz
Amplifier Small Signal Bandwidth	1.0V_{P-P} Sine Wave Input, to -3dB Loss (Note 3)	-	10	-	MHz
Reference Input Impedance	(Note 3)	-	4.6	-	kΩ
Reference Input Multiplying Bandwidth	R_L = 50Ω, 100mV Sine Wave, to -3dB Loss at I_{OUT} (Note 3)	-	75	-	MHz
DIGITAL INPUTS (D9-D0, CLK, INVERT)					
Input Logic High Voltage, V_{IH}	(Note 4)	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 4)	-	-	0.8	V
Input Logic Current, I_{IH}	(Note 4)	-	-	400	µA
Input Logic Current, I_{IL}	(Note 4)	-	-	700	µA
Digital Input Capacitance, C_{IN}	(Note 3)	-	3.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 3 (Note 3)	2.0	-	-	ns
Data Hold Time, t_{HLD}	See Figure 3 (Note 3)	0.5	-	-	ns
Propagation Delay Time, t_{PD}	See Figure 3 (Note 3)	-	4.5	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 3 (Note 3)	1.0	0.85	-	ns
POWER SUPPLY CHARACTERISITICS					
IAV_{EE}	(Note 4)	-	100	110	mA
IDV_{EE}	(Note 4)	-	-	15	mA
V_{CC}	(Note 4)	-	14	25	mA
Power Dissipation	(Note 4)	-	700	775	mW
Power Supply Rejection Ratio	V_{CC} ±5%, V_{EE} ±5%	-	50	-	µA/V

NOTES:

2. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 640µA). Ideally the ratio should be 32.
3. Parameter guaranteed by design or characterization and not production tested.
4. All devices are 100% tested at 25°C. 100% productions tested at temperature extremes for military temperature devices, sample tested for industrial temperature devices.
5. Spectral measurements made without external filtering.

Timing Diagrams

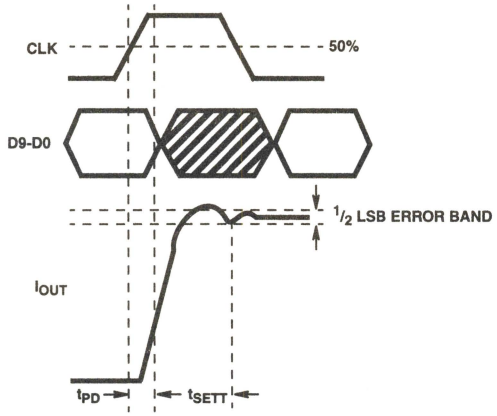


FIGURE 1. FULL SCALE SETTLING TIME DIAGRAM

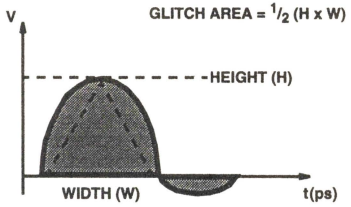


FIGURE 2. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

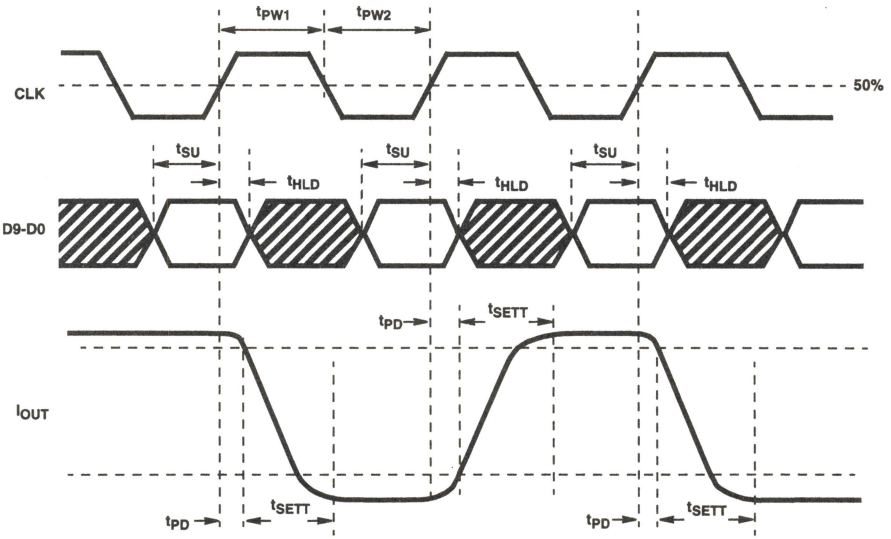


FIGURE 3. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Typical Performance Curves

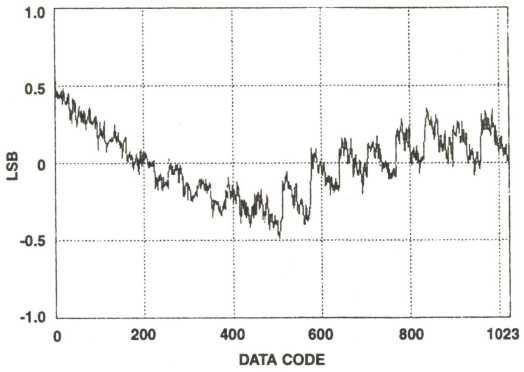


FIGURE 4. INTEGRAL NON-LINERARITY "BEST FIT" STRAIGHT LINE

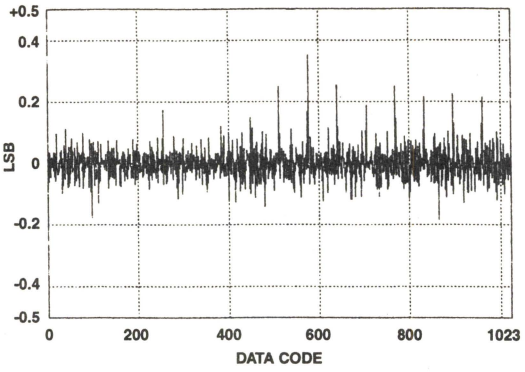


FIGURE 5. DIFFERENTIAL NON-LINEARITY

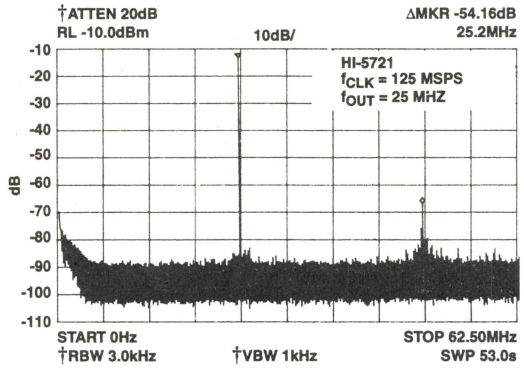


FIGURE 6. SPURIOUS FREE DYNAMIC RANGE TO NYQUIST 25MHz FUNDAMENTAL

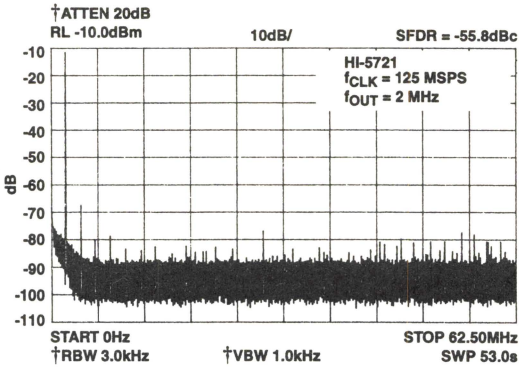


FIGURE 7. SPURIOUS FREE DYNAMIC RANGE TO NYQUIST 2MHz FUNDAMENTAL

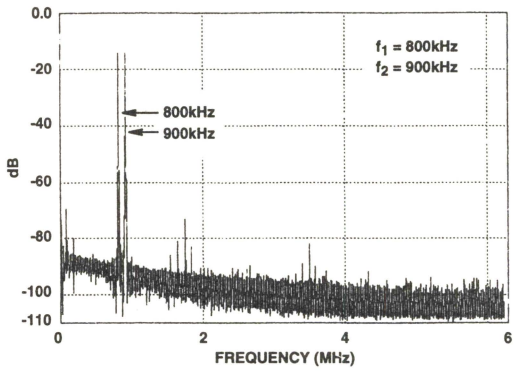


FIGURE 8. INTERMODULATION DISTORTION

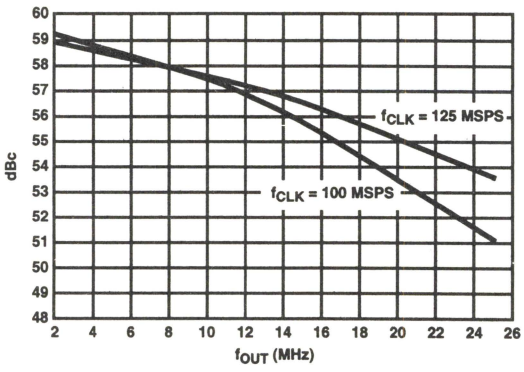


FIGURE 9. SPURIOUS FREE DYNAMIC RANGE (TO NYQUIST) vs OUTPUT FREQUENCY

Typical Performance Curves (Continued)

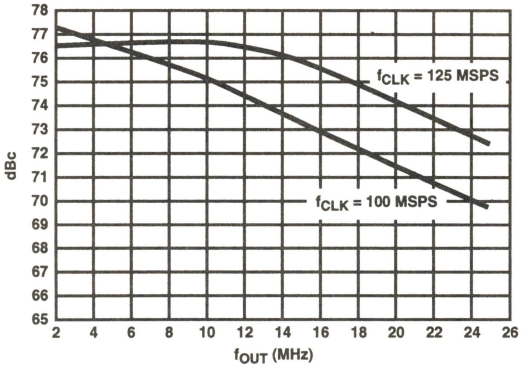


FIGURE 10. SPURIOUS FREE DYNAMIC RANGE (±1MHz WINDOW) vs FREQUENCY

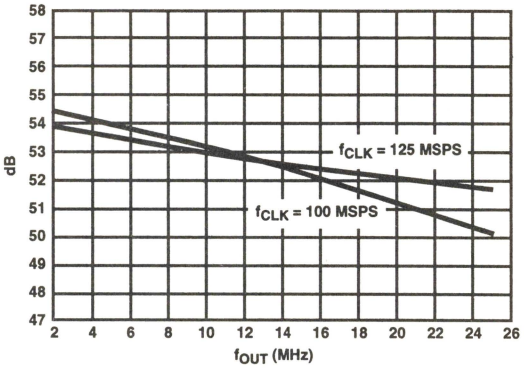


FIGURE 11. SIGNAL TO NOISE RATIO vs OUTPUT FREQUENCY

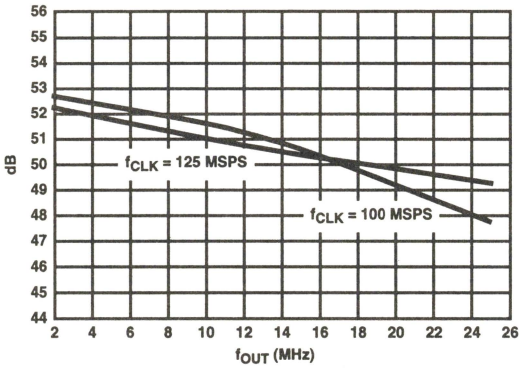


FIGURE 12. SIGNAL TO NOISE + DISTORTION vs OUTPUT FREQUENCY

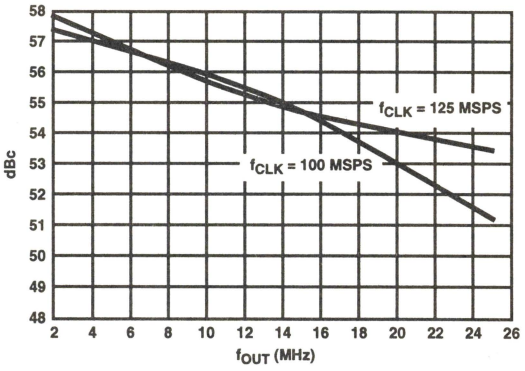


FIGURE 13. TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

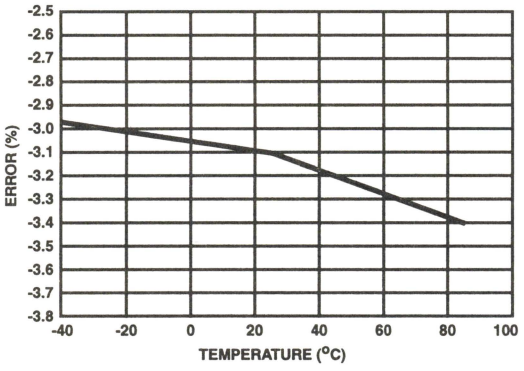


FIGURE 14. GAIN ERROR vs TEMPERATURE

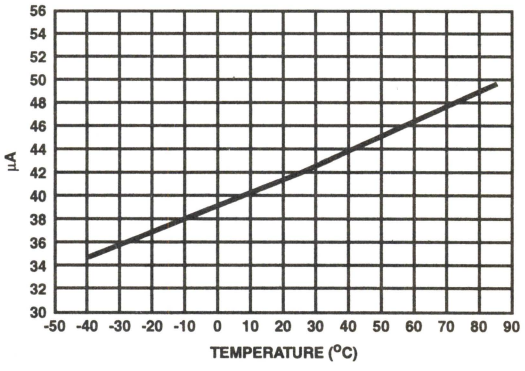


FIGURE 15. OFFSET ERROR vs TEMPERATURE

Typical Performance Curves (Continued)

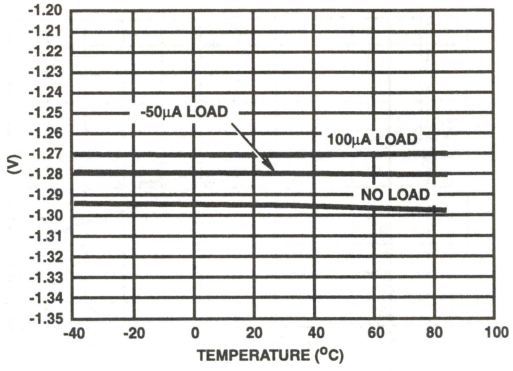
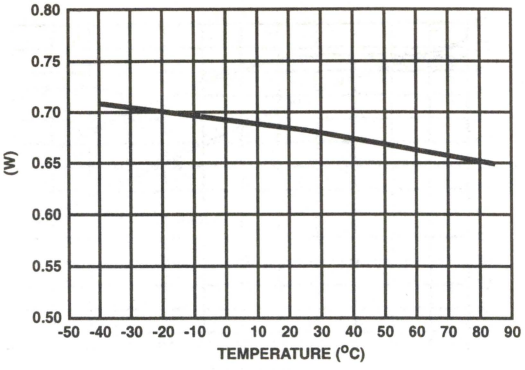


FIGURE 16. REFERENCE VOLTAGE vs TEMPERATURE



NOTE: Clock Frequency does not alter power dissipation.

FIGURE 17. POWER DISSIPATION vs TEMPERATURE

Pin Descriptions

PIN NO.	PIN NAME	PIN DESCRIPTION
1-10	D0 (LSB) through D9 (MSB)	Digital Data Bit 0, the Least Significant Bit through Digital Data Bit 9, the Most Significant Bit.
11	CLK	Data Clock pin 100kHz to 125 MSPS.
12	NC	No Connect.
13	INVERT	Data Invert control for bits D0 (LSB) through D8. D9 (MSB) is not affected.
14	V_{CC}	Digital Logic Supply +5V.
15, 28	DGND	Digital Ground.
16, 27	DV_{EE}	-5.2V Logic Supply.
17	R_{SET}	External resistor to set the full scale output current. I_{FS} = 32 x (CTRL AMP IN/R_{SET}). Typically 1960Ω.
18	AGND	Analog Ground supply current return pin.
19	ARTN	Analog Signal Return for the R/2R ladder.
20	I_{OUT}	Current Output pin.
21	$\overline{I_{OUT}}$	Complementary Current Output pin.
22	AV_{EE}	-5.2V Analog Supply.
23	REF IN	Reference Input pin. Typically connected to CTRL AMP OUT and a 0.1µF capacitor should be connected to AV_{EE} to bypass the reference voltage. Provides a reference for the current switching network.
24	CTRL AMP OUT	Control Amplifier Output. Used to convert the internal reference or an external signal to the precision reference current.
25	REF OUT	Internal Reference Output. Output of the internal -1.25V (typical) bandgap voltage reference.
26	CTRL AMP IN	Control Amplifier Input. High impedance, inverting input of the reference control/buffer amplifier.

Detailed Description

The HI5721 is a 10-bit, current out D/A converter. The DAC can convert at 125 MSPS and runs on +5V and -5.2V supplies. The architecture is an R/2R and segmented switching current cell arrangement to reduce glitch and maintain 10-bit linearity without laser trimming. The HI5721 achieves its low power and high speed performance from an advanced BiCMOS process. The HI5721 consumes 700mW (typical) and has an improved hold time of only 0.5ns (typical). The HI5721 is an excellent converter to be used for communications applications and high performance video systems.

Digital Inputs

The HI5721 is a TTL/CMOS compatible D/A. The inputs can be inverted using the INVERT pin. When INVERT is LOW ('0') the input quadrature logic simply passes the data through unchanged.

When INVERT is HIGH ('1') bits D0 (LSB) through D8 are inverted. D9 is not inverted and can be considered a sign bit when enabling this quadrature compatible mode. The INVERT function can simplify the requirements for large sine wave lookup tables in a Numerically Controlled Oscillator. The NCO used in a DDS application would only have to store or generate 90 degrees of information and then use the INVERT control to control the sign of the output waveform.

Data Buffer/Level Shifters

Data inputs D0 (LSB) through D9 (MSB) are internally translated from TTL to ECL. The internal latch and switching current source controls are implemented in ECL technology to maintain high switching speeds and low noise characteristics.

Decoder/Driver

The architecture employs a split R/2R and Segmented Current source arrangement. Bits D0 (LSB) through D5 directly drive a typical R/2R network to create the binary weighted current sources. Bits D6 through D9 (MSB) pass through a "thermometer" encoder that converters the incoming data into 15 individual segmented current source enables. The split architecture helps to improve glitch while maintaining 10-bit linearity without laser trimming. The worst case glitch is more constant across the entire output transfer function.

Clocks and Termination

The internal 10-bit register is updated on the rising edge of the clock. Since the HI5721 clock rate can run to 125 MSPS, to minimize reflections and clock noise into the part proper termination should be used. In PCB layout clock runs should be kept short and have a minimum of loads. To guarantee consistent results from board to board, controlled impedance PCBs should be used with a characteristic line impedance Z_O of 50Ω.

To terminate the clock line a shunt terminator to ground is the most effective type at a 125 MSPS clock rate. A typical value for termination can be determined by the equation:

$R_T = Z_O$,

for the termination resistor. For a controlled impedance board with a Z_O of 50Ω, the R_T = 50Ω. Shunt termination is best used at the receiving end of the transmission line or as close to the HI5721 CLK pin as possible.

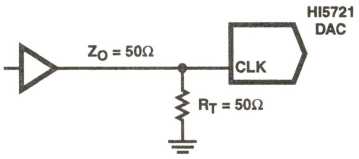


FIGURE 18. AC TERMINATION OF THE HI5721 CLOCK LINE

Rise and Fall times and propagation delay of the line will be affected by the Shunt Terminator. The terminator can be connected to DGND.

Noise Reduction

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1µF and 0.01µF ceramic capacitors placed as close to the body of the HI5721 as possible on the analog (AV_{EE}) and digital (DV_{EE}) supplies. The analog and digital ground returns should be connected together back at the device to ensure proper operation on power up. The V_{CC} power pin should be decoupled with a 0.1µF capacitor.

Reference

The internal reference in the HI5721 is a -1.25V (typical) bandgap voltage reference with a 100µV/°C temperature drift (typical). The internal reference should be buffered by the Control Amplifier to provide adequate drive for the segmented current cells and the R/2R resistor ladder. Reference Out (REF OUT) should be connected to the Control Amplifier Input (CTRL AMP IN). The Control Amplifier Output (CTRL AMP OUT) should be used to drive the Reference Input (REF IN) and a 0.1µF capacitor to analog V- (AV_{EE}). This improves settling time by decoupling switching noise from the analog output of the HI5721.

The Full Scale Output Current is controlled by the CTRL AMP IN pin and the set resistor (R_{SET}). The ratio is:

I_{OUT} (Full Scale) = ($V_{CTRL\ AMP\ IN}/R_{SET}$) x 32.

Multiplying Capability

The HI5721 can operate in two different multiplying configurations. First, using the CTRL AMP IN input pin, a -0.6V to -1.2V signal can be applied with a bandwidth up to 1MHz. To increase the multiplying bandwidth, the 0.1µF capacitor connected from REF IN to AV_{EE} can be reduced.

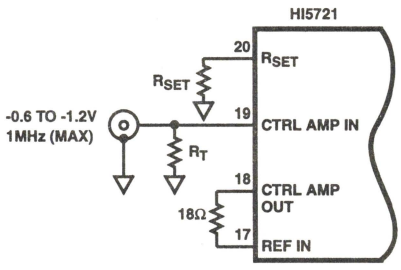


FIGURE 19. LOW FREQUENCY MULTIPLYING CIRCUIT

If higher multiplying frequencies are desired, the reference input can be directly driven. The analog signal range is -3.3V to -4.25V. The multiplying signal must be capacitively coupled into REF IN onto a DC bias between -3.3V to -4.25V (-3.8V typically).

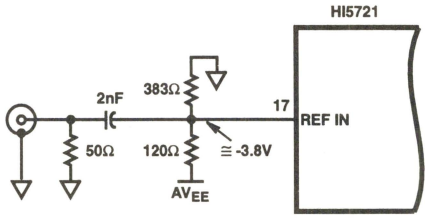


FIGURE 20. WIDEBAND MULTIPLYING CIRCUIT

Outputs

The outputs I_{OUT} and $I_{\overline{OUT}}$ are complementary current outputs. Current is steered to either I_{OUT} or $I_{\overline{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full scale current minus one LSB. The current output can be converted to a voltage by using a load resistor. Both current outputs should have the same load resistor (64Ω typically). By using a 64Ω load on the output, a 50Ω effective output resistance (R_{OUT}) is achieved due to the 227Ω (±15%) parallel resistance seen looking back into the output. This is the nominal value of the R2R ladder of the DAC. The 50Ω output is needed for matching the output with a 50Ω line. The load resistor should be chosen so that the effective output resistance (R_{OUT}) matches the line resistance. The output voltage is:

$V_{OUT} = I_{OUT} \times R_{OUT}$.

I_{OUT} is defined in the reference section. The compliance range of the output is from -1.5V to +3.0V, with a $1V_{P-P}$ voltage swing allowed within this range.

Glitch

TABLE 1. INPUT CODING vs CURRENT OUTPUT

INPUT CODE (D9-D0)	I_{OUT} (mA)	$I_{\overline{OUT}}$ (mA)
11 1111 1111	-20.48	0
10 0000 0000	-10.24	-10.24
00 0000 0000	0	-20.48

The output glitch of the HI5721 is measured by summing the area under the switching transients after an update of the DAC. Glitch is caused by the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). Unequal delay paths through the device can also cause one current source to change before another. To minimize this the Harris HI5721 employes an internal register, just prior to the current sources, that is updated on the clock edge. Lastly the worst case glitch usually happens at the major transition i.e., 01 1111 1111 to 10 0000 0000. But in the HI5721 the glitch is moved to the 00 0001 1111 to 11 1110 0000 transition. This is achieved by the split R/2R segmented current source architecture. This decreases the amount of current switching at any one time and makes the glitch practically constant over the entire output range. By making the glitch a constant size over the entire output range this effectively integrates this error out of the end application.

In measuring the output glitch of the HI5721 the output is terminated into a 64Ω load. The glitch is measured at the major carrys throughout the DAC's output range.

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 21 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt • seconds (pV • s).

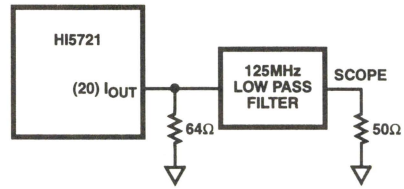


FIGURE 21. GLITCH TEST CIRCUIT

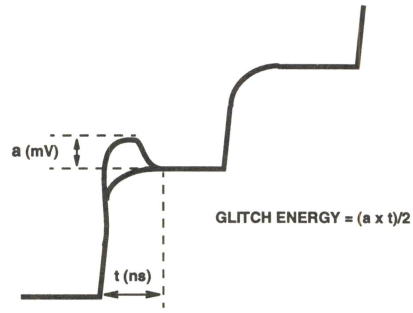


FIGURE 22. GLITCH ENERGY

Applications

Voltage Conversion of the Output

To convert the output current of the D/A converter to a voltage, an amplifier should be used as shown in Figure 23 below. The DAC needs a 50Ω termination resistor on the I_{OUT} pin to ensure proper settling. The HFA1110 has an internal feedback resistor to compensate for high frequency operation.

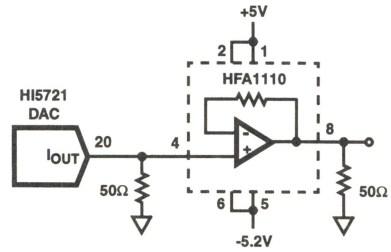


FIGURE 23. HIGH SPEED CURRENT TO VOLTAGE CONVERSION

Bipolar Applications

To convert the output to a bipolar ±2.0V output swing the following applications circuit is recommended. The Reference can only provide 100µA of drive, so it must be buffered to create the bipolar offset current needed to generate -2.0V output with all bits 'off'. The output current must be converted to a voltage and then gained up and offset to produce the proper swing. Care must be taken to compensate for the output voltage swing and error.

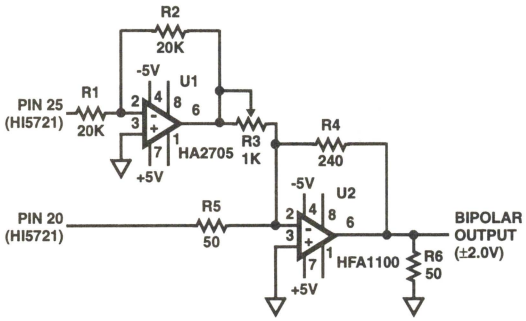


FIGURE 24. BIPOLAR OUTPUT CONFIGURATION

Interfacing to the HSP45106 NCO-16

The HSP45106 is a 16-bit output, Numerically-Controlled Oscillator (NCO). The HSP45106 can be used to generate various modulation schemes for Direct Digital Synthesis (DDS) applications. Figure 25 shows how to interface an HI5721 to the HSP45106.

Interfacing to the HSP45102 NCO-12

The HSP45102 is a 12-bit output Numerically Controlled Oscillator (NCO). The HSP45102 can be used to generate various modulation schemes for Direct Digital Synthesis (DDS) applications. Figure 26 shows how to interface an HI5721 to the HSP45102.

This high level block diagram is that of a basic PSK modulator. In this example the encoder generates the PSK waveform by driving the Phase Modulation Inputs (P1, P0) of the HSP45102. The P1-0 inputs impart a phase shift to the carrier wave as defined in Table 2.

TABLE 2. PHASE MODULATION INPUT CODING

P1	P0	PHASE SHIFT (DEGREES)
0	0	0
0	1	90
1	0	270
1	1	180

The 10 MSBs of the HSP45102 drive the 10-bit HI5721 DAC which converts the NCO output into an analog waveform. The output filter connected to the DAC can be tailored to remove unwanted spurs for the desired carrier frequency. The controller is used to load the desired center frequency and control the HSP45102. The HI5721 coupled with the HSP45102 make an inexpensive PSK modulator with Spurious Free operation down to -76dBc.

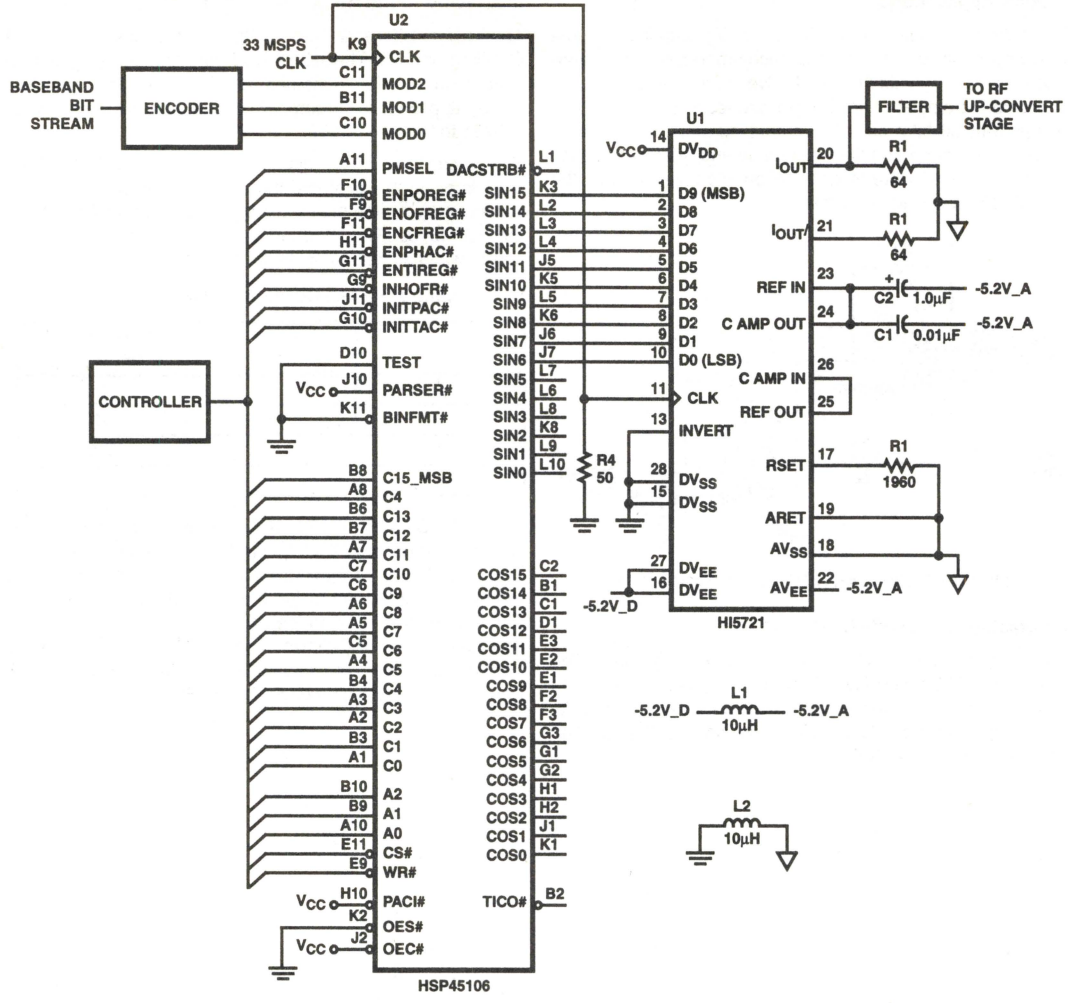


FIGURE 25. PSK MODULATOR USING THE HI5721 AND THE HSP45106 12-BIT NCO

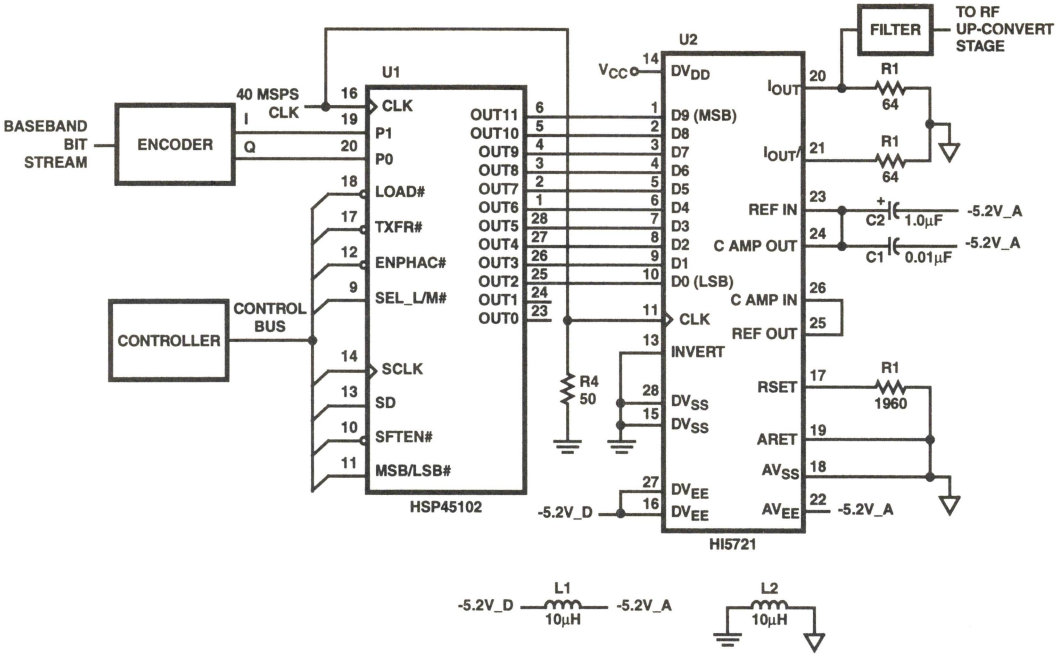


FIGURE 26. PSK MODULATOR USING THE HI5721 AND THE HSP45102 12-BIT NCO

Definition of Specifications

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Feedthru is the measure of the undesirable switching noise coupled to the output.

Output Voltage Full Scale Settling Time, is the time required from the 50% point on the clock input for a full scale step to settle within an $^1/_2$ LSB error band.

Output Voltage Small Scale Settling Time, is the time required from the 50% point on the clock input for a 100mV step to settle within an $^1/_2$ LSB error band. This is used by applications reconstructing highly correlated signals such as sine waves with more than 5 points per cycle.

Glitch Area, GE, is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a Volt-Time specification.

Differential Gain, ΔA_V, is the gain error from an ideal sine wave with a normalized amplitude.

Differential Phase, $\Delta\Phi$, is the phase error from and ideal sine wave.

Signal to Noise Ratio, SNR, is the ratio of a fundamental to the noise floor of the analog output. The first 5 harmonics are ignored, and an output filter of $^1/_2$ the clock frequency is used to eliminate alias products.

Total Harmonic Distortion, THD, is the ratio of the DAC output fundamental to the RMS sum of the harmonics. The first 5 harmonics are included, and an output filter of $^1/_2$ the clock frequency is used to eliminate alias products.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at $^1/_2$ the clock frequency to eliminate noise from clocking alias terms.

Intermodulation Distortion, IMD is the measure of the sum and difference products produced when a two tone input is driven into the D/A. The distortion products created will arise at sum and difference frequencies of the two tones. IMD is

$$IMD = \frac{20\log\ (\text{RMS of sum and difference distortion products})}{(\text{RMS amplitude of the fundamental})}$$

HARRIS SEMICONDUCTOR

HI5728

PRELIMINARY

August 1997

10-Bit, 125 MSPS, Dual High Speed D/A Converter

Features

- Throughput Rate ..... 125 MSPS
- Low Power (Typ).....300mW
- Integral Linearity Error ..... ±1 LSB
- Low Glitch Energy
- TTL/CMOS Compatible Inputs
- Excellent Spurious Free Dynamic Range

Applications

- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Test Equipment
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

Description

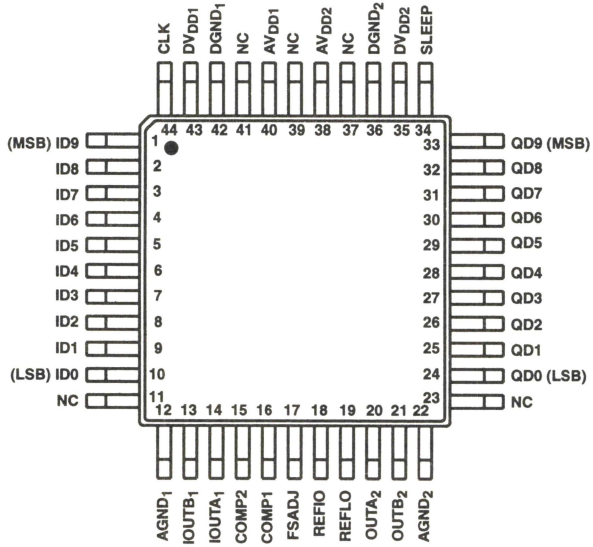
The HI5728 is a 10 bit, dual 125 MSPS D/A converter which is implemented in 0.6µm CMOS process. Operating from a single +5V supply, the converter provides 20.48mA of full scale output current and includes an input data register. Low glitch energy and excellent frequency domain performance are achieved using a segmented architecture.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5728IN	-40 to 85	44 Ld MQFP	Q44.10x10

Pinout

HI5728
(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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HARRIS SEMICONDUCTOR

HI5731

August 1997

12-Bit, 100 MSPS, High Speed D/A Converter

Features

- Throughput Rate ..... 100 MSPS
- Low Power 650mW
- Integral Linearity Error ..... 0.75 LSB
- Low Glitch Energy 3.0pV-s
- TTL/CMOS Compatible Inputs
- Improved Hold Time 0.25ns
- Excellent Spurious Free Dynamic Range

Applications

- Cellular Base Stations
- GSM Base Stations
- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Test Equipment
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

Description

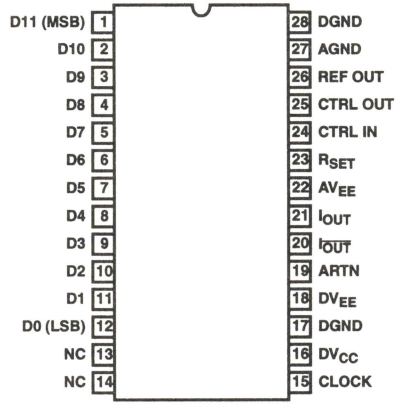
The HI5731 is a 12-bit, 100 MSPS, D/A converter which is implemented in the Harris BiCMOS 10V (HBC-10) process. Operating from +5V and -5.2V, the converter provides -20.48mA of full scale output current and includes an input data register and bandgap voltage reference. Low glitch energy and excellent frequency domain performance are achieved using a segmented architecture. The digital inputs are TTL/CMOS compatible and translated internally to ECL. All internal logic is implemented in ECL to achieve high switching speed with low noise. The addition of laser trimming assures 12-bit linearity is maintained along the entire transfer curve.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5731BIP	-40 to 85	28 Ld PDIP	E28.6
HI5731BIB	-40 to 85	28 Ld SOIC	M28.3
HI5731-EVP	25	Evaluation Board (PDIP)	
HI5731-EVS	25	Evaluation Board (SOIC)	

Pinout

HI5731
(PDIP, SOIC)
TOP VIEW



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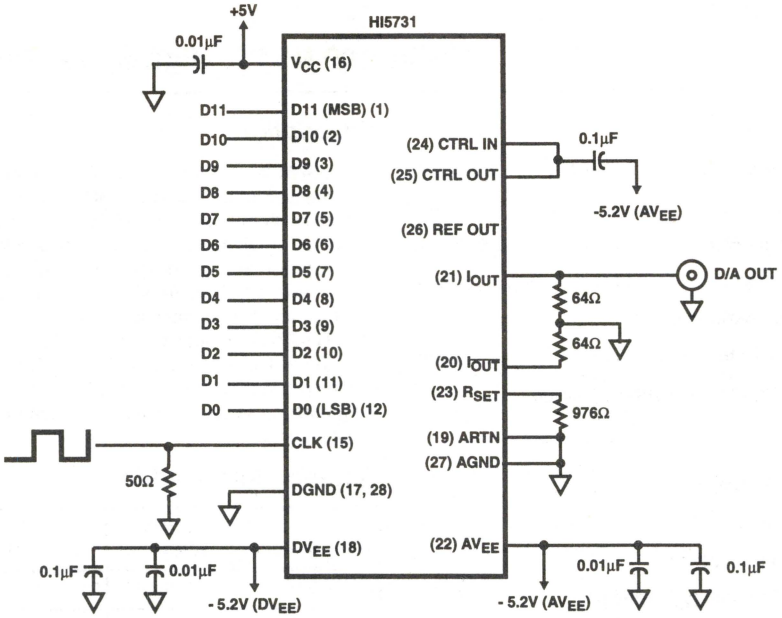
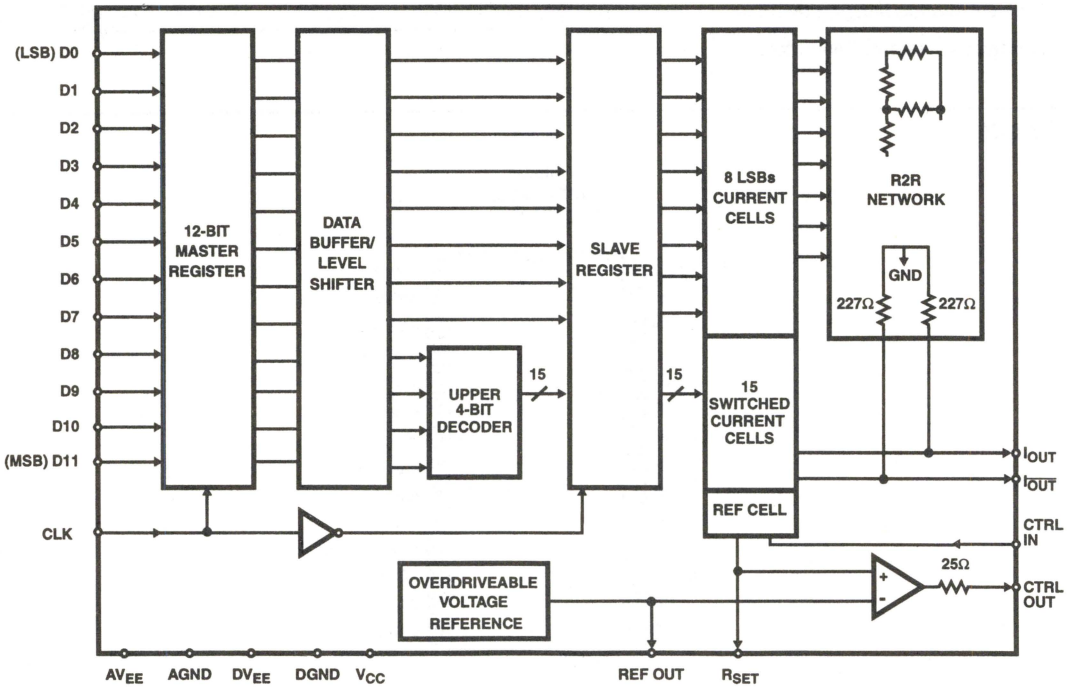
File Number 4070.3

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings

Digital Supply Voltage V_{CC} to DGND ..... +5.5V
Negative Digital Supply Voltage DV_{EE} to DGND ..... -5.5V
Negative Analog Supply Voltage AV_{EE} to AGND, ARTN ..... -5.5V
Digital Input Voltages (D11-D0, CLK) to DGND ..... DV_{CC} to -0.5V
Internal Reference Output Current ..... ±2.5mA
Voltage from CTRL IN to AV_{EE} ..... 2.5V to 0V
Control Amplifier Output Current ..... ±2.5mA
Reference Input Voltage Range ..... -3.7V to AV_{EE}
Analog Output Current (I_{OUT}) 30mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	55
SOIC Package	70

Maximum Junction Temperature
HI5731BIx ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range ..... -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = Internal
T_A = 25°C for All Typical Values

PARAMETER	TEST CONDITIONS	HI5731BI T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		12	-	-	Bits
Integral Linearity Error, INL	(Note 4) ("Best Fit" Straight Line)	-	0.75	1.5	LSB
Differential Linearity Error, DNL	(Note 4)	-	0.5	1.0	LSB
Offset Error, I_{OS}	(Note 4)	-	20	75	µA
Full Scale Gain Error, FSE	(Notes 2, 4)	-	1	10	%
Offset Drift Coefficient	(Note 3)	-	-	0.05	µA/°C
Full Scale Output Current, I_{FS}		-	20.48	-	mA
Output Voltage Compliance Range	(Notes 3, 5)	-1.25	-	+3.0	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	(Note 3)	100	-	-	MSPS
Output Voltage Full Scale Step Settling Time, t_{SETT}, Full Scale	To ±0.5 LSB Error Band R_L = 50Ω (Note 3)	-	20	-	ns
Singlet Glitch Area, GE (Peak)	R_L = 50Ω (Note 3)	-	5	-	pV-s
Doublet Glitch Area, (Net)		-	3	-	pV-s
Output Slew Rate	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	1,000	-	V/µs
Output Rise Time	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	675	-	ps
Output Fall Time	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	470	-	ps
Spurious Free Dynamic Range within a Window (Note 3)	f_{CLK} = 10 MSPS, f_{OUT} = 1.23MHz, 2MHz Span	-	85	-	dBc
	f_{CLK} = 20 MSPS, f_{OUT} = 5.055MHz, 2MHz Span	-	77	-	dBc
	f_{CLK} = 40 MSPS, f_{OUT} = 16MHz, 10MHz Span	-	75	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 10.1MHz, 2MHz Span	-	80	-	dBc
	f_{CLK} = 80 MSPS, f_{OUT} = 5.1MHz, 2MHz Span	-	78	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 10.1MHz, 2MHz Span	-	79	-	dBc

Electrical Specifications AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = Internal T_A = 25°C for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	HI5731BI T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
Spurious Free Dynamic Range to Nyquist (Note 3)	f_{CLK} = 40 MSPS, f_{OUT} = 2.02MHz, 20MHz Span	-	70	-	dBc
	f_{CLK} = 80 MSPS, f_{OUT} = 2.02MHz, 40MHz Span	-	70	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, 50MHz Span	-	69	-	dBc
REFERENCE/CONTROL AMPLIFIER					
Internal Reference Voltage, V_{REF}	(Note 4)	-1.27	-1.23	-1.17	V
Internal Reference Voltage Drift	(Note 3)	-	175	-	µV/°C
Internal Reference Output Current Sink/Source Capability	(Note 3)	-125	-	+50	µA
Internal Reference Load Regulation	I_{REF} = 0 to I_{REF} = -125µA	-	50	-	µV
Input Impedance at REF OUT pin	(Note 3)	-	1.4	-	kΩ
Amplifier Large Signal Bandwidth ($0.6V_{P-P}$)	Sine Wave Input, to Slew Rate Limited (Note 3)	-	3	-	MHz
Amplifier Small Signal Bandwidth ($0.1V_{P-P}$)	Sine Wave Input, to -3dB Loss (Note 3)	-	10	-	MHz
Reference Input Impedance	(Note 3)	-	12	-	kΩ
Reference Input Multiplying Bandwidth (CTL IN)	R_L = 50Ω, 100mV Sine Wave, to -3dB Loss at I_{OUT} (Note 3)	-	200	-	MHz
DIGITAL INPUTS (D9-D0, CLK, INVERT)					
Input Logic High Voltage, V_{IH}	(Note 4)	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 4)	-	-	0.8	V
Input Logic Current, I_{IH}	(Note 4)	-	-	400	µA
Input Logic Current, I_{IL}	(Note 4)	-	-	700	µA
Digital Input Capacitance, C_{IN}	(Note 3)	-	3.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 1 (Note 3)	3.0	2.0	-	ns
Data Hold Time, t_{HLD}	See Figure 1 (Note 3)	0.5	0.25	-	ns
Propagation Delay Time, t_{PD}	See Figure 1 (Note 3)	-	4.5	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 1 (Note 3)	3.0	-	-	ns
POWER SUPPLY CHARACTERISITICS					
I_{EEA}	(Note 4)	-	42	50	mA
I_{EED}	(Note 4)	-	70	85	mA
I_{CCD}	(Note 4)	-	13	20	mA
Power Dissipation	(Note 4)	-	650	-	mW
Power Supply Rejection Ratio	V_{CC} ±5%, V_{EE} ±5%	-	5	-	µA/V

NOTES:

2. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 1.28mA). Ideally the ratio should be 16.
3. Parameter guaranteed by design or characterization and not production tested.
4. All devices are 100% tested at 25°C. 100% production tested at temperature extremes for military temperature devices, sample tested for industrial temperature devices.
5. Dynamic Range must be limited to a 1V swing within the compliance range.

Timing Diagrams

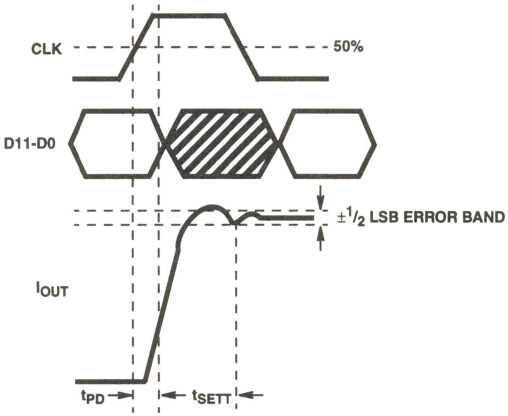


FIGURE 1. FULL SCALE SETTLING TIME DIAGRAM

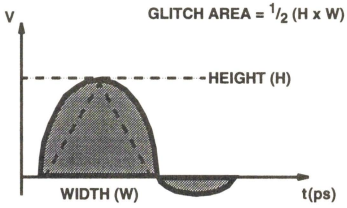


FIGURE 2. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

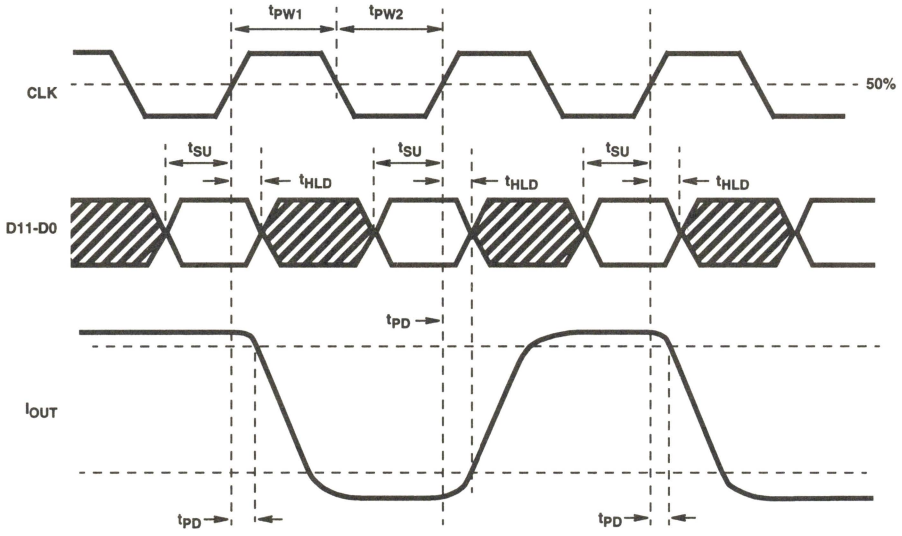


FIGURE 3. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Typical Performance Curves

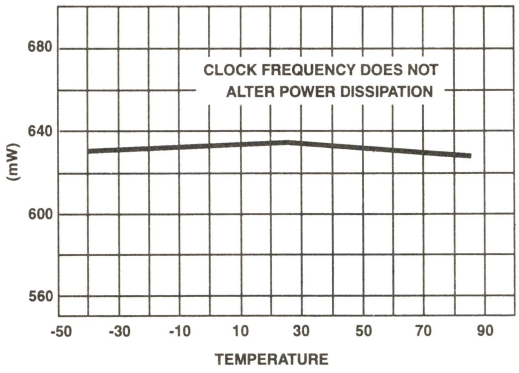


FIGURE 4. TYPICAL POWER DISSIPATION OVER TEMPERATURE

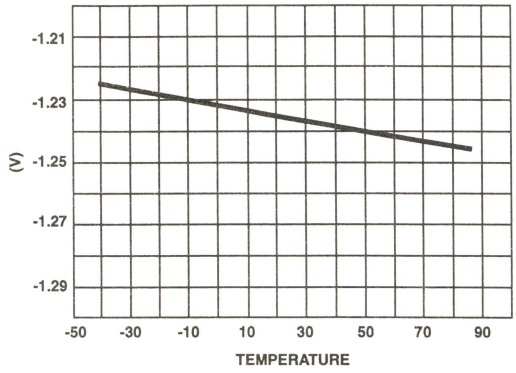


FIGURE 5. TYPICAL REFERENCE VOLTAGE OVER TEMPERATURE

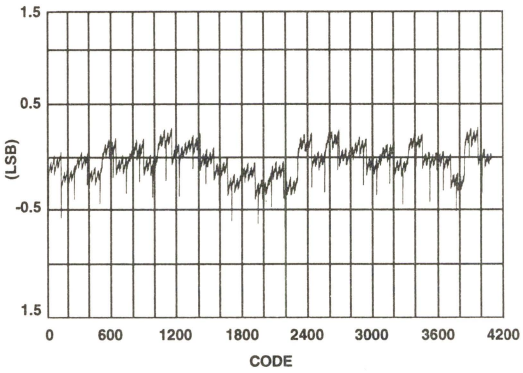


FIGURE 6. TYPICAL INL

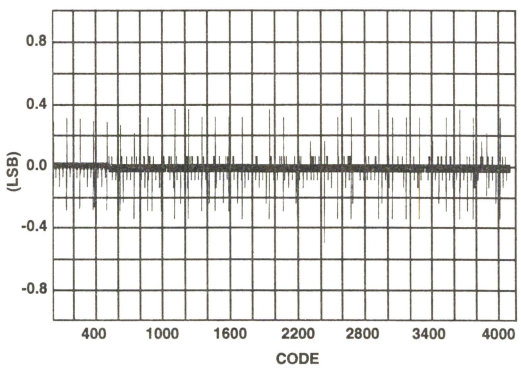


FIGURE 7. TYPICAL DNL

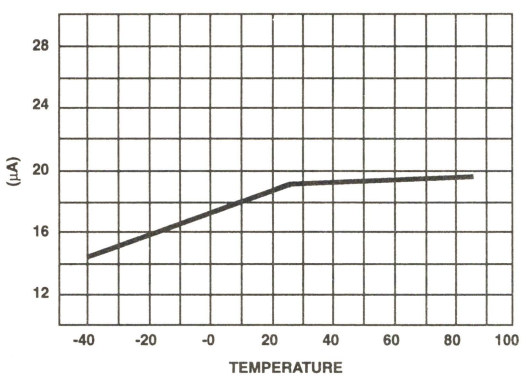


FIGURE 8. OFFSET CURRENT OVER TEMPERATURE

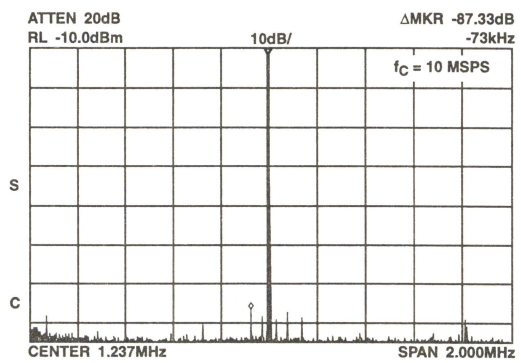


FIGURE 9. SPURIOUS FREE DYNAMIC RANGE = 87.3dBc

Typical Performance Curves (Continued)

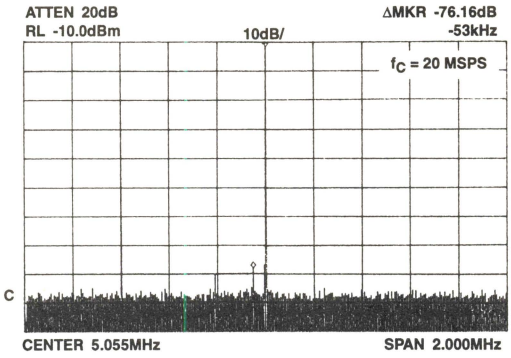


FIGURE 10. SPURIOUS FREE DYNAMIC RANGE = 76.16dBc

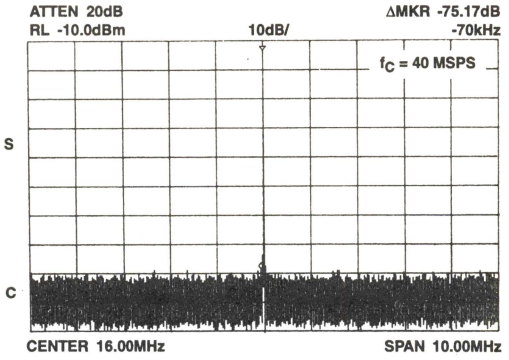


FIGURE 11. SPURIOUS FREE DYNAMIC RANGE = 75.17dBc

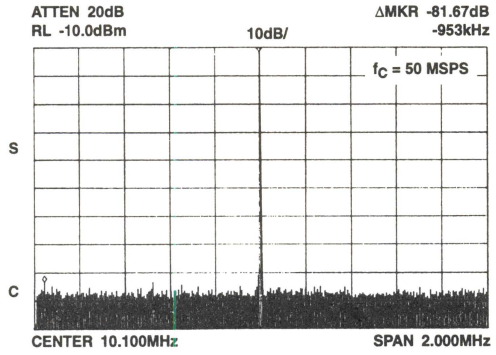


FIGURE 12. SPURIOUS FREE DYNAMIC RANGE = -81.67dBc

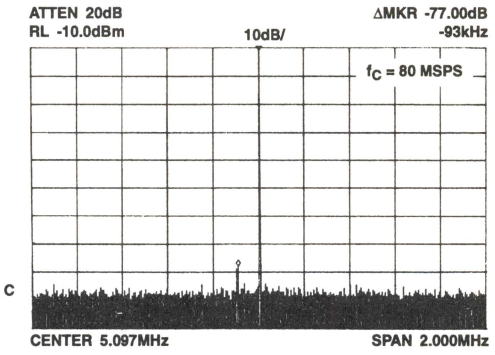


FIGURE 13. SPURIOUS FREE DYNAMIC RANGE = 77dBc

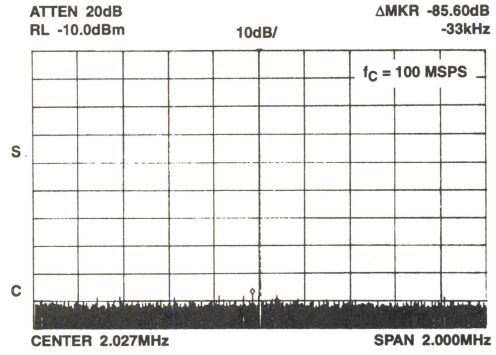


FIGURE 14. SPURIOUS FREE DYNAMIC RANGE = -85.60dBc

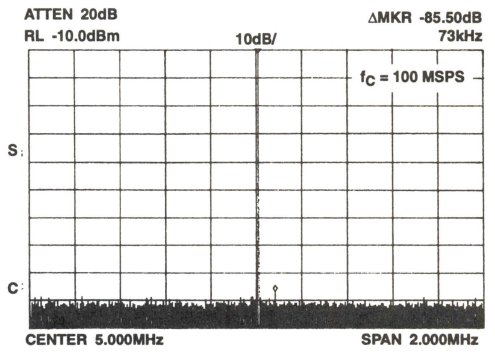


FIGURE 15. SPURIOUS FREE DYNAMIC RANGE = 85.5dBc

Typical Performance Curves (Continued)

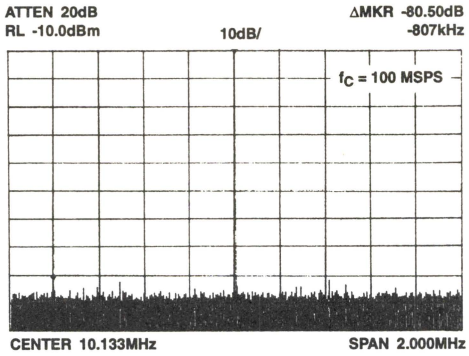


FIGURE 16. SPURIOUS FREE DYNAMIC RANGE = 80.5dBc

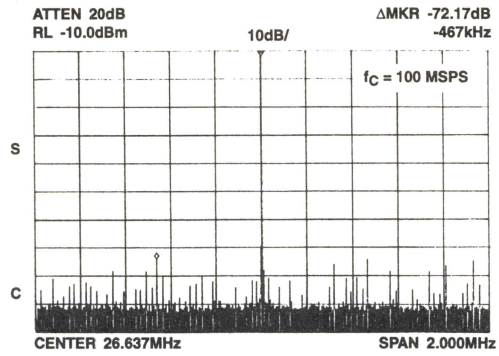


FIGURE 17. SPURIOUS FREE DYNAMIC RANGE = 72.17dBc

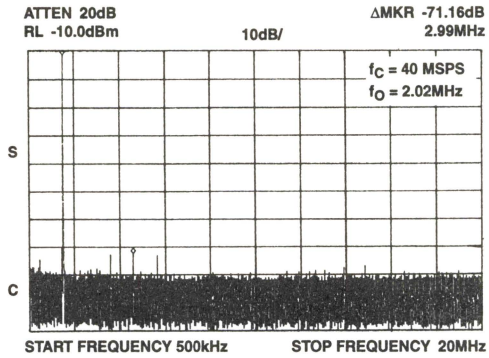


FIGURE 18. SPURIOUS FREE DYNAMIC RANGE = 71.16dBc

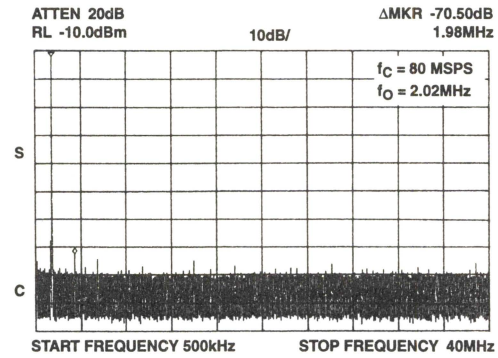


FIGURE 19. SPURIOUS FREE DYNAMIC RANGE = 70.5dBc

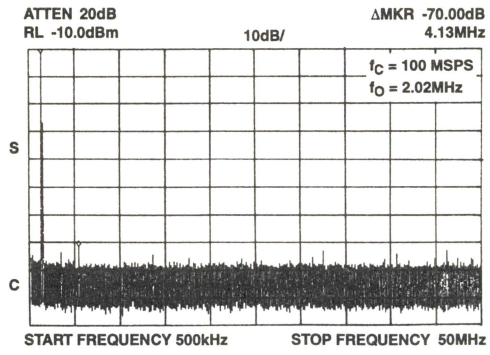


FIGURE 20. SPURIOUS FREE DYNAMIC RANGE = 70dBc

Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1-12	D11 (MSB) thru D0 (LSB)	Digital Data Bit 11, the Most Significant Bit thru Digital Data Bit 0, the Least Significant Bit
15	CLK	Data Clock Pin DC to 100 MSPS
13, 14	NC	No Connect
16	V_{CC}	Digital Logic Supply +5V
17, 28	DGND	Digital Ground
18	DV_{EE}	-5.2V Logic supply
23	R_{SET}	External resistor to set the full scale output current. $I_{FS} = 16 \times (V_{REF\ OUT} / R_{SET})$. Typically 976Ω.
27	AGND	Analog Ground supply current return pin.
19	ARTN	Analog Signal Return for the R/2R ladder.
21	I_{OUT}	Current Output Pin
20	$I_{\overline{OUT}}$	Complementary Current Output Pin
22	AV_{EE}	-5.2V Analog Supply
24	CTRL IN	Input to the current source base rail. Typically connected to CTRL OUT and a 0.1µF capacitor to AV_{EE}. Allows external control of the current sources.
25	CTRL OUT	Control Amplifier Out. Provides precision control of the current sources when connected to CTRL IN such that $I_{FS} = 16 \times (V_{REF\ OUT} / R_{SET})$.
26	REF OUT	-1.23V (Typ) bandgap reference voltage output. Can sink up to 125µA or be overdriven by an external reference capable of delivering up to 2mA.

Detailed Description

The HI5731 is a 12-bit, current out D/A converter. The DAC can convert at 100 MSPS and runs on +5V and -5.2V supplies. The architecture is an R/2R and segmented switching current cell arrangement to reduce glitch. Laser trimming is employed to tune linearity to true 12-bit levels. The HI5731 achieves its low power and high speed performance from an advanced BiCMOS process. The HI5731 consumes 650mW (typical) and has an improved hold time of only 0.25ns (typical). The HI5731 is an excellent converter for use in communications applications and high performance instrumentation systems.

Digital Inputs

The HI5731 is a TTL/CMOS compatible D/A. Data is latched by a Master register. Once latched, data inputs D0 (LSB) thru D11 (MSB) are internally translated from TTL to ECL. The internal latch and switching current source controls are implemented in ECL technology to maintain high switching speeds and low noise characteristics.

Decoder/Driver

The architecture employs a split R/2R ladder and Segmented Current source arrangement. Bits D0 (LSB) thru D7 directly drive a typical R/2R network to create the binary weighted current sources. Bits D8 thru D11 (MSB) pass thru a "thermometer" decoder that converts the incoming data into 15 individual segmented current source enables. This split architecture helps to improve glitch, thus resulting in a more constant glitch characteristic across the entire output transfer function.

Clocks and Termination

The internal 12-bit register is updated on the rising edge of the clock. Since the HI5731 clock rate can run to 100 MSPS, to minimize reflections and clock noise into the part proper termination should be used. In PCB layout clock runs should be kept short and have a minimum of loads. To guarantee consistent results from board to board controlled impedance PCBs should be used with a characteristic line impedance Z_O of 50Ω.

To terminate the clock line, a shunt terminator to ground is the most effective type at a 100 MSPS clock rate. A typical value for termination can be determined by the equation:

$R_T = Z_O$,

for the termination resistor. For a controlled impedance board with a Z_O of 50Ω, the R_T = 50Ω. Shunt termination is best used at the receiving end of the transmission line or as close to the HI5731 CLK pin as possible.

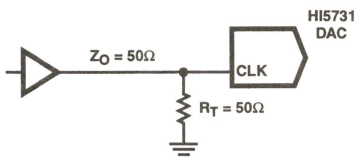


FIGURE 21. CLOCK LINE TERMINATION

Rise and Fall times and propagation delay of the line will be affected by the Shunt Terminator. The terminator should be connected to DGND.

Noise Reduction

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1µF and 0.01µF

ceramic capacitors placed as close to the body of the HI5731 as possible on the analog (AV_{EE}) and digital (DV_{EE}) supplies. The analog and digital ground returns should be connected together back at the device to ensure proper operation on power up. The V_{CC} power pin should also be decoupled with a 0.1µF capacitor.

Reference

The internal reference of the HI5731 is a -1.23V (typical) bandgap voltage reference with 175µV/°C of temperature drift (typical). The internal reference is connected to the Control Amplifier which in turn drives the segmented current cells. Reference Out (REF OUT) is internally connected to the Control Amplifier. The Control Amplifier Output (CTRL OUT) should be used to drive the Control Amplifier Input (CTRL IN) and a 0.1µF capacitor to analog V_{EE}. This improves settling time by providing an AC ground at the current source base node. The Full Scale Output Current is controlled by the REF OUT pin and the set resistor (R_{SET}). The ratio is:

I_{OUT} (Full Scale) = ($V_{REF\ OUT}/R_{SET}$) x 16,

The internal reference (REF OUT) can be overdriven with a more precise external reference to provide better performance over temperature. Figure 22 illustrates a typical external reference configuration.

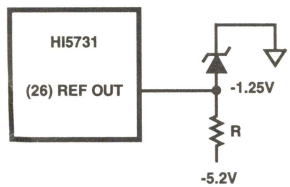


FIGURE 22. EXTERNAL REFERENCE CONFIGURATION

Multiplying Capability

The HI5731 can operate in two different multiplying configurations. For frequencies from DC to 100kHz, a signal of up to 0.6V_{P-P} can be applied directly to the REF OUT pin as shown in Figure 23.

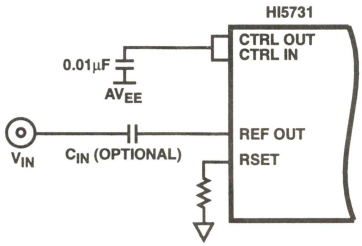


FIGURE 23. LOW FREQUENCY MULTIPLYING BANDWIDTH CIRCUIT

The signal must have a DC value such that the peak negative voltage equals -1.25V. Alternately, a capacitor can be placed in series with REF OUT if DC multiplying is not required. The lower input bandwidth can be calculated using the following formula:

$$C_{IN} = \frac{1}{(2\pi)(1400)(f_{IN})}.$$

For multiplying frequencies above 100kHz, the CTRL IN pin can be driven directly as seen in Figure 24.

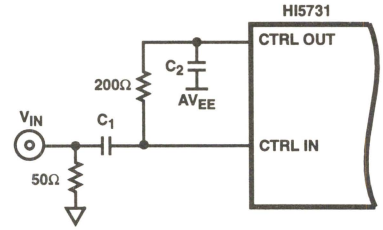


FIGURE 24. HIGH FREQUENCY MULTIPLYING BANDWIDTH CIRCUIT

The nominal input/output relationship is defined as:

$$\Delta I_{OUT} = \frac{\Delta V_{IN}}{80\Omega}.$$

In order to prevent the full scale output current from exceeding 20.48mA, the R_{SET} resistor must be adjusted according to the following equation:

$$R_{SET} = \frac{16V_{REF}}{I_{OUT(FULL\ SCALE)} - \left(\frac{V_{IN(PEAK)}}{80\Omega}\right)}.$$

The circuit in Figure 24 can be tuned to adjust the lower cutoff frequency by adjusting capacitor values. Table 1 below illustrates the relationship:

TABLE 1. CAPACITOR SELECTION

f_{IN}	C1	C2
100kHz	0.01µF	1µF
>1MHz	0.001µF	0.1µF

Also, the input signal must be limited to 1V_{P-P} to avoid distortion in the DAC output current caused by excessive modulation of the internal current sources.

Outputs

The outputs I_{OUT} and $I_{\overline{OUT}}$ are complementary current outputs. Current is steered to either I_{OUT} or $I_{\overline{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full scale current minus one LSB. The current output can be converted to a voltage by using a load resistor. Both current outputs should have the same load resistor (64Ω typically). By using a 64Ω load on the output, a 50Ω effective output resistance (R_{OUT}) is achieved due to the 227Ω (±15%) parallel resistance seen looking back into the output. This is the nominal value of the R2R ladder of the DAC. The 50Ω output is needed for matching the output with a 50Ω line. The load resistor should be chosen so that the effective output resistance (R_{OUT}) matches the line resistance. The output voltage is:

$V_{OUT} = I_{OUT} \times R_{OUT}$.

I_{OUT} is defined in the reference section. $I_{\overline{OUT}}$ is not trimmed to 12 bits, so it is not recommended that it be used in conjunction with I_{OUT} in a differential-to-single-ended application. The compliance range of the output is from -1.25V to +3.0V, with a 1V_{P-P} voltage swing allowed within this range.

TABLE 2. INPUT CODING vs CURRENT OUTPUT

INPUT CODE (D11-D0)	I_{OUT} (mA)	$I_{\overline{OUT}}$ (mA)
1111 1111 1111	-20.48	0
1000 0000 0000	-10.24	-10.24
0000 0000 0000	0	-20.48

Settling Time

The settling time of the HI5731 is measured as the time it takes for the output of the DAC to settle to within a $^1/_2$ LSB error band of its final value during a full scale (code 0000... to 1111.... or 1111... to 0000...) transition. All claims made by Harris with respect to the settling time performance of the HI5731 have been fully verified by the National Institute of Standards and Technology (NIST) and are fully traceable.

Glitch

The output glitch of the HI5731 is measured by summing the area under the switching transients after an update of the DAC. Glitch is caused by the time skew between bits of the incoming digital data. Typically, the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). Unequal delay paths through the device can also cause one current source to change before another. In order to minimize this, the Harris HI5731 employes an internal register, just prior to the current sources, which is updated on the clock edge. Lastly, the worst case glitch on traditional D/A converters usually occurs at the major transition (i.e., code 2047 to 2048). However, due to the split architecture of the HI5731, the glitch is moved to the 255 to 256 transition (and every subsequent 256 code transitions thereafter). This split R/2R segmented current source architecture, which decreases the amount of current switching at any one time, makes the glitch practically constant over the entire output range. By making the glitch a constant size over the entire output range this effectively integrates this error out of the end application.

In measuring the output glitch of the HI5731 the output is terminated into a 64Ω load. The glitch is measured at any one of the current cell carry (code 255 to 256 transition or any multiple thereof) throughout the DACs output range.

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 26 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt-seconds (pV-s).

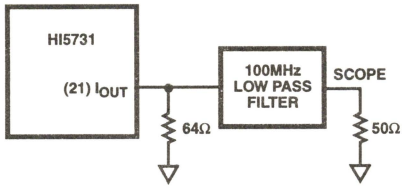


FIGURE 25. GLITCH TEST CIRCUIT

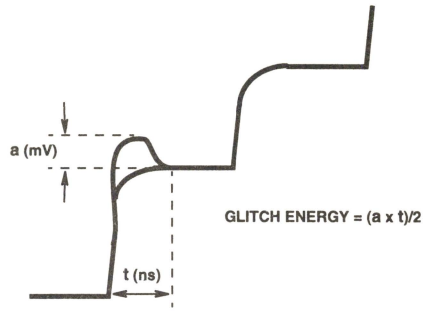


FIGURE 26. MEASURING GLITCH ENERGY

Applications

Bipolar Applications

To convert the output of the HI5731 to a bipolar 4V swing, the following applications circuit is recommended. The reference can only provide 125µA of drive, so it must be buffered to create the bipolar offset current needed to generate the -2V output with all bits 'off'. The output current must be converted to a voltage and then gained up and offset to produce the proper swing. Care must be taken to compensate for the voltage swing and error.

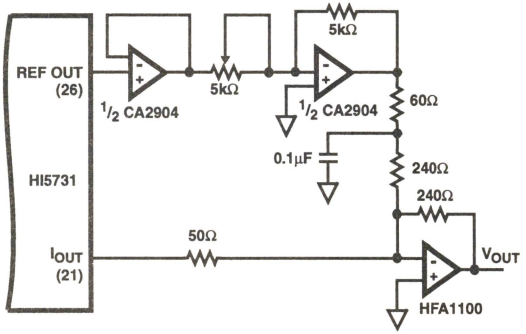


FIGURE 27. BIPOLAR OUTPUT CONFIGURATION

Interfacing to the HSP45106 NCO-16

The HSP45106 is a 16-bit, Numerically Controlled Oscillator (NCO). The HSP45106 can be used to generate various modulation schemes for Direct Digital Synthesis (DDS) applications. Figure 28 shows how to interface an HI5731 to the HSP45106.

Interfacing to the HSP45102 NCO-12

The HSP45102 is a 12-bit, Numerically Controlled Oscillator (NCO). The HSP45102 can be used to generate various modulation schemes for Direct Digital Synthesis (DDS) applications. Figure 29 shows how to interface an HI5731 to the HSP45102.

This high level block diagram is that of a basic PSK modulator. In this example the encoder generates the PSK waveform by driving the Phase Modulation Inputs (P1, P0) of the HSP45102. The P1-0 inputs impart a phase shift to the carrier wave as defined in Table 2.

TABLE 3. PHASE MODULATION INPUT CODING

P1	P0	PHASE SHIFT (DEGREES)
0	0	0
0	1	90
1	0	270
1	1	180

The data port of the HSP45102 drives the 12-bit HI5731 DAC which converts the NCO output into an analog waveform. The output filter connected to the DAC can be tailored to remove unwanted spurs for the desired carrier frequency. The controller is used to load the desired center frequency and control the HSP45102. The HI5731 coupled with the HSP45102 make an inexpensive PSK modulator with Spurious Free performance down to -76dBc.

Definition of Specifications

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL, is the measure of the error in step size between adjacent codes along the converter's transfer curve. Ideally, the step size is 1 LSB from one code to the next, and the deviation from 1 LSB is known as DNL. A DNL specification of greater than -1 LSB guarantees monotonicity.

Feedthru, is the measure of the undesirable switching noise coupled to the output.

Output Voltage Full Scale Settling Time, is the time required from the 50% point on the clock input for a full scale step to settle within an $\pm 1/2$ LSB error band.

Output Voltage Small Scale Settling Time, is the time required from the 50% point on the clock input for a 100mV step to settle within an $1/2$ LSB error band. This is used by applications reconstructing highly correlated signals such as sine waves with more than 5 points per cycle.

Glitch Area, GE, is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a picoVolt-time specification (typically pV-s).

Differential Gain, ΔA_V, is the gain error from an ideal sine wave with a normalized amplitude.

Differential Phase, $\Delta\Phi$, is the phase error from an ideal sine wave.

Signal to Noise Ratio, SNR, is the ratio of a fundamental to the noise floor of the analog output. The first 5 harmonics are ignored, and an output filter of $1/2$ the clock frequency is used to eliminate alias products.

Total Harmonic Distortion, THD, is the ratio of the DAC output fundamental to the RMS sum of the harmonics. The first 5 harmonics are included, and an output filter of $1/2$ the clock frequency is used to eliminate alias products.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at $1/2$ the clock frequency to eliminate noise from clocking alias terms.

Intermodulation Distortion, IMD, is the measure of the sum and difference products produced when a two tone input is driven into the D/A. The distortion products created will arise at sum and difference frequencies of the two tones. IMD can be calculated using the following equation:

$$IMD = \frac{20\text{Log (RMS of Sum and Difference Distortion Products)}}{\text{(RMS Amplitude of the Fundamental)}}.$$

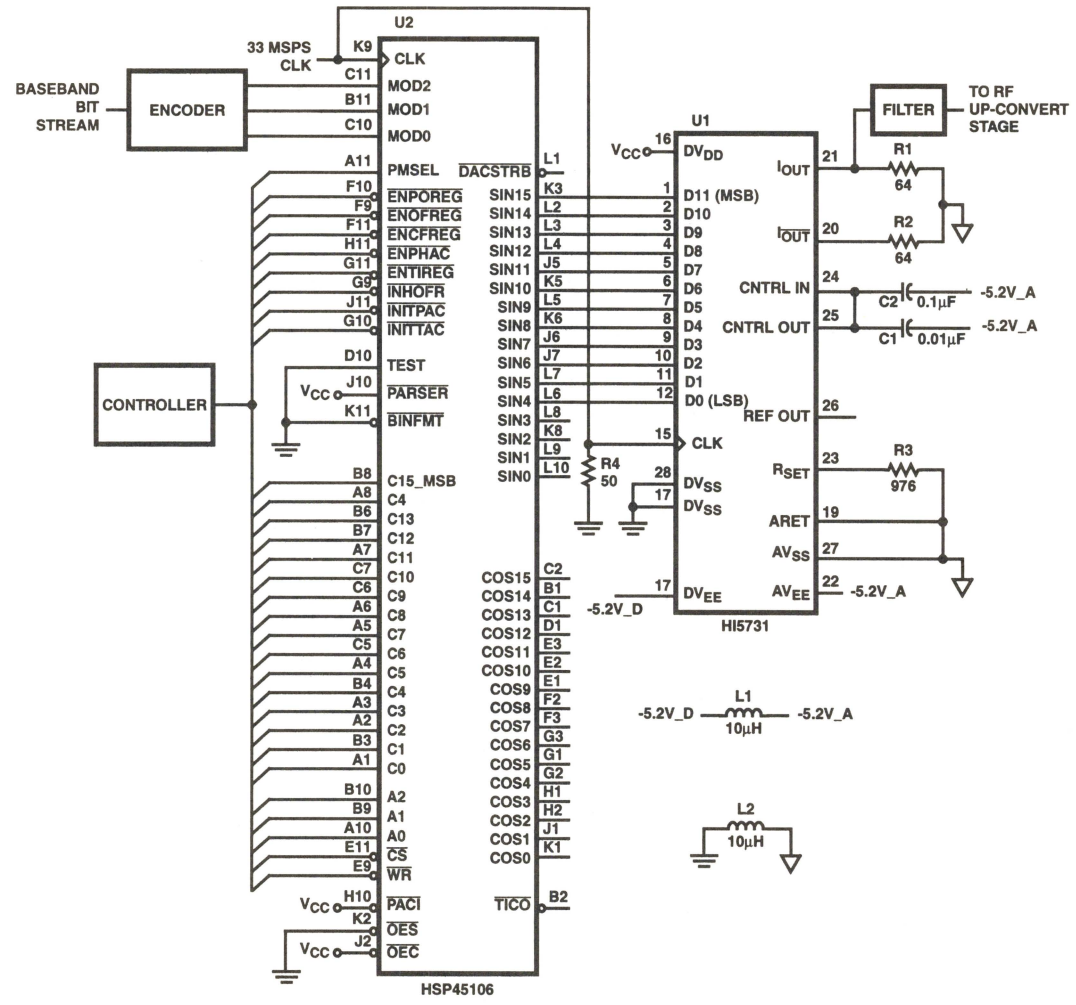


FIGURE 28. MODULATOR USING THE HI5731 AND THE HSP45106 16-BIT NCO

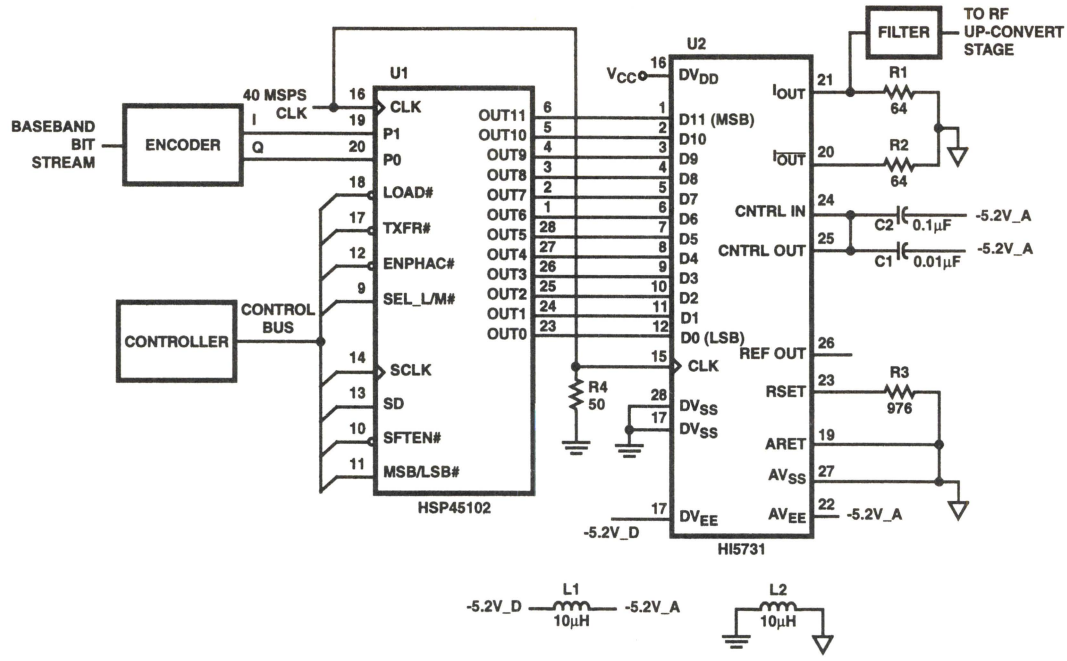


FIGURE 29. PSK MODULATOR USING THE HI5731 AND THE HSP45102 12-BIT NCO

Die Characteristics

DIE DIMENSIONS:

161.5 mils x 160.7 mils x 19 mils

METALLIZATION:

Type: AlSiCu
Thickness: M1 - 8kÅ, M2 - 17kÅ

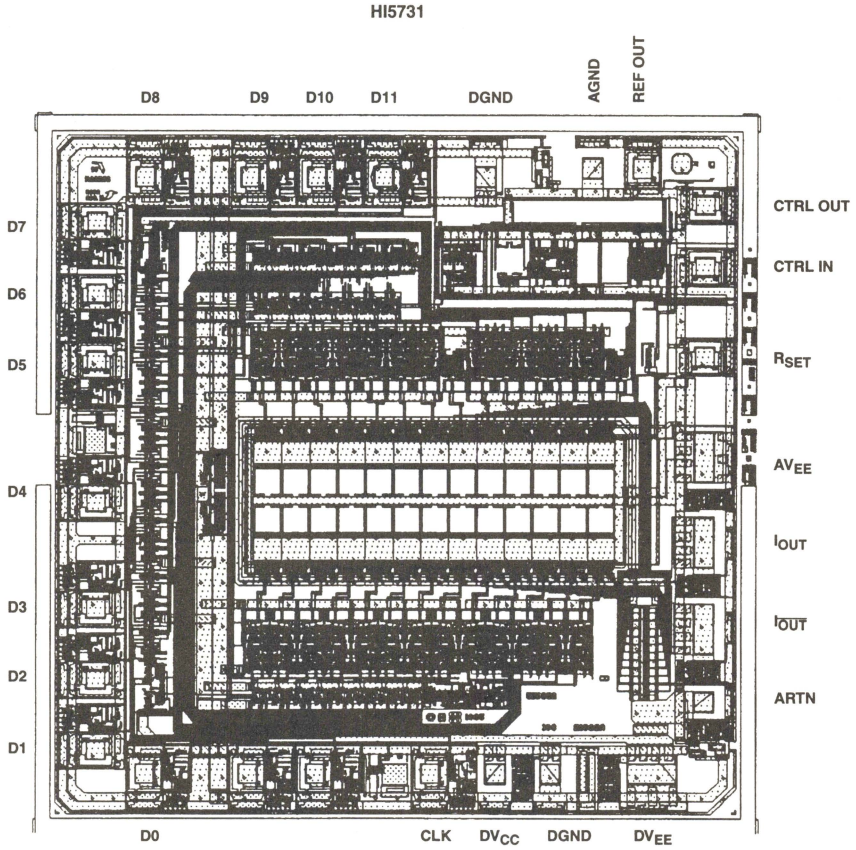
PASSIVATION:

Type: Sandwich Passivation
Undoped Silicon Glass (USG) + Nitride
Thickness: USG - 8kÅ, Nitride - 4.2kÅ
Total 12.2kÅ + 2kÅ

SUBSTRATE POTENTIAL (Powered Up):

V_{EED}

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HI5735

12-Bit, 80 MSPS, High Speed Video D/A Converter

August 1997

Features

- Throughput Rate ..... 80 MSPS
- Low Power 650mW
- Integral Linearity Error ..... 0.75 LSB
- Low Glitch Energy 3.0pV-s
- TTL/CMOS Compatible Inputs
- Improved Hold Time 0.25ns
- Excellent Spurious Free Dynamic Range

Applications

- Professional Video
- Cable TV Headend Equipment

Description

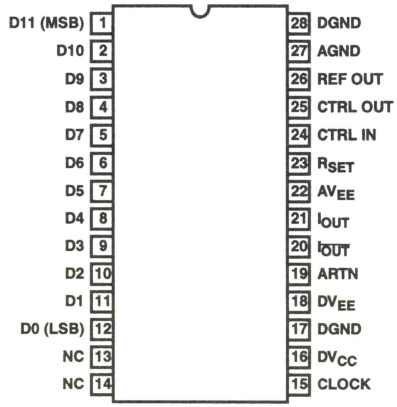
The HI5735 is a 12-bit, 80 MSPS, D/A converter which is implemented in the Harris BiCMOS 10V (HBC-10) process. Operating from +5V and -5.2V, the converter provides -20.48mA of full scale output current and includes an input data register and bandgap voltage reference. Low glitch energy and excellent frequency domain performance are achieved using a segmented architecture. The digital inputs are TTL/CMOS compatible and translated internally to ECL. All internal logic is implemented in ECL to achieve high switching speed with low noise. The addition of laser trimming assures 12-bit linearity is maintained along the entire transfer curve.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5735KCP	0 to 70	28 Lead PDIP	E28.6
HI5735KCB	0 to 70	28 Lead SOIC	M28.3

Pinout

HI5735
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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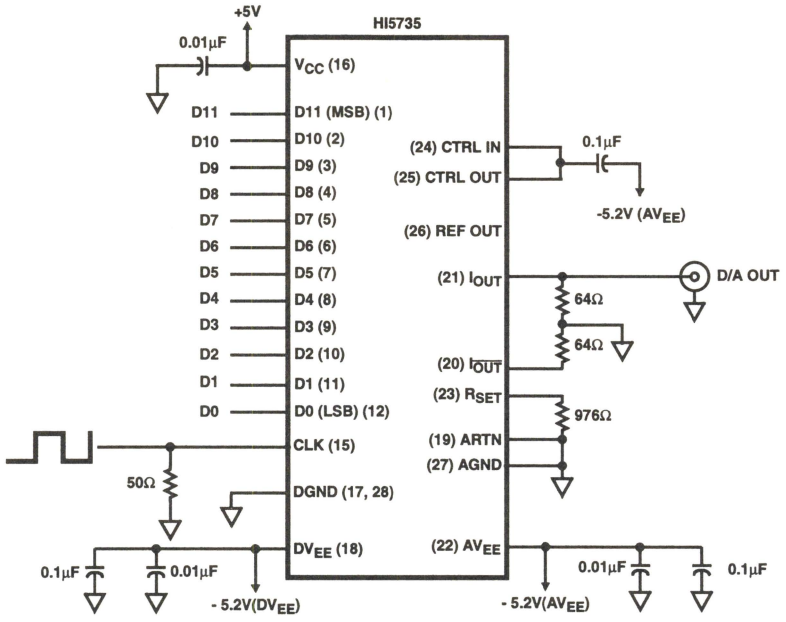
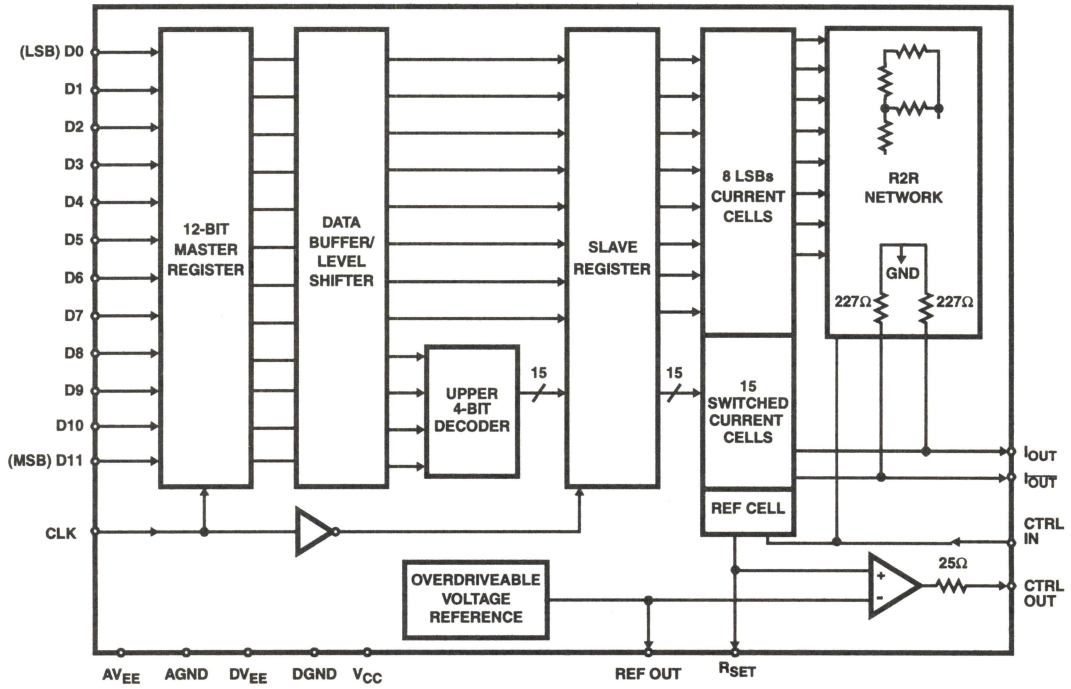
File Number **4133.2**

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings

Digital Supply Voltage V_{CC} to DGND . . . . . +5.5V
Negative Digital Supply Voltage DV_{EE} to DGND . . . . . -5.5V
Negative Analog Supply Voltage AV_{EE} to AGND, ARTN . . . . . -5.5V
Digital Input Voltages (D11-D0, CLK) to DGND . . . . . DV_{CC} to -0.5V
Internal Reference Output Current . . . . . ±2.5mA
Voltage from CTRL IN to AV_{EE} . . . . . 2.5V to 0V
Control Amplifier Output Current . . . . . ±2.5mA
Reference Input Voltage Range . . . . . -3.7V to AV_{EE}
Analog Output Current (I_{OUT}) 30mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
PDIP Package	55
SOIC Package	70

Maximum Junction Temperature
Plastic Packages . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range
HI5735BIx . . . . . -40^{o}C to 85^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = Internal
T_A = 25^{o}C for All Typical Values

PARAMETER	TEST CONDITIONS	HI5735BI T_A = 0^{o}C TO 70^{o}C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		12	-	-	Bits
Integral Linearity Error, INL	(Note 4) ("Best Fit" Straight Line)	-	0.75	1.5	LSB
Differential Linearity Error, DNL	(Note 4)	-	0.5	1.0	LSB
Offset Error, I_{OS}	(Note 4)	-	20	75	µA
Full Scale Gain Error, FSE	(Notes 2, 4)	-	1	10	%
Offset Drift Coefficient	(Note 3)	-	-	0.05	µA/^{o}C
Full Scale Output Current, I_{FS}		-	20.48	-	mA
Output Voltage Compliance Range	(Notes 3, 5)	-1.25	-	+3.0	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	(Note 3)	80	-	-	MSPS
Output Voltage Full Scale Step Settling Time, t_{SETT} Full Scale	To ±0.5 LSB Error Band R_L = 50Ω (Note 3)	-	20	-	ns
Single Glitch Area, GE (Peak)	R_L = 50Ω (Note 3)	-	5	-	pV-s
Doublet Glitch Area, (Net)		-	3	-	pV-s
Output Slew Rate	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	1,000	-	V/µs
Output Rise Time	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	675	-	ps
Output Fall Time	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	470	-	ps
Differential Gain	R_L = 50Ω (Note 3)	-	0.15	-	%
Differential Phase	R_L = 50Ω (Note 3)	-	0.07	-	Deg

Electrical Specifications AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = Internal T_A = 25°C for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	HI5735BI T_A = 0°C TO 70°C			UNITS
		MIN	TYP	MAX	
Spurious Free Dynamic Range to Nyquist (Note 3)	f_{CLK} = 40MHz, f_{OUT} = 2.02MHz, 20MHz Span	-	70	-	dBc
	f_{CLK} = 80MHz, f_{OUT} = 2.02MHz, 40MHz Span	-	70	-	dBc
REFERENCE/CONTROL AMPLIFIER					
Internal Reference Voltage, V_{REF}	(Note 4)	-1.27	-1.23	-1.17	V
Internal Reference Voltage Drift	(Note 3)	-	50	-	µV/°C
Internal Reference Output Current Sink/Source Capability	(Note 3)	-125	-	+50	µA
Internal Reference Load Regulation	I_{REF} = 0 to I_{REF} = -125µA	-	50	-	µV
Input Impedance at REF OUT pin	(Note 3)	-	1.4	-	kΩ
Amplifier Large Signal Bandwidth ($0.6V_{P-P}$)	Sine Wave Input, to Slew Rate Limited (Note 3)	-	3	-	MHz
Amplifier Small Signal Bandwidth ($0.1V_{P-P}$)	Sine Wave Input, to -3dB Loss (Note 3)	-	10	-	MHz
Reference Input Impedance	(Note 3)	-	12	-	kΩ
Reference Input Multiplying Bandwidth (CTL IN)	R_L = 50Ω, 100mV Sine Wave, to -3dB Loss at I_{OUT} (Note 3)	-	200	-	MHz
DIGITAL INPUTS (D9-D0, CLK, INVERT)					
Input Logic High Voltage, V_{IH}	(Note 4)	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 4)	-	-	0.8	V
Input Logic Current, I_{IH}	(Note 4)	-	-	400	µA
Input Logic Current, I_{IL}	(Note 4)	-	-	700	µA
Digital Input Capacitance, C_{IN}	(Note 3)	-	3.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 1 (Note 3)	3.0	2.0	-	ns
Data Hold Time, t_{HLD}	See Figure 1 (Note 3)	0.5	0.25	-	ns
Propagation Delay Time, t_{PD}	See Figure 1 (Note 3)	-	4.5	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 1 (Note 3)	3.0	-	-	ns
POWER SUPPLY CHARACTERISITICS					
I_{EEA}	(Note 4)	-	42	50	mA
I_{EED}	(Note 4)	-	70	85	mA
I_{CCD}	(Note 4)	-	13	20	mA
Power Dissipation	(Note 4)	-	650	-	mW
Power Supply Rejection Ratio	V_{CC} ±5%, V_{EE} ±5%	-	5	-	µA/V

NOTES:

2. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 1.28mA). Ideally the ratio should be 16.
3. Parameter guaranteed by design or characterization and not production tested.
4. All devices are 100% tested at 25°C. 100% production tested at temperature extremes for military temperature devices, sample tested for industrial temperature devices.
5. Dynamic Range must be limited to a 1V swing within the compliance range.

Timing Diagrams

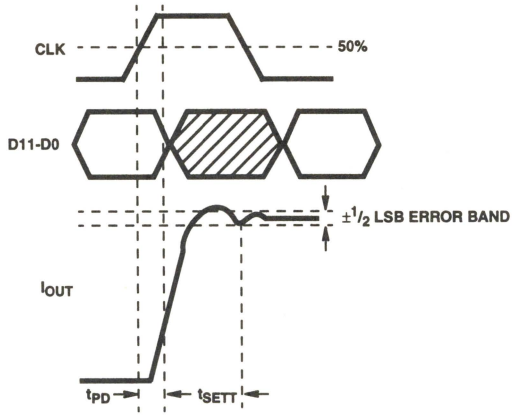


FIGURE 1. FULL SCALE SETTLING TIME DIAGRAM

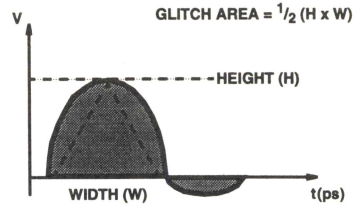


FIGURE 2. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

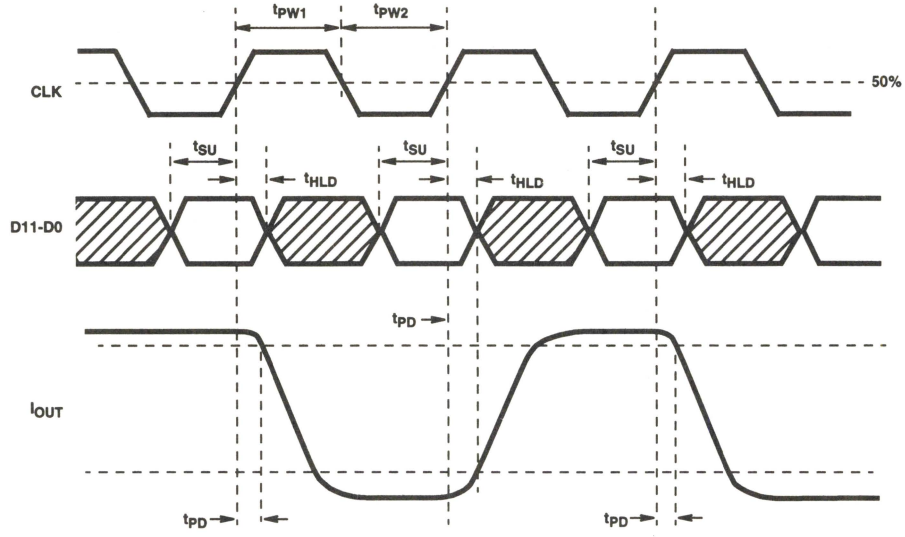


FIGURE 3. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Typical Performance Curves

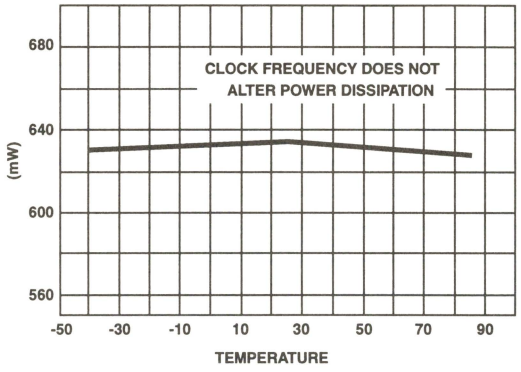


FIGURE 4. TYPICAL POWER DISSIPATION OVER TEMPERATURE

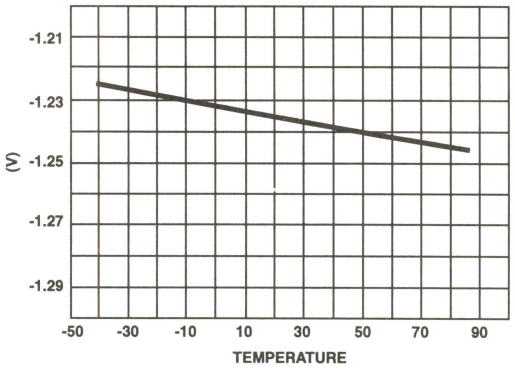


FIGURE 5. TYPICAL REFERENCE VOLTAGE OVER TEMPERATURE

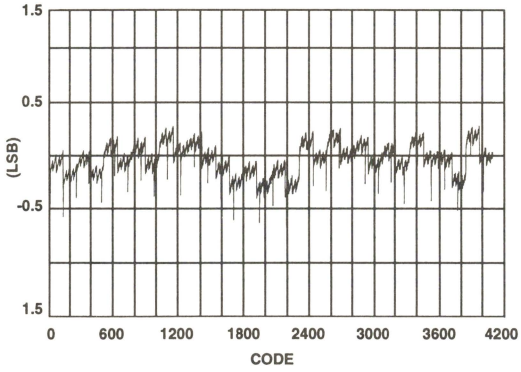


FIGURE 6. TYPICAL INL

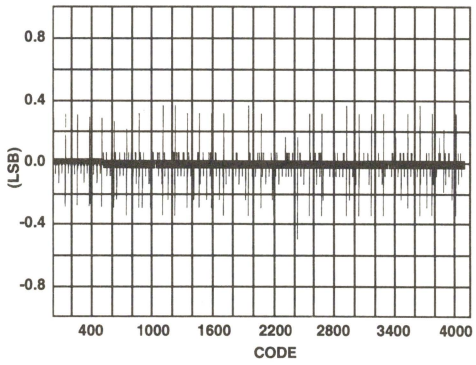


FIGURE 7. TYPICAL DNL

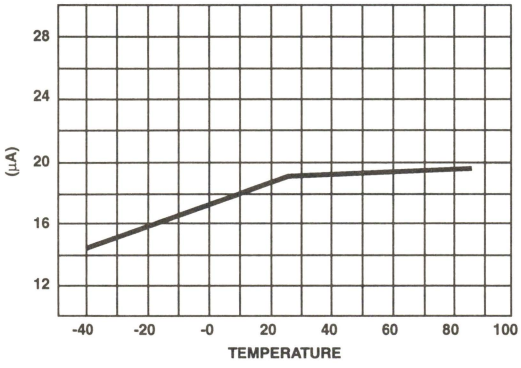


FIGURE 8. OFFSET CURRENT OVER TEMPERATURE

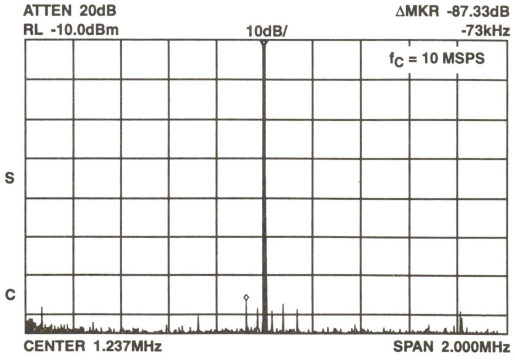


FIGURE 9. SPURIOUS FREE DYNAMIC RANGE = 87.3dBc

Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1-12	D11 (MSB) thru D0 (LSB)	Digital Data Bit 11, the Most Significant Bit thru Digital Data Bit 0, the Least Significant Bit.
15	CLK	Data Clock Pin DC to 80 MSPS.
13, 14	NC	No Connect.
16	V_{CC}	Digital Logic Supply +5V.
17, 28	DGND	Digital Ground.
18	DV_{EE}	-5.2V Logic Supply.
23	R_{SET}	External resistor to set the full scale output current. $I_{FS} = 16 \times (V_{REF\ OUT} / R_{SET})$. Typically 976Ω.
27	AGND	Analog Ground supply current return pin.
19	ARTN	Analog Signal Return for the R/2R ladder.
21	I_{OUT}	Current Output Pin.
20	$I_{\overline{OUT}}$	Complementary Current Output Pin.
22	AV_{EE}	-5.2V Analog Supply.
24	CTRL IN	Input to the current source base rail. Typically connected to CTRL OUT and a 0.1µF capacitor to AV_{EE}. Allows external control of the current sources.
25	CTRL OUT	Control Amplifier Out. Provides precision control of the current sources when connected to CTRL IN such that $I_{FS} = 16 \times (V_{REF\ OUT} / R_{SET})$.
26	REF OUT	-1.23V (typical) bandgap reference voltage output. Can sink up to 125µA or be overdriven by an external reference capable of delivering up to 2mA.

Detailed Description

The HI5735 is a 12-bit, current out D/A converter. The DAC can convert at 80 MSPS and runs on +5V and -5.2V supplies. The architecture is an R/2R and segmented switching current cell arrangement to reduce glitch. Laser trimming is employed to tune linearity to true 12-bit levels. The HI5735 achieves its low power and high speed performance from an advanced BiCMOS process. The HI5735 consumes 650mW (typical) and has an improved hold time of only 0.25ns (typical).

Digital Inputs

The HI5735 is a TTL/CMOS compatible D/A. Data is latched by a Master register. Once latched, data inputs D0 (LSB) thru D11 (MSB) are internally translated from TTL to ECL. The internal latch and switching current source controls are implemented in ECL technology to maintain high switching speeds and low noise characteristics.

Decoder/Driver

The architecture employs a split R/2R ladder and Segmented Current source arrangement. Bits D0 (LSB) thru D7 directly drive a typical R/2R network to create the binary weighted current sources. Bits D8 thru D11 (MSB) pass thru a "thermometer" decoder that converts the incoming data into 15 individual segmented current source enables. This split architecture helps to improve glitch, thus resulting in a more constant glitch characteristic across the entire output transfer function.

Clocks and Termination

The internal 12-bit register is updated on the rising edge of the clock. Since the HI5735 clock rate can run to 80 MSPS, to minimize reflections and clock noise into the part, proper termination should be used. In PCB layout clock runs should be kept short and have a minimum of loads. To guarantee consistent results from board to board, controlled impedance PCBs should be used with a characteristic line impedance Z_O of 50Ω.

To terminate the clock line, a shunt terminator to ground is the most effective type at a 80 MSPS clock rate. A typical value for termination can be determined by the equation:

$R_T = Z_O$,

for the termination resistor. For a controlled impedance board with a Z_O of 50Ω, the R_T = 50Ω. Shunt termination is best used at the receiving end of the transmission line or as close to the HI5735 CLK pin as possible.

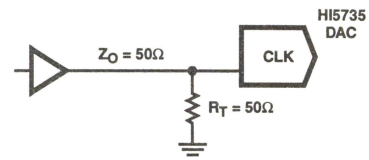


FIGURE 10. CLOCK LINE TERMINATION

Rise and Fall times and propagation delay of the line will be affected by the Shunt Terminator. The terminator should be connected to DGND.

Noise Reduction

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1µF and 0.01µF ceramic capacitors placed as close to the body of the HI5735 as possible on the analog (AV_{EE}) and digital (DV_{EE}) supplies. The analog and digital ground returns should be connected together back at the device to ensure proper operation on power up. The V_{CC} power pin should also be decoupled with a 0.1µF capacitor.

Reference

The internal reference of the HI5735 is a -1.23V (typical) bandgap voltage reference with 50µV/°C of temperature drift (typical). The internal reference is connected to the Control Amplifier which in turn drives the segmented current cells. Reference Out (REF OUT) is internally connected to the Control Amplifier. The Control Amplifier Output (CTRL OUT) should be used to drive the Control Amplifier Input (CTRL IN) and a 0.1µF capacitor to analog V_{EE}. This improves settling time by providing an AC ground at the current source base node. The Full Scale Output Current is controlled by the REF OUT pin and the set resistor (R_{SET}). The ratio is:

$$I_{OUT} \text{ (Full Scale)} = (V_{REF\ OUT}/R_{SET}) \times 16.$$

The internal reference (REF OUT) can be overdriven with a more precise external reference to provide better performance over temperature. Figure 11 illustrates a typical external reference configuration.

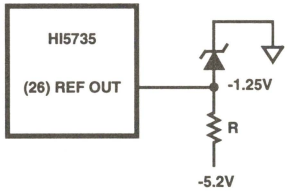


FIGURE 11. EXTERNAL REFERENCE CONFIGURATION

Outputs

The outputs I_{OUT} and $I_{\overline{OUT}}$ are complementary current outputs. Current is steered to either I_{OUT} or $I_{\overline{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full scale current minus one LSB. The current output can be converted to a voltage by using a load resistor. Both current outputs should have the same load resistor (64Ω typically). By using a 64Ω load on the output, a 50Ω effective output resistance (R_{OUT}) is achieved due to the 227Ω (±15%) parallel resistance seen looking back into the output. This is the nominal value of the R2R ladder of the DAC. The 50Ω output is needed for matching the output with a 50Ω line. The load resistor should be chosen so that the effective output resistance (R_{OUT}) matches the line resistance. The output voltage is:

$$V_{OUT} = I_{OUT} \times R_{OUT}.$$

I_{OUT} is defined in the reference section. $I_{\overline{OUT}}$ is not trimmed to 12 bits, so it is not recommended that it be used in conjunction with I_{OUT} in a differential-to-single-ended application. The compliance range of the output is from -1.25V to +3.0V, with a $1V_{P-P}$ voltage swing allowed within this range.

TABLE 2. INPUT CODING vs CURRENT OUTPUT

INPUT CODE (D11-D0)	I_{OUT} (mA)	$I_{\overline{OUT}}$ (mA)
1111 1111 1111	-20.48	0
1000 0000 0000	-10.24	-10.24
0000 0000 0000	0	-20.48

Settling Time

The settling time of the HI5735 is measured as the time it takes for the output of the DAC to settle to within a 1/2 LSB error band of its final value during a full scale (code 0000... to 1111.... or 1111... to 0000...) transition. All claims made by Harris with respect to the settling time performance of the HI5735 have been fully verified by the National Institute of Standards and Technology (NIST) and are fully traceable.

Glitch

The output glitch of the HI5735 is measured by summing the area under the switching transients after an update of the DAC. Glitch is caused by the time skew between bits of the incoming digital data. Typically, the switching time of digital inputs are asymmetrical, meaning that the turn off time is faster than the turn on time (TTL designs). Unequal delay paths through the device can also cause one current source to change before another. In order to minimize this, the Harris HI5735 employes an internal register, just prior to the current sources, which is updated on the clock edge. Lastly, the worst case glitch on traditional D/A converters usually occurs at the major transition (i.e., code 2047 to 2048). However, due to the split architecture of the HI5735, the glitch is moved to the 255 to 256 transition (and every subsequent 256 code transitions thereafter). This split R/2R segmented current source architecture, which decreases the amount of current switching at any one time, makes the glitch practically constant over the entire output range. By making the glitch a constant size over the entire output range, this effectively integrates this error out of the end application.

In measuring the output glitch of the HI5735 the output is terminated into a 64Ω load. The glitch is measured at any one of the current cell carry (code 255 to 256 transition or any multiple thereof) throughout the DACs output range.

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 13 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt-seconds (pV-s).

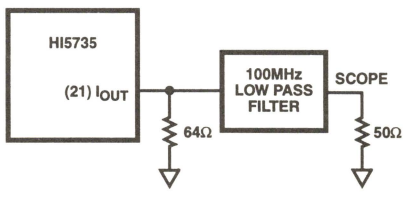


FIGURE 12. GLITCH TEST CIRCUIT

Applications

Bipolar Applications

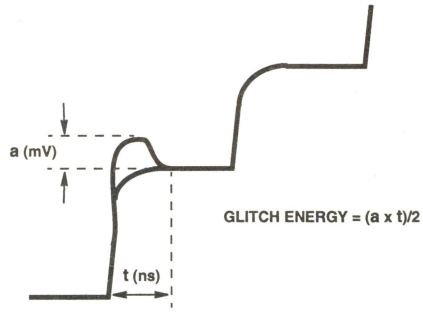


FIGURE 13. MEASURING GLITCH ENERGY

To convert the output of the HI5735 to a bipolar 4V swing, the following applications circuit is recommended. The reference can only provide 125µA of drive, so it must be buffered to create the bipolar offset current needed to generate the -2V output with all bits "off". The output current must be converted to a voltage and then gained up and offset to produce the proper swing. Care must be taken to compensate for the voltage swing and error

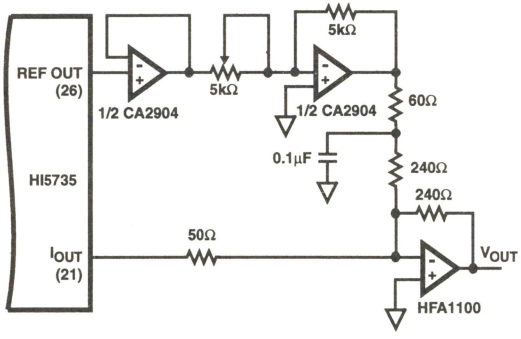


FIGURE 14. BIPOLAR OUTPUT CONFIGURATION

Definition of Specifications

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL, is the measure of the error in step size between adjacent codes along the converter's transfer curve. Ideally, the step size is 1 LSB from one code to the next, and the deviation from 1 LSB is known as DNL. A DNL specification of greater than -1 LSB guarantees monotonicity.

Feedthru, is the measure of the undesirable switching noise coupled to the output.

Output Voltage Full Scale Settling Time, is the time required from the 50% point on the clock input for a full scale step to settle within an $\pm 1/2$ LSB error band.

Output Voltage Small Scale Settling Time, is the time required from the 50% point on the clock input for a 100mV step to settle within an $1/2$ LSB error band. This is used by applications reconstructing highly correlated signals such as sine waves with more than 5 points per cycle.

Glitch Area, GE, is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a picoVolt•Time specification (typically pV•s).

Differential Gain, ΔA_V, is the gain error from an ideal sine wave with a normalized amplitude.

Differential Phase, $\Delta\Phi$, is the phase error from an ideal sine wave.

Signal to Noise Ratio, SNR, is the ratio of a fundamental to the noise floor of the analog output. The first 5 harmonics are ignored, and an output filter of $1/2$ the clock frequency is used to eliminate alias products.

Total Harmonic Distortion, THD, is the ratio of the DAC output fundamental to the RMS sum of the harmonics. The first 5 harmonics are included, and an output filter of $1/2$ the clock frequency is used to eliminate alias products.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at $1/2$ the clock frequency to eliminate noise from clocking alias terms.

Intermodulation Distortion, IMD, is the measure of the sum and difference products produced when a two tone input is driven into the D/A. The distortion products created will arise at sum and difference frequencies of the two tones. IMD can be calculated using the following equation:

$$IMD = \frac{20\text{Log (RMS of Sum and Difference Distortion Products)}}{\text{(RMS Amplitude of the Fundamental)}}.$$

Die Characteristics

DIE DIMENSIONS:

161.5 mils x 160.7 mils x 19 mils ±1 mil

METALLIZATION:

Type: AlSiCu
Thickness: M1 - 8kÅ, M2 - 17kÅ

PASSIVATION:

Type: Sandwich Passivation
Undoped Silicon Glass (USG) + Nitride
Thickness: USG - 8kÅ, Nitride - 4.2kÅ
Total 12.2kÅ ± +2kÅ

DIE ATTACH:

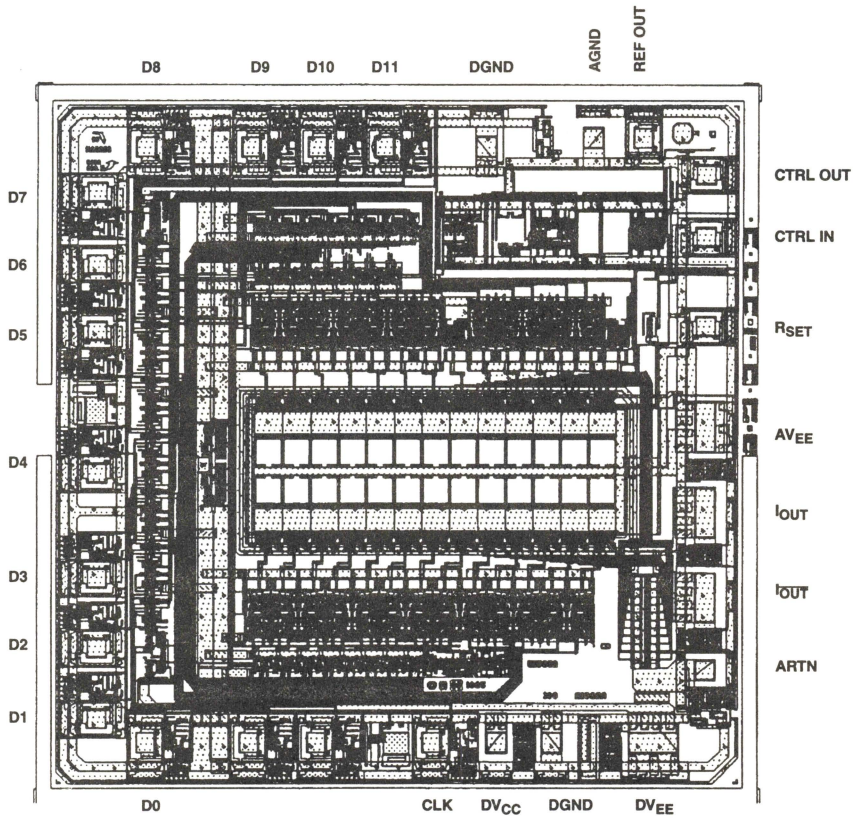
Silver Filled Epoxy

SUBSTRATE POTENTIAL (Powered Up):

V_{EED}

Metallization Mask Layout

HI5735



HARRIS SEMICONDUCTOR

HI5741

August 1997

14-Bit, 100 MSPS, High Speed D/A Converter

Features

- Throughput Rate ..... 100 MSPS
- Low Power 650mW
- Integral Linearity Error .....1 LSB
- Low Glitch Energy 1pV-s
- TTL/CMOS Compatible Inputs
- Improved Hold Time 0.25ns
- Excellent Spurious Free Dynamic Range

Applications

- Cellular Base Stations
- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Test Equipment
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

Description

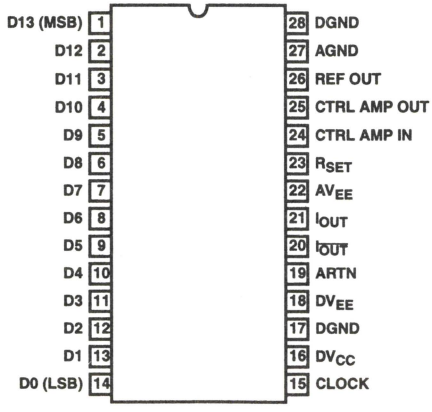
The HI5741 is a 14-bit, 100 MSPS, D/A converter which is implemented in the Harris BiCMOS 10V (HBC-10) process. Operating from +5V and -5.2V, the converter provides 20.48mA of full scale output current and includes an input data register and bandgap voltage reference. Low glitch energy and excellent frequency domain performance are achieved using a segmented architecture. The digital inputs are TTL/CMOS compatible and translated internally to ECL. All internal logic is implemented in ECL to achieve high switching speed with low noise. The addition of laser trimming assures 14-bit linearity is maintained along the entire transfer curve.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5741BIP	-40 to 85	28 Ld PDIP	E28.6
HI5741BIB	-40 to 85	28 Ld SOIC	M28.3
HI5741-EVS	25	Evaluation Board (SOIC)	

Pinout

HI5741
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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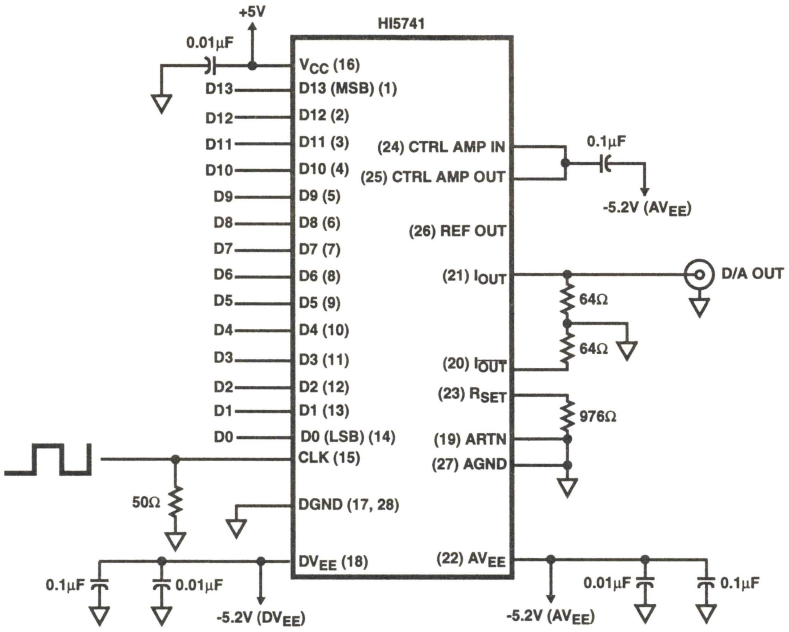
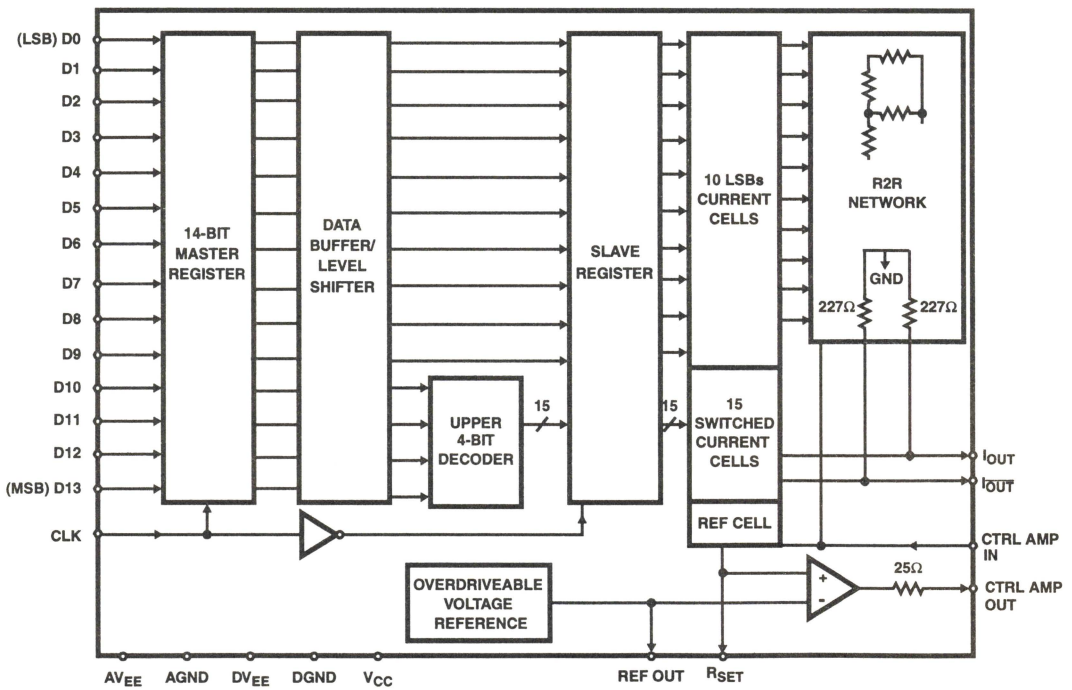
File Number 4071.3

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Digital Supply Voltage V_{CC} to DGND . . . . . +5.5V
Negative Digital Supply Voltage DV_{EE} to DGND . . . . . -5.5V
Negative Analog Supply Voltage AV_{EE} to AGND, ARTN . . . . . -5.5V
Digital Input Voltages (D13-D0, CLK) to DGND . . . . . DV_{CC} to -0.5V
Internal Reference Output Current . . . . . ±2.5mA
Voltage from CTRL AMP IN to AV_{EE} . . . . . 2.5V to 0V
Control Amplifier Output Current . . . . . ±2.5mA
Reference Input Voltage Range . . . . . -3.7V to AV_{EE}
Analog Output Current (I_{OUT}) 30mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	55
SOIC Package	70

Maximum Junction Temperature
HI5741BIx . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = Internal, $T_A = 25^oC$

PARAMETER	TEST CONDITIONS	HI5741BI T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		14	-	-	Bits
Integral Linearity Error, INL (Notes 5)	"Best Fit Straight Line", $T_A = 25^oC$	-	1.0	1.5	LSB
	"Best Fit Straight Line", T_A = -40°C to 85°C	-	-	1.75	LSB
Differential Linearity Error, DNL	(Note 5)	-	0.5	1.0	LSB
Offset Error, I_{OS}	(Note 5)	-	8	75	µA
Full Scale Gain Error, FSE	(Notes 3, 5)	-	3.2	10	%
Offset Drift Coefficient	(Note 4)	-	-	0.05	µA/°C
Full Scale Output Current, I_{FS}		-	-20.48	-	mA
Output Voltage Compliance Range	(Note 4)	-1.25	-	+3.0	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	(Note 4)	100	-	-	MSPS
Output Voltage Settling Time ($^1/_{16}$th Scale Step Across Segment)	R_L = 64Ω (Note 4) - Settling to 0.024%	-	11	-	ns
	R_L = 64Ω (Note 4) - Settling to 0.012%	-	20	-	ns
Singlet Glitch Area, GE (Peak)	R_L = 64Ω (Note 4)	-	1	-	pV•s
Output Slew Rate	R_L = 64Ω, DAC Operating in Latched Mode (Note 4)	-	1,000	-	V/µs
Output Rise Time	R_L = 64Ω, DAC Operating in Latched Mode (Note 4)	-	675	-	ps
Output Fall Time	R_L = 64Ω, DAC Operating in Latched Mode (Note 4)	-	470	-	ps
Spurious Free Dynamic Range within a Window (Note 4)	f_{CLK} = 10 MSPS, f_{OUT} = 1.23MHz, 2MHz Span	-	87	-	dBc
	f_{CLK} = 20 MSPS, f_{OUT} = 5.055MHz, 2MHz Span	-	77	-	dBc
	f_{CLK} = 40 MSPS, f_{OUT} = 16MHz, 10MHz Span	-	75	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 10.1MHz, 2MHz Span	-	80	-	dBc
	f_{CLK} = 80 MSPS, f_{OUT} = 5.1MHz, 2MHz Span	-	78	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 10.1MHz, 2MHz Span	-	79	-	dBc
Spurious Free Dynamic Range to Nyquist (Notes 4)	f_{CLK} = 10 MSPS, f_{OUT} = 1.023MHz, 5MHz Span	-	86	-	dBc
	f_{CLK} = 10 MSPS, f_{OUT} = 2.02MHz, 5MHz Span	-	85	-	dBc
	f_{CLK} = 25 MSPS, f_{OUT} = 2.02MHz, 12.5MHz Span	-	77	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 5.055MHz, 25MHz Span	-	74	-	dBc
	f_{CLK} = 75 MSPS, f_{OUT} = 7.52MHz, 37.5MHz Span	-	73	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 10.1MHz, 50MHz Span	-	71	-	dBc

Electrical Specifications AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = Internal, T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS	HI5741BI T_A = -40°C TO 85°C MIN	TYP	MAX	UNITS
Multi-Tone Power Ratio (MTPR)	8 Tones, no Clipping, 110kHz Spacing, 220kHz spacing between tones 4 and 5, f_{CLK} = 20 MSPS (Note 7)	-	76	-	dBc
REFERENCE/CONTROL AMPLIFIER					
Internal Reference Voltage, V_{REF}	(Notes 5)	-1.27	-1.23	-1.17	V
Internal Reference Voltage Drift	(Note 4)	-	50	-	µV/°C
Internal Reference Output Current Sink/Source Capability	(Note 4)	-500	-	+50	µA
Internal Reference Load Regulation	I_{REF} = 0 to I_{REF} = -500µA	-	100	-	µV
Amplifier Input Impedance	(Note 4)	-	3	-	MΩ
Amplifier Large Signal Bandwidth	4.0V_{P-P} Sine Wave Input, to Slew Rate Limited (Note 4)	-	1	-	MHz
Amplifier Small Signal Bandwidth	1.0V_{P-P} Sine Wave Input, to -3dB Loss (Note 4)	-	5	-	MHz
Reference Input Impedance (CTL IN)	(Note 4)	-	12	-	kΩ
Reference Input Multiplying Bandwidth (CTL IN)	R_L = 50Ω, 100mV Sine Wave, to -3dB Loss at I_{OUT} (Note 4)	-	75	-	MHz
DIGITAL INPUTS (D9-D0, CLK, INVERT)					
Input Logic High Voltage, V_{IH}	(Note 5)	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 5)	-	-	0.8	V
Input Logic Current, I_{IH}	(Note 5)	-	-	400	µA
Input Logic Current, I_{IL}	(Note 5)	-	-	700	µA
Digital Input Capacitance, C_{IN}	(Note 4)	-	3.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 1 (Note 4)	3	2.0	-	ns
Data Hold Time, t_{HLD}	See Figure 1 (Note 4)	0.5	0.25	-	ns
Propagation Delay Time, t_{PD}	See Figure 1 (Note 4)	-	4.5	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 1 (Note 4)	1.0	0.85	-	ns
POWER SUPPLY CHARACTERISTICS					
IV_{EEA}	(Note 5)	-	42	50	mA
IV_{EED}	(Note 5)	-	66	85	mA
IV_{CCD}	(Note 5)	-	13	20	mA
Power Dissipation	(Note 5)	-	650	-	mW
Power Supply Rejection Ratio	V_{CC} ±5%, V_{EE} ±5%	-	5	-	µA/V

NOTES:

2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 1.28mA). Ideally the ratio should be 16.
4. Parameter guaranteed by design or characterization and not production tested.
5. All devices are 100% tested at 25°C.
6. Dynamic Range must be limited to a 1V swing within the compliance range.
7. In testing MTPR, tone frequencies ranged from 1.95MHz to 3.05MHz. The ratio is measured as the range from peak power to peak distortion in the region of removed tones.

Timing Diagrams

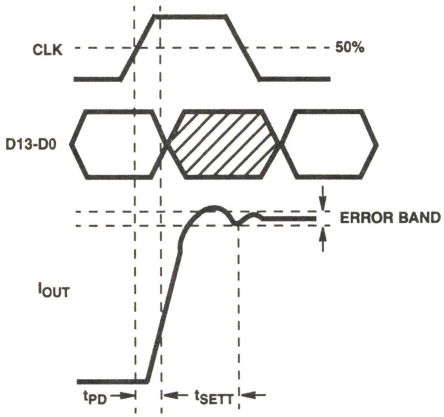


FIGURE 1. FULL SCALE SETTLING TIME DIAGRAM

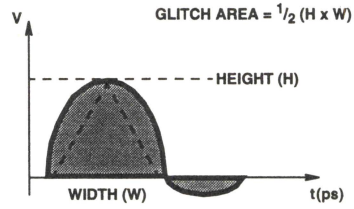


FIGURE 2. PEAK GLITCH AEA (SINGLET) MEASUREMENT METHOD

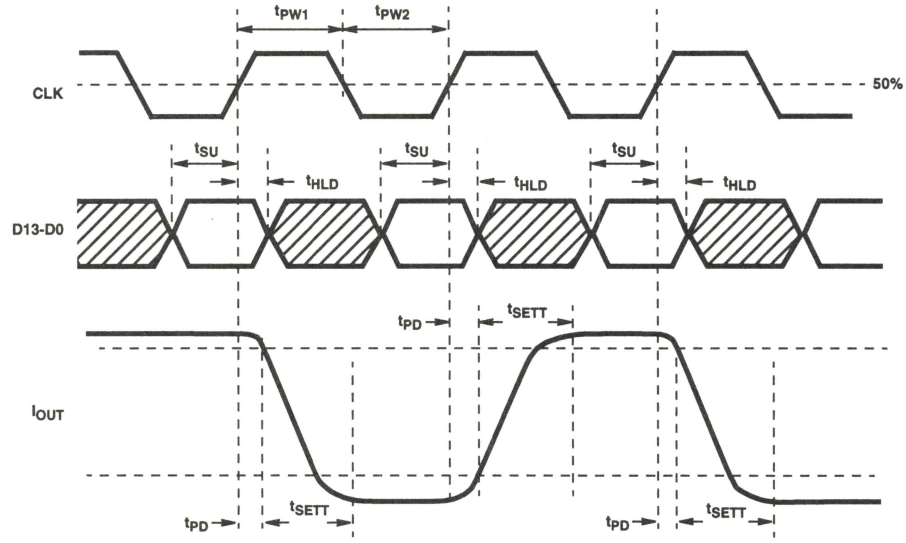


FIGURE 3. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Typical Performance Curves

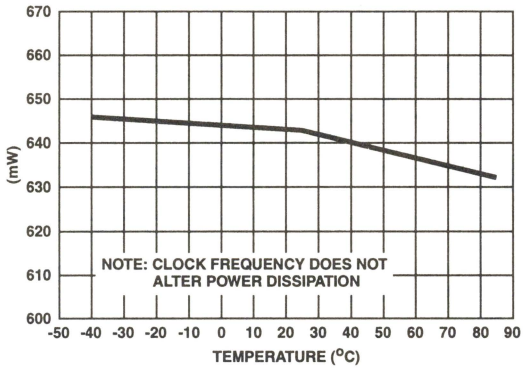


FIGURE 4. TYPICAL POWER DISSIPATION OVER TEMPERATURE

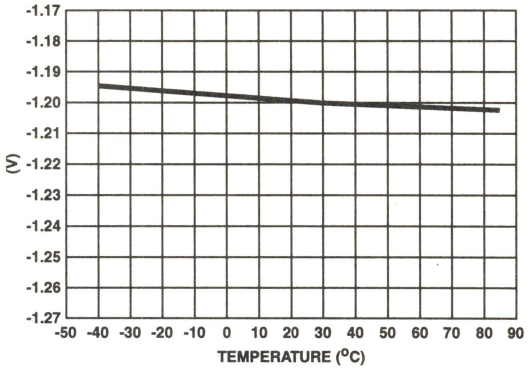


FIGURE 5. TYPICAL REFERENCE VOLTAGE OVER TEMPERATURE

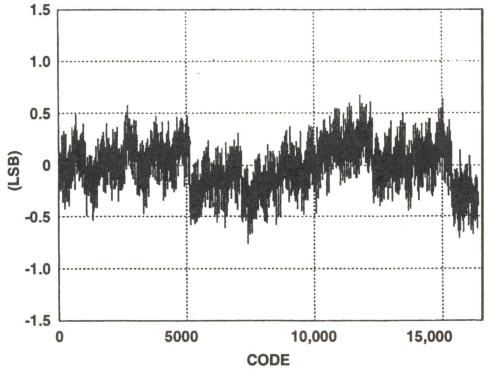


FIGURE 6. TYPICAL INL PERFORMANCE

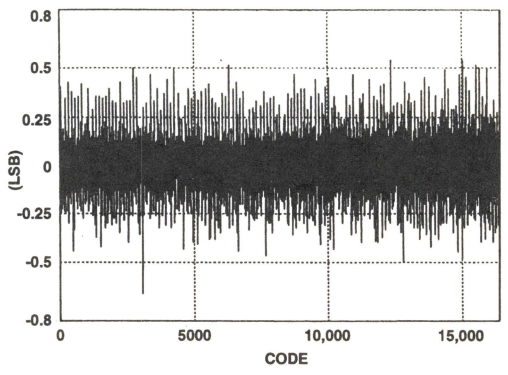


FIGURE 7. TYPICAL DNL PERFORMANCE

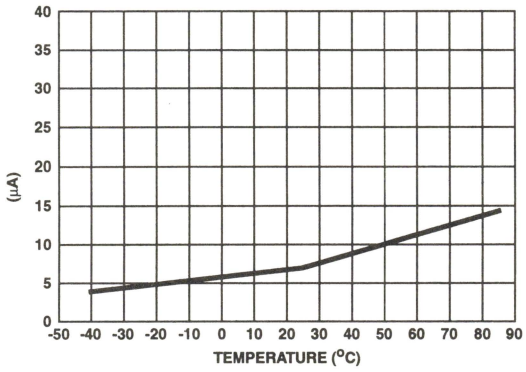


FIGURE 8. TYPICAL OFFSET CURRENT OVER TEMPERATURE

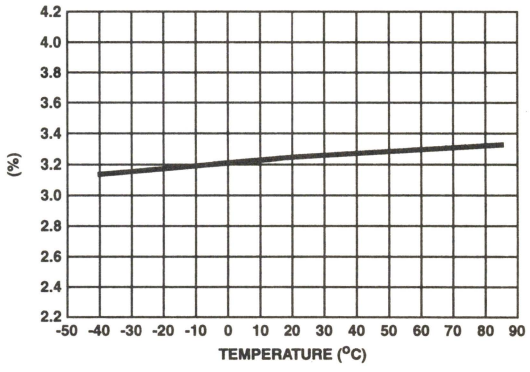


FIGURE 9. TYPICAL GAIN ERROR OVER TEMPERATURE

Typical Performance Curves (Continued)

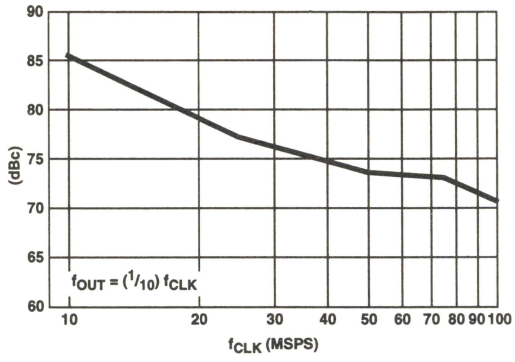


FIGURE 10. SFDR vs CLOCK FREQUENCY

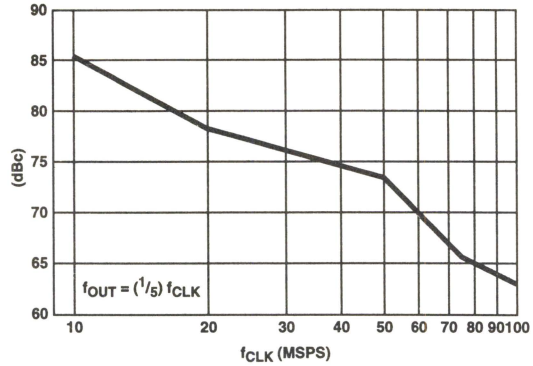


FIGURE 11. SFDR vs CLOCK FREQUENCY

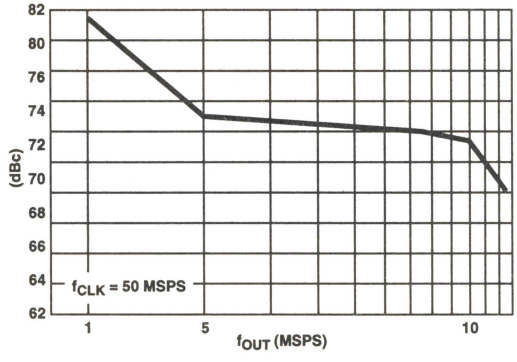


FIGURE 12. SFDR vs f_{OUT}

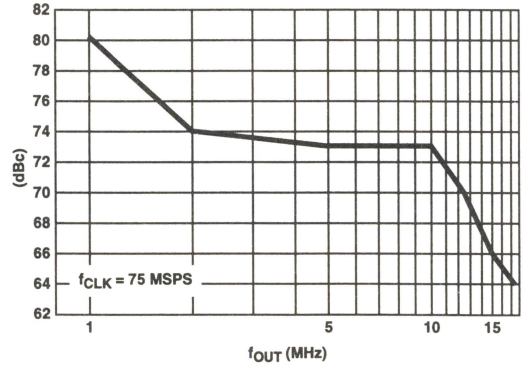


FIGURE 13. SFDR vs f_{OUT}

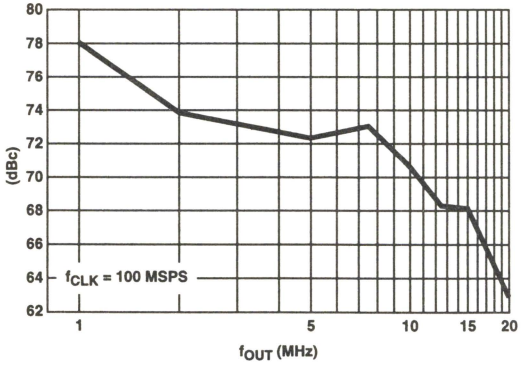


FIGURE 14. SFDR vs f_{OUT}

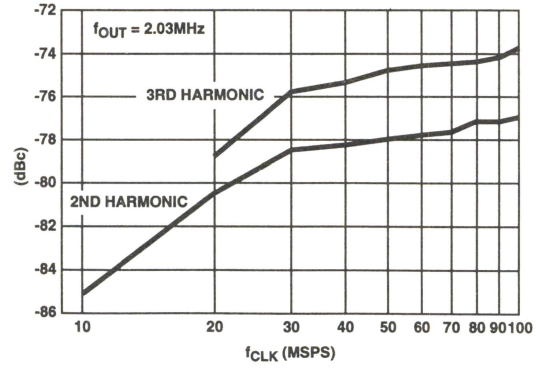


FIGURE 15. HARMONIC DISTORTION vs CLOCK FREQUENCY

Typical Performance Curves (Continued)

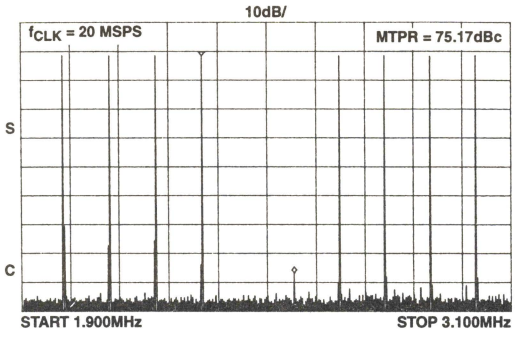


FIGURE 16. TYPICAL MTPR PERFORMANCE

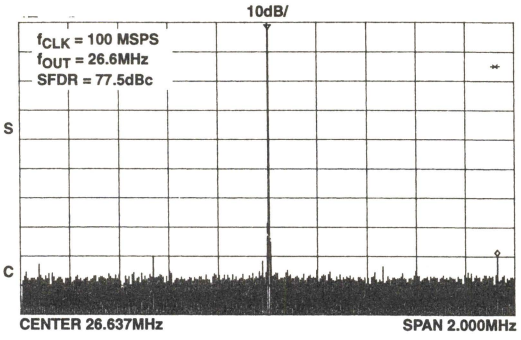


FIGURE 17. SFDR WITHIN A WINDOW

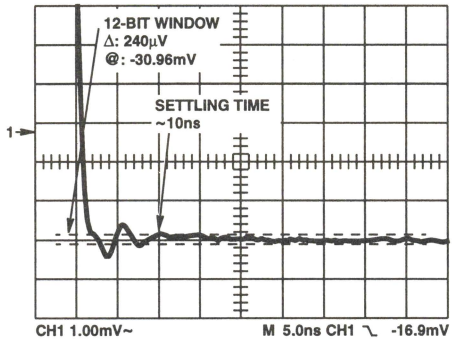


FIGURE 18. TYPICAL SETTLING TIME PERFORMANCE

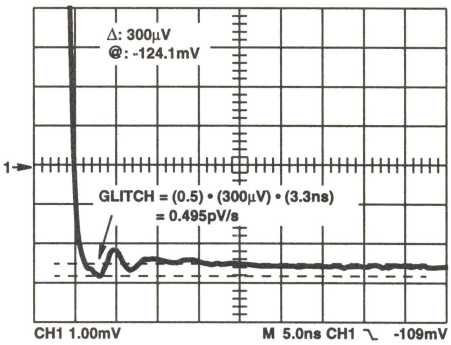


FIGURE 19. TYPICAL GLITCH ENERGY

Pin Descriptions

PIN NO.	PIN NAME	PIN DESCRIPTION
1-14	D13 (MSB) thru D0 (LSB)	Digital Data Bit 13, the Most Significant Bit through Digital Data Bit 0, the Least Significant Bit.
15	CLK	Data Clock Pin 100kHz to 100 MSPS.
16	V_{CC}	Digital Logic Supply +5V.
17, 28	DGND	Digital Ground.
18	DV_{EE}	-5.2V Logic Supply.
23	R_{SET}	External Resistor to set the full scale output current. $I_{FS} = 16 \times (V_{REFOUT}/R_{SET})$. Typically 976Ω.
27	AGND	Analog Ground Supply current return pin.
19	ARTN	Analog Signal Return for the R/2R ladder.
21	I_{OUT}	Current Output Pin.
20	$I_{\overline{OUT}}$	Complementary Current Output pin.
22	AV_{EE}	-5.2V Analog Supply.
24	CTRL AMP IN	Input to the current source base rail. Typically connected to CTRL AMP OUT and a 0.1µF capacitor to AV_{EE}. Allows external control of the current sources.
25	CTRL AMP OUT	Control amplifier out. Provides precision control of the current sources when connected to CTRL AMP IN such that $I_{FS} = 16 \times (V_{REFOUT}/R_{SET})$.
26	REF OUT	-1.23V (typical) bandgap reference voltage output. Can sink up to 500µA or be overdriven by an external reference capable of delivering up to 2mA.

Detailed Description

The HI5741 is a 14-bit, current out D/A converter. The DAC can convert at 100 MSPS and runs on +5V and -5.2V supplies. The architecture is an R/2R and segmented switching current cell arrangement to reduce glitch. Laser trimming is employed to tune linearity to true 14-bit levels. The HI5741 achieves its low power and high speed performance from an advanced BiCMOS process. The HI5741 consumes 650mW (typical) and has an improved hold time of only 0.25ns (typical). The HI5741 is an excellent converter for use in communications applications and high performance video systems.

Digital Inputs

The HI5741 is a TTL/CMOS compatible D/A. Data is latched by a Master register. Once latched, data inputs D0 (LSB) through D13 (MSB) are internally translated from TTL to ECL. The internal latch and switching current source controls are implemented in ECL technology to maintain high switching speeds and low noise characteristics.

Decoder/Driver

The architecture employs a split R/2R ladder and segmented current source arrangement. Bits D0 (LSB) through D9 directly drive a typical R/2R network to create the binary weighted current sources. Bits D10 through D13 (MSB) pass through a "thermometer" decoder that converts the incoming data into 15 individual segmented current source enables. This split architecture helps to improve glitch, thus resulting in a more constant glitch characteristic across the entire output transfer function.

Clocks and Termination

The internal 14-bit register is updated on the rising edge of the clock. Since the HI5741 clock rate can run to 100 MSPS, to minimize reflections and clock noise into the part, proper termination should be used. In PCB layout clock runs should be kept short and have a minimum of loads. To guarantee consistent results from board to board, controlled impedance PCBs should be used with a characteristic line impedance Z_O of 50Ω.

To terminate the clock line, a shunt terminator to ground is the most effective type at a 100 MSPS clock rate. A typical value for termination can be determined by the equation,

$$R_T = Z_O$$

for the termination resistor. For a controlled impedance board with a Z_O of 50Ω, the R_T = 50Ω. Shunt termination is best used at the receiving end of the transmission line or as close to the HI5741 CLK pin as possible.

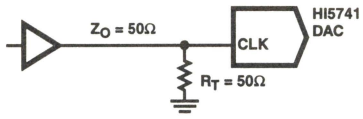


FIGURE 20. HI5741 CLOCK LINE TERMINATION

Rise and Fall times and propagation delay of the line will be affected by the shunt terminator. The terminator should be connected to DGND.

Noise Reduction

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1µF and 0.01µF ceramic capacitors placed as close to the body of the HI5741 as possible on the analog (AV_{EE}) and digital (DV_{EE}) supplies. The analog and digital ground returns should be connected together back at the device to ensure proper operation on power up. The V_{CC} power pin should also be decoupled with a 0.1µF capacitor.

Reduction of digital noise (caused by high slew rates on the bit inputs to the HI5741) can be accomplished through the use of series termination resistors. The use of serial resistors, which combine with the input capacitance of the HI5741 to induce a low pass filter characteristic, keeps the noise generated by high slew rate digital signals from corrupting the high accuracy analog data. Refer to Application Note AN9619 "Optimizing setup conditions for high accuracy measurements of the HI5741" for further details on selecting the proper value of series termination to meet application specific needs.

Reference

The internal reference of the HI5741 is a -1.23V (typical) bandgap voltage reference with 50µV/°C of temperature drift (typical). The internal reference is connected to the Control Amplifier which in turn drives the segmented current cells. Reference Out (REF OUT) is internally connected to the Control Amplifier. The Control Amplifier Output (CTRL OUT) should be used to drive the Control Amplifier Input (CTRL IN) and a 0.1µF capacitor to analog V_{EE}. This improves settling time by providing an AC ground at the current source base node. The Full Scale Output Current is controlled by the REF OUT pin and the set resistor (R_{SET}). The ratio is:

$$I_{OUT} \text{ (Full Scale)} = (V_{REF\ OUT}/R_{SET}) \times 16.$$

The internal reference (REF OUT) can be overdriven with a more precise external reference to provide better performance over temperature. Figure 21 illustrates a typical external reference configuration.

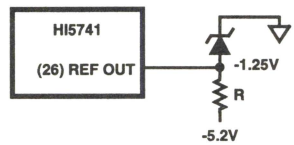


FIGURE 21. EXTERNAL REFERENCE CONFIGURATION

Multiplying Capability

The HI5741 can operate in two different multiplying configurations. For frequencies from DC to 100kHz, a signal of up to $0.6V_{P-P}$ can be applied directly to the REF OUT pin as shown in Figure 22.

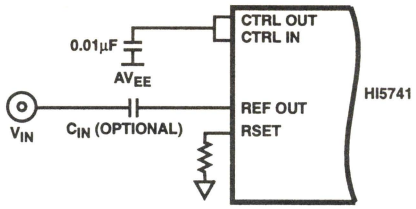


FIGURE 22. LOW FREQUENCY MULTIPLYING BANDWIDTH CIRCUIT

The signal must have a DC value such that the peak negative voltage equals -1.25V. Alternately, a capacitor can be placed in series with REF OUT if a DC multiplying is not required. The lower input bandwidth can be calculated using the following formula:

$$C_{IN} = \frac{1}{(2\pi)(1400)(f_{IN})}$$

For multiplying frequencies above 100kHz, the CTRL IN pin can be driven directly as seen in Figure 23.

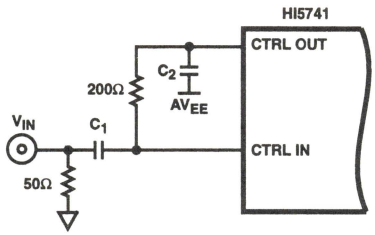


FIGURE 23. HIGH FREQUENCY MULTIPLYING BANDWIDTH CIRCUIT

The nominal input/output relationship is defined as:

$$\Delta I_{OUT} = \frac{\Delta V_{IN}}{80\Omega}$$

In order to prevent the full scale output current from exceeding 20.48mA, the R_{SET} resistor must be adjusted according to the following equation:

$$R_{SET} = \frac{16V_{REF}}{I_{OUT}(\text{Full scale}) - \left(\frac{V_{IN(PEAK)}}{80\Omega}\right)}$$

The circuit in Figure 23 can be tuned to adjust the lower cutoff frequency by adjusting capacitor values. Table 1 below illustrates the relationship:

TABLE 1. CAPACITOR SELECTION

f_{IN}	C_1	C_2
100kHz	0.01µF	1µF
>1MHz	0.001µF	0.1µF

Also, the input signal must be limited to $1V_{P-P}$ to avoid distortion in the DAC output current caused by excessive modulation of the internal current sources.

Outputs

The outputs I_{OUT} and $I_{\overline{OUT}}$ are complementary current outputs. Current is steered to either I_{OUT} or $I_{\overline{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full scale current minus one LSB. The current output can be converted to a voltage by using a load resistor. Both current outputs should have the same load resistor (64Ω typically). By using a 64Ω load on the output, a 50Ω effective output resistance (R_{OUT}) is achieved due to the 227Ω (±15%) parallel resistance seen looking back into the output. This is the nominal value of the R2R ladder of the DAC. The 50Ω output is needed for matching the output with a 50Ω line. The load resistor should be chosen so that the effective output resistance (R_{OUT}) matches the line resistance. The output voltage is:

$V_{OUT} = I_{OUT} \times R_{OUT}$.

I_{OUT} is defined in the reference section. $I_{\overline{OUT}}$ is not trimmed to 14 bits, so it is not recommended that it be used in conjunction with I_{OUT} in a differential-to-single-ended application. The compliance range of the output is from -1.25V to +3.0V, with a $1V_{P-P}$ voltage swing allowed within this range.

TABLE 2. INPUT CODING vs CURRENT OUTPUT

INPUT CODE (D11-D0)	I_{OUT} (mA)	$I_{\overline{OUT}}$ (mA)
1111 1111 1111	-20.48	0
1000 0000 0000	-10.24	-10.24
0000 0000 0000	0	-20.48

Settling Time

The settling time of the HI5741 is measured as the time it takes for the output of the DAC to settle to within a defined error band of its final value during a $^1/_{16}$th (code 0000... to 0001 0000.... or 1111... to 1110 1111...) scale transition. In defining settling time specifications for the HI5741, two levels of accuracy are considered. The accuracy levels defined for the HI5741 are 12 (or 0.024%) and 13 (0.012%) bits.

Glitch

The output glitch of the HI5741 is measured by summing the area under the switching transients after an update of the DAC. Glitch is caused by the time skew between bits of the incoming digital data. Typically, the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). Unequal delay paths through the device can also cause one current source to change before another. In order to minimize this, the Harris HI5741 employes an internal register, just prior to the current sources, which is updated on the clock edge. Lastly, the worst case glitch on traditional D/A converters usually occurs at the major transition (i.e., code 8191 to 8192). However, due to the split architecture of the HI5741, the glitch is moved to the 1023 to 1024 transition (and every subsequent 1024 code transitions thereafter). This split R/2R segmented current source architecture, which decreases the amount of current switching at any one time, makes the glitch practically constant over the entire output range. By making the glitch a constant size over the entire output range this effectively integrates this error out of the end application.

In measuring the output glitch of the HI5741 the output is terminated into a 64Ω load. The glitch is measured at any

one of the current cell carry (code 1023 to 1024 transition or any multiple thereof) throughout the DACs output range.

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 25 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt/seconds (pV/s).

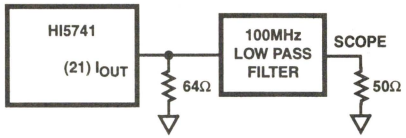


FIGURE 24. GLITCH TEST CIRCUIT

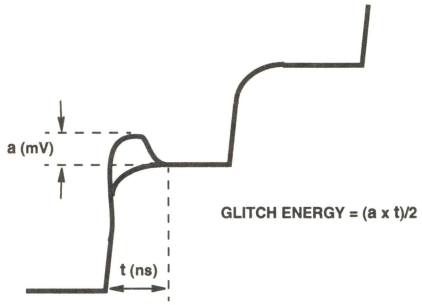


FIGURE 25. MEASURING GLITCH ENERGY

Applications

Bipolar Applications

To convert the output of the HI5741 to a bipolar 4V swing, the following applications circuit is recommended. The reference can only provide 125µA of drive, so it must be buffered to create the bipolar offset current needed to generate the -2V output with all bits 'off'. The output current must be converted to a voltage and then gained up and offset to produce the proper swing. Care must be taken to compensate for the voltage swing and error.

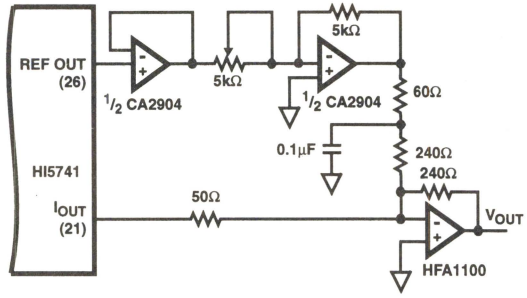


FIGURE 26. BIPOLAR OUTPUT CONFIGURATION

Interfacing to the HSP45106 NCO-16

The HSP45106 is a 16-bit Numerically Controlled Oscillator (NCO). The HSP45106 can be used to generate various modulation schemes for Direct Digital Synthesis (DDS) applications. Figure 27 shows how to interface an HI5741 to the HSP45106.

Definition of Specifications

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL, is the measure of the error in step size between adjacent codes along the converter's transfer curve. Ideally, the step size is 1 LSB from one code to the next, and the deviation from 1 LSB is known as DNL. A DNL specification of greater than -1 LSB guarantees monotonicity.

Feedthru, is the measure of the undesirable switching noise coupled to the output.

Output Voltage Full Scale Settling Time, is the time required from the 50% point on the clock input for a full scale step to settle within an $\pm 1/2$ LSB error band.

Output Voltage Small Scale Settling Time, is the time required from the 50% point on the clock input for a 100mV step to settle within an $1/2$ LSB error band. This is used by applications reconstructing highly correlated signals such as sine waves with more than 5 points per cycle.

Glitch Area, GE, is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a volt • time specification (typically pV-s).

Differential Gain, ΔA_V, is the gain error from an ideal sine wave with a normalized amplitude.

Differential Phase, $\Delta\Phi$, is the phase error from an ideal sine wave.

Signal to Noise Ratio, SNR, is the ratio of a fundamental to the noise floor of the analog output. The first 5 harmonics are ignored, and an output filter of $1/2$ the clock frequency is used to eliminate alias products.

Total Harmonic Distortion, THD, is the ratio of the DAC output fundamental to the RMS sum of the harmonics. The first 5 harmonics are included, and an output filter of $1/2$ the clock frequency is used to eliminate alias products.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at $1/2$ the clock frequency to eliminate noise from clocking alias terms.

Multi-Tone Power Ratio, MTPR, is the amplitude difference from peak amplitude to peak distortion (either harmonic or non-harmonic). An 8 tone pattern is loaded into the D/A. The tone spacing of this pattern (Δf) is created such that tones 1 through 4 and 5 through 8 are spaced equally, with tones 4 and 5 spaced at $2\Delta f$. MTPR is measured as the dynamic range from peak power to peak distortion in the $2\Delta f$ gap.

Intermodulation Distortion, IMD, is the measure of the sum and difference products produced when a two tone input is driven into the D/A. The distortion products created will arise at sum and difference frequencies of the two tones. IMD can be calculated using the following equation:

$$IMD = \frac{20\text{Log (RMS of Sum and Difference Distortion Products)}}{\text{(RMS Amplitude of the Fundamental)}}$$

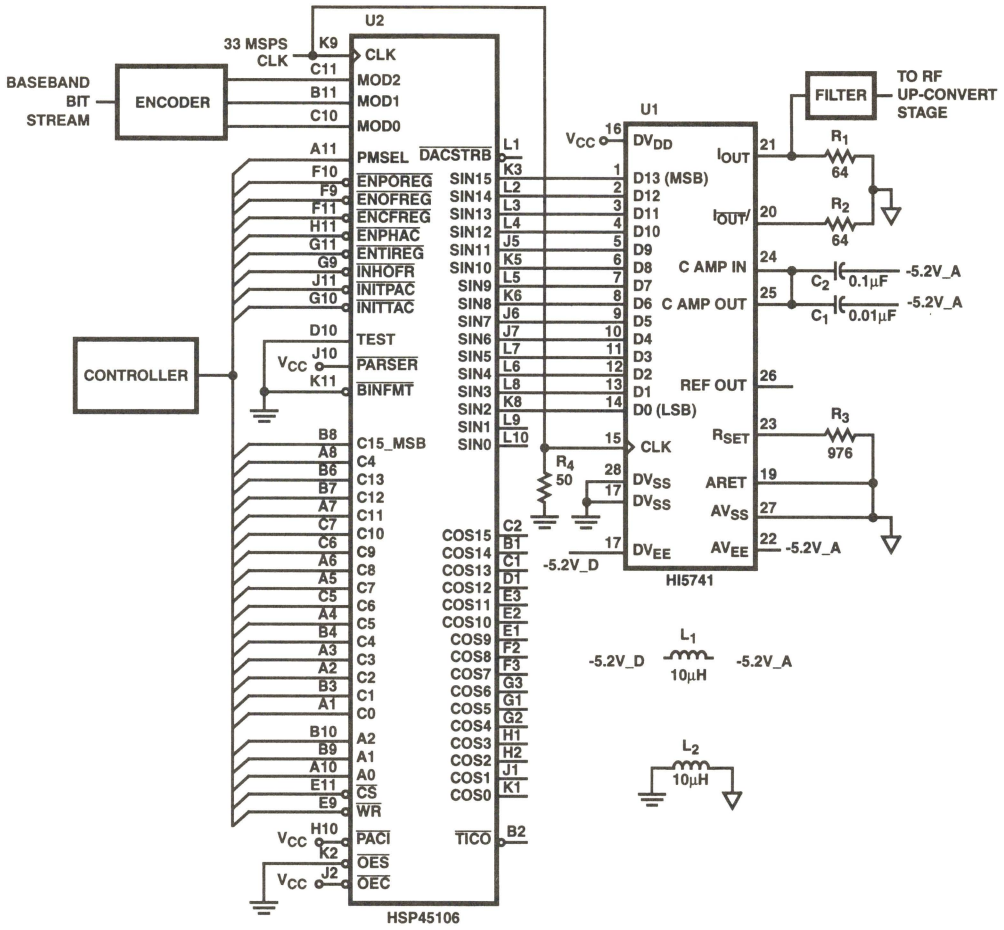


FIGURE 27. PSK MODULATOR USING THE HI5741 AND HSP45106 16-BIT NCO

HARRIS SEMICONDUCTOR

HI5760

PRELIMINARY

August 1997

10-Bit, 125 MSPS, High Speed D/A Converter

Features

- Throughput Rate ..... 125 MSPS
- Low Power ..... 190mW at 5V, 45mW at 3V
- Power Down Mode ..... 25mW at 5V
- Integral Linearity Error ..... ±1 LSB
- Programmable Full Scale Output Current ... 2mA to 20mA
- Fully Differential Current Outputs
- Internal 1.2V Temperature Compensated Bandgap Voltage Reference
- Single +5V or +3V Power Supplies
- Low Glitch Energy
- CMOS Compatible Inputs
- Excellent Spurious Free Dynamic Range

Applications

- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Test Instrumentation
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

Description

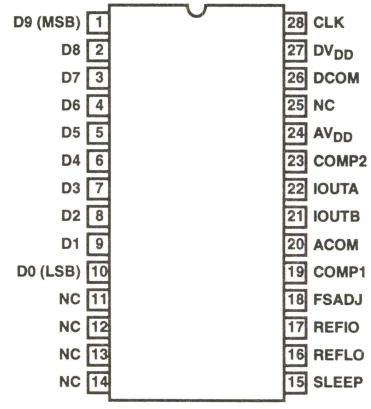
The HI5760 is a 10-bit, 125 MSPS, high speed, low power, D/A converter which is implemented in 0.6µm CMOS process. Operating from a single +5V supply, the converter provides 20mA of full scale output current and includes edge-triggered CMOS input data latches. Low glitch energy and excellent frequency domain performance are achieved using a segmented current source architecture.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5760BIB	-40 to 85	28 Ld SOIC	M28.3

Pinout

HI5760
(SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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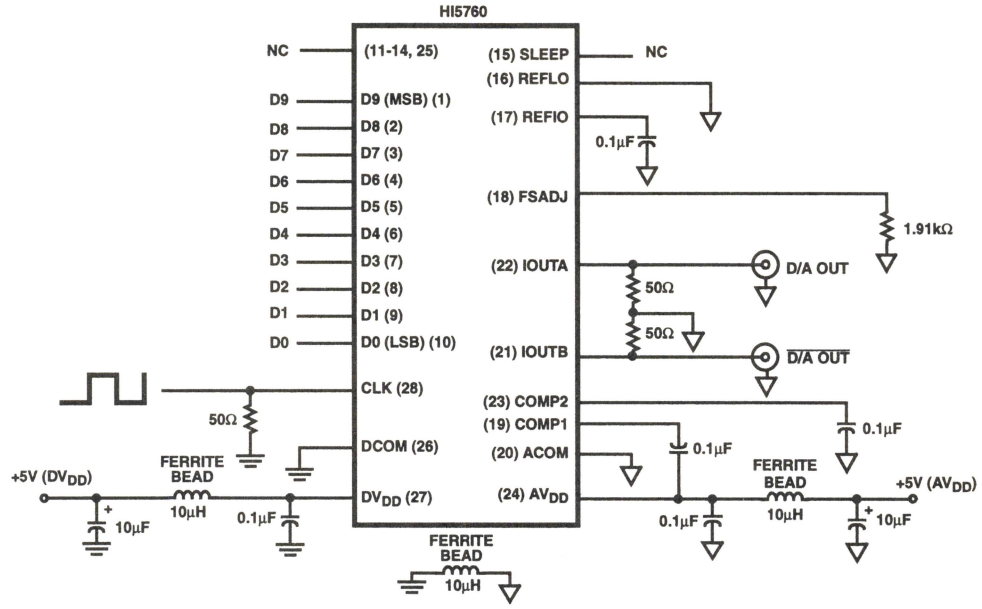
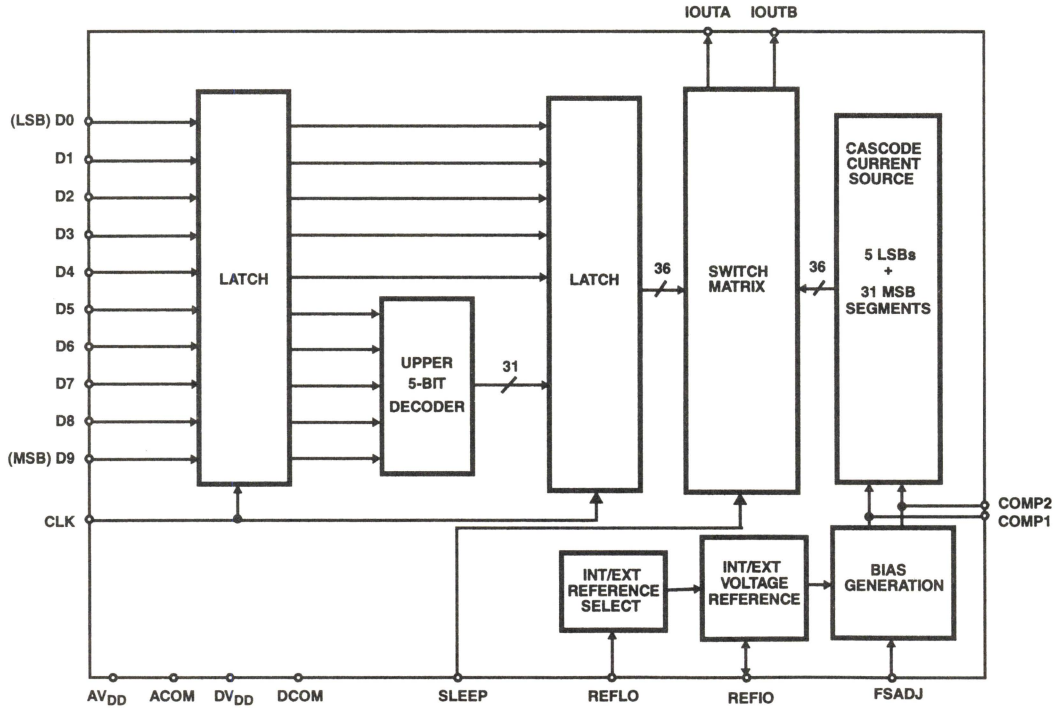
File Number **4320**

Typical Applications Circuit



Functional Block Diagram



Absolute Maximum Ratings

Digital Supply Voltage DV_{DD} to DCOM . . . . . +5.5V
Analog Supply Voltage AV_{DD} to ACOM . . . . . +5.5V
Grounds, ACOM TO DCOM . . . . . -0.3V To + 0.3V
Digital Input Voltages (D9-D0, CLK, SLEEP) . . . . . DV_{DD} + 0.3V
Internal Reference Output Current . . . . . ±50µA
Reference Input Voltage Range . . . . . +0.1V to +1.25V
Analog Output Current (I_{OUT}) 20mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}(°C/W)
SOIC Package	70

Maximum Power Dissipation
HI5760 . . . . . TBD
Maximum Junction Temperature
HI5760 . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{DD} = +5V, DV_{DD} = +5V, V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = 25°C for All Typical Values

PARAMETER	TEST CONDITIONS	HI5760BIB T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	"Best Fit" Straight Line	-	±1	-	LSB
Differential Linearity Error, DNL		-1	±0.5	+1	LSB
Offset Error, I_{OS}		-	±0.01	-	% FSR
Full Scale Gain Error, FSE	With Internal Reference (Note 2)	-	±2	-	% FSR
	Without Internal Reference (Note 2)	-	±1	-	% FSR
Offset Drift Coefficient	(Note 3)	-	TBD	-	ppm of FSR/°C
Full Scale Output Current, I_{FS}		2	-	20	mA
Output Voltage Compliance Range	(Note 3)	-0.3	-	1.25	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	(Note 3)	125.0	-	-	MHz
Output Voltage Full Scale Step Settling Time, $t_{SETT\ FS}$	To ±0.5 LSB Error Band, R_L = 50Ω (Note 3)	-	TBD	-	ns
Output Voltage Small Step Settling Time, $t_{SETT\ SM}$	100mV Step To ±0.5 LSB Error Band, R_L = 50Ω (Note 3)	-	TBD	-	ns
Singlet Glitch Area, GE (Peak Glitch)	R_L = 50Ω (Note 3)	-	TBD	-	pV•s
Doublet Glitch Area, (Net Glitch)		-	TBD	-	pV•s
Output Slew Rate	R_L = 50Ω	-	TBD	-	V/µs
Output Rise Time	(Note 3)	-	TBD	-	ns
Output Fall Time	(Note 3)	-	TBD	-	ns
Output Noise	IOUTFS = 20mA (Note 3)	-	TBD	-	PA/√Hz
	IOUTFS = 2mA (Note 3)	-	TBD	-	PA/√Hz

Electrical Specifications AV_{DD} = +5V, DV_{DD} = +5V, V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = 25°C for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	HI5760BIB T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
Spurious Free Dynamic Range, SFDR to Nyquist	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, 2MHz Span (Notes 3, 4)	-	TBD	-	dBc
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz, 2MHz Span (Notes 3, 4)	-	TBD	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, 50MHz Span (Notes 3, 4)	-	TBD	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz, 50MHz Span (Notes 3, 4)	-	TBD	-	dBc
Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, 2MHz Span (Notes 3, 4)	-	TBD	-	dBc
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz, 2MHz Span (Notes 3, 4)	-	TBD	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, 2MHz Span (Notes 3, 4)	-	TBD	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz, 2MHz Span (Notes 3, 4)	-	TBD	-	dBc
Signal to Noise Ratio (SNR) to Nyquist (Ignoring the First 5 Harmonics)	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 4)	-	TBD	-	dB
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz (Notes 3, 4)	-	TBD	-	dB
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 4)	-	TBD	-	dB
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz (Notes 3, 4)	-	TBD	-	dB
Signal to Noise Ratio + Distortion (SINAD) to Nyquist	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 4)	-	TBD	-	dB
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz (Notes 3, 4)	-	TBD	-	dB
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 4)	-	TBD	-	dB
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz (Notes 3, 4)	-	TBD	-	dB
Total Harmonic Distortion (THD) to Nyquist	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 4)	-	TBD	-	dBc
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz (Notes 3, 4)	-	TBD	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 4)	-	TBD	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz (Notes 3, 4)	-	TBD	-	dBc
Intermodulation Distortion (IMD) to Nyquist	f_{CLK} = 125 MSPS, f_{OUT1} = 800kHz, f_{OUT2} = 900kHz (Notes 3, 4)	-	TBD	-	dB
	f_{CLK} = 100 MSPS, f_{OUT1} = 800kHz, f_{OUT2} = 900kHz (Notes 3, 4)	-	TBD	-	dB

Electrical Specifications AV_{DD} = +5V, DV_{DD} = +5V, V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = 25°C for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	HI5760BIB T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
VOLTAGE REFERENCE					
Internal Reference Voltage, V_{REF}		-	1.2	-	V
Internal Reference Voltage Drift	(Note 3)	-	TBD	-	µV/°C
Internal Reference Output Current Sink/Source Capability		-	±50	-	µA
Reference Input Impedance	(Note 3)	-	1	-	MΩ
Reference Input Multiplying Bandwidth	(Note 3)	-	TBD	-	MHz
DIGITAL INPUTS D9-D0, CLK, INVERT					
Input Logic High Voltage with 5V Supply, V_{IH}		TBD	5	-	V
Input Logic High Voltage with 3V Supply, V_{IH}		TBD	3	-	V
Input Logic Low Voltage with 5V Supply, V_{IL}		-	0	TBD	V
Input Logic Low Voltage with 3V Supply, V_{IL}			0	TBD	V
Input Logic Current, I_{IH}		-	TBD	-	µA
Input Logic Current, I_{IL}		-	TBD	-	µA
Digital Input Capacitance, C_{IN}	(Note 3)	-	TBD	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 3 (Note 3)	-	2	-	ns
Data Hold Time, t_{HLD}	See Figure 3 (Note 3)	-	2	-	ns
Propagation Delay Time, t_{PD}	See Figure 3 (Note 3)	-	1	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 3 (Note 3)	-	4	-	ns
POWER SUPPLY CHARACTERISITICS					
Analog Supply Current (I_{AVDD})	(Note 3)	-	25	-	mA
Digital Supply Current (I_{DVDD})	(Note 3)	-	3	-	mA
Supply Current (I_{AVDD}) Sleep Mode	(Note 3)	-	5	-	mA
Power Dissipation	(5V, IOUTFS = 20mA)	-	190	-	mW
	(3V, IOUTFS = 2mA)	-	45	-	mW
Power Supply Rejection Ratio	AV_{DD}	-	TBD	-	% FSR/V
	DV_{DD}	-	TBD	-	% FSR/V

NOTES:

2. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 625µA). Ideally the ratio should be 32.
3. Parameter guaranteed by design or characterization and not production tested.
4. Spectral measurements made without external filtering.

Timing Diagrams

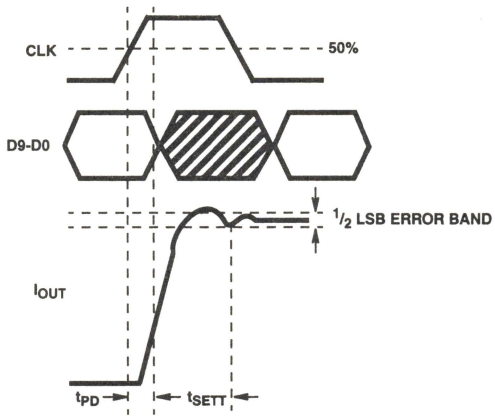


FIGURE 1. FULL SCALE SETTLING TIME DIAGRAM

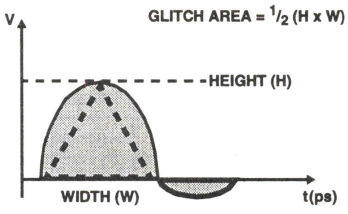


FIGURE 2. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

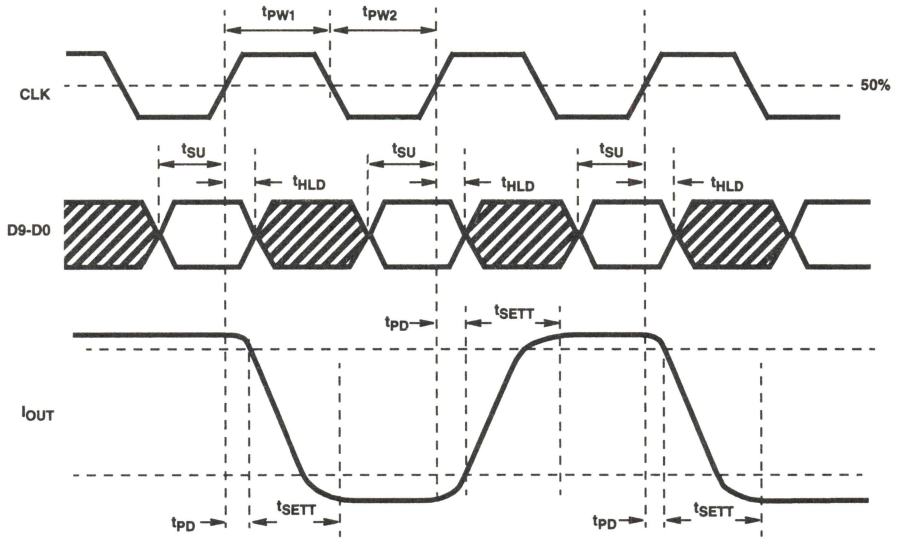


FIGURE 3. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Pin Descriptions

PIN NO.	PIN NAME	PIN DESCRIPTION
1-10	D0 (LSB) Through D9 (MSB)	Digital Data Bit 0, the Least Significant Bit through Digital Data Bit 9, the Most Significant Bit.
11-14	NC	No Connect.
15	SLEEP	Control Pin for Power-Down mode. Can be put into sleep mode with active high or normal mode by leaving unterminated due to active pull-down circuit.
16	REFLO	Connect to analog ground to enable internal 1.2V reference or connect to AV_{DD} to disable.
17	REFIO	Reference input if internal reference is disabled and reference output if internal reference is enabled.
18	FSADJ	Use a resistor to ground to adjust full scale output current.
19	COMP1	For use in reducing bandwidth/noise. Recommended: connect 0.1µF to AV_{DD}.
20	ACOM	Analog Ground.
21	IOUTB	The complimentary current output of the device. Bits set to all 0s gives full scale current.
22	IOUTA	Current output of the device. Bits set to all 1s gives full scale current.
23	COMP2	Internal bias node for switch driver. Connect to ACOM with 0.1µF capacitor.
24	AV_{DD}	Analog Supply (+2.7V to +5.5V).
25	NC	No Connect.
26	DCOM	Digital Ground.
27	DV_{DD}	Supply voltage for digital circuitry.
28	CLK	Input for clock. Positive edge of clock latches data.

Definition of Specifications

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Feedthru, is the measure of the undesirable switching noise coupled to the output.

Output Voltage Full Scale Settling Time, is the time required from the 50% point on the clock input for a full scale step to settle within an $^1/_2$ LSB error band.

Output Voltage Small Scale Settling Time, is the time required from the 50% point on the clock input for a 100mV step to settle within an $^1/_2$ LSB error band. This is used by applications reconstructing highly correlated signals such as sine waves with more than 5 points per cycle.

Glitch Area, GE, is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a Volt-Time specification.

Differential Gain, ΔA_V, is the gain error from an ideal sine wave with a normalized amplitude.

Differential Phase, $\Delta\Phi$, is the phase error from and ideal sine wave.

Signal to Noise Ratio, SNR, is the ratio of a fundamental to the noise floor of the analog output. The first 5 harmonics are ignored, and an output filter of $^1/_2$ the clock frequency is used to eliminate alias products.

Total Harmonic Distortion, THD, is the ratio of the DAC output fundamental to the RMS sum of the harmonics. The first 5 harmonics are included, and an output filter of $^1/_2$ the clock frequency is used to eliminate alias products.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at $^1/_2$ the clock frequency to eliminate noise from clocking alias terms.

Intermodulation Distortion, IMD is the measure of the sum and difference products produced when a two tone input is driven into the D/A. The distortion products created will arise at sum and difference frequencies of the two tones. IMD is:

$$IMD = \frac{20\log\ (\text{RMS of sum and difference distortion products})}{(\text{RMS amplitude of the fundamental})}.$$

HARRIS SEMICONDUCTOR

HI5780

10-Bit, 80 MSPS, High Speed, Low Power D/A Converter

August 1997

Features

- Throughput Rate ..... 80 MSPS
- Low Power 150mW
- Differential Linearity Error ..... ±0.5 LSB
- TTL/CMOS Compatible Inputs
- Built in Bandgap Voltage Reference
- Power Down and Blanking Control Pins
- Direct Replacement for Sony CXD2306

Applications

- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Test Equipment
- High Resolution Imaging and Graphics Systems
- Arbitrary Waveform Generators

Description

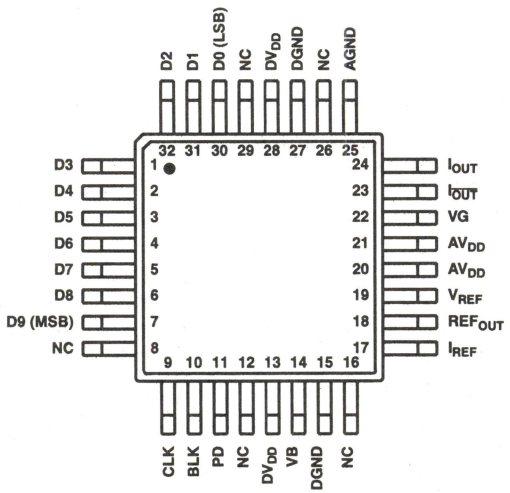
The HI5780 is a 10-bit, 80 MSPS, high speed, low power CMOS D/A converter. The converter incorporates a 10-bit input data register with current outputs. The HI5780 includes a power down feature that reduces power consumption and a blanking control. The on-chip bandgap reference can be used to set the output current range of the D/A.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5780JCQ	-20 to 75	32 Ld MQFP	Q32.7x7-S
HI5780-EV	25	Evaluation Kit	

Pinout

HI5780
(MQFP)



10 D/A CONVERTERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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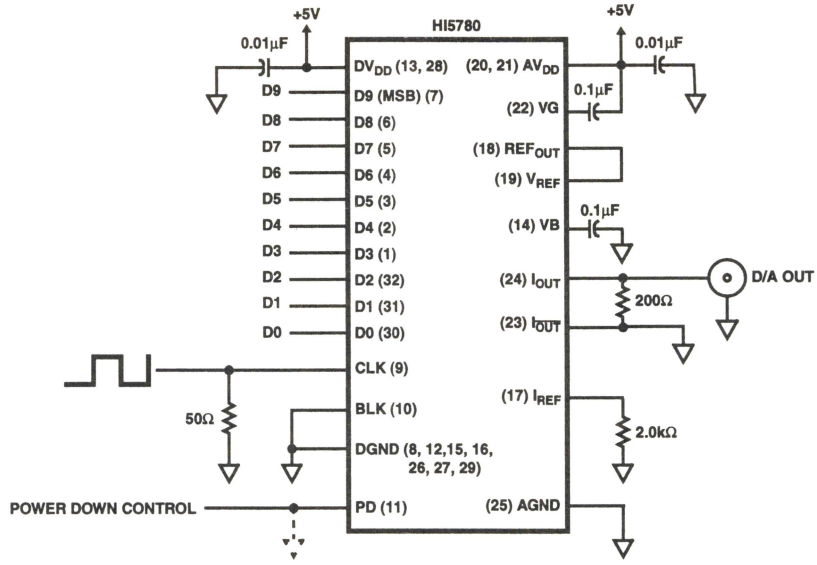
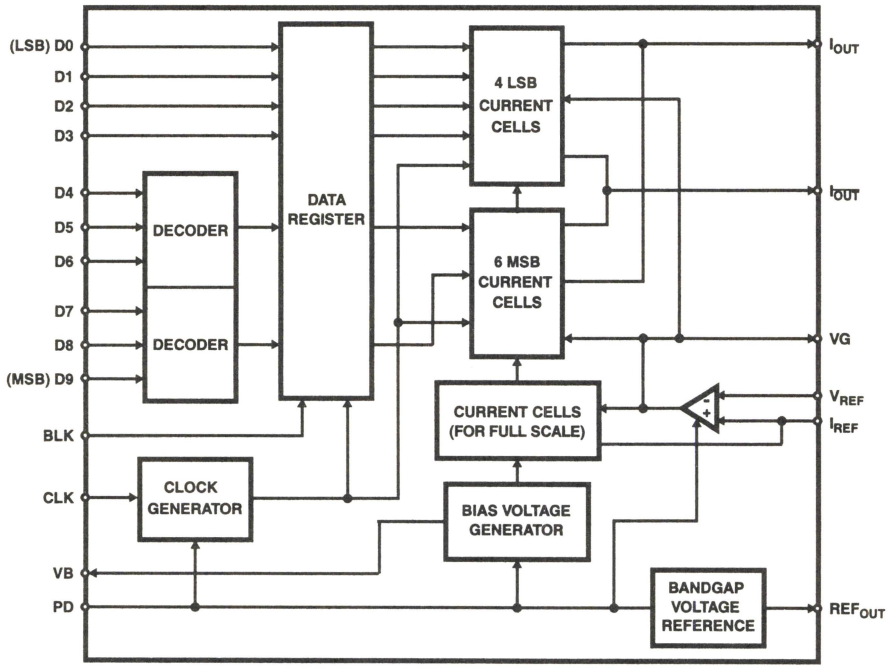
File Number 4024.4

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage V_{DD} to DGND . . . . . +7.0V
Digital Input Voltages (D9-D0, CLK, BLANK, PD) . . . . V_{DD} to -0.5V
Internal Reference Output Current . . . . . ±2.5mA
Reference Input Voltage Range (V_{REF}) . . . . . V_{DD} to -0.5 V
Analog Output Current (I_{OUT}) 15mA

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (^{o}C/W)
MQFP Package 122
Maximum Junction Temperature (Plastic Package)
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(MQFP - Lead Tips Only)

Operating Conditions

Temperature Range, HI5780BIx . . . . . -20^{o}C to 75^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{DD}, DV_{DD} = 5.00V, V_{REF} = 2.0V, f_{CLK} = 80 MSPS, R_{LOAD} = 200Ω, R_{REF} = 3.3kΩ, T_A = 25^{o}C

PARAMETER	TEST CONDITIONS	HI5780JCQ			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	(Notes 4, 5) ("Best Fit" Straight Line)	-2.0	1.25	2.0	LSB
Differential Linearity Error, DNL	(Notes 4, 5)	-0.5	0.25	0.5	LSB
Offset Error, I_{OS}	(Notes 4, 5)	-	-	5	µA
Full Scale Output Current, I_{FS}	(Note 4)	9.0	9.6	10	mA
Full Scale Drift Coefficient, I_{DRIFT}	(Note 2)	-	0.26	-	mV/^{o}C
Output Voltage Compliance Range	(Note 3), 10-Bit Accuracy	1.8	1.92	2.0	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	(Note 3)	80.0	-	-	MSPS
Output Voltage Full Scale Step Settling Time, $t_{SETT\ FS}$	To ±0.5 LSB Error Band R_L = 75Ω, 10-Bit Accuracy (Note 3)	-	6.0	-	ns
Singlet Glitch Area, GE (Peak)	R_{LOAD} = 75Ω, V_{OUT} = 1.0V_{P-P} (Note 3)	-	40	-	pV-s
Differential Gain, DG	(Note 4)	-	2.5	-	%
Differential Phase, DP	(Note 4)	-	1.3	-	Degrees
Spurious Free Dynamic Range, SFDR to Nyquist	f_{CLK} = 40 MSPS, f_{OUT} = 2.02MHz, 20MHz Span (Note 3)	-	48.5	-	dBc
	f_{CLK} = 80 MSPS, f_{OUT} = 2.02MHz, 40MHz Span (Note 3)	-	47.5	-	dBc
	f_{CLK} = 40 MSPS, f_{OUT} = 10MHz, 20MHz Span (Note 3)	-	40.75	-	dBc
	f_{CLK} = 80 MSPS, f_{OUT} = 20MHz, 40MHz Span (Note 3)	-	38.5	-	dBc
Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 40 MSPS, f_{OUT} = 2.02MHz, 2MHz Span (Note 3)	-	75.0	-	dBc
	f_{CLK} = 80 MSPS, f_{OUT} = 2.02MHz, 2MHz Span (Note 3)	-	73.5	-	dBc
	f_{CLK} = 40 MSPS, f_{OUT} = 10MHz, 2MHz Span (Note 3)	-	56.5	-	dBc
	f_{CLK} = 80 MSPS, f_{OUT} = 20MHz, 2MHz Span (Note 3)	-	49.0	-	dBc
REFERENCE					
Internal Reference Voltage, REF_{OUT}	(Notes 4, 5)	1.0	1.25	1.3	V
Internal Reference Voltage Drift	(Note 3)	-	0.34	-	mV/^{o}C
Reference Input Voltage Range, V_{REF}	(Note 3)	0.5	-	2.0	V

Electrical Specifications AV_{DD}, DV_{DD} = 5.00V, V_{REF} = 2.0V, f_{CLK} = 80 MSPS, R_{LOAD} = 200Ω, R_{REF} = 3.3kΩ, T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS	HI5780JCQ			UNITS
		MIN	TYP	MAX	
DIGITAL INPUTS (D9-D0, CLK, BLK, PD)					
Input Logic High Voltage, V_{IH}	(Note 5)	2.15	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 5)	-	-	0.85	V
Input Logic Current, I_{IH}	(Note 5)	-	-	5	µA
Input Logic Current, I_{IL}	(Note 5)	-5	-	-	µA
Digital Input Capacitance, C_{IN}	(Note 3)	-	3.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	(See Figure 1, Note 3)	5.0	3.0	-	ns
Data Hold Time, t_{HLD}	(See Figure 1, Note 3)	1.0	0	-	ns
Propagation Delay Time, t_{PD}	(See Figure 1, Note 3)	-	8.0	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	(See Figure 1, Note 3)	6.25	-	-	ns
POWER SUPPLY CHARACTERISTICS					
IV_{DD}	(Notes 4, 5)	-	20	30	mA
Power Dissipation	(Note 5)	-	100	150	mW
Sleep Mode Power Consumption	PD = 1 (Note 4)	-	1.25	-	mW

NOTES:

2. R_{LOAD} is connected to I_{OUT} (pin 24) and R_{REF} is connected to I_{REF} (pin 17).
3. Parameter guaranteed by design or characterization and not production tested.
4. Typical values are test results at T_A = 25°C.
5. All devices are 100% tested at 25°C.

Timing Diagrams

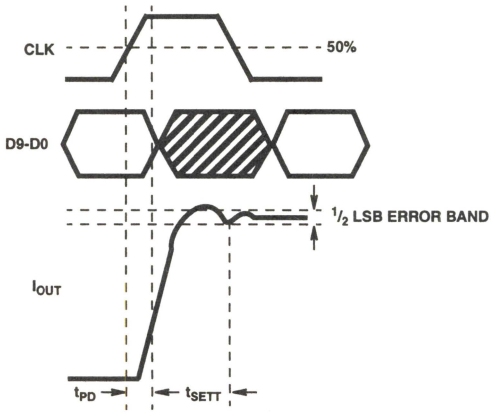


FIGURE 1. FULL SCALE SETTLING TIME DIAGRAM

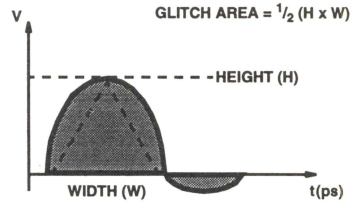


FIGURE 2. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

Timing Diagrams (Continued)

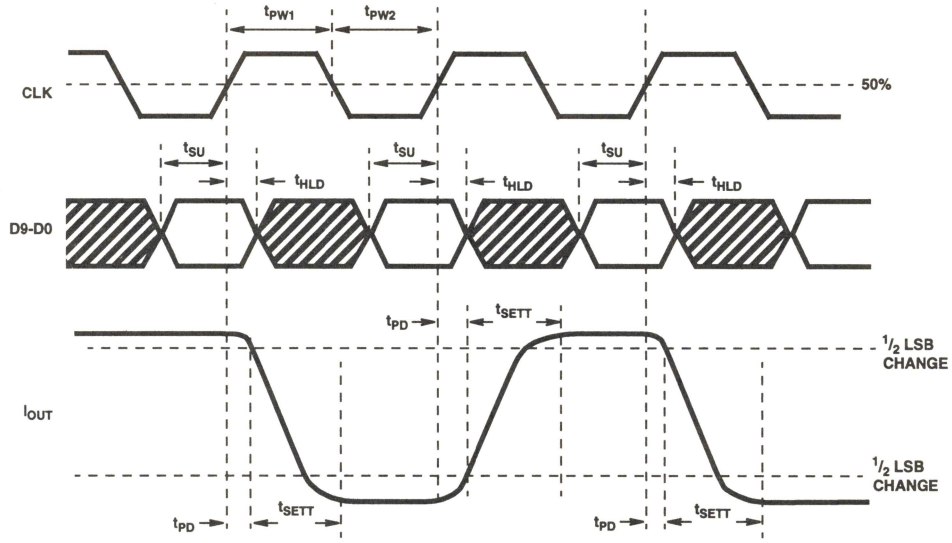


FIGURE 3. PROPAGATION DELAY, SETUP TIME AND MINIMUM PULSE WIDTH DIAGRAM

Pin Descriptions

PIN	PIN NAME	DESCRIPTION
1-7, 30-32	D0 (LSB) thru D9 (MSB)	Digital Data Bit 0, the least significant bit thru digital data Bit 9, the most significant bit.
9	CLK	Data Clock Pin 100kHz to 80MHz.
13, 28	DV_{DD}	Digital Logic Supply +5V.
15, 27	DGND	Digital Ground.
20, 21	AV_{DD}	Analog Supply +5V.
23	BLK	Output Blanking pin. When set ('1') this pin zeros the I_{OUT} pin.
25	AGND	Analog Ground Supply Current Return pin.
11	PD	Power Down Mode pin. This pin when set ('1') places the HI5780 in lower power mode and zeros the output. Power consumption is reduced.
24	I_{OUT}	Current Output pin.
23	I_{OUT}	Complementary Current Output pin.
18	REF_{OUT}	Bandgap Reference Voltage Output.
17	I_{REF}	Reference Current setting resistor connected from here to Ground.
19	V_{REF}	Reference Voltage Input pin.
14	VB	Bias Voltage Generator Bypass Capacitor connected from here to Ground.
22	VG	Reference Amplifier Bypass Capacitor connected from here to AV_{DD}.

Typical Performance Curves

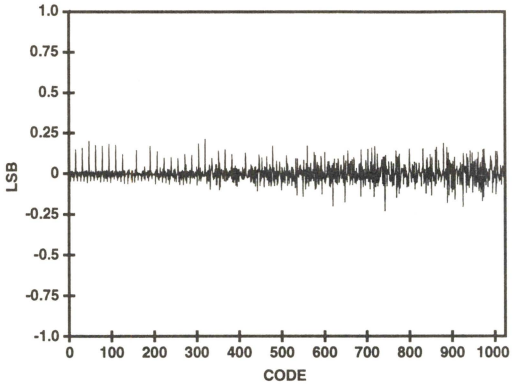


FIGURE 4. DIFFERENTIAL LINEARITY

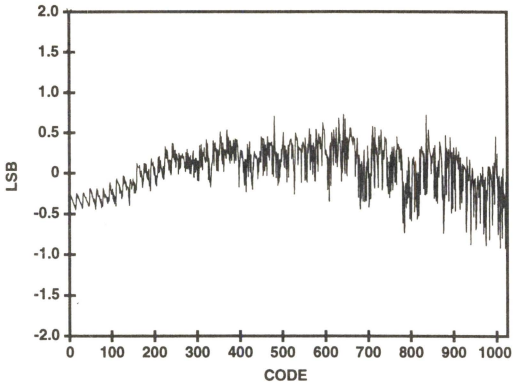


FIGURE 5. INTEGRAL LINEARITY (BEST FIT - STRAIGHT LINE)

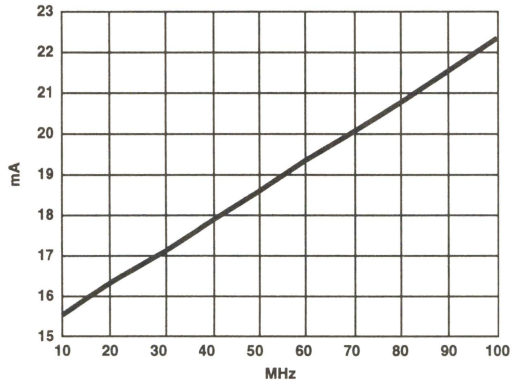


FIGURE 6. POWER SUPPLY CURRENT vs CLOCK FREQUENCY

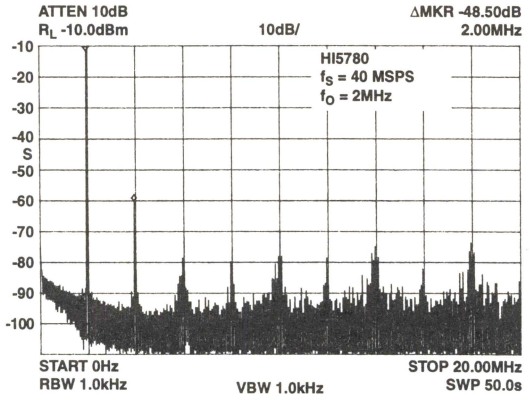


FIGURE 7. SPURIOUS FREE DYNAMIC RANGE TO NYQUIST

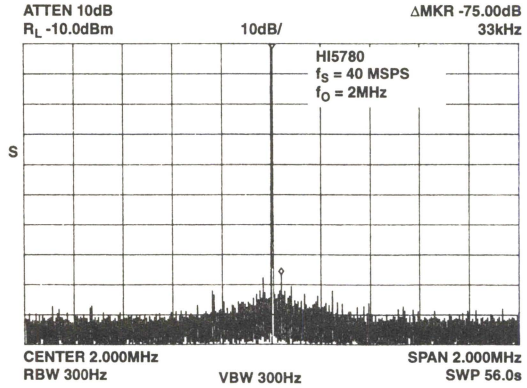


FIGURE 8. SPURIOUS FREE DYNAMIC RANGE WITHIN A WINDOW

Detailed Description

The HI5780 is a 10-bit, current out D/A converter. The DAC can convert at 80 MSPS and runs on +5V supplies. The HI5780 achieves its low power and high speed performance from an advanced CMOS process. The HI5780 consumes 150mW (Maximum) and has a power down mode that only consumes 1.25mW when in sleep mode. The HI5780 is an excellent converter to be used for communications applications and high performance video systems.

Digital Inputs

The HI5780 is a TTL/CMOS-compatible D/A. Data is latched by a 10-bit latch. Once latched data inputs D0 (LSB) thru D9 (MSB) are decoded to the internal current cells; the internal latch and switching current source controls are implemented in CMOS technology to maintain high switching speeds and low power consumption.

Clocks and Termination

The internal 10-bit register is updated on the rising edge of the clock. Since the HI5780 clock rate can run to 80MHz, to minimize reflections and clock noise into the part, proper termination should be used. In PCB layout clock runs should be kept short and have a minimum of loads. To guarantee consistent results from board to board, controlled impedance PCBs should be used with a characteristic line impedance, Z_O, of 50Ω.

To terminate the clock line a shunt terminator to ground is the most effective type at a 80 MSPS clock rate. A typical value for termination can be determined by the equation:

$R_T = Z_O$,

for the termination resistor. For a controlled impedance board with a Z_O of 50Ω, the R_T = 50Ω. Shunt termination is best used at the receiving end of the transmission line or as close to the HI5780 CLK pin as possible.

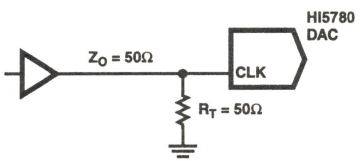


FIGURE 9. AC TERMINATION OF THE HI5780 CLOCK LINE

Rise and Fall times and propagation delay of the line will be affected by the Shunt Terminator. The terminator can be connected to DGND.

Noise Reduction

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1µF and 0.01µF ceramic capacitors placed as close to the body of the HI5780 as possible on the analog (AV_{DD}) and digital (DV_{DD}) supplies. The analog and digital ground returns should be connected together back at the device to ensure proper operation on power up.

Reference

The internal reference in the HI5780 is a 1.25V (typical) bandgap voltage reference. The internal reference is buffered by an amplifier to provide adequate drive for the current cells. Reference Out (REF_{OUT}) is connected to the V_{REF} pin. The Full Scale Output Current is controlled by the resistor connected to I_{REF}. The full scale output voltage, is set by the following equation:

$V_{OUT}(\text{Full Scale}) = V_{REF} \times 16(R_{LOAD}/R_{REF})$.

Applications

Voltage Conversion of the Output

To convert the output current of the D/A converter to a voltage, an amplifier should be used as shown in Figure 5. The DAC needs a 50Ω termination resistor on the I_{OUT} pin to ensure proper settling. The HFA1110 has an internal feedback resistor to compensate for high frequency operation.

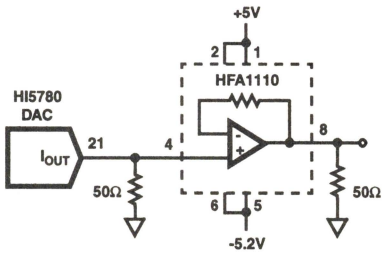


FIGURE 10. HIGH SPEED CURRENT TO VOLTAGE CONVERSION

Definition of Specifications

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Output Voltage Full Scale Settling Time, is the time required from the 50% point on the clock input for a full scale step to settle within an $^1/_2$ LSB error band.

Glitch Area, GE, is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a Volt-Time specification.

Differential Gain, ΔA_V, is the gain error from an ideal sine wave with a normalized amplitude.

Differential Phase, $\Delta\Phi$, is the phase error from and ideal sine wave.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at $^1/_2$ the clock frequency to eliminate noise from clocking alias terms.

DATA ACQUISITION 11

MULTIPLEXERS

		PAGE
Selection Guide		11-2
Multiplexer Data Sheets		
DG406, DG407	Single 16-Channel/Differential 8-Channel, CMOS Analog Multiplexers	11-13
DG408, DG409	Single 8-Channel/Differential 4-Channel, CMOS Analog Multiplexers	11-25
DG506A, DG507A, DG508A, DG509A	CMOS Analog Multiplexers	11-39
HI-1818A, HI-1828A	Low Resistance, Single 8-Channel, and Differential 4-Channel, CMOS Analog Multiplexers	11-52
HI-506, HI-507, HI-508, HI-509	Single 16 and 8/Differential 8-Channel and 4-Channel CMOS Analog Multiplexers	11-54
HI-506A, HI-507A HI-508A, HI-509A	16-Channel, 8-Channel, Differential 8-Channel and Differential 4-Channel, CMOS Analog MUXs with Active Overvoltage Protection	11-70
HI-516	16-Channel/Differential 8-Channel, CMOS High Speed Analog Multiplexer	11-84
HI-518	8-Channel/Differential 4-Channel, CMOS High Speed Analog Multiplexer	11-91
HI-524	4-Channel Wideband and Video Multiplexer	11-98
HI-539	Monolithic, 4-Channel, Low-Level, Differential Multiplexer	11-104
HI-546, HI-547, HI-548, HI-549	Single 16 and 8, Differential 8-Channel and 4-Channel CMOS Analog MUXs with Active Overvoltage Protection	11-114

SINGLE 1 x 8 MULTIPLEXER (FIGURES 1, 2)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
DG408	DJ, DY, EJ, EY	Y	40	2.4	0.8	44V CMOS-JI		115	105	Low $r_{DS(ON)}$
DG508A	AK, BK, BY, CJ, CK, CY	Y	450	2.4	0.8	44V CMOS-DI	0.3	250	250	
HI1-0508	-2, -4, -5, -7, -8, -9	Y	400	2.4	0.8	44V CMOS-DI	0.3	250	250	
HI3-0508	-5									
HI4P0508	-5									
HI9P0508	-5, -9									
HI4-0508/883		Y								
HI1-0508A	-2, -5, -7, -8		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Over-Voltage Protection. See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0508A	-5									
HI1-0518	-2, -5, -8, -9		750	2.4	0.8	33V CMOS-DI	0.015	120	140	Programmable 1 of 8, Differential 2 of 4, Figure 2, See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0518	-5, -9									
HI4-0518	-8									
HI4P0518	-5, -9									
HI9P0518	-5, -9									
HI1-0548	-2, -4, -5	Y	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Over-Voltage Protection. 7% $r_{DS(ON)}$ Matching. See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0548	-5, -9									
HI4P0548	-5									
HI9P0548	-5, -9									
HI4-0548/883		Y								
HI1-1818A	-2, -5, -7	Y	400	4.0	0.4	40V CMOS-DI	0.1	300	300	
HI3-1818A	-5									
HI4P1818A	-5									

SINGLE 1 x 16 MULTIPLEXER (FIGURE 3)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
DG406	DJ, DY, EJ, EY	Y	50	2.4	0.8	44V CMOS-JI	0.01	150	70	Low $r_{DS(ON)}$, Low Leakage
DG506A	AK, BK, BY, CJ, CK, CY	Y	450	2.4	0.8	44V CMOS-DI	0.3	250	250	
HI1-0506	-2, -4, -5, -7, -8, -9	Y	400	2.4	0.8	44V CMOS-DI	0.3	250	250	
HI3-0506	-5									
HI4P0506	-5									
HI9P0506	-5, -9									
HI4-0506/883		Y								
HI1-0506A	-2, -5, -7, -8		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Over-Voltage Protection. See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0506A	-5									
HI1-0516	-2, -5, -8	Y	750	2.4	0.8	33V CMOS-DI	0.03	120	140	Programmable, 1 of 16, Differential 2 of 8. See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0516	-5									
HI4-0516	-8	Y								
HI4P0516	-5									
HI9P0516	-5, -9									
HI1-0546	-2, -4, -5, -7	Y	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Over-Voltage Protection. See Over-Voltage Protected Multiplexers Table, (Note 5) 7% $r_{DS(ON)}$ Matching
HI3-0546	-5, -9									
HI4P0546	-5									
HI9P0546	-5, -9									
HI4-0546/883		Y								

DUAL 1 x 4 MULTIPLEXER (FIGURE 4)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
DG409	DJ, DY, EJ, EY	Y	40	2.4	0.8	44V CMOS-JI		115	105	Low $r_{DS(ON)}$
DG509A	AK, BK, BY, CJ, CK, CY	Y	400	2.4	0.8	44V CMOS-JI	0.3	250	250	

DUAL 1 x 4 MULTIPLEXER (FIGURE 4) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
HI1-0509	-2, -4, -5, -7, -8, -9	Y	400	2.4	0.8	44V CMOS-DI	0.3	250	250	
HI3-0509	-5									
HI4P0509	-5									
HI9P0509	-5, -9									
HI4-0509/883		Y								
HI1-0509A	-2, -5, -7, -8		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Over-Voltage Protection, See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0509A	-5									
HI1-0518	-2, -5, -8, -9		750	2.4	0.8	33V CMOS-DI	0.015	120	140	Programmable 1 of 8, Differential 2 of 4, (Figure 2), See Programmable Configuration Table
HI3-0518	-5, -9									
HI4-0518	-8									
HI4P0518	-5, -9									
HI9P0518	-5, -9									
HI1-0539	-2, -4, -5, -8		850	4.0	0.8	33V CMOS-DI	0.001	250	160	Low Level Signals, 3% Max $r_{DS(ON)}$ Matching
HI3-0539	-5									
HI4P0539	-5									
HI1-0549	-2, -4, -5	Y	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	70V Active Over-Voltage Protection, 7% $r_{DS(ON)}$ Matching, See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0549	-5, -9									
HI4P0549	-5									
HI9P0549	-5, -9									
HI4-0549/883		Y								
HI1-1828A	-2, -5, -7	Y	400	4.0	0.4	40V CMOS-DI	125 Max	300	300	
HI3-1828A	-5									
HI4P1828A	-5, -8									
HI4-1828A/883		Y								

DUAL 1 x 8 MULTIPLEXER (FIGURE 5)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
DG407	DJ, DY, EJ, EY	Y	50	2.4	0.8	44V CMOS-JI	0.01	150	70	Low $r_{DS(ON)}$, Low Leakage
DG507A	AK, BK, BY, CJ, CK, CY	Y	450	2.4	0.8	44V CMOS-JI	0.03	250	250	
HI1-0507	-2, -4, -5, -7, -8, -9	Y	400	2.4	0.8	44V CMOS-DI	0.3	250	250	
HI3-0507	-5									
HI4P0507	-5									
HI9P0507	-5, -9									
HI4-0507/883		Y								
HI1-0507A	-2, -5, -7, -8		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Over-Voltage Protection, See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0507A	-5									
HI1-0516	-2, -5, -8	Y	750	2.4	0.8	33V CMOS-DI	0.03	120	140	Programmable, 1 of 16, Differential 2 of 8, See Over-Voltage Protected Multiplexers Table
HI3-0516	-5									
HI4-0516	-8	Y								
HI4P0516	-5									
HI9P0516	-5, -9									
HI1-0547	-2, -4, -5, -9	Y	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Over-Voltage Protection, 7% $r_{DS(ON)}$ Matching, See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0547	-5, -9									
HI4P0547	-5									
HI9P0547	-5, -9									
HI4-0547/883		Y								

PROGRAMMABLE CONFIGURATION SINGLE (1 OF 16) OR DIFFERENTIAL (2 OF 8) MULTIPLEXER (FIGURE 6)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
HI1-0516	-2, -5, -8	Y	750	2.4	0.8	33V CMOS-DI	0.03	120	140	Programmable, 1 of 16, Differential 2 of 8
HI3-0516	-5									
HI4-0516	-8	Y								
HI4P0516	-5									
HI9P0516	-5, -9									

PROGRAMMABLE CONFIGURATION SINGLE (1 OF 8) OR DIFFERENTIAL (2 OF 4) MULTIPLEXER (FIGURE 7)

(NOTES 2, 3) DEVICE	SUFFIX CODES	(NOTE 1) $r_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
HI1-0518	-2, -5, -8, -9	750	2.4	0.8	33V CMOS-DI	0.015	120	140	Programmable, 1 of 8, Differential 2 of 4
HI3-0518	-5, -9								
HI4-0518	-8								
HI4P0518	-5, -9								

OVER-VOLTAGE PROTECTED MULTIPLEXERS (NOTE 6)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	NO. OF CHANNELS	FEATURES
HI1-0506A	-2, -5, -7		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	1 x 16	
HI3-0506A	-5										
HI4-0506A	-8										
HI1-0507A	-2, -5, -7		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 8	Differential Inputs
HI3-0507A	-5										
HI4-0507A	-8										

OVER-VOLTAGE PROTECTED MULTIPLEXERS (NOTE 6) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	NO. OF CHANNELS	FEATURES
HI1-0508A	-2, -5, -7		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	1 x 8	
HI3-0508A	-5										
HI4-0508A	-8										
HI1-0509A	-2, -5, -7		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 4	Differential Inputs
HI3-0509A	-5										
HI4-0509A	-8										
HI1-0546	-2, -4, -5	Y	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	1 x 16	7% $r_{DS(ON)}$ Matching
HI3-0546	-5										
HI4P0546	-5										
HI9P0546	-5, -9										
HI4-0546/883		Y									
HI1-0547		Y	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 8	7% $r_{DS(ON)}$ Matching Differential Inputs
HI3-0547	-2, -4, -5										
HI4P0547	-5										
HI9P0547	-5, -9										
HI4-0547/883		Y									
HI1-0548	-2, -4, -5	Y	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	1 x 8	7% $r_{DS(ON)}$ Matching
HI3-0548	-5										
HI4P0548	-5										
HI9P0548	-5, -9										
HI4-0548/883		Y									
HI1-0549	-2, -4, -5	Y	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 4	7% $r_{DS(ON)}$ Matching Differential Inputs
HI3-0549	-5										
HI4P0549	-5										
HI9P0549	-5, -9										
HI4-0549/883		Y									

DIFFERENTIAL INPUT MULTIPLEXERS

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	NO. OF CHANNELS	FEATURES
DG507A	AK, BK, BY, CJ, CK, CY	Y	450	2.4	0.8	44V CMOS-JI	0.03	250	250	8	
DG509A	AK, BK, CJ, CK	Y	400	2.4	0.8	44V CMOS-JI	0.3	250	250	4	
HI1-0507	-2, -4, -5, -7, -8, -9	Y	400	2.4	0.8	44V CMOS-DI	0.1	250	250	2 x 8	
HI3-0507	-5										
HI4P0507	-5										
HI9P0507	-5, -9										
HI4-0507/883		Y									
HI1-0507A	-2, -5, -7, -8		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 8	Active Over-Voltage Protection, See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0507A	-5										
HI4-0507A	-8										
HI1-0509	-2, -4, -5, -7, -8, -9	Y	450	2.4	0.8	44V CMOS-DI	0.3	250	250	2 x 4	
HI3-0509	-5										
HI4P0509	-5										
HI9P0509	-5, -9										
HI4-0509/883		Y									
HI1-0509A	-2, -5, -7, -8		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 4	Active Over-Voltage Protection, See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0509A	-5										
HI4-0509A	-8										

DIFFERENTIAL INPUT MULTIPLEXERS (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	NO. OF CHANNELS	FEATURES
HI1-0516	-2, -5, -8	Y	1800	4.0	0.8	33V CMOS-DI	0.1	500	500	1 x 16	7% $r_{DS(ON)}$ Matching
HI3-0516	-5										
HI4-0516	-8	Y									
HI4P0516	-5										
HI9P0516	-5, -9										
HI1-0518	-2, -5, -8, -9		750	2.4	0.8	33V CMOS-DI	0.015	120	140	4	Programmable 1 of 8, Differential 2 of 4, Figure 2, See Programmable Configuration Table
HI3-0518	-5, -9										
HI4-0518	-8										
HI4P0518	-5, -9										
HI9P0518	-5, -9										
HI1-0539	-2, -4, -5, -8		850	4.0	0.8	33V CMOS-DI	0.001	250	160	4	Low Level Signals, 3% Max $r_{DS(ON)}$ Matching
HI3-0539	-5										
HI4P0539	-5										
HI1-0547	-2, -4, -5, -9	Y	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 8	Active Over-Voltage Protection, 7% $r_{DS(ON)}$ Matching See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0547	-5, -9										
HI4P0547	-5										
HI9P0547	-5, -9										
HI4-0547/883		Y									
HI1-0549	-2, -4, -5	Y	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 4	70V Active Over-Voltage Protection, 7% $r_{DS(ON)}$ Matching, See Over-Voltage Protected Multiplexers Table, (Note 5)
HI3-0549	-5, -9										
HI4P0549	-5										
HI9P0549	-5, -9										
HI4-0549/883		Y									

DIFFERENTIAL INPUT MULTIPLEXERS (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	NO. OF CHANNELS	FEATURES
HI1-1828A	-2, -5, -7	Y	400	4.0	0.4	40V CMOS-DI	125 Max	300	300	2 x 4	
HI3-1828A	-5										
HI4-1828A	-8	Y									
HI4P1828A	-5										

NOTES:

1. The $r_{DS(ON)}$ of a CMOS switch varies as a function of supply voltage, analog signal voltage, and temperature. Values shown are maximum (unless noted "Typ" = typical) at 25°C.
   SWITCH "ON" V: Digital Threshold to "CLOSE" a particular switch. (Minimum if greater than "OFF". Maximum if less than "OFF".)
   SWITCH "OFF" V: Digital Threshold to "OPEN" a particular switch. (Minimum if greater than "ON". Maximum if less than "ON".)
   V_{INL}: Digital Threshold to represent a "Low" select signal. (Maximum, voltage levels greater than this value are not guaranteed to produce a "LOW".)
   V_{INH}: Digital Threshold to represent a "HIGH" select signal. (Minimum, voltage levels less than this value are not guaranteed to produce a "HIGH".)
2. Package codes:
   DG Types - SUFFIX:
   A 10 Lead TO-100 J Plastic DIP K CERDIP P SBDIP Y SOIC
   IH Types - Middle SUFFIX Letter:
   J CERDIP P Plastic DIP T TO-100 Can B SOIC HI4P PLCC
   HI Types - PREFIX:
   HI1 Ceramic DIP HI2 Metal Can HI3 Plastic DIP HI4 Ceramic LCC HI9 Flatpack HI9P SOIC
3. Temperature Code Suffix:
   -1: 0° to 200°C
   -2, A, or M: -55°C to 125°C
   -4 or B: -25°C to 85°C
   -5: 0°C to 75°C
   C: 0°C to 70°C
   -7: 0°C to 75°C with Burn-In
   -8: -55°C to 125°C with Burn-In
   -9: -40°C to 85°C
   /883: MIL-STD-883, Class B, -55°C to 125°C with Burn-In
   D: -40°C to 85°C
   E: -40°C to 85°C with Extended Process Flow
   I: Industrial, -25°C or -40°C to 85°C, see data sheet.
4. Double Throw switches have one switch ON and the other switch OFF for each input state. See data sheet.
5. Over-Voltage Protection: Analog Inputs can withstand up to 70V peak to peak levels, with no channel interaction.
6. Fault Protection: All channels are OFF when supply power is off, up to 25V inputs. Any channel turns OFF when input exceeds supply rail.

MULTIPLEXER CONFIGURATIONS

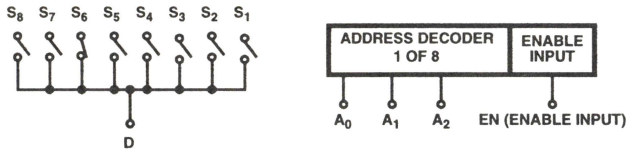


FIGURE 1. 1 x 8 MULTIPLEXER

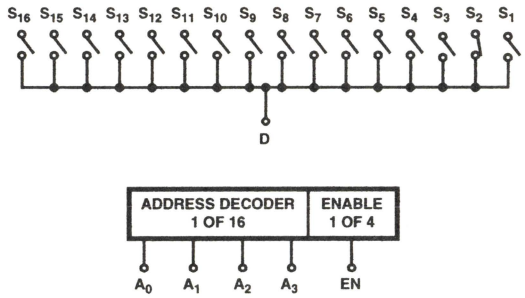


FIGURE 3. 1 x 16 MULTIPLEXER

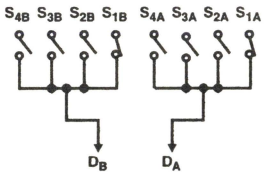
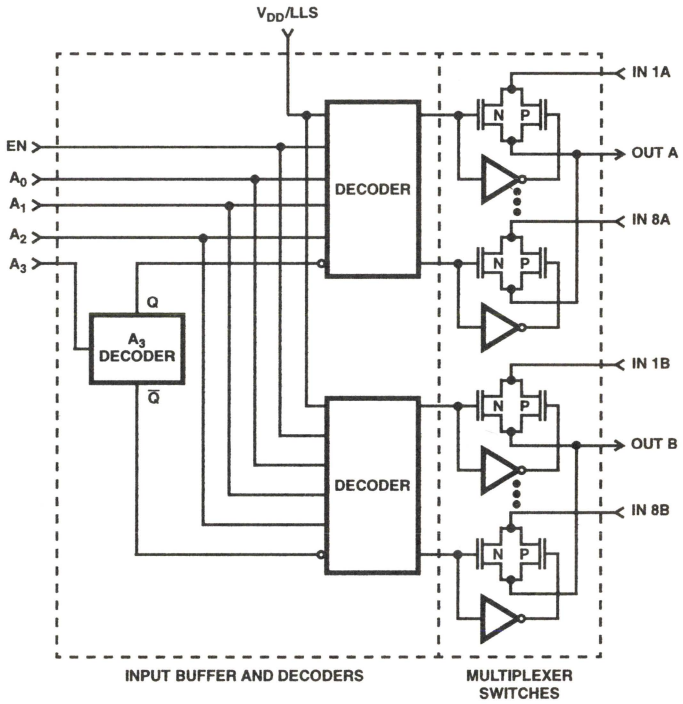


FIGURE 4. DUAL 1 x 4 MUX



A3 DECODER		
A3	Q	Q̄
H	H	L
L	L	H
V-	L	L

FIGURE 2. PROGRAMMABLE

MULTIPLEXER CONFIGURATIONS (Continued)

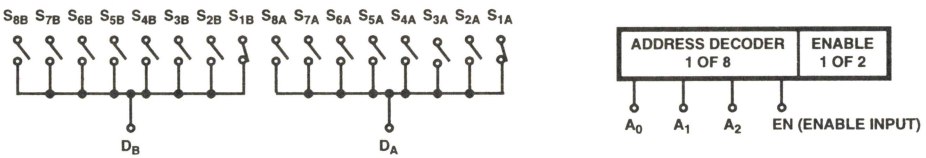
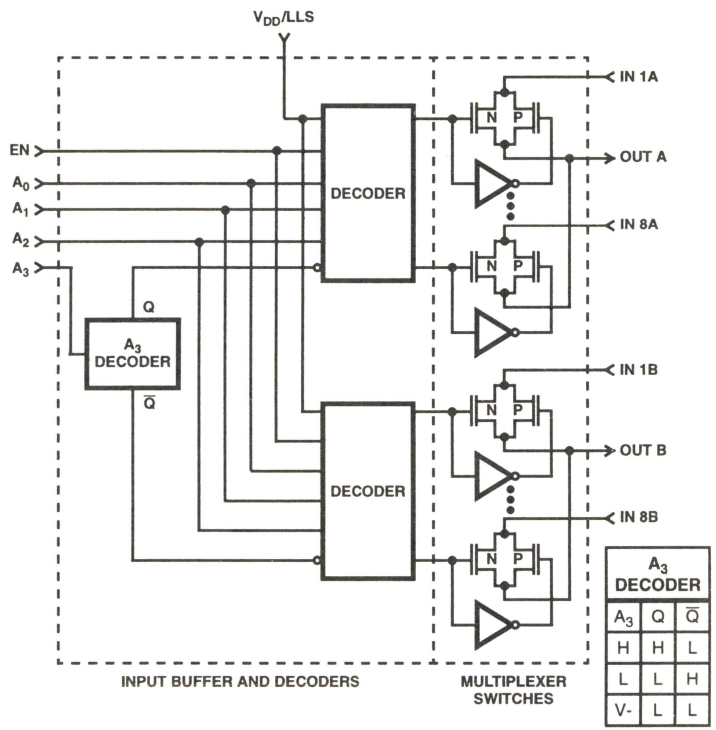
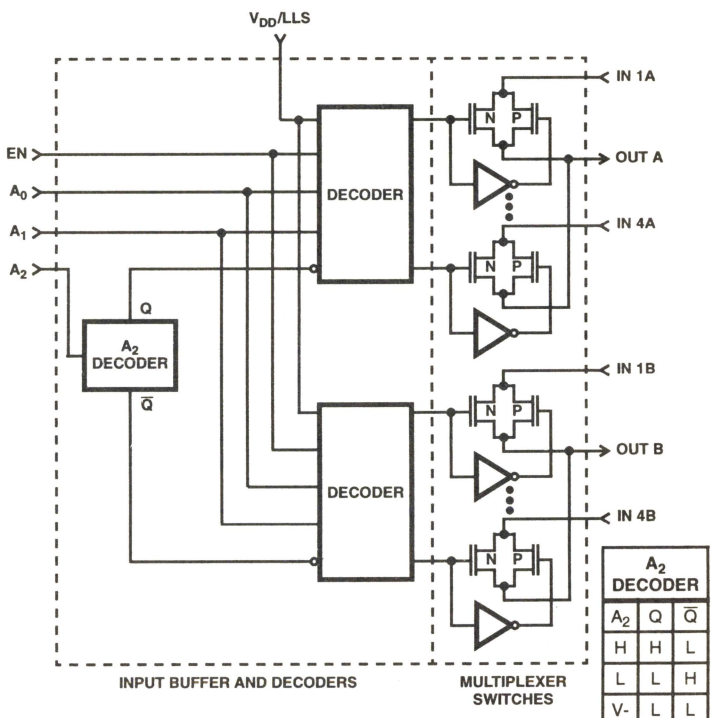


FIGURE 5. DUAL 1 x 8 MUX



A3 DECODER		
A3	Q	$\overline{Q}$
H	H	L
L	L	H
V-	L	L

FIGURE 6. PROGRAMMABLE SINGLE 16 OR DIFFERENTIAL 8



A2 DECODER		
A2	Q	$\overline{Q}$
H	H	L
L	L	H
V-	L	L

FIGURE 7. PROGRAMMABLE SINGLE 8 OR DIFFERENTIAL 4

HARRIS SEMICONDUCTOR

DG406, DG407

Single 16-Channel/Differential 8-Channel, CMOS Analog Multiplexers

August 1997

Features

- ON-Resistance (Max) 100Ω
- Low Power Consumption (P_D) . . . . . <1.2mW
- Fast Transition Time (Max) 300ns
- Low Charge Injection
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Battery Operated Systems
- Data Acquisition
- Medical Instrumentation
- Hi-Rel Systems
- Communication Systems
- Automatic Test Equipment

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG406DJ	-40 to 85	28 Ld PDIP	E28.6
DG406DY	-40 to 85	28 Ld SOIC	M28.3
DG406EJ (Note)	-40 to 85	28 Ld PDIP	E28.6
DG406EY (Note)	-40 to 85	28 Ld SOIC	M28.3
DG406DN	-40 to 85	28 Ld PLCC	N28.45
DG407DJ	-40 to 85	28 Ld PDIP	E28.6
DG407DY	-40 to 85	28 Ld SOIC	M28.3
DG407EJ (Note)	-40 to 85	28 Ld PDIP	E28.6
DG407EY (Note)	-40 to 85	28 Ld SOIC	M28.3
DG407DN	-40 to 85	28 Ld PLCC	N28.45

NOTE: Extended Processing Flow

Description

The DG406 and DG407 monolithic CMOS analog multiplexers are drop-in replacements for the popular DG506A and DG507A series devices. They each include an array of sixteen analog switches, a TTL and CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

These multiplexers feature lower signal ON resistance (<100Ω) and faster transition time (t_{TRANS} < 300ns) compared to the DG506A and DG507A. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG406 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling $30V_{P-P}$ signals when operating with ±15V power supplies.

The sixteen switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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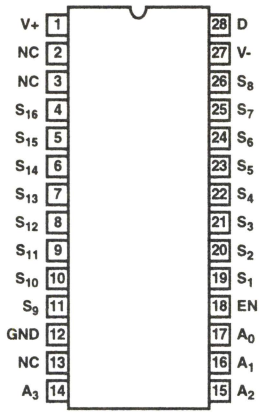
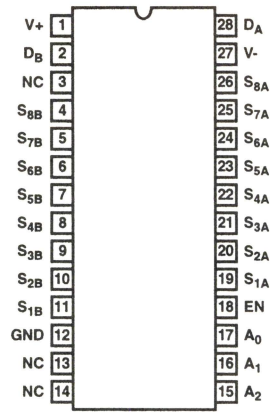
File Number **3116.4**

Pinouts

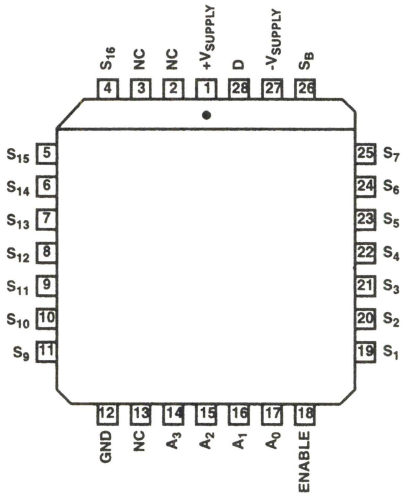
DG406 (PDIP, SOIC)
TOP VIEW



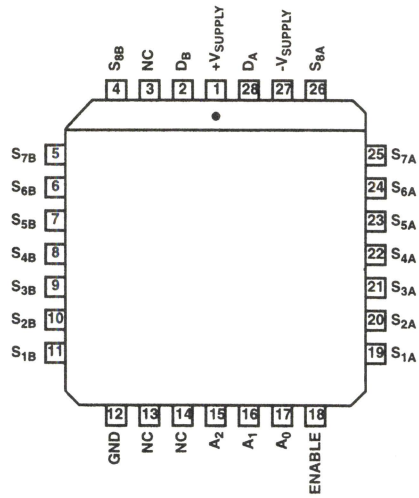
DG407 (PDIP, SOIC)
TOP VIEW



DG406 (PLCC)
TOP VIEW

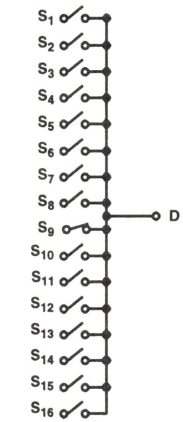


DG407 (PLCC)
TOP VIEW

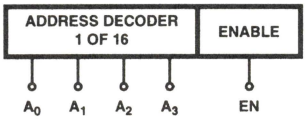


Functional Block Diagrams

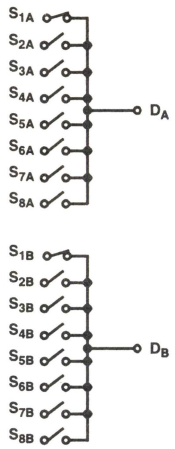
DG406



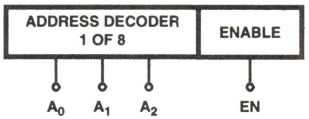
TO DECODER LOGIC CONTROLLING BOTH TIERS OF MUXING



DG407



TO DECODER LOGIC CONTROLLING BOTH TIERS OF MUXING



DG406 TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG407 TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} < 0.8V$
Logic "1" = $V_{AH} > 2.4V$
X = Don't Care

Absolute Maximum Ratings

Voltages Referenced to V-
V+ . . . . . +44.0V
GND 25V
Digital Inputs, V_S, V_D (Note 1) . . . . . (V-) -2V to (V+) +2V or 20mA, Whichever Occurs First
Current (Any Terminal) 30mA
Peak Current, S or D 100mA
(Pulsed 1ms, 10% Duty Cycle Max)

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	60
SOIC Package	75
PLCC Package	65

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(PLCC and SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEMP	D SUFFIX 40°C TO 85°C (NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
ANALOG SWITCH						
Drain-Source ON Resistance, $r_{DS(ON)}$	$V_D = \pm 10V$, $I_S = \mp 10mA$ (Note 6)	Room	-	50	100	Ω
		Full	-	-	125	Ω
$r_{DS(ON)}$ Matching Between Channels, $\Delta r_{DS(ON)}$	V_D = 10V, -10V (Note 7)	Room	-	5	-	%
Source OFF Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, $V_S = \pm 10V$, $V_D = \mp 10V$	Room	-0.5	0.01	0.5	nA
		Full	-5	-	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$ DG406		Room	-1	0.04	1	nA
		Full	-40	-	40	nA
DG407		Room	-1	0.04	1	nA
		Full	-20	-	20	nA
Drain ON Leakage Current, $I_{D(ON)}$ DG406	$V_S = V_D = \pm 10V$ (Note 6)	Room	-1	0.04	1	nA
		Full	-40	-	40	nA
DG407		Room	-1	0.04	1	nA
		Full	-20	-	20	nA
DIGITAL CONTROL						
Logic High Input Voltage, V_{INH}		Full	2.4	-	-	V
Logic Low Input Voltage, V_{INL}		Full	-	-	0.8	V
Logic High Input Current, I_{AH}	V_A = 2.4V, 15V	Full	-1	-	1	µA
Logic Low Input Current, I_{AL}	V_{EN} = 0V, 2.4V, V_A = 0V	Full	-1	-	1	µA
Logic Input Capacitance, C_{IN}	f = 1MHz	Room	-	7	-	pF

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEMP	D SUFFIX 40°C TO 85°C (NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Transition Time, t_{TRANS}	(See Figure 1)	Room	-	200	300	ns
		Full	-	-	400	ns
Break-Before-Make Interval, t_{OPEN}	(See Figure 3)	Room	25	50	-	ns
		Full	10	-	-	ns
Enable Turn-ON Time, $t_{ON(EN)}$	(See Figure 2)	Room	-	150	200	ns
		Full	-	-	400	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$		Room	-	70	150	ns
		Full	-	-	300	ns
Charge Injection, Q	C_L = 1nF, V_S = 0V, R_S = 0Ω	Room	-	40	-	pC
OFF Isolation, OIRR	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz (Note 8)	Room	-	-69	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	V_{EN} = 0V, V_S = 0V, f = 1MHz	Room	-	8	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$ DG406	V_{EN} = 0V, V_D = 0V, f = 1MHz	Room	-	160	-	pF
DG407		Room	-	80	-	pF
Drain ON Capacitance, $C_{D(ON)}$ DG406	V_{EN} = 5V, V_D = 0V, f = 1MHz	Room	-	180	-	pF
DG407		Room	-	90	-	pF
POWER SUPPLIES						
Positive Supply Current, I+	V_{EN} = V_A = 0V or 5V Stand By	Room	-	13	30	µA
		Full	-	-	75	µA
Negative Supply Current, I-		Room	-1	-0.01	-	µA
		Full	-10	-	-	µA
Positive Supply Current, I+	V_{EN} = 2.4V, V_A = 0V	Room	-	-0.01	100	µA
		Full	-	-	200	µA
Negative Supply Current, I-		Room	-1	-	-	µA
		Full	-10	-	-	µA

Electrical Specifications (Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEMP	D SUFFIX -40°C TO 85°C (NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Switching Time of Multiplexer, t_{TRANS}	V_{S1} = 8V, V_{S8} = 0V, V_{IN} = 2.4V	Room	-	300	450	ns

Electrical Specifications (Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEMP	D SUFFIX -40°C TO 85°C (NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
Enable Turn-ON Time, $T_{ON(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V	Room	-	250	600	ns
Enable Turn-OFF Time, $T_{OFF(EN)}$		Room	-	150	300	ns
Charge Injection, Q	C_L = 1nF, V_S = 6V, R_S = 0Ω	Room	-	20	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON-Resistance, $r_{DS(ON)}$	V_D = 3V, 10V, I_S = -1mA (Note 6)	Room	-	90	120	Ω
$r_{DS(ON)}$ Matching Between Channels (Note 7), $\Delta r_{DS(ON)}$		Room	-	5	-	%
Source Off Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, V_D = 10V or 0.5V, V_S = 0.5V or 10V	Room	-	0.01	-	nA
Drain Off Leakage Current, $I_{D(OFF)}$ DG406		Room	-	0.04	-	nA
DG407		Room	-	0.04	-	nA
Drain On Leakage Current, $I_{D(ON)}$ DG406	V_S = V_D = ±10V (Note 6)	Room	-	0.04	-	nA
DG407		Room	-	0.04	-	nA
POWER SUPPLIES						
Positive Supply Current (I+)	V_{EN} = 0V or 5V, V_A = 0V or 5V	Room	-	13	30	µA
		Full	-	13	75	µA
Negative Supply Current (I-)		Room	-1	-0.01	-	µA
		Full	-5	-0.01	-	µA

NOTES:

3. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
4. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
5. Typical values are for Design Aid Only, not guaranteed nor production tested.
6. Sequence each switch ON.
7. $\Delta r_{DS(ON)} = r_{DS(ON)}$ (Max) - $r_{DS(ON)}$ (Min) ÷ r_{DS} average
8. Worst case isolation occurs on channel 8B due to proximity to the drain pin.

Test Circuits and Waveforms

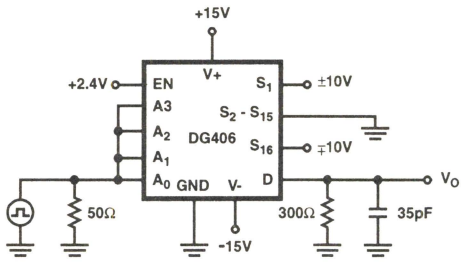


FIGURE 1A.

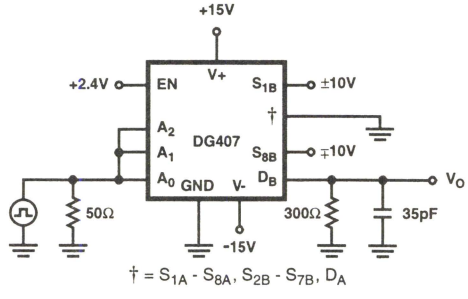


FIGURE 1B.

Test Circuits and Waveforms (Continued)

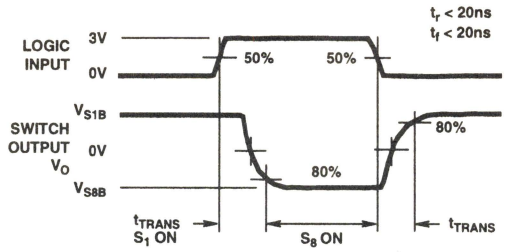


FIGURE 1C.

FIGURE 1. TRANSITION TIME

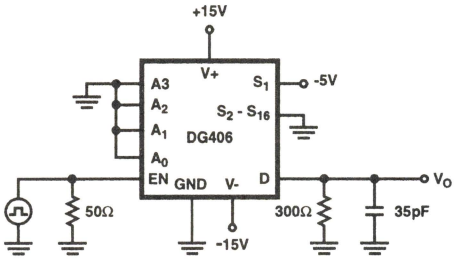


FIGURE 2A.

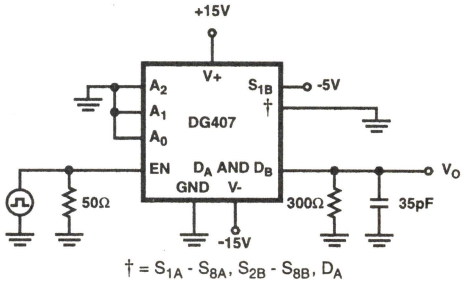


FIGURE 2B.

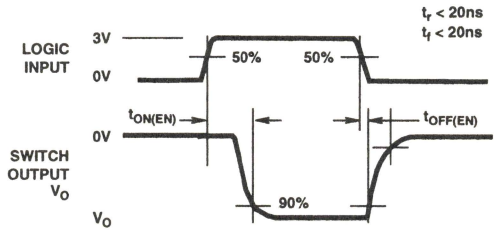


FIGURE 2C.

FIGURE 2. ENABLE SWITCHING TIME

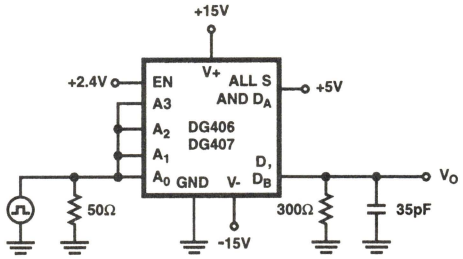


FIGURE 3A.

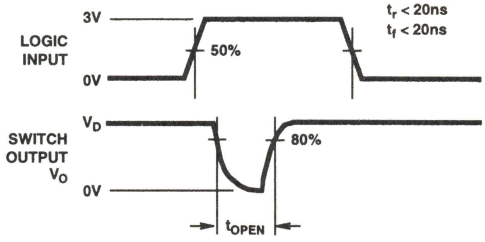


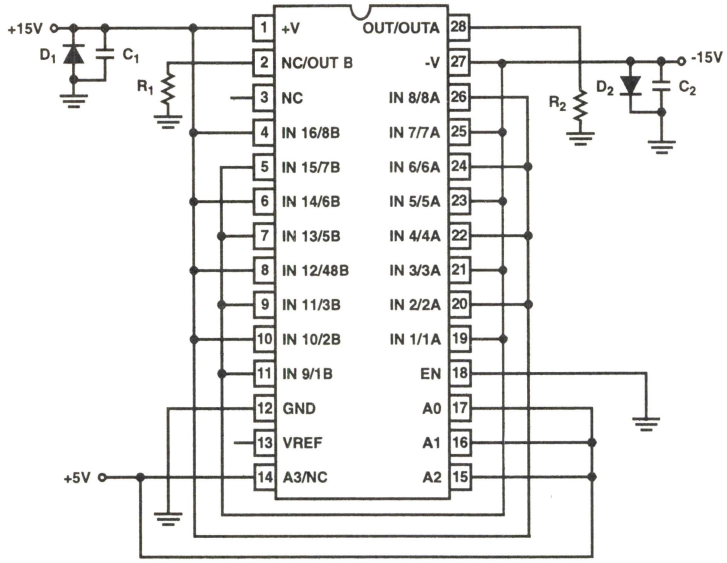
FIGURE 3B.

FIGURE 3. BREAK-BEFORE-MAKE INTERVAL

Burn-In Circuit

CERDIP/SOIC BURN-IN SCHEMATIC

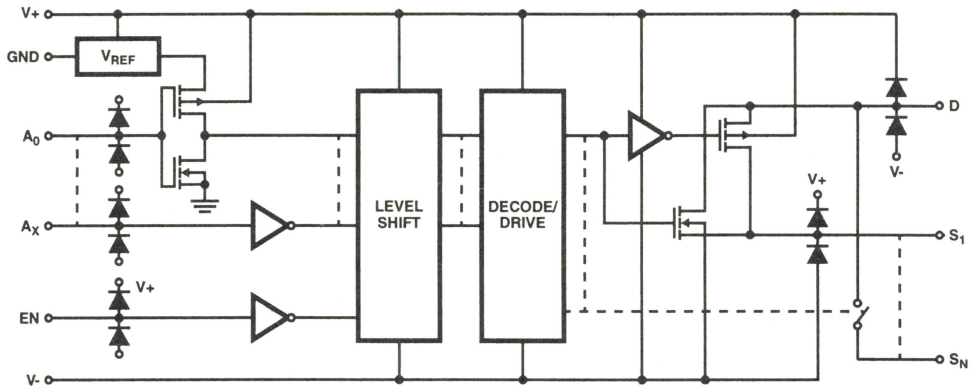
DG406/407EY/EJ



NOTE:

R_1, R_2 = 10kΩ ±5%, $^1/_2$W or $^1/_4$W (Per Socket)
C_1, C_2 = 0.01µF (Min, Per Socket) or 0.1µF (Min, Per Row)
D_1, D_2 = IN402 (or Equivalent, Per Board)

Schematic Diagram (Typical Channel)



Typical Performance Curves

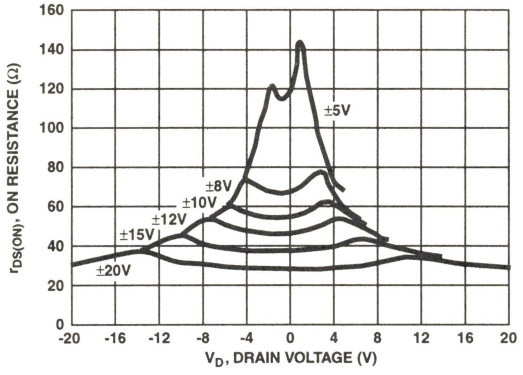


FIGURE 4. $r_{DS(ON)}$ vs V_D AND SUPPLY

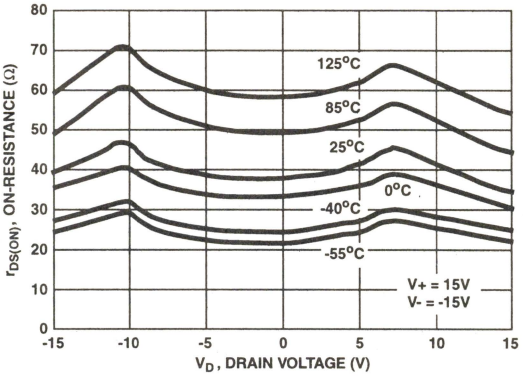


FIGURE 5. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

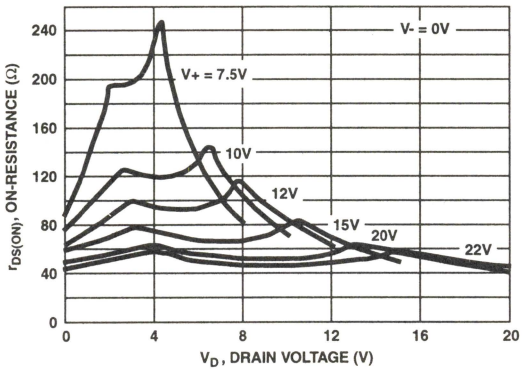


FIGURE 6. $r_{DS(ON)}$ vs V_D AND SUPPLY

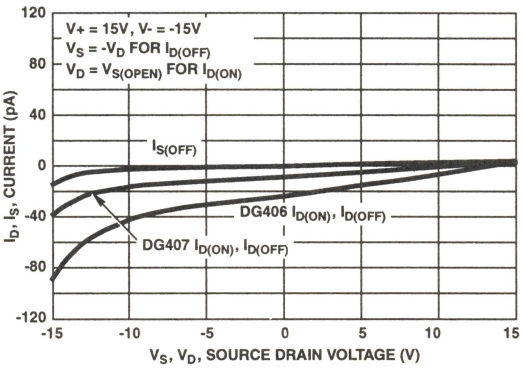


FIGURE 7. I_D, I_S LEAKAGE CURRENTS vs ANALOG VOLTAGE

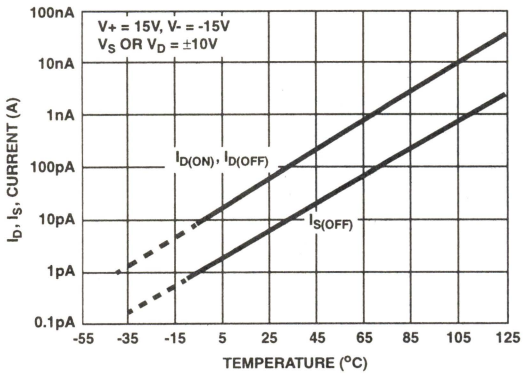


FIGURE 8. I_D, I_S LEAKAGE vs TEMPERATURE

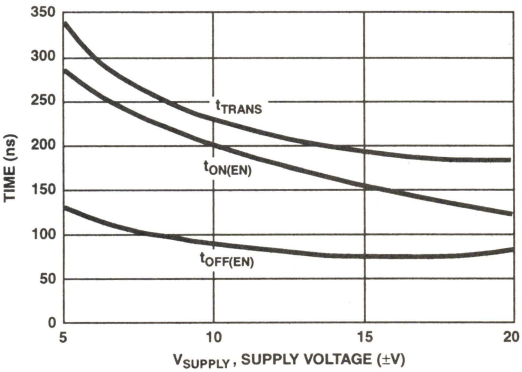


FIGURE 9. SWITCHING TIMES vs BIPOLAR SUPPLIES

Typical Performance Curves (Continued)

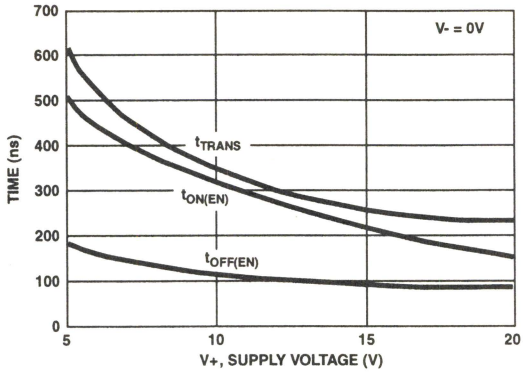


FIGURE 10. SWITCHING TIMES vs SINGLE SUPPLY

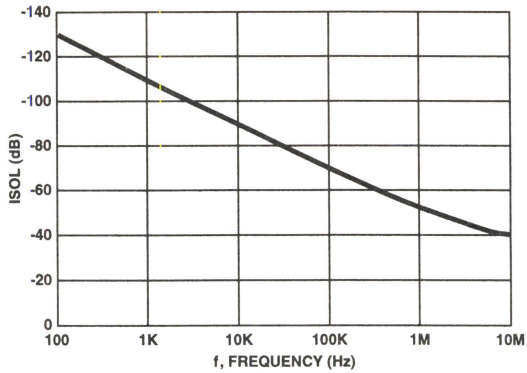


FIGURE 11. OFF-ISOLATION vs FREQUENCY

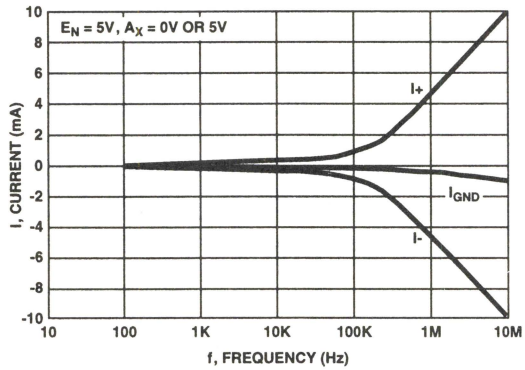


FIGURE 12. SUPPLY CURRENTS vs SWITCHING FREQUENCY

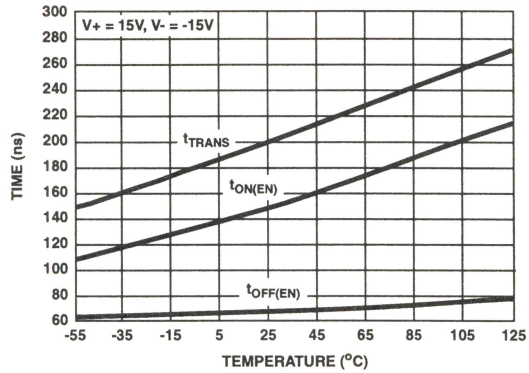


FIGURE 13. t_{ON}/t_{OFF} vs TEMPERATURE

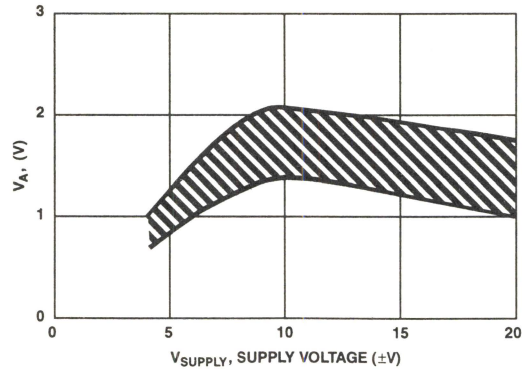


FIGURE 14. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

2490µm x 4560µm x 485µm ±25µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

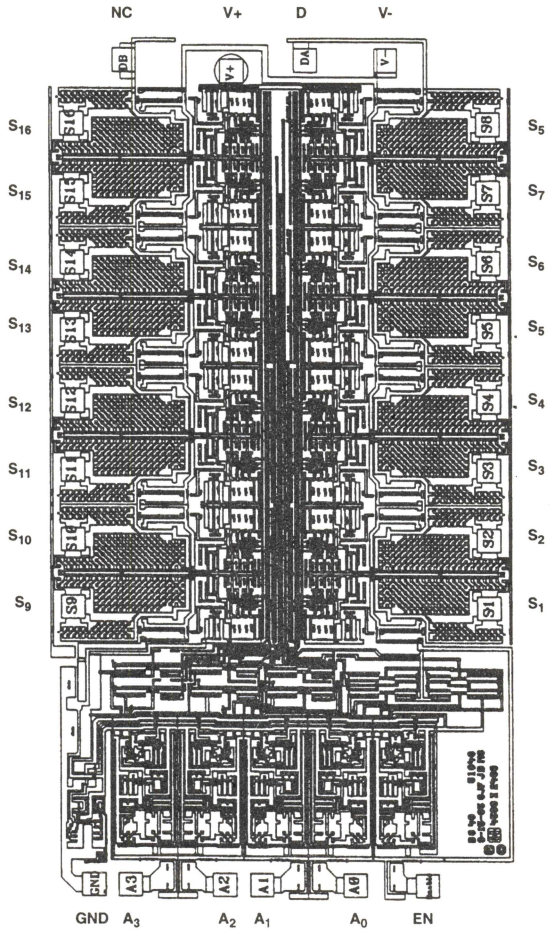
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG406



Die Characteristics

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Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

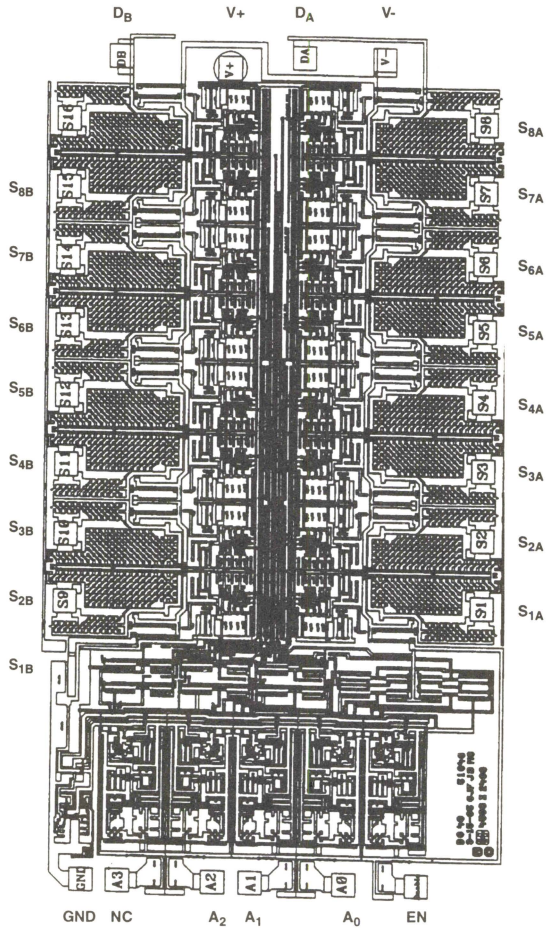
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG407



HARRIS SEMICONDUCTOR

DG408, DG409

Single 8-Channel/Differential 4-Channel, CMOS Analog Multiplexers

August 1997

Features

- ON Resistance (25°C Max) 100Ω
- Low Power Consumption (P_D) . . . . . .<11mW
- Fast Switching Action
  - t_{TRANS} . . . . . .<250ns
  - $t_{ON/OFF(EN)}$ . . . . . .<150ns
- Low Charge Injection
- Upgrade from DG508A/DG509A
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Data Acquisition Systems
- Audio Switching Systems
- Automatic Testers
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Analog Selector Switch

Description

The DG408 Single 8-Channel, and DG409 Differential 4-Channel monolithic CMOS analog multiplexers are drop-in replacements for the popular DG508A and DG509A series devices. They each include an array of eight analog switches, a TTL/CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds and an ENABLE input for device selection when several multiplexers are present.

The DG408 and DG409 feature lower signal ON resistance (<100Ω) and faster switch transition time (t_{TRANS} < 250ns) compared to the DG508A or DG509A. Charge injection has been reduced, simplifying sample and hold applications. The improvements in the DG408 series are made possible by using a high-voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

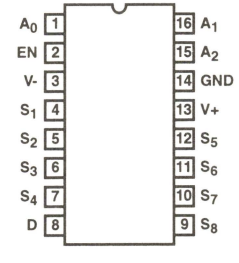
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG408AK/883 (Note 2)	-55 to 125	16 Ld CERDIP	F16.3
DG408DJ	-40 to 85	16 Ld PDIP	E16.3
DG408DY	-40 to 85	16 Ld SOIC	M16.15
DG408EJ (Note 1)	-40 to 85	16 Ld PDIP	E16.3
DG408EY (Note 1)	-40 to 85	16 Ld SOIC	M16.15
DG409AK/883 (Note 2)	-55 to 125	16 Ld CERDIP	F16.3
DG409DJ	-40 to 85	16 Ld PDIP	E16.3
DG409DY	-40 to 85	16 Ld SOIC	M16.15
DG409EJ (Note 1)	-40 to 85	16 Ld PDIP	E16.3
DG409EY (Note 1)	-40 to 85	16 Ld SOIC	M16.15

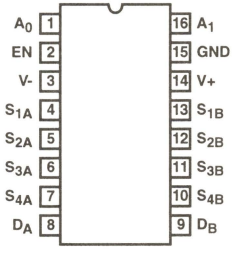
NOTES:
1. Extended Processing Flow
2. Refer to military data sheet for complete specifications.

Pinouts

DG408 (PDIP, CERDIP, SOIC)
TOP VIEW



DG409 (PDIP, CERDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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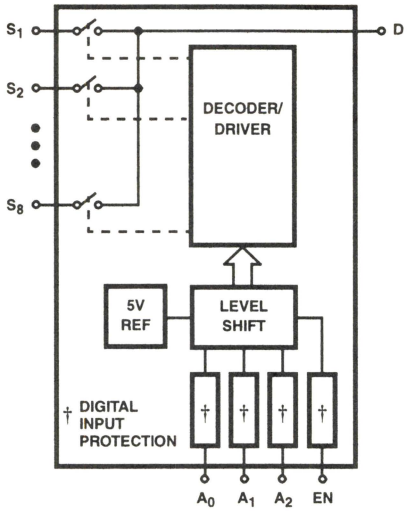
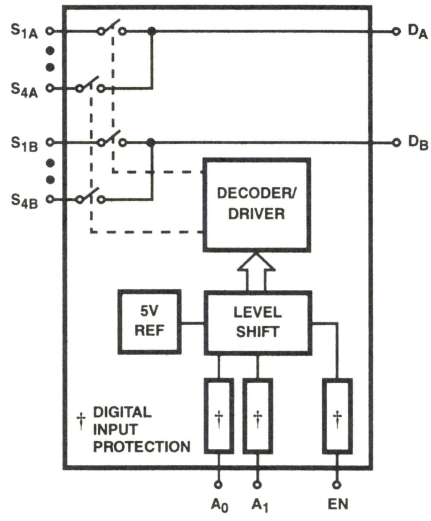
File Number **3283.4**

Functional Block Diagrams

DG408



DG409



Absolute Maximum Ratings

V+ to V- . . . . . +44.0V
GND to V- 25V
Digital Inputs, V_S, V_D (Note 7) . . . . . (V-) -2V to (V+) + 2V or 20mA, Whichever Occurs First
Current (Any Terminal) 30mA
Peak Current, S or D 100mA
(Pulsed 1ms, 10% Duty Cycle)

Operating Conditions

Operating Temperature (D Suffix) . . . . . -40C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	100	N/A
SOIC Package	115	N/A
CERDIP Package	70	18

Maximum Junction Temperature (D Suffix) . . . . . 150°C
Maximum Storage Temperature Range (D Suffix) . -65°C to 125°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 8) TEMP	D SUFFIX -40°C TO 85°C (NOTE 2) MIN	(NOTE 3) TYP	(NOTE 2) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Transition Time, t_{TRANS}	(See Figure 25)	Full	-	160	250	ns
Break-Before-Make Interval, t_{OPEN}	(See Figure 27)	Room	10	-	-	ns
Enable Turn-ON Time, $t_{ON(EN)}$	(See Figure 26)	Room	-	115	150	ns
		Full	-	-	225	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$	(See Figure 26)	Full	-	105	150	ns
Charge Injection, Q	C_L = 10nF, V_S = 0V	Room	-	20	-	pC
OFF Isolation	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz (Note 6)	Room	-	-75	-	dB
Logic Input Capacitance, C_{IN}	f = 1MHz	Room	-	8	-	pF
Source OFF Capacitance, $C_{S(OFF)}$	V_{EN} = 0V, V_S = 0V, f = 1MHz	Room	-	3	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$ DG408	V_{EN} = 0V, V_D = 0V, f = 1MHz	Room	-	26	-	pF
DG409		Room	-	14	-	pF
Drain ON Capacitance, $C_{D(ON)}$ DG408	V_{EN} = 3V, V_D = 0V, f = 1MHz, V_A = 0V or 3V	Room	-	37	-	pF
DG409		Room	-	25	-	pF
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	V_D = ±10V, I_S = -10mA (Note 4)	Room	-	40	100	Ω
		Full	-	-	125	Ω
$r_{DS(ON)}$ Matching Between Channels, $\Delta r_{DS(ON)}$	V_D = 10V, -10V (Note 5)	Room	-	-	15	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, V_S = ±10V, V_D = ∓10V	Room	-0.5	-	0.5	nA
		Full	-5	-	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$ DG408	V_{EN} = 0V, V_D = ±10V, V_S = ∓10V	Room	-1	-	1	nA
		Full	-20	-	20	nA
DG409		Room	-1	-	1	nA
		Full	-10	-	10	nA

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 8) TEMP	D SUFFIX -40°C TO 85°C (NOTE 2) MIN	(NOTE 3) TYP	(NOTE 2) MAX	UNITS
Drain ON Leakage Current, $I_{D(ON)}$ DG408	$V_S = V_D = \pm 10V$ Sequence Each Switch ON	Room	-1	-	1	nA
		Full	-20	-	20	nA
DG409		Room	-1	-	1	nA
		Full	-10	-	10	nA
DIGITAL CONTROL						
Logic Input Current, Input Voltage High, I_{AH}	V_A = 2.4V, 15V	Full	-10	-	10	µA
Logic Input Current, Input Voltage Low, I_{AL}	V_{EN} = 0V, 2.4V, V_A = 0V	Full	-10	-	10	µA
POWER SUPPLIES						
Positive Supply Current, I+	V_{EN} = 0V, V_A = 0V	Full	-	10	75	µA
Negative Supply Current, I-		Full	-75	1	-	µA
Positive Supply Current, I+	V_{EN} = 2.4V, V_A = 0V	Room Full	-	0.2	0.5 2	mA
Negative Supply Current, I-		Full	-500	-	-	µA

Electrical Specifications (Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITION	(NOTE 8) TEMP	D SUFFIX -40°C TO 85°C (NOTE 2) MIN	(NOTE 3) TYP	(NOTE 2) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Switching Time of Multiplexer, t_{TRANS}	V_{S1} = 8V, V_{S8} = 0V, V_{IN} = 2.4V	Room	-	180	-	ns
Enable Turn-ON Time, $T_{ON(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V	Room	-	180	-	ns
Enable Turn-OFF Time, $T_{OFF(EN)}$		Room	-	120	-	ns
Charge Injection, Q	C_L = 10nF, V_{GEN} = 0V, R_{GEN} = 0Ω	Room	-	5	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON-Resistance, $r_{DS(ON)}$	V_D = 3V, 10V, I_S = -1mA (Note 4)	Room	-	90	-	Ω

NOTES:

1. All leads soldered to PC Board.
2. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor production tested.
4. Sequence each switch ON.
5. $\Delta r_{DS(ON)} = r_{DS(ON)}$ (Max) - $r_{DS(ON)}$ (Min).
6. Worst case isolation occurs on channel 4 due to proximity to the drain pin.
7. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
8. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

Typical Performance Curves

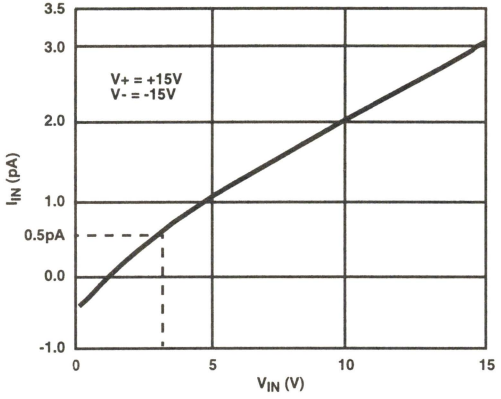


FIGURE 1. INPUT LOGIC CURRENT vs LOGIC INPUT VOLTAGE

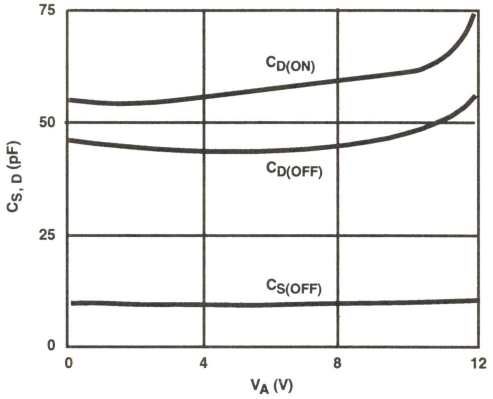


FIGURE 2. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

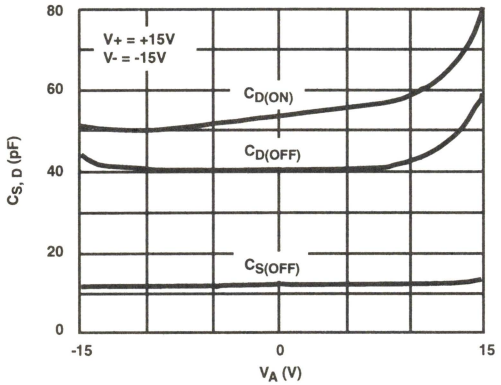


FIGURE 3. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

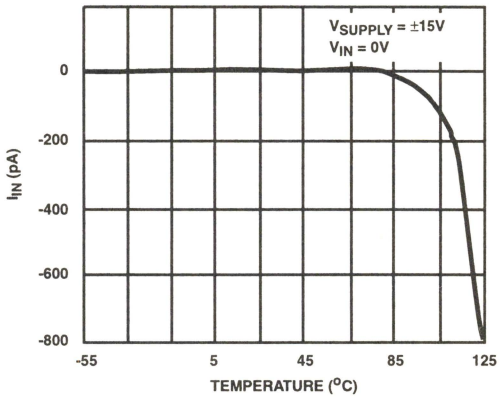


FIGURE 4. LOGIC INPUT CURRENT vs TEMPERATURE

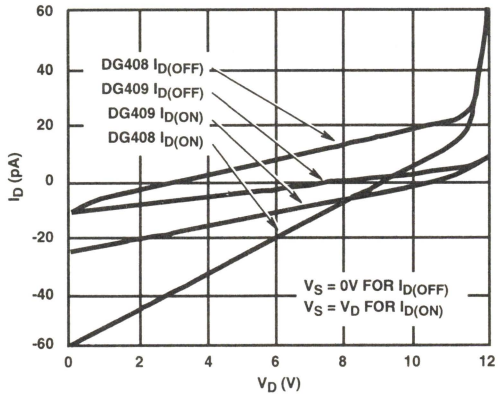


FIGURE 5. DRAIN LEAKAGE CURRENT vs SOURCE/DRAIN VOLTAGE (SINGLE 12V SUPPLY)

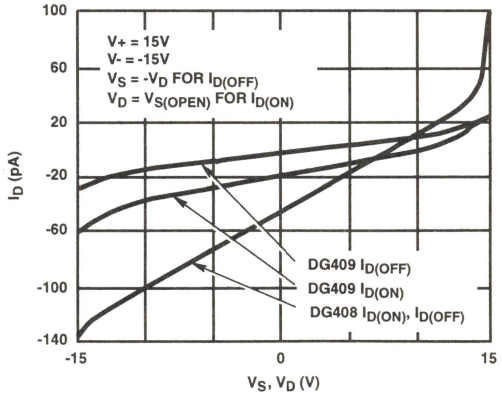


FIGURE 6. DRAIN LEAKAGE CURRENT vs SOURCE/DRAIN VOLTAGE

Typical Performance Curves (Continued)

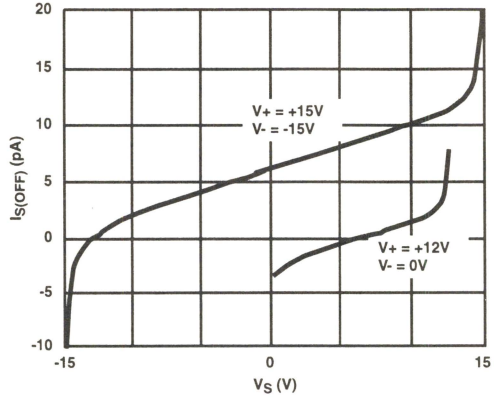


FIGURE 7. SOURCE LEAKAGE CURRENT vs SOURCE VOLTAGE

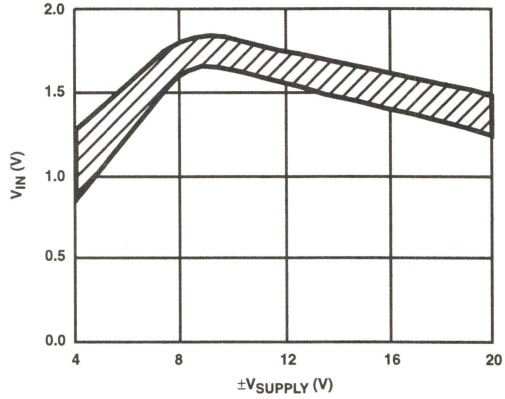


FIGURE 8. INPUT SWITCHING THRESHOLD vs SUPPLY VOLTAGE

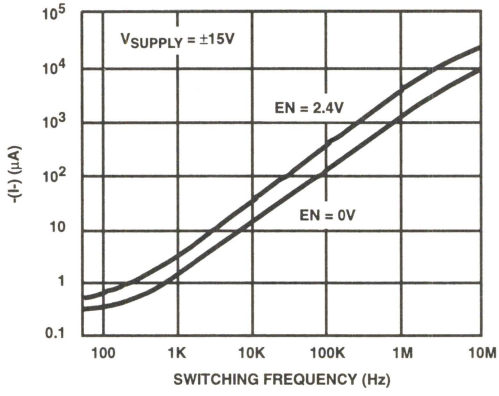


FIGURE 9. NEGATIVE SUPPLY CURRENT vs SWITCHING FREQUENCY

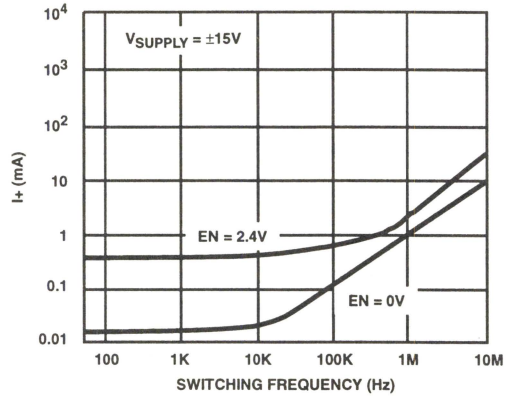


FIGURE 10. POSITIVE SUPPLY CURRENT vs SWITCHING FREQUENCY

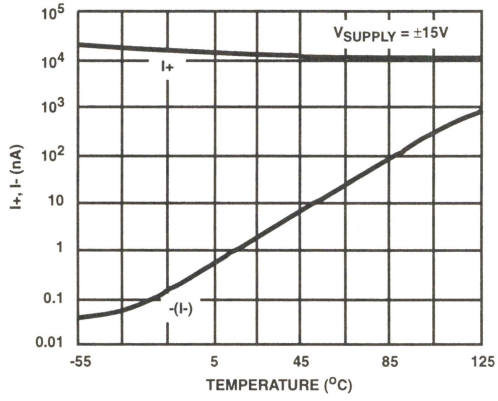


FIGURE 11. I_{SUPPLY} vs TEMPERATURE (LOG SCALE)

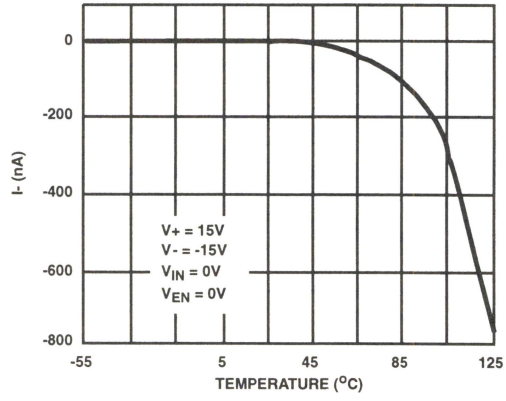


FIGURE 12. NEGATIVE SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

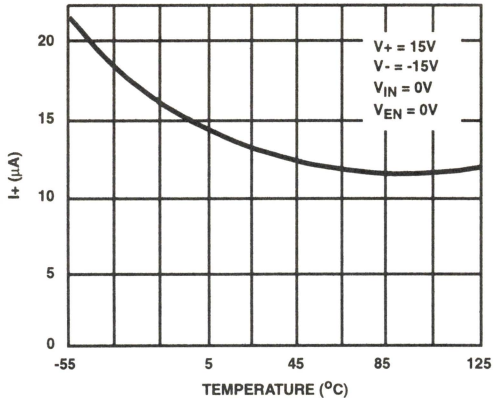


FIGURE 13. POSITIVE SUPPLY CURRENT vs TEMPERATURE (DG408)

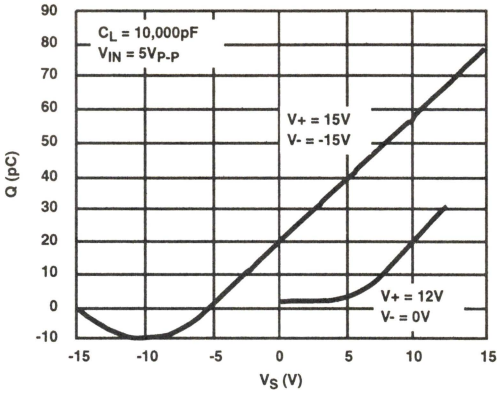


FIGURE 14. CHARGE INJECTION vs ANALOG VOLTAGE V_S (DG408, DG409)

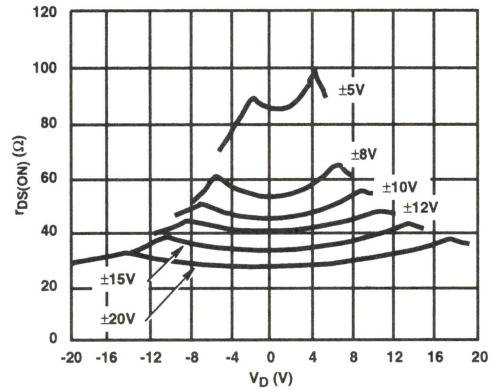


FIGURE 15. $r_{DS(ON)}$ vs V_D AND SUPPLY

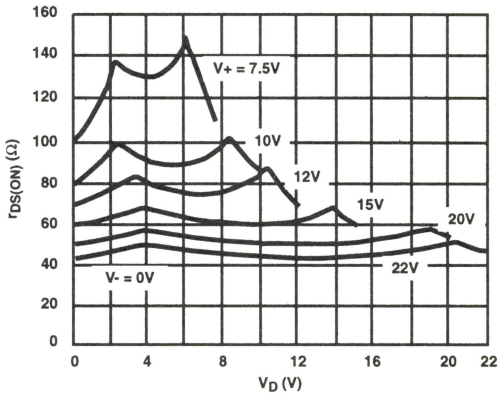


FIGURE 16. $r_{DS(ON)}$ vs V_D (SINGLE SUPPLY)

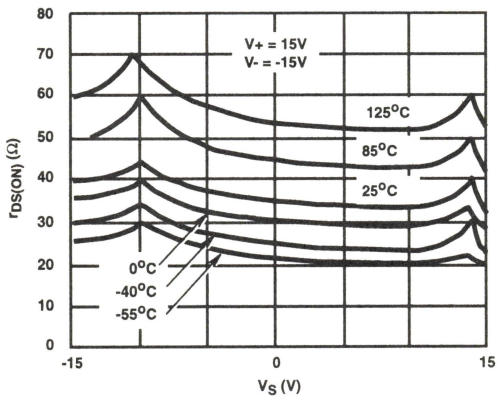


FIGURE 17. $r_{DS(ON)}$ vs V_S AND TEMPERATURE

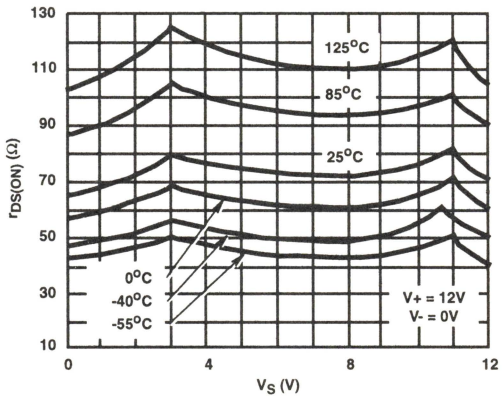


FIGURE 18. $r_{DS(ON)}$ vs V_S AND TEMPERATURE (SINGLE SUPPLY)

Typical Performance Curves (Continued)

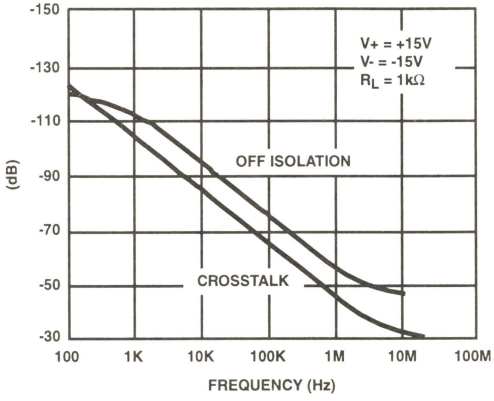


FIGURE 19. OFF ISOLATION AND CROSSTALK vs FREQUENCY

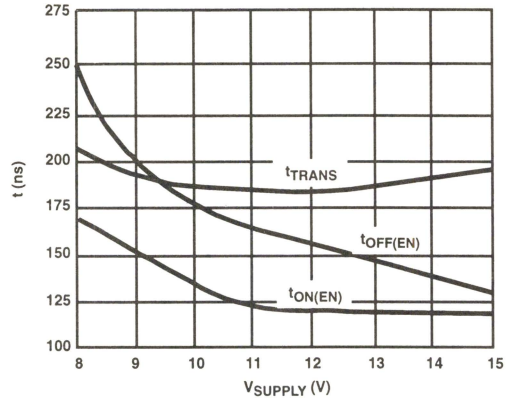


FIGURE 20. SWITCHING TIME vs SINGLE SUPPLY

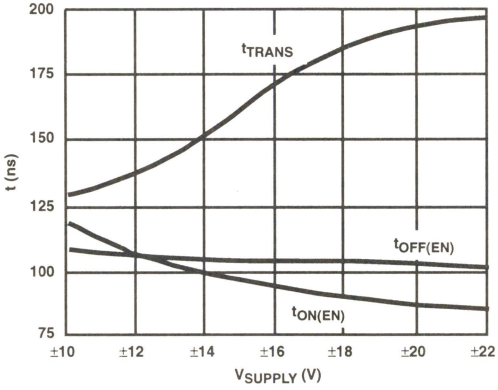


FIGURE 21. SWITCHING TIME vs BIPOLAR SUPPLY

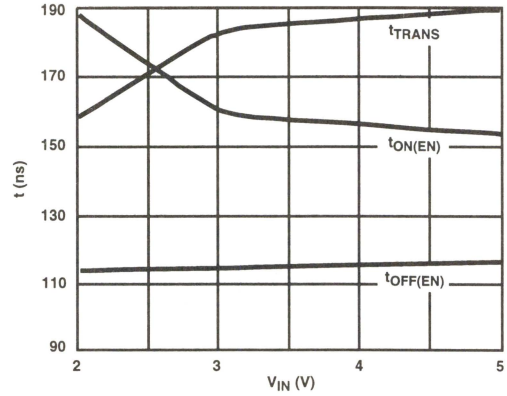


FIGURE 22. SWITCHING TIME vs V_{IN} (SINGLE SUPPLY)

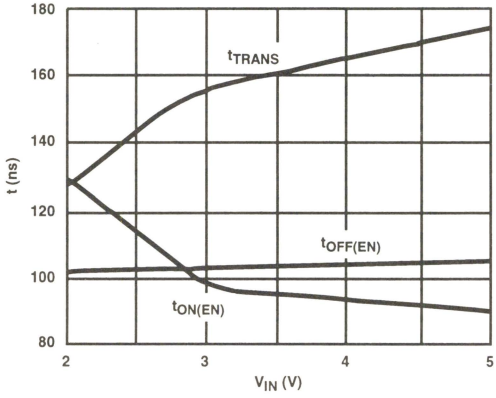


FIGURE 23. SWITCHING TIME vs V_{IN} (BIPOLAR SUPPLY)

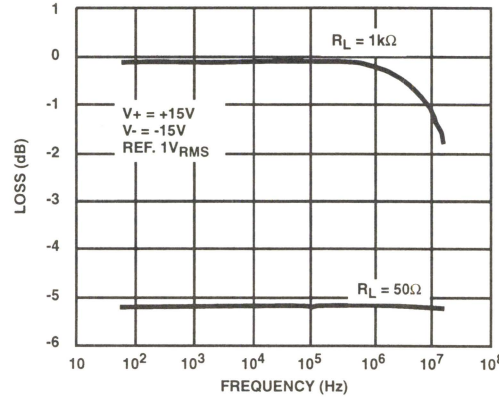


FIGURE 24. INSERTION LOSS vs FREQUENCY

Pin Descriptions - (DG408)

PIN	SYMBOL	DESCRIPTION
1	A_0	Logic Decode Input (Bit 0, LSB)
2	EN	Enable Input
3	V-	Negative Power Supply Terminal
4	S_1	Source (Input) for Channel 1
5	S_2	Source (Input) for Channel 2
6	S_3	Source (Input) for Channel 3
7	S_4	Source (Input) for Channel 4
8	D	Drain (Output)
9	S_8	Source (Input) for Channel 8
10	S_7	Source (Input) for Channel 7
11	S_6	Source (Input) for Channel 6
12	S_5	Source (Input) for Channel 5
13	V+	Positive Power Supply Terminal (Substrate)
14	GND	Ground Terminal (Logic Common)
15	A_2	Logic Decode Input (Bit 2, MSB)
16	A_1	Logic Decode Input (Bit 1)

Pin Descriptions - (DG409)

PIN	SYMBOL	DESCRIPTION
1	A_0	Logic Decode Input (Bit 0, LSB)
2	EN	Enable Input
3	V-	Negative Power Supply Terminal
4	S_{1A}	Source (Input) for Channel 1a
5	S_{2A}	Source (Input) for Channel 2a
6	S_{3A}	Source (Input) for Channel 3a
7	S_{4A}	Source (Input) for Channel 4a
8	D_A	Drain a (Output a)
9	D_B	Drain b (Output b)
10	S_{4B}	Source (Input) for Channel 4b
11	S_{3B}	Source (Input) for Channel 3b
12	S_{2B}	Source (Input) for Channel 2b
13	S_{1B}	Source (Input) for Channel 1b
14	V+	Positive Power Supply Terminal
15	GND	Ground Terminal (Logic Common)
16	A_1	Logic Decode Input (Bit 1, MSB)

TRUTH TABLE DG408

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE DG409

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

NOTES:

1. V_{AH} Logic "1" ≥2.4V.
2. V_{AL} Logic "0" ≤0.8V.

Test Circuits and Waveforms

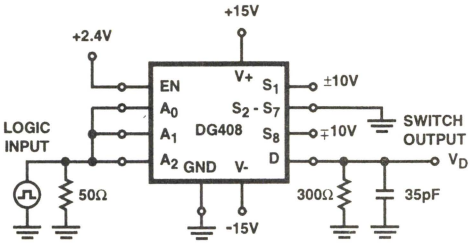


FIGURE 25A.

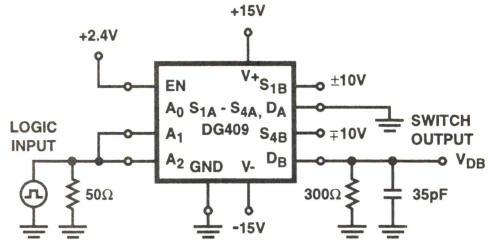


FIGURE 25B.

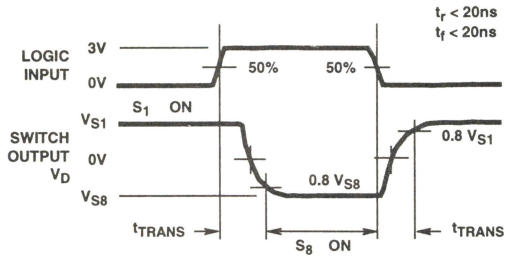


FIGURE 25C.

FIGURE 25. TRANSITION TIME

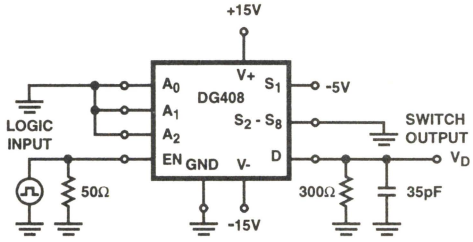


FIGURE 26A.

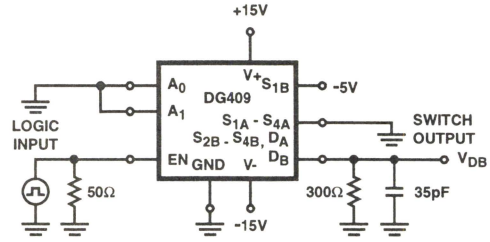


FIGURE 26B.

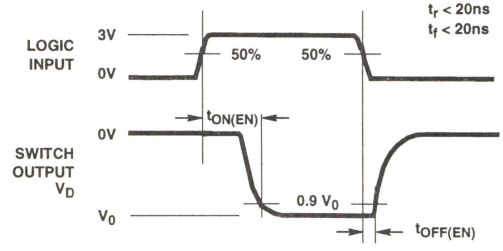


FIGURE 26C.

FIGURE 26. $t_{ON(EN)}$, $t_{OFF(EN)}$

Test Circuits and Waveforms (Continued)

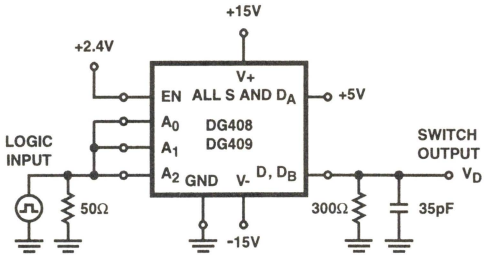


FIGURE 27A.

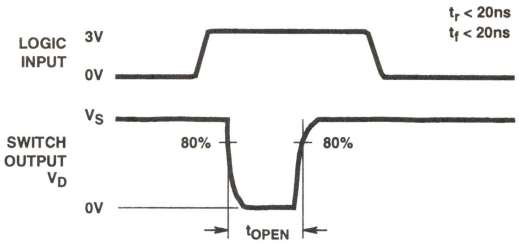


FIGURE 27B.

FIGURE 27. BREAK-BEFORE-MAKE INTERVAL

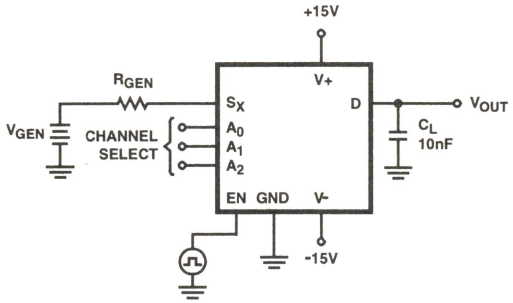
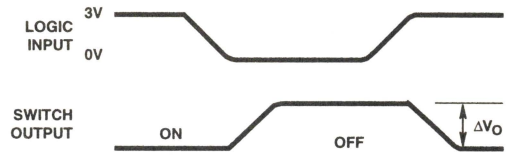


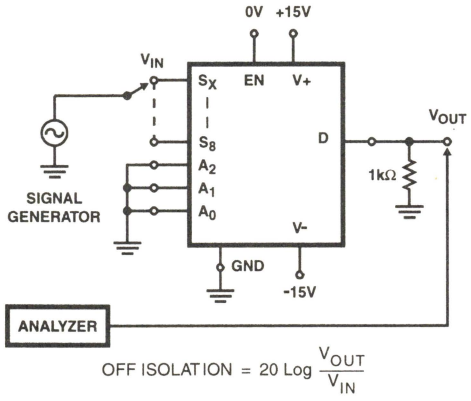
FIGURE 28A.



ΔV_O IS THE MEASURED VOLTAGE DUE TO CHARGE TRANSFER ERROR, Q
$Q = C_L \times \Delta V_O$

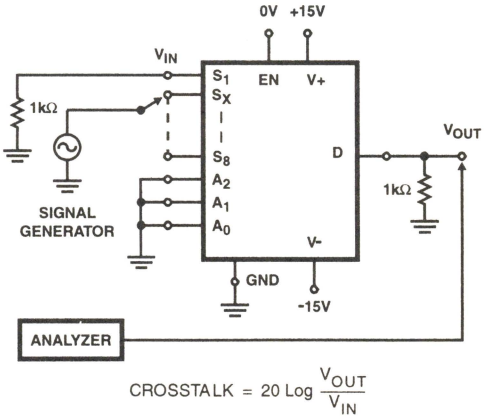
FIGURE 28B.

FIGURE 28. CHARGE INJECTION



$$\text{OFF ISOLATION} = 20 \text{ Log } \frac{V_{OUT}}{V_{IN}}$$

FIGURE 29. OFF ISOLATION



$$\text{CROSSTALK} = 20 \text{ Log } \frac{V_{OUT}}{V_{IN}}$$

FIGURE 30. CROSSTALK

Test Circuits and Waveforms (Continued)

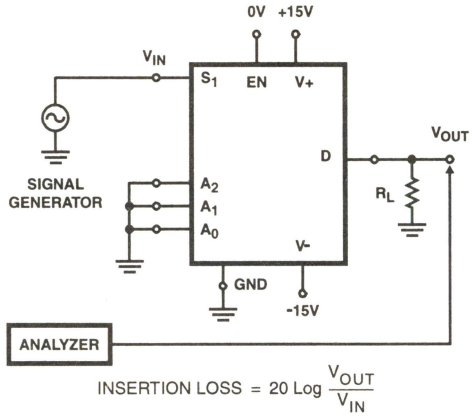


FIGURE 31. INSERTION LOSS

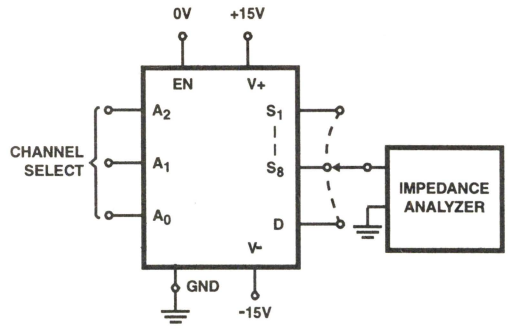


FIGURE 32. SOURCE/DRAIN CAPACITANCES

Typical Applications

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 33). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference V_S - (V-) doesn't exceed -44V. The addition of these diodes will reduce the analog signal range to 1V below V+ and 1V above V-, but it preserves the low channel resistance and low leakage characteristics.

Typical application information is for Design Aid Only, not guaranteed and not subject to production testing.

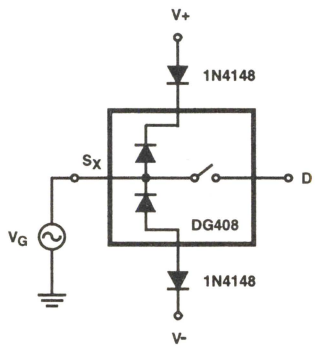


FIGURE 33. OVERVOLTAGE PROTECTION USING BLOCKING DIODES

Die Characteristics

DIE DIMENSIONS:

1800µm x 3320µm x 485µm ±25µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

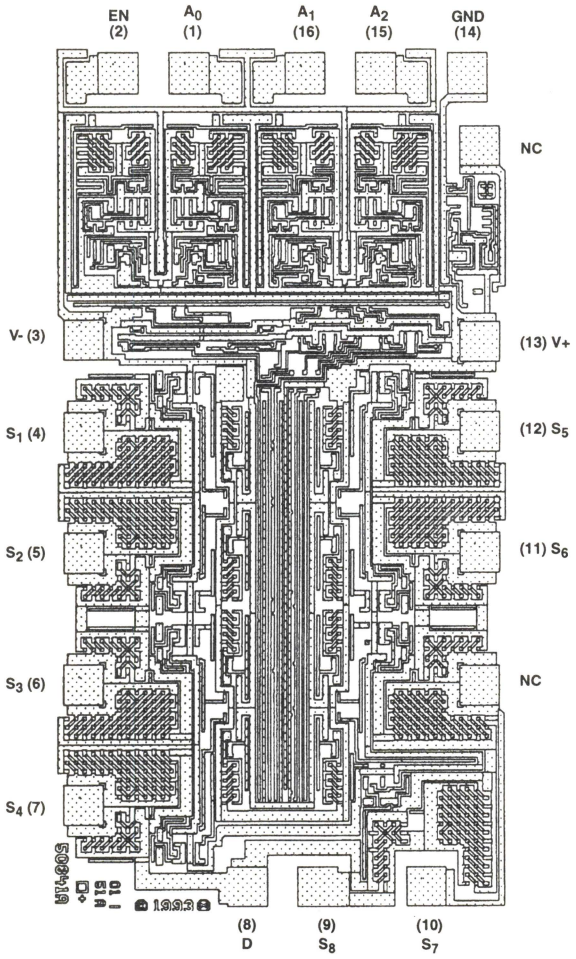
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG408



Die Characteristics

DIE DIMENSIONS:

1800µm x 3320µm x 485µm ±25µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

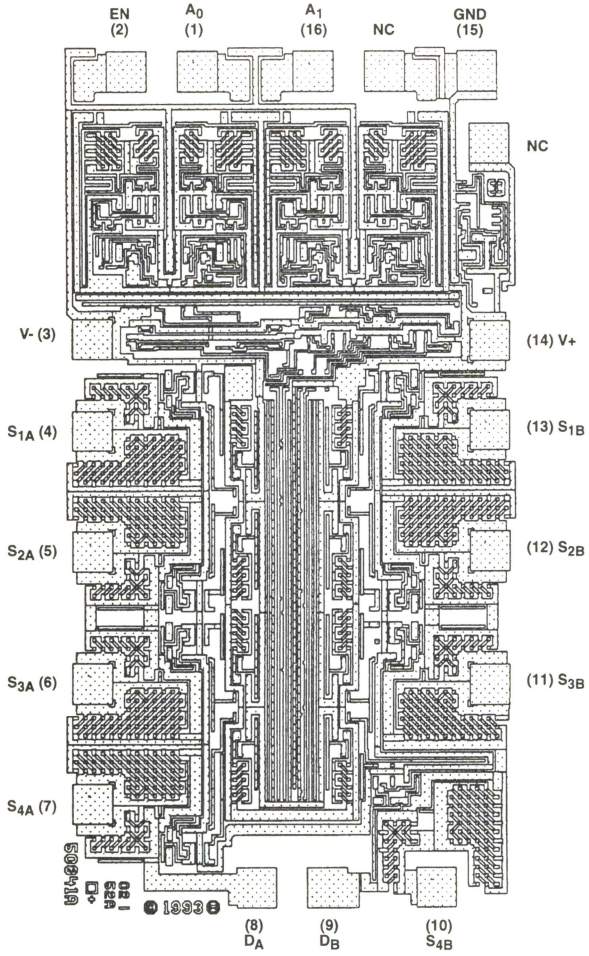
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG409



HARRIS SEMICONDUCTOR

DG506A, DG507A, DG508A, DG509A

August 1997

CMOS Analog Multiplexers

Features

- Low Power Consumption
- TTL and CMOS-Compatible Address and Enable Inputs
- 44V Maximum Power Supply Rating
- High Latch-Up Immunity
- Break-Before-Make Switching
- Alternate Source

Applications

- Data Acquisition Systems
- Communication Systems
- Signal Multiplexing/Demultiplexing
- Audio Signal Multiplexing

Description

The DG506A, DG507A, DG508A and DG509A are CMOS Monolithic 16-Channel/Dual 8-Channel and 8-Channel/Dual 4-Channel Analog Multiplexers, which can also be used as demultiplexers. An enable input is provided. When the enable input is high, a channel is selected by the address inputs, and when low, all channels are off.

A channel in the ON state conducts current equally well in both directions. In the OFF state each channel blocks voltages up to the supply rails. The address inputs and the enable input are TTL and CMOS compatible over the full specified operating temperature range.

The DG506A, DG507A, DG508A and DG509A are pinout compatible with the industry standard devices.

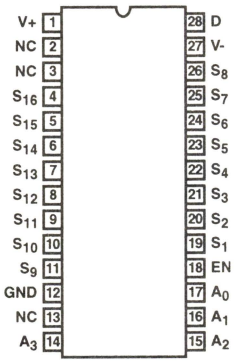
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG506AAK	-55 to 125	28 Ld CERDIP	F28.6
DG506AAK/883B	-55 to 125	28 Ld CERDIP	F28.6
DG506ABK	-25 to 85	28 Ld CERDIP	F28.6
DG506ABY	-25 to 85	28 Ld PDIP	E28.6
DG506ACJ	0 to 70	28 Ld PDIP	E28.6
DG506ACY	0 to 70	28 Ld SOIC	M28.3
DG507AAK	-55 to 125	28 Ld CERDIP	F28.6
DG507AAK/883B	-55 to 125	28 Ld CERDIP	F28.6
DG507ABK	-25 to 85	28 Ld CERDIP	F28.6
DG507ABY	-25 to 85	28 Ld PDIP	E28.6
DG507ACJ	0 to 70	28 Ld PDIP	E28.6
DG507ACK	0 to 70	28 Ld CERDIP	F28.6
DG507ACY	0 to 70	28 Ld SOIC	M28.3
DG508AAK	-55 to 125	16 Ld CERDIP	F16.3

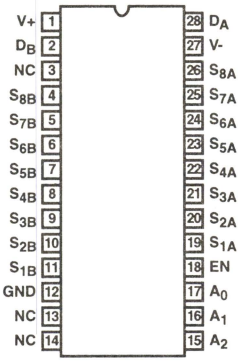
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG508AAK/883B	-55 to 125	16 Ld CERDIP	F16.3
DG508ABK	-25 to 85	16 Ld CERDIP	F16.3
DG508ABY	-25 to 85	16 Ld SOIC	M16.3
DG508ACJ	0 to 70	16 Ld PDIP	E16.3
DG508ACK	0 to 70	16 Ld CERDIP	F16.3
DG508ACY	0 to 70	16 Ld SOIC	M16.3
DG509AAK	-55 to 125	16 Ld CERDIP	F16.3
DG509AAK/883B	-55 to 125	16 Ld CERDIP	F16.3
DG509ABK	-25 to 85	16 Ld CERDIP	F16.3
DG509ABY	-25 to 85	16 Ld SOIC	M16.3
DG509ACJ	0 to 70	16 Ld PDIP	E16.3
DG509ACK	0 to 70	16 Ld CERDIP	F16.3
DG509ACY	0 to 70	16 Ld SOIC	M16.3

Pinouts

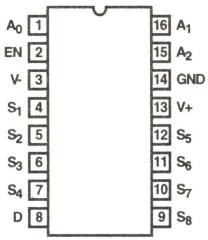
DG506A (PDIP, CERDIP, SOIC)
TOP VIEW



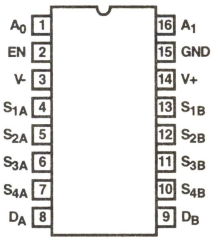
DG507A (PDIP, CERDIP, SOIC)
TOP VIEW



DG508A (PDIP, CERDIP, SOIC)
TOP VIEW



DG509A (PDIP, CERDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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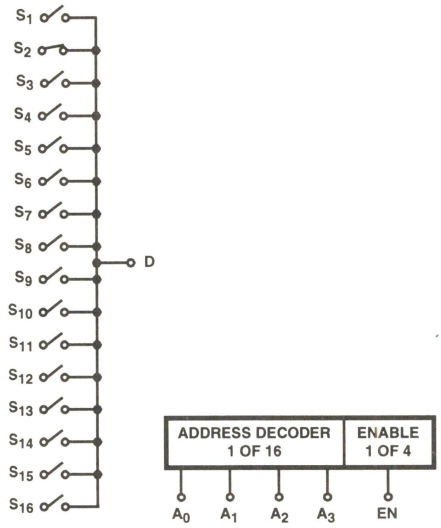
File Number **3137.1**

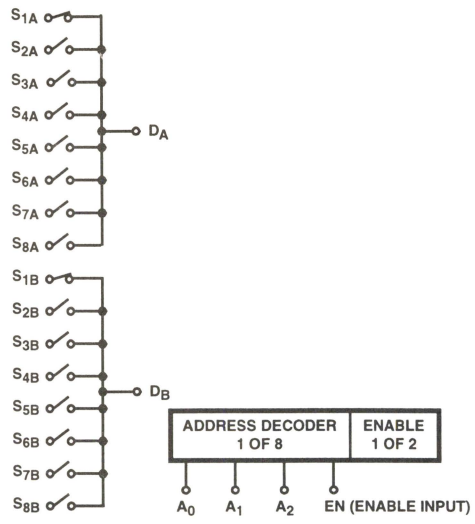
Functional Block Diagrams

DG506A



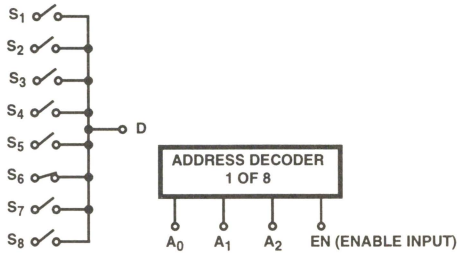
4 Line Binary Address Inputs
(0 0 0 1) and EN = 5V
Above example shows channel 2 turned ON.

DG507A



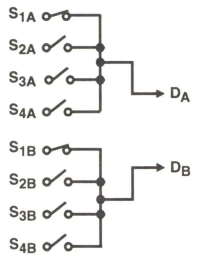
3 Line Binary Address Inputs
(0 0 0) and EN = 5V
Above example shows channels 1_A and 1_B turned ON.

DG508A



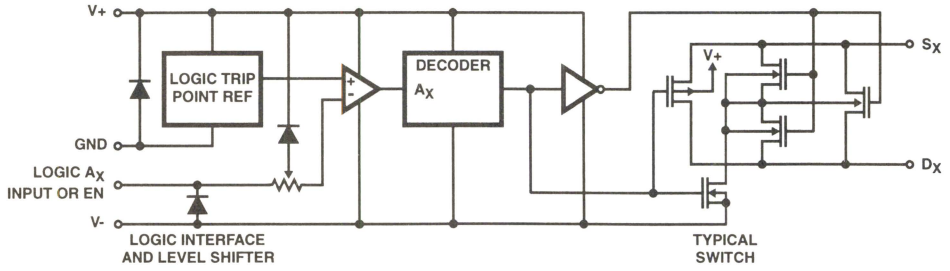
3 Line Binary Address Inputs
(1 0 1) and EN = 1
Above example shows channel 6 turned ON.

DG509A



2 Line Binary Address Inputs
(0 0) and EN = 1
Above example shows channels 1_A and 1_B turned ON.

Schematic Diagram



Absolute Maximum Ratings

V+ to V- 44V
V- to Ground . . . . . -25V
V_{IN} to Ground (Note 1) . . . . . (V- -2V), (V+ +2V)
V_S or V_D to V+ (Note 1) . . . . . +2, (V- -2V)
V_S or V_D to V- (Note 1) . . . . . -2, (V+ +2V)
Current, any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max) 40mA

Operating Conditions

Operating Temperature Range
C Suffix . . . . . 0^oC to 70^oC
B Suffix . . . . . -25^oC to 85^oC
A Suffix . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
16 Ld CERDIP Package	75	20
28 Ld CERDIP Package	55	18
16 Ld PDIP Package	100	N/A
28 Ld PDIP Package	60	N/A
16 Ld SOIC Package	100	N/A
28 Ld SOIC Package	70	N/A

Maximum Junction Temperature
CERDIP Package . . . . . 175^oC
PDIP Package . . . . . 150^oC
Maximum Storage Temperature
C Suffix . . . . . -65^oC to 125^oC
A and B Suffix . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:
1. Signals on V_S, V_D or V_{IN} exceeding V+ or V- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, V+ = +15V, V- = -15V, GND = 0V, V_{EN} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	DG506AA, DG507AA, DG508AA, DG509AA MIN	(NOTE 1) TYP	MAX	DG506AB/C, DG507AB/C, DG508AB/C, DG509AB/C MIN	(NOTE 1) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS								
Switching Time of Multiplexer, $t_{TRANSITION}$	See Figure 3	-	0.6	1	-	0.6	-	µs
Break-Before-Make Interval, t_{OPEN}	See Figure 5	-	0.2	-	-	0.2	-	µs
Enable Turn-On Time, $t_{ON(EN)}$	See Figure 4	-	1	1.5	-	1	-	µs
Enable Turn-Off Time, $t_{OFF(EN)}$	See Figure 4	-	0.4	1.0	-	0.4	-	µs
Off Isolation, OIRR	V_{EN} = 0V, R_L = 1kΩ, C_L = 15pF, V_S = $7V_{RMS}$, f = 500kHz (Note 3)	-	68	-	-	68	-	dB
Source Off Capacitance, $C_{S(OFF)}$	V_S = 0V, V_{EN} = 0V, f = 140kHz							
DG506A, DG507A		-	6	-	-	6	-	pF
DG508A, DG509A		-	5	-	-	5	-	pF
Drain Off Capacitance, $C_{D(OFF)}$	V_D = 0V, V_{EN} = 0V, f = 140kHz							
DG506A		-	45	-	-	45	-	pF
DG507A		-	23	-	-	23	-	pF
DG508A		-	25	-	-	25	-	pF
DG509A		-	12	-	-	12	-	pF
Charge Injection, Q	See Figure 6							
DG506A, DG507A		-	6	-	-	6	-	pC
DG508A, DG509A		-	4	-	-	4	-	pC
INPUT								
Address Input Current, Input Voltage High, I_{AH}	V_A = 2.4V	-10	-0.002	-	-10	-0.002	-	µA
	V_A = 15V	-	0.006	10	-	0.006	10	µA

Electrical Specifications $T_A = 25^oC$, V+ = +15V, V- = -15V, GND = 0V, V_{EN} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS		DG506AA, DG507AA, DG508AA, DG509AA MIN	(NOTE 1) TYP	MAX	DG506AB/C, DG507AB/C, DG508AB/C, DG509AB/C MIN	(NOTE 1) TYP	MAX	UNITS
Address Input Current Input Voltage Low, I_{AL}	V_{EN} = 2.4V	V_A = 0V	-10	-0.002	-	-10	-0.002	-	µA
	V_{EN} = 0V		-10	-0.002	-	-10	-0.0002	-	µA
SWITCH									
Analog Signal Range, V_{ANALOG}	(Note 5)		-15	-	+15	-15	-	+15	V
Drain Source On Resistance, $r_{DS(ON)}$	Sequence Each Switch On V_{AL} = 0.8V V_{AH} = 2.4V	I_S = -200µA, V_D = +10V	-	270	400	-	270	450	Ω
		I_S = -200µA, V_D = -10V	-	230	400	-	230	450	Ω
Greatest Change in Drain Source On Resistance Between Channels, $\Delta r_{DS(ON)}$	-10V ≤ V_S ≤ +10V $\Delta r_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)AVG}}$		-	6	-	-	6	-	%
Source Off Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V	V_S = +10V, V_D = -10V	-1	0.002	1	-5	0.002	5	nA
		V_S = -10V, V_D = +10V	-1	-0.005	1	-5	-0.005	5	nA
Drain Off Leakage Current, $I_{D(OFF)}$ DG506A	V_{EN} = 0V	V_S = -10V, V_D = +10V	-10	0.02	10	-20	0.02	20	nA
		V_S = +10V, V_D = -10V	-10	-0.03	10	-20	-0.03	20	nA
DG507A		V_S = -10V, V_D = +10V	-5	0.007	5	-10	0.007	10	nA
		V_S = +10V, V_D = -10V	-5	-0.015	5	-10	-0.015	10	nA
DG508A		V_S = -10V, V_D = +10V	-	0.01	10	-	0.01	20	nA
		V_S = +10V, V_D = -10V	-10	-0.015	-	-20	-0.015	-	nA
DG509A		V_S = -10V, V_D = +10V	-	0.005	10	-	0.005	20	nA
		V_S = +10V, V_D = -10V	-10	-0.008	-	-20	-0.008	-	nA
Drain On Leakage Current, $I_{D(ON)}$ DG506A	(Note 4) Sequence Each Switch On V_{AL} = 0.8V V_{AH} = 2.4V	$V_D = V_{S(ALL)}$ = +10V	-10	0.03	10	-20	0.03	20	nA
		$V_D = V_{S(ALL)}$ = -10V	-10	-0.06	10	-20	-0.06	20	nA
DG507A		$V_D = V_{S(ALL)}$ = +10V	-5	0.015	5	-10	0.015	10	nA
		$V_D = V_{S(ALL)}$ = -10V	-5	-0.03	5	-10	-0.03	10	nA
DG508A		$V_D = V_{S(ALL)}$ = +10V	-	0.015	10	-	0.015	20	nA
		$V_D = V_{S(ALL)}$ = -10V	-10	-0.03	-	-20	-0.03	-	nA
DG509A		$V_D = V_{S(ALL)}$ = +10V	-	0.007	10	-	0.007	20	nA
		$V_D = V_{S(ALL)}$ = -10V	-10	-0.015	-	-20	-0.015	-	nA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I+	V_{EN} = 5.0V, V_A = 0V		-	1.3	2.4	-	1.3	2.4	mA
Negative Supply Current, I-	V_{EN} = 5.0V, V_A = 0V		-1.5	-0.7	-	-1.5	-0.7	-	mA
Positive Supply Current, I+ Standby	V_{EN} = 0V, V_A = 0V		-	1.3	2.4	-	1.3	2.4	mA
Negative Supply Current, I- Standby	V_{EN} = 0V, V_A = 0V		-1.5	-0.7	-	-1.5	-0.7	-	mA

Electrical Specifications T_A = Over Operating Temperature Range, V+ = +15V, V- = -15V, GND = 0V, V_{EN} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS		DG506AA, DG507AA, DG508AA, DG509AA MIN	(NOTE 2) TYP	MAX	DG506AB/C, DG507AB/C, DG508AB/C, DG509AB/C MIN	(NOTE 2) TYP	MAX	UNITS
INPUT									
Address Input Current, Input Voltage High, I_{AH}	V_A = 2.4V		-30	-	-	-	-	-	µA
	V_A = 15V		-	-	30	-	-	-	µA
Address Input Current Input Voltage Low, I_{AL}	V_{EN} = 2.4V	V_A = 0V	-30	-	-	-	-	-	µA
	V_{EN} = 0V		-30	-	-	-	-	-	µA
SWITCHING CHARACTERISTICS									
Analog Signal Range, V_{ANALOG}	(Note 5)		-15	-	+15	-	-	-	V
Drain Source On Resistance, $r_{DS(ON)}$	Sequence Each Switch On V_{AL} = 0.8V V_{AH} = 2.4V	I_S = -200µA, V_D = +10V	-	-	500	-	-	-	Ω
		I_S = -200µA, V_D = -10V	-	-	500	-	-	-	Ω
Source Off Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V	V_S = +10V, V_D = -10V	-	-	50	-	-	-	nA
		V_S = -10V, V_D = +10V	-50	-	-	-	-	-	nA
Drain Off Leakage Current, $I_{D(OFF)}$ DG506A	V_{EN} = 0V	V_S = -10V, V_D = +10V	-	-	300	-	-	-	nA
		V_S = +10V, V_D = -10V	-300	-	-	-	-	-	nA
DG507A		V_S = -10V, V_D = +10V	-	-	200	-	-	-	nA
		V_S = +10V, V_D = -10V	-200	-	-	-	-	-	nA
DG508A		V_S = -10V, V_D = +10V	-	-	200	-	-	-	nA
		V_S = +10V, V_D = -10V	-200	-	-	-	-	-	nA
DG509A		V_S = -10V, V_D = +10V	-	-	100	-	-	-	nA
		V_S = +10V, V_D = -10V	-100	-	-	-	-	-	nA
Drain On Leakage Current, $I_{D(ON)}$ DG506A	(Note 4) Sequence Each Switch On V_{AL} = 0.8V V_{AH} = 2.4V	$V_D = V_{S(ALL)}$ = +10V	-	-	300	-	-	-	nA
		$V_D = V_{S(ALL)}$ = -10V	-300	-	-	-	-	-	nA
DG507A		$V_D = V_{S(ALL)}$ = +10V	-	-	200	-	-	-	nA
		$V_D = V_{S(ALL)}$ = -10V	-200	-	-	-	-	-	nA
DG508A		$V_D = V_{S(ALL)}$ = +10V	-	-	200	-	-	-	nA
		$V_D = V_{S(ALL)}$ = -10V	-200	-	-	-	-	-	nA
DG509A		$V_D = V_{S(ALL)}$ = +10V	-	-	100	-	-	-	nA
		$V_D = V_{S(ALL)}$ = -10V	-100	-	-	-	-	-	nA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I+		V_{EN} = 5.0V, V_A = 0V	-3.2	-	4.5	-	-	-	mA
Negative Supplu Current I-		V_{EN} = 5.0V, V_A = 0V	-3.2	-	4.5	-	-	-	mA
Positive Standby Supply Current I+		V_{EN} = 0V, V_A = 0V	-3.2	-	4.5	-	-	-	mA
Negative Standby Supply Current I-		V_{EN} = 0V, V_A = 0V	-3.2	-	4.5	-	-	-	mA

NOTES:

1. Typical values are for design aid only, not guaranteed and not subject to production testing.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Off isolation = 20Log $|V_S|/|V_D|$, where V_S = input to Off switch, and V_D = output due to V_S.
4. $I_{D(ON)}$ is leakage from driver into "ON" switch.
5. Parameter not tested. Parameter guaranteed by design or characterization.

Typical Performance Curves

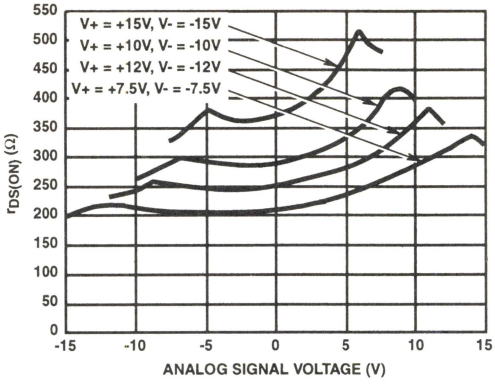


FIGURE 1. $r_{DS(ON)}$ vs ANALOG SIGNAL VOLTAGE vs SUPPLY VOLTAGE

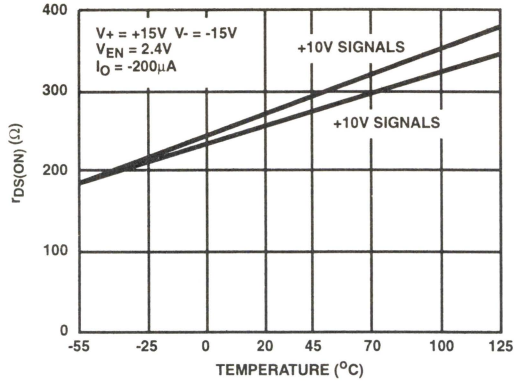
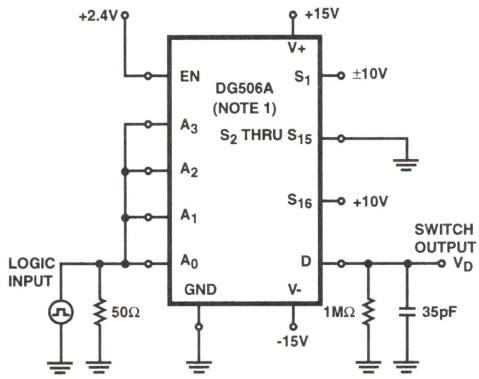


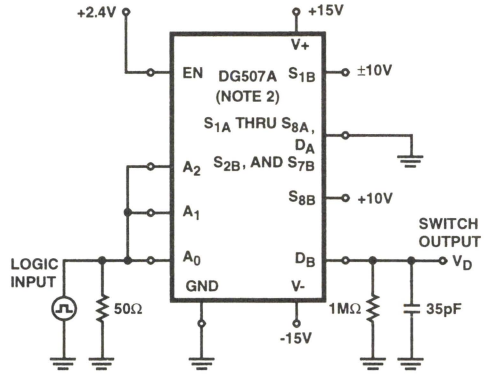
FIGURE 2. TYPICAL $r_{DS(ON)}$ VARIATION WITH TEMPERATURE

Test Circuits and Waveforms



NOTE: 1. Similar connections for DG508A

FIGURE 3A. $t_{TRANSITION}$ SWITCHING TIME TEST CIRCUIT



NOTE: 2. Similar connections for DG509A

FIGURE 3B. $t_{TRANSITION}$ SWITCHING TIME TEST CIRCUIT

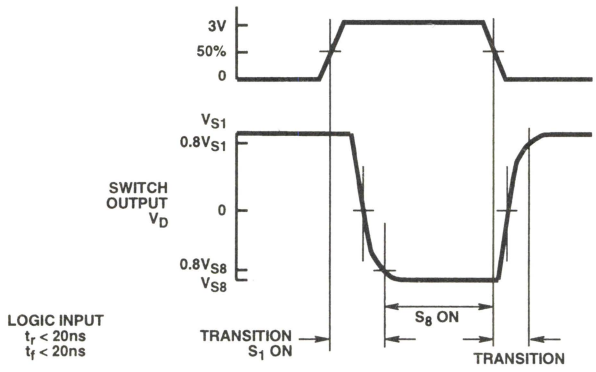
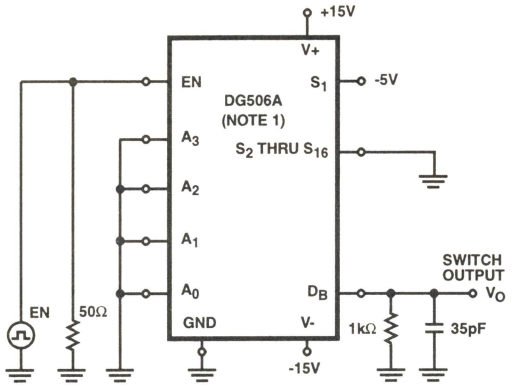


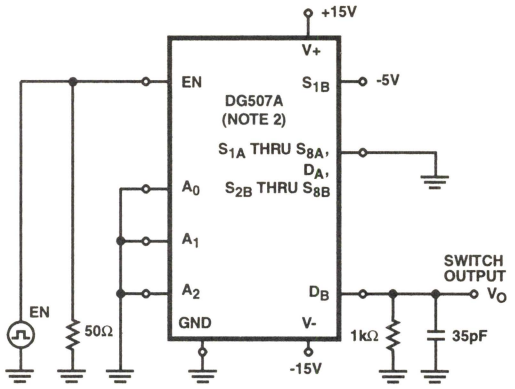
FIGURE 3C. $t_{TRANSITION}$ SWITCHING TIME WAVEFORMS

Test Circuits and Waveforms (Continued)



NOTE: 1. Similar connections for DG508A

FIGURE 4A. ENABLE t_{ON} and t_{OFF} SWITCHING TIME TEST CIRCUIT



NOTE: 2. Similar connections for DG509A

FIGURE 4B. ENABLE t_{ON} and t_{OFF} SWITCHING TIME TEST CIRCUIT

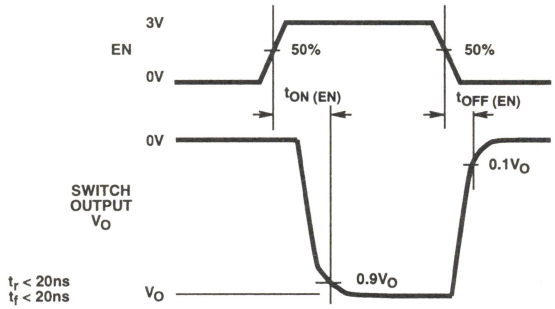
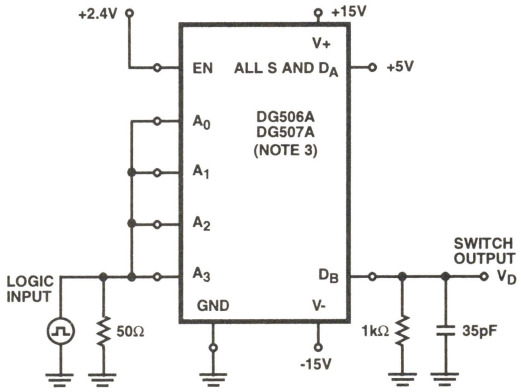


FIGURE 4C. ENABLE t_{ON} and t_{OFF} SWITCHING TIME WAVEFORMS



NOTE: 3. Similar connections for DG508A, DG509A.

FIGURE 5A. t_{OPEN} (BREAK-BEFORE-MAKE) SWITCHING TIME TEST CIRCUIT

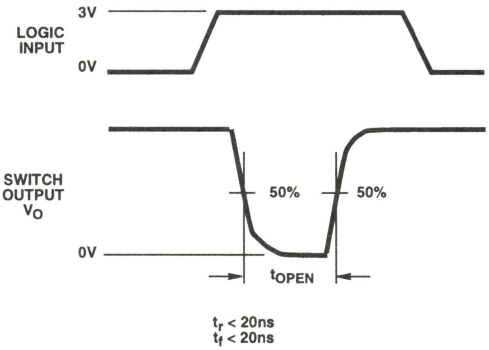
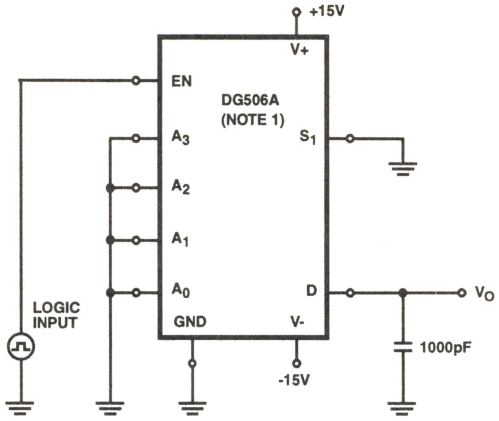


FIGURE 5B. t_{OPEN} (BREAK-BEFORE-MAKE) SWITCHING TIME WAVEFORMS

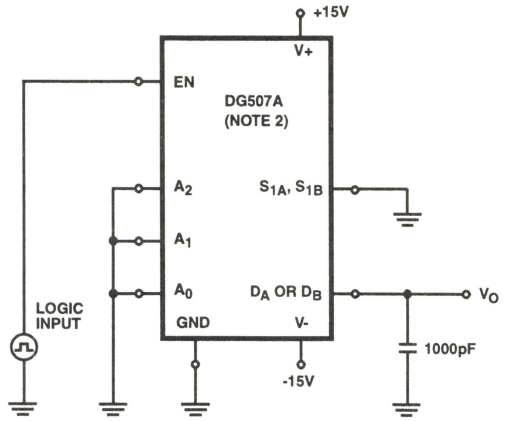
Test Circuits and Waveforms (Continued)



NOTE:

1. Similar connections for DG508A.

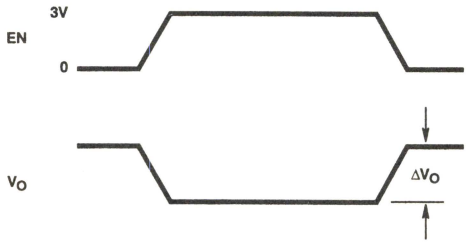
FIGURE 6A. CHARGE INJECTION TEST CIRCUIT



NOTE:

2. Similar connections for DG509A.

FIGURE 6B. CHARGE INJECTION TEST CIRCUIT



ΔV_O is the measured voltage error due to charge injection.
The error voltage in Coulombs is $Q = C_L \times \Delta V_O$.

FIGURE 6C. CHARGE INJECTION WAVEFORMS

Truth Tables

DG506A

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "0" = V_{AL}, $V_{ENL} \leq 0.8V$, Logic "1" = V_{AH}, $V_{ENH} \geq 2.4V$.

DG508A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2, EN
Logic "1" = $V_{AH} \geq 2.4V$, Logic "0" = $V_{AL} \leq 0.8V$

DG507A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = V_{AL}, $V_{ENL} \leq 0.8V$, Logic "1" = V_{AH}, $V_{ENH} \geq 2.4V$.

DG509A

A_1	A_0	EN	ON SWITCH
X	X	0	None
0	0	1	1A, 1B
0	1	1	2A, 2B
1	0	1	3A, 3B
1	1	1	4A, 4B

A_0, A_1, EN
Logic "1" = $V_{AH} \geq 2.4V$, Logic "0" = $V_{AL} \leq 0.8V$.

Die Characteristics

DIE DIMENSIONS:

3810µm x 2770µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

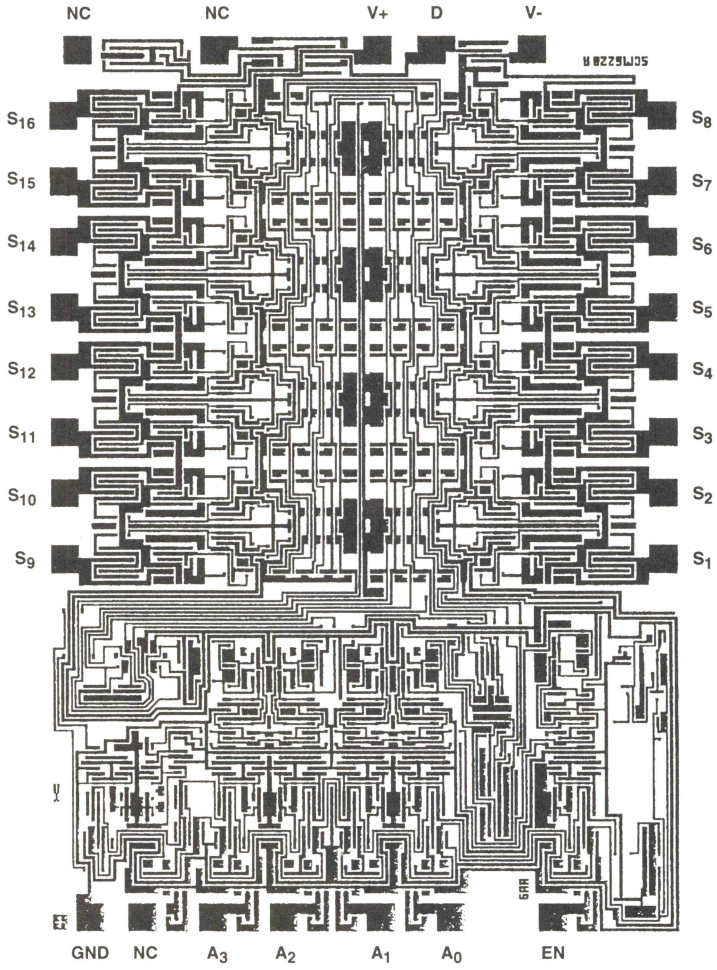
Type: PSG/Nitride
Thickness: PSG: 7kÅ ±1.4kÅ
Nitride: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG506A



Die Characteristics

DIE DIMENSIONS:

3810µm x 2770µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

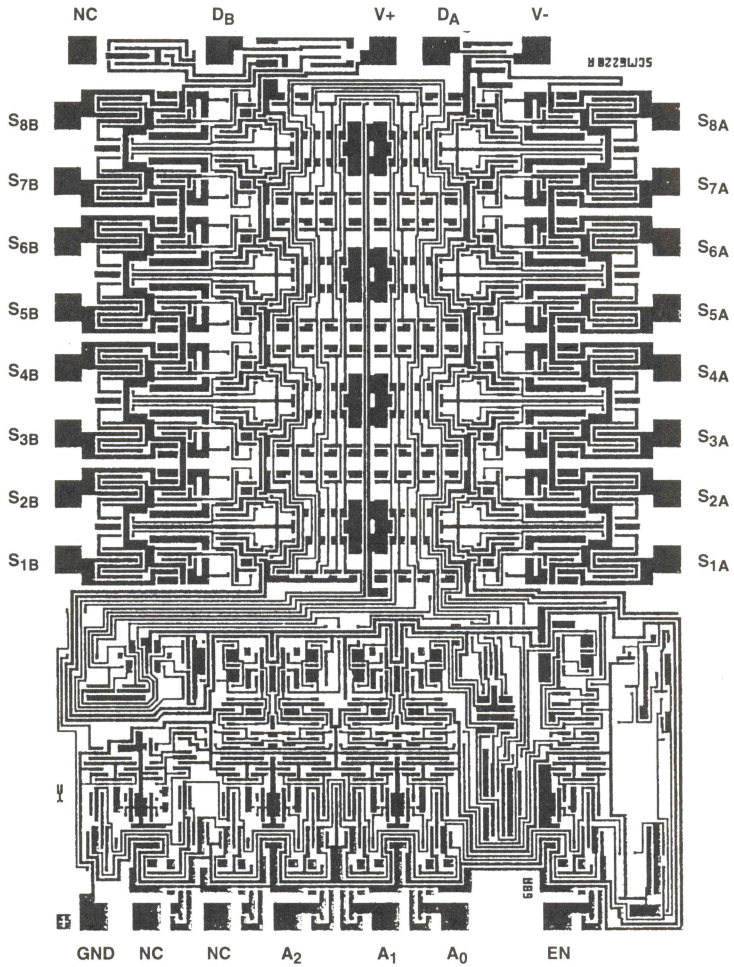
Type: PSG/Nitride
Thickness: PSG: 7kÅ ±1.4kÅ
Nitride: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG507A



Die Characteristics

DIE DIMENSIONS:

3100µm x 2083µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

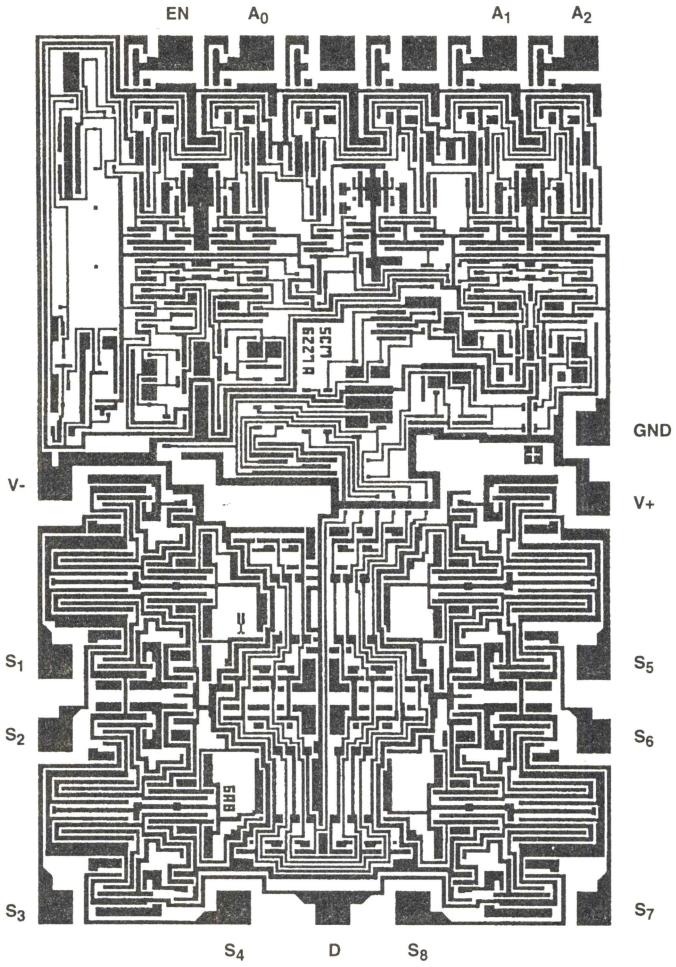
Type: PSG/Nitride
Thickness: PSG: 7kÅ ±1.4kÅ
Nitride: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG508A



Die Characteristics

DIE DIMENSIONS:

3100µm x 2083µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

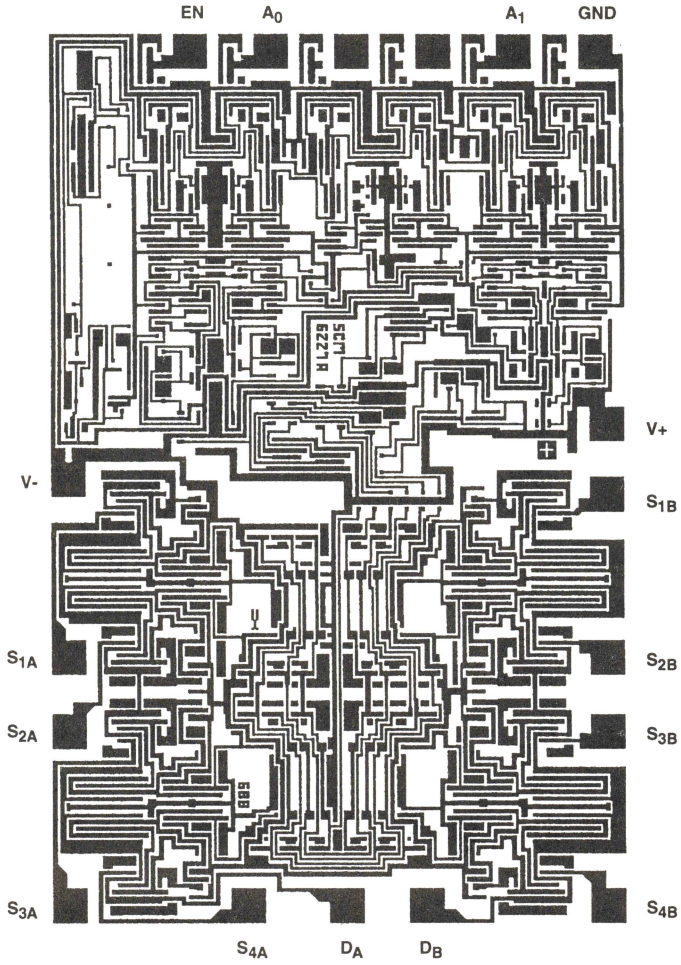
Type: PSG/Nitride
Thickness: PSG: 7kÅ ±1.4kÅ
Nitride: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG509A



HARRIS SEMICONDUCTOR HI-1818A, HI-1828A

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

Low Resistance, Single 8-Channel, and Differential 4-Channel, CMOS Analog Multiplexers

Features

- Signal Range ..... +15V
- "ON" Resistance 250Ω
- Input Leakage (Max) 50nA
- Access Time 350ns
- Power Consumption 5mW
- DTL/TTL Compatible Address
- Operation ..... -55°C to 125°C

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

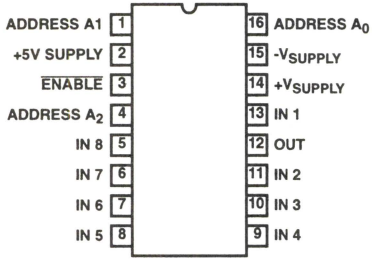
The HI-1818A and HI-1828A are monolithic, high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250Ω) assure optimum performance in low level or current mode applications.

The HI-1818A is a single-ended, 8-Channel multiplexer, while the HI-1828A is a differential 4-Channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

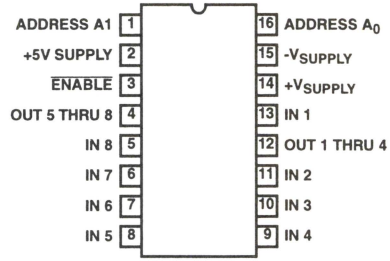
For MIL-STD-883 compliant parts, request the HI-1818A/883; HI-1828A/883 data sheet.

Pinouts

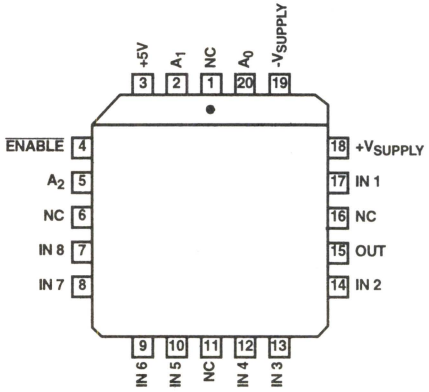
HI-1818A (CERDIP, PDIP)
TOP VIEW



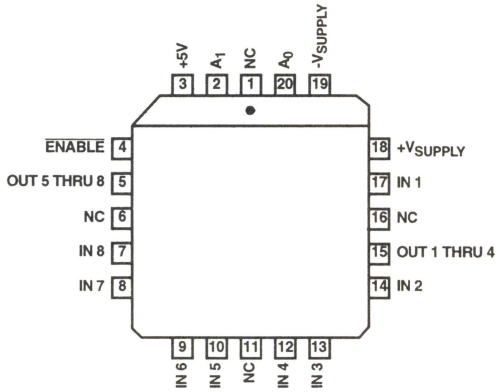
HI-1828A (CERDIP, PDIP)
TOP VIEW



HI-1818A (PLCC)
TOP VIEW



HI-1828A (CLCC, PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3141.1**

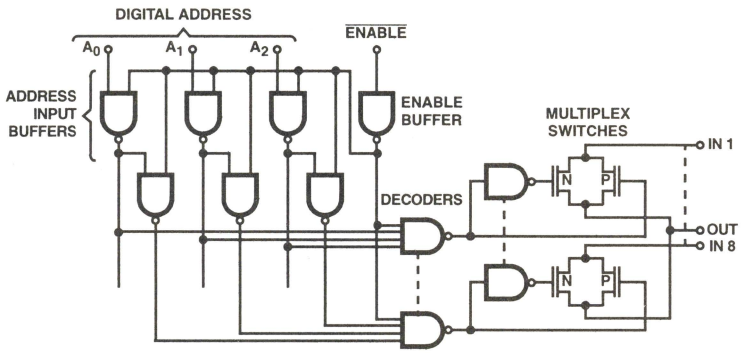
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3-1818A-5	0 to 75	16 Ld PDIP	E16.3
HI1-1818A-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-1818A-5	0 to 75	16 Ld CERDIP	F16.3
HI4P1818A-5	0 to 75	20 Ld PLCC	N20.35
HI1-1818A/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-1828A-5	0 to 75	16 Ld CERDIP	F16.3

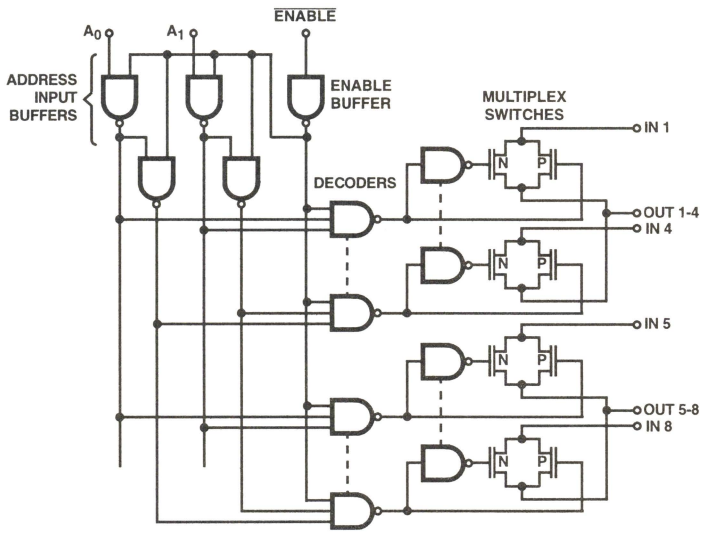
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-1828A-7	0 to 75 + 96 Hour Burn-In	16 Ld CERDIP	F16.3
HI3-1828A-5	0 to 75	16 Ld PDIP	E16.3
HI1-1828A-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-1828A/883	-55 to 125	16 Ld CERDIP	F16.3
HI4-1828A/883	-55 to 125	20 Ld CLCC	J20.A

Functional Block Diagrams

HI-1818A



HI-1828A



HARRIS SEMICONDUCTOR

HI-506, HI-507, HI-508, HI-509

Single 16 and 8/Differential 8-Channel and 4-Channel CMOS Analog Multiplexers

August 1997

Features

- Low ON Resistance 180Ω
- Wide Analog Signal Range ..... ±15V
- TTL/CMOS Compatible
- Access Time 250ns
- Maximum Power Supply 44V
- Break-Before-Make Switching
- No Latch-Up
- Replaces DG506A/DG506AA and DG507A/DG507AA
- Replaces DG508A/DG508AA and DG509A/DG509AA

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

The HI-506/HI-507 and HI-508/HI-509 monolithic CMOS multiplexers each include an array of sixteen and eight analog switches respectively, a digital decoder circuit for channel selection, voltage reference for logic thresholds, and an enable input for device selection when several multiplexers are present. The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latchup. DI also offers much lower substrate leakage and parasitic capacitance than conventional junction isolated CMOS (see Application Note AN521).

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for logic "1" and maximum 0.8V for logic "0". This allows direct interface without pullup resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and diode clamp to each supply.

The HI-506 is a single 16-Channel, the HI-507 is an 8-Channel differential, the HI-508 is a single 8-Channel and the HI-509 is a 4-Channel differential multiplexer. The HI-506/HI-507 are available in a 28 lead ceramic or plastic DIP, 28 pad leadless chip carrier (CLCC), 28 pin plastic leaded chip carrier (PLCC) and 28 lead SOIC packages. The HI-508/HI-509 are available in a 16 pin plastic or ceramic DIP, a 20 pin plastic leaded chip carrier (PLCC), 20 pad ceramic leadless chip carrier (CLCC) and 16 lead SOIC packages.

If input overvoltages are present, the HI-546/HI-547/HI-548/HI-549 multiplexers are recommended. For further information see Application Notes AN520 and AN521. The HI-506/HI-507/HI-508/HI-509 is offered in both commercial and military grades. For additional High Reliability Screening including 160 hour burn-in specify the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-506/883, HI-507/883, HI-508/883 or HI-509/883 data sheet.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3142.1**

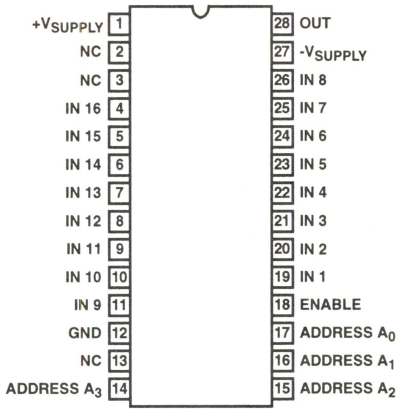
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0506/883	-55 to 125	28 Ld CERDIP	F28.6
HI1-0506-8	Hi-Rel Pressing with Burn-In	28 Ld CERDIP	F28.6
HI4-0506/883	-55 to 125	28 Ld CLCC	J28.A
HI1-0507/883	-55 to 125	28 Ld CERDIP	F28.6
HI9P0506-9	-40 to 85	28 Ld SOIC	M28.6
HI3-0506-5	0 to 75	28 Ld PDIP	E28.6
HI1-0506-7	0 to 75 + 96 Hour Burn-In	28 Ld CERDIP	F28.6
HI9P0506-5	0 to 75	28 Ld SOIC	M28.3
HI1-0506-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0506-4	-25 to 85	28 Ld CERDIP	F28.6
HI1-0506-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0507-8	Hi-Rel Pressing with Burn-In	28 Ld CERDIP	F28.6
HI4-0507/883	-55 to 125	28 Ld CLCC	J28.A
HI1-0507-4	-25 to 85	28 Ld CERDIP	F28.6
HI4P0507-5	0 to 75	28 Ld PLCC	N28.45
HI9P0507-5	0 to 75	28 Ld SOIC	M28.3
HI1-0507-5	0 to 75	28 Ld CERDIP	F28.6
HI3-0507-5	0 to 75	28 Ld PDIP	E28.3
HI9P0507-9	-40 to 85	28 Ld SOIC	M28.3
HI1-0507-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0508/883	-55 to 125	16 Ld CERDIP	F16.3

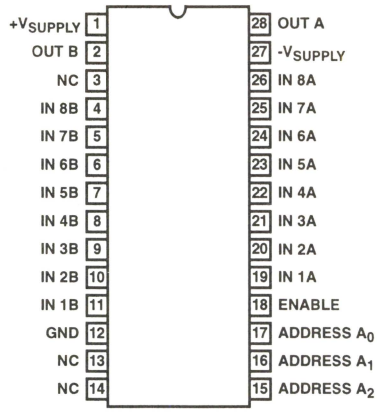
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0508-8	Hi-Rel Pressing with Burn-In	16 Ld CERDIP	F16.3
HI4-0508/883	-55 to 125	20 Ld CLCC	J20.A
HI1-0509/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-0508-5	0 to 75	16 Ld CERDIP	F16.3
HI3-0508-5	0 to 75	16 Ld PDIP	E16.3
HI1-0508-4	-25 to 85	16 Ld CERDIP	F16.3
HI1-0508-2	-55 to 125	16 Ld CERDIP	F16.3
HI4P0508-5	0 to 75	20 Ld PLCC	N20.35
HI9P0508-9	-40 to 85	16 Ld SOIC	M16.15
HI9P0508-5	0 to 75	16 Ld SOIC	M16.15
HI1-0509-8	Hi-Rel Pressing with Burn-In	16 Ld CERDIP	F16.3
HI4-0509/883	-55 to 125	20 Ld CLCC	J20.A
HI9P0509-5	0 to 75	16 Ld SOIC	M16.15
HI9P0509-9	-40 to 85	16 Ld SOIC	M16.15
HI1-0509-4	-25 to 85	16 Ld CERDIP	F16.3
HI1-0509-5	0 to 75	16 Ld CERDIP	F16.3
HI3-0509-5	0 to 75	16 Ld PDIP	E16.3
HI4P0509-5	0 to 75	20 Ld PLCC	N20.35
HI1-0509-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0509-7	0 to 75 + 96 Hour Burn-In	16 Ld CERDIP	F16.3

Pinouts

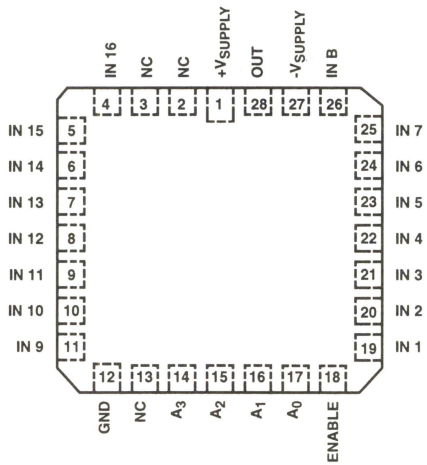
HI-506
(PDIP, CERDIP, SOIC)
TOP VIEW



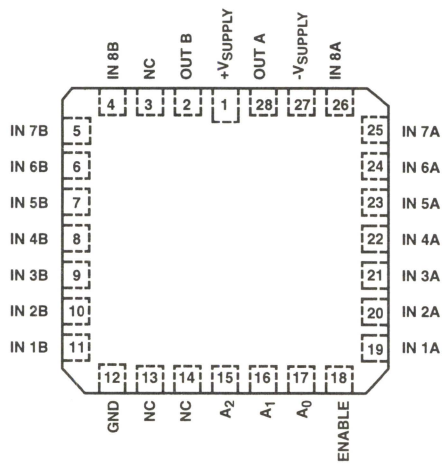
HI-507
(PDIP, CERDIP, SOIC)
TOP VIEW



HI-506
(CLCC, PLCC)
TOP VIEW

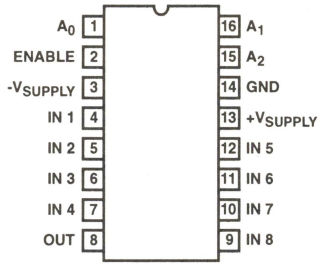


HI-507
(CLCC, PLCC)
TOP VIEW

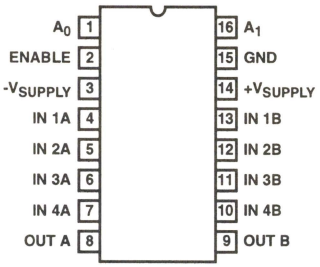


Pinouts (Continued)

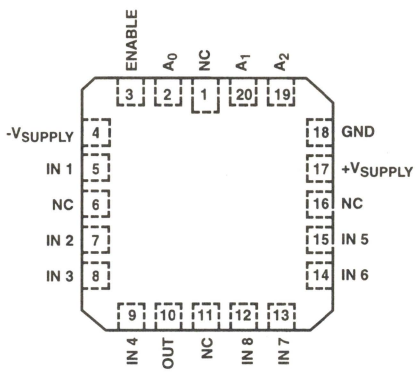
HI-508
(PDIP, CERDIP, SOIC)
TOP VIEW



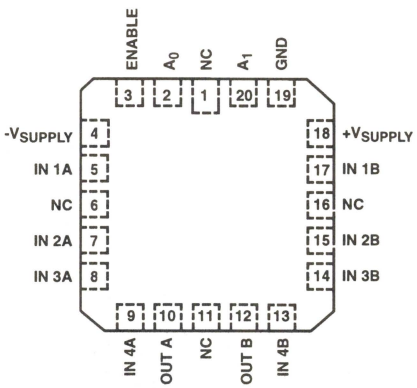
HI-509
(PDIP, CERDIP, SOIC)
TOP VIEW



HI-508
(CLCC, PLCC)
TOP VIEW

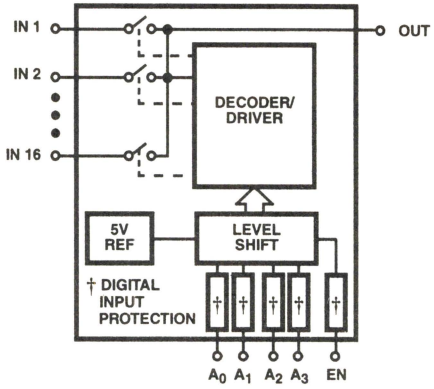


HI-509
(CLCC, PLCC)
TOP VIEW

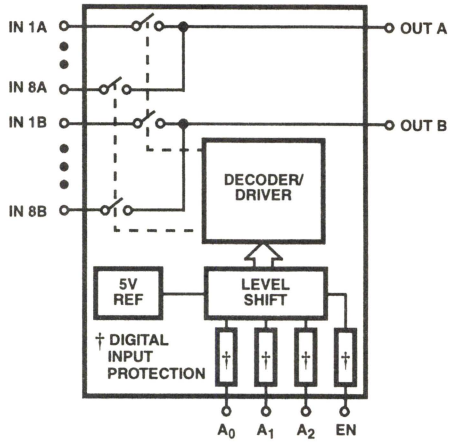


Functional Diagrams

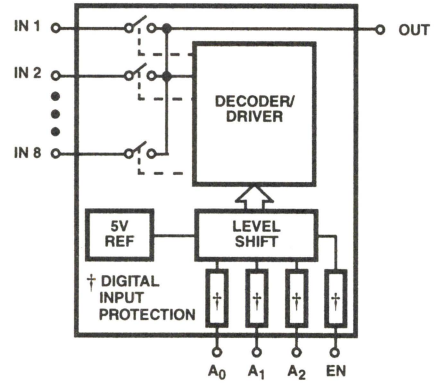
HI-506



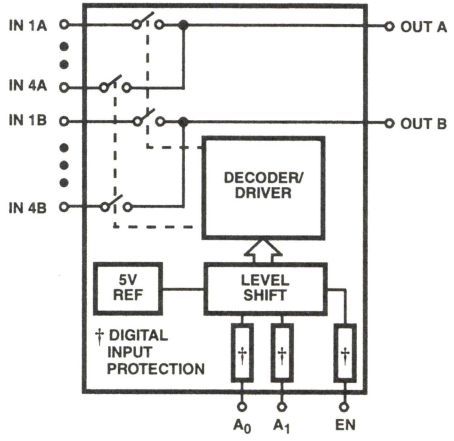
HI-507



HI-508

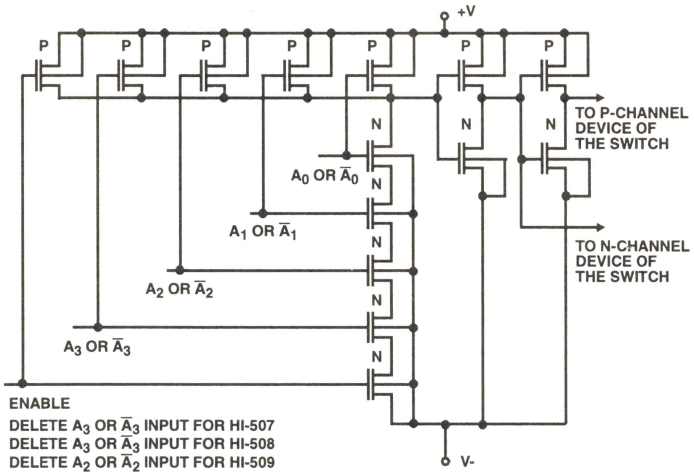


HI-509



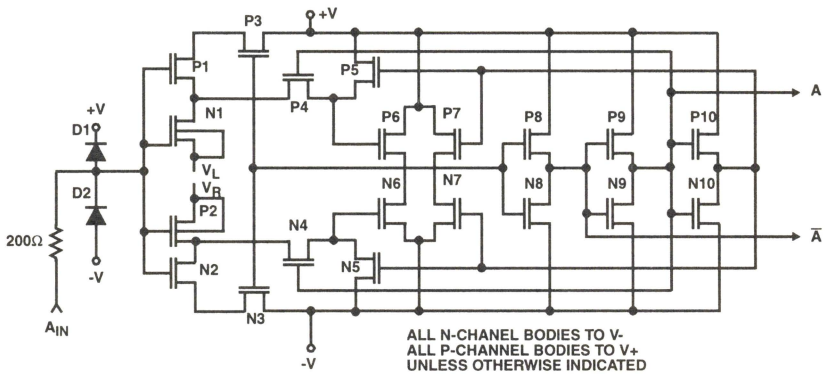
Schematic Diagrams

ADDRESS DECODER

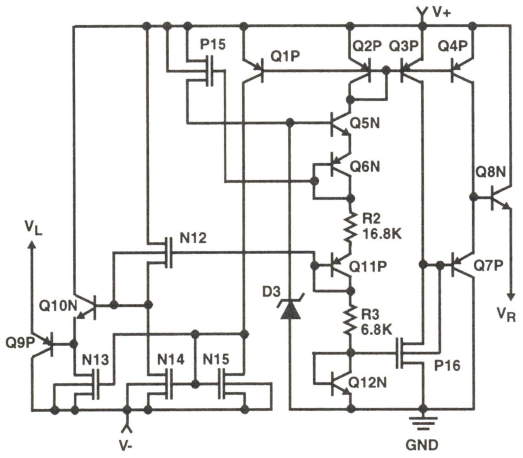


DELETE A_3 OR $\bar{A}_3$ INPUT FOR HI-507
DELETE A_3 OR $\bar{A}_3$ INPUT FOR HI-508
DELETE A_2 OR $\bar{A}_2$ INPUT FOR HI-509

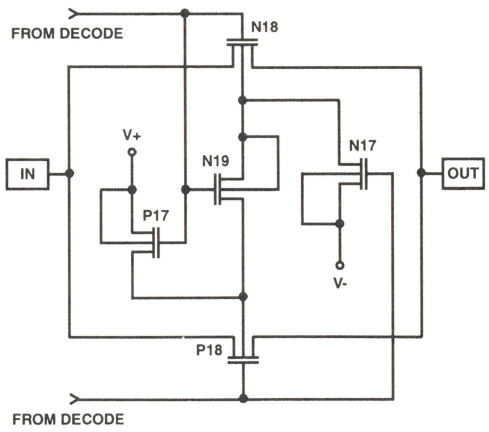
ADDRESS INPUT BUFFER LEVER SHIFTER



TTL REFERENCE CIRCUIT



MULTIPLEX SWITCH



Absolute Maximum Ratings

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ . . . . . +44V
$V_{SUPPLY(+)}$ to GND . . . . . +22V
$V_{SUPPLY(-)}$ to GND. . . . . -25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ . . . . . $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ . . . . . $-V_{SUPPLY}$ -4V
or 20mA, Whichever Occurs First
Analog Signal Overvoltage (Note 7)
$+V_S$ . . . . . $+V_{SUPPLY}$ +2V
$-V_S$ . . . . . $-V_{SUPPLY}$ -2V
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed at 1ms, 10% Duty Cycle Max)

Operating Conditions

Temperature Ranges
HI-506/507/508/509-2, -8 . . . . . -55^oC to 125^oC
HI-506/507/508/509-4 . . . . . -25^oC to 85^oC
HI-506/507/508/509-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
16 Ld CERDIP Package	85	32
16 Ld SOIC Package	115	N/A
16 Ld PDIP Package	100	N/A
20 Ld CLCC Package	80	28
20 Ld PLCC Package	80	N/A
28 Ld CERDIP Package	55	18
28 Ld PDIP Package	60	N/A
28 Ld SOIC Package	70	N/A
28 Ld CLCC Package	70	20
28 Ld PLCC Package	70	N/A

Maximum Junction Temperature
Ceramic Package . . . . . 175^oC
Plastic Package . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC and PLCC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves

PARAMETER	TEST CONDITIONS	TEMP (^oC)	HI-5XX-2, HI-5XX-8			HI-5XX-4, HI-5XX-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, t_A	(Note 1)	25	-	250	500	-	250	-	ns
		Full	-	-	1000	-	-	1000	ns
Break-Before-Make Delay, t_{OPEN}	(Note 1)	25	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$	(Note 1)	25	-	250	500	-	250	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$	(Note 1)	25	-	250	500	-	250	-	ns
		Full	-	-	1000	-	-	1000	ns
Settling Time to 0.1%, t_S (HI-506 and HI-507)		25	-	1.2	-	-	1.2	-	µs
Settling Time to 0.01%, t_S (HI-506 and HI-507)		25	-	2.4	-	-	2.4	-	µs
Settling Time to 0.1%, t_S (HI-508 and HI-509)		25	-	360	-	-	360	-	ns
Settling Time to 0.01%, t_S (HI-508 and HI-509)		25	-	600	-	-	600	-	ns
"Off Isolation"	(Note 5)	25	50	68	-	50	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	10	-	-	10	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-506)		25	-	52	-	-	52	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-507)		25	-	30	-	-	30	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-508)		25	-	17	-	-	17	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-509)		25	-	12	-	-	12	-	pF

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-5XX-2, HI-5XX-8			HI-5XX-4, HI-5XX-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Digital Input Capacitance, C_A		25	-	6	-	-	6	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$		25	-	0.08	-	-	0.08	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL}	(Note 1)	Full	-	-	+0.8	-	-	+0.8	V
Input High Threshold, V_{AH}	(Note 1)	Full	+2.4	-	-	+2.4	-	-	V
Input Leakage Current (High or Low), I_A	(Notes 1, 4)	Full	-	-	1.0	-	-	1.0	µA
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_S		Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON}	(Notes 1, 2)	25	-	180	300	-	180	400	Ω
Δr_{ON}, (Any Two Channels)		25	-	5	-	-	5	-	%
Off Input Leakage Current, $I_{S(OFF)}$	(Note 3)	25	-	0.03	-	-	0.03	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$	(Note 3)	25	-	0.3	-	-	0.3	-	nA
HI-506		Full	-	-	300	-	-	300	nA
HI-507		Full	-	-	200	-	-	200	nA
HI-508		Full	-	-	200	-	-	200	nA
HI-509		Full	-	-	100	-	-	100	nA
On Channel Leakage Current, $I_{D(ON)}$	(Note 3)	25	-	0.3	-	-	0.3	-	nA
HI-506		Full	-	-	300	-	-	300	nA
HI-507		Full	-	-	200	-	-	200	nA
HI-508		Full	-	-	200	-	-	200	nA
HI-509		Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current, I_{DIFF} (HI-507, HI-509 Only)	(Note 1)	Full	-	-	50	-	-	50	nA
POWER REQUIREMENTS									
Current, I+, Pin 1 HI-506/HI-507	(Note 6)	Full	-	1.5	3.0	-	1.5	3.0	mA
Current, I+, HI-508/HI-509	(Note 6)	Full	-	1.5	2.4	-	1.5	2.4	mA
Current, I-, Pin 27 HI-506/HI-507	(Note 6)	Full	-	0.4	1.0	-	0.4	1.0	mA
Current, I-, HI-508/HI-509	(Note 6)	Full	-	0.4	1.0	-	0.4	1.0	mA
Power Dissipation, P_D									
HI-506/HI-507		Full	-	-	60	-	-	60	mW
HI-508/HI-509		Full	-	-	51	-	-	51	mW

NOTES:

1. 100% tested for Dash 8. Leakage currents not tested at -55°C.
2. $V_{OUT} = \pm 10V$, $I_{OUT} = \mp 1mA$.
3. 10nA is the practical lower limit for high speed measurement in the production test environment.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
5. $V_{EN} = 0.8V$, $R_L = 1K$, $C_L = 15pF$, $V_S = 7V_{RMS}$, f = 100kHz.
6. V_{EN}, $V_A = 0V$ or 2.4V.
7. Signal voltage at any analog input or output (S or D) will be clamped to the supply rail by internal diodes. Limit the resulting current as shown under absolute maximum ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the Harris HI-546/HI-547/HI-548/HI-549 multiplexers are recommended.

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$, Unless Otherwise Specified

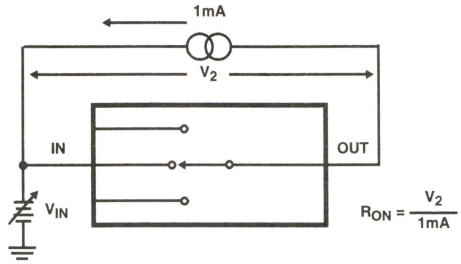


FIGURE 1A. TEST CIRCUIT

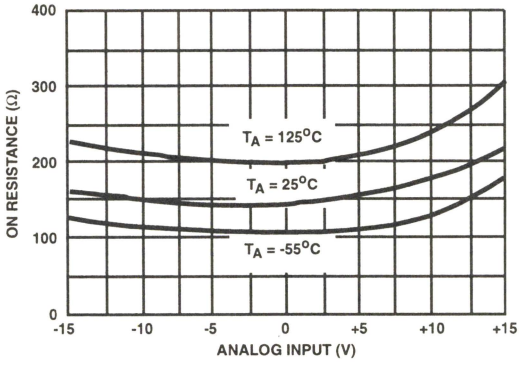


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE, TEMPERATURE

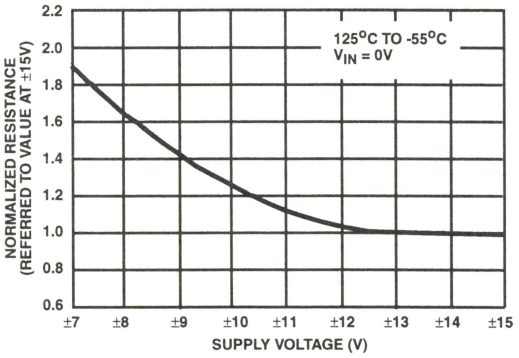


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

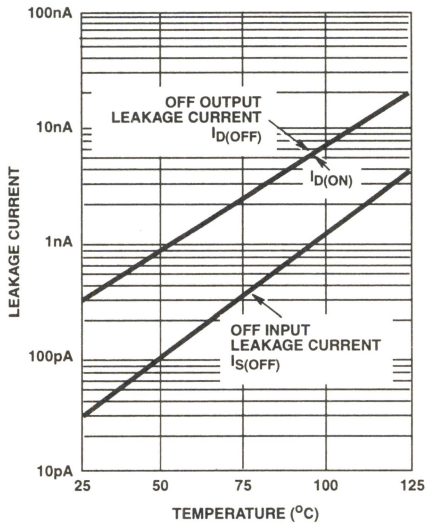


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

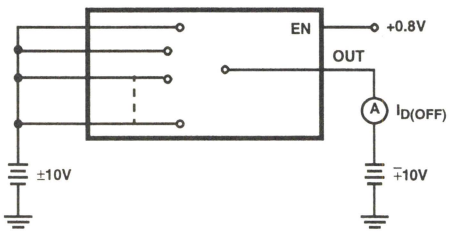


FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$, Unless Otherwise Specified (Continued)

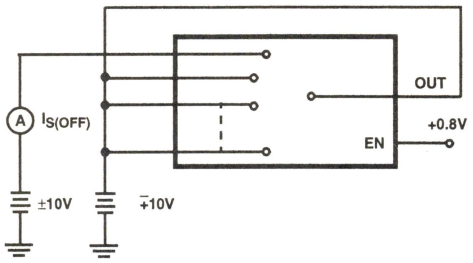


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT

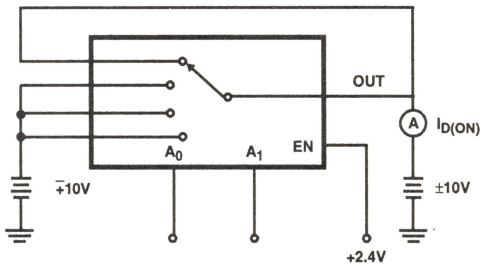


FIGURE 2D. $I_{D(ON)}$ TEST CIRCUIT

FIGURE 2. ON RESISTANCE

NOTE:

1. Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$ +10V/-10V and -10V/+10V.)

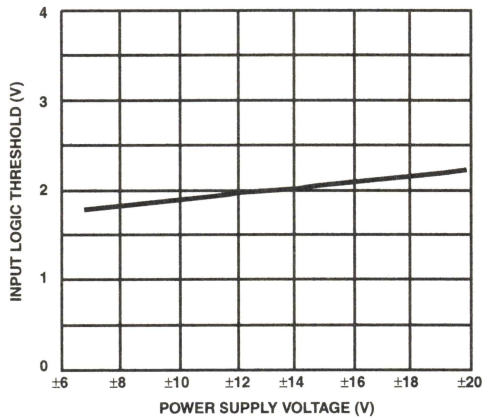


FIGURE 3. LOGIC THRESHOLD vs POWER SUPPLY VOLTAGE

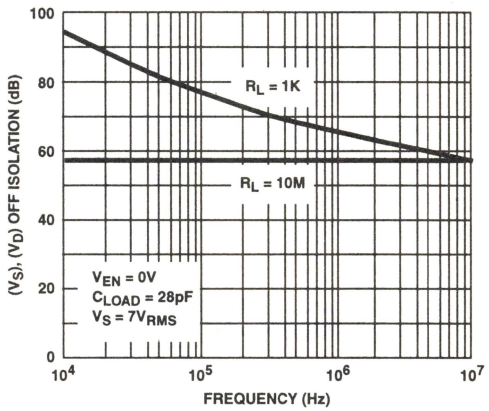


FIGURE 4. OFF ISOLATION vs FREQUENCY

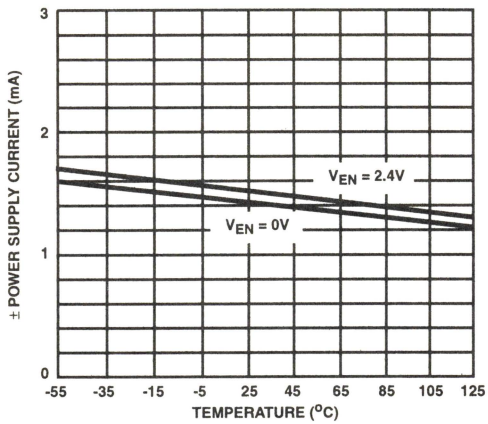


FIGURE 5A. HI-506/HI-507

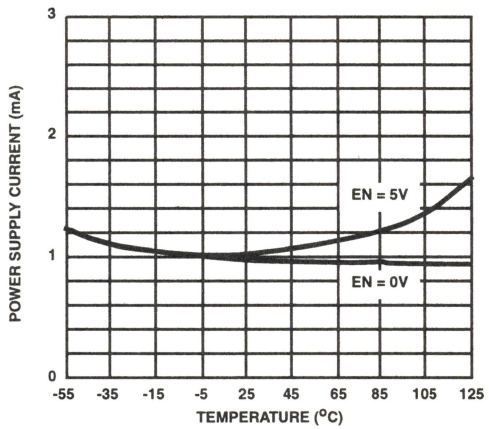


FIGURE 5B. HI-508/HI-509

FIGURE 5. POWER SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$, Unless Otherwise Specified (Continued)

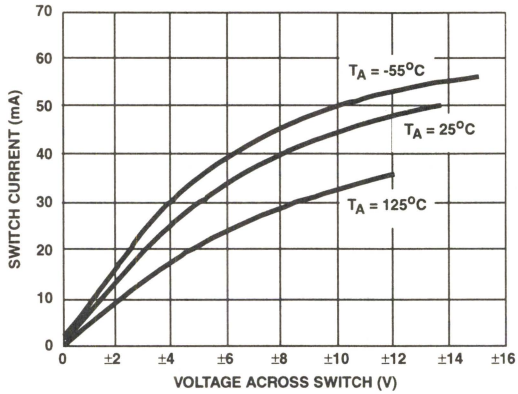


FIGURE 6A. ON CHANNEL CURRENT vs VOLTAGE

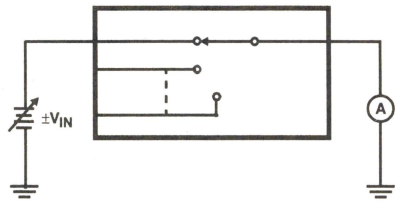


FIGURE 6B. TEST CIRCUIT

FIGURE 6. ON CHANNEL CURRENT vs VOLTAGE

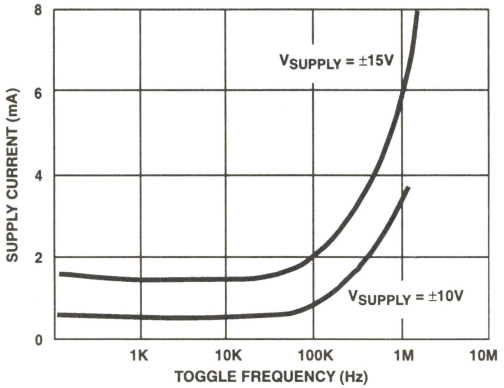


FIGURE 7A. SUPPLY CURRENT vs TOGGLE FREQUENCY

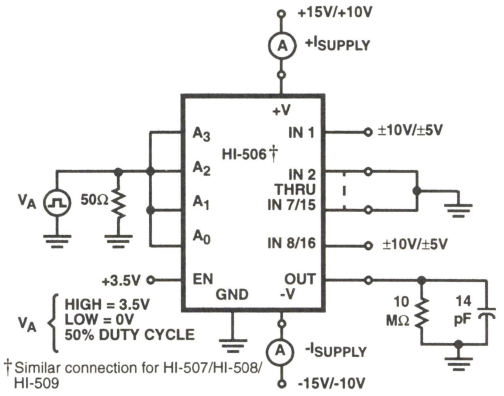


FIGURE 7B. TEST CIRCUIT

FIGURE 7. SUPPLY CURRENT

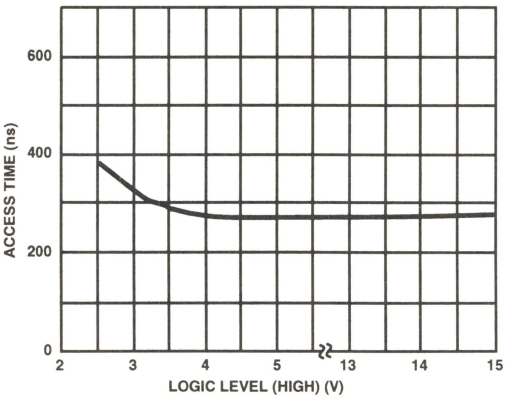


FIGURE 8A. ACCESS TIME vs LOGIC LEVEL (HIGH)

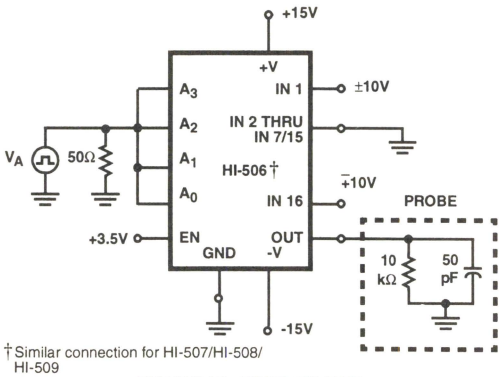


FIGURE 8B. TEST CIRCUIT

Switching Waveforms

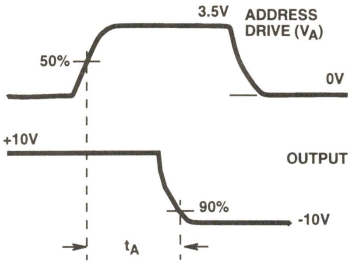


FIGURE 8C. WAVEFORMS

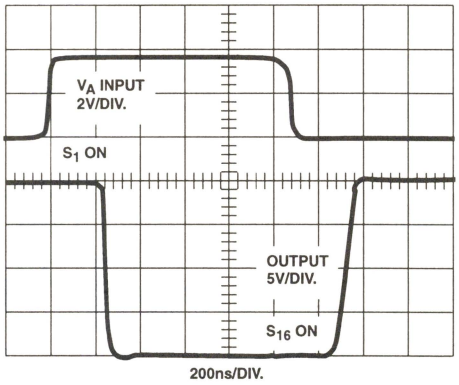
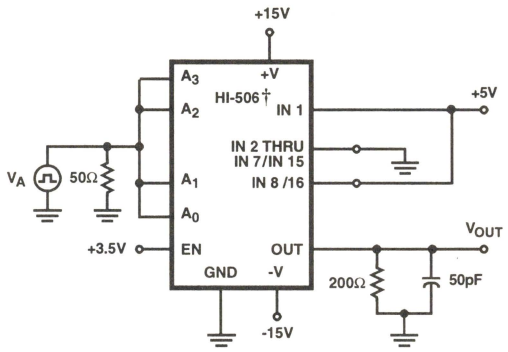


FIGURE 8D. ACCESS TIME

FIGURE 8. ACCESS TIME



† Similar connection for HI-507/HI-508/HI-509

FIGURE 9A. TEST CIRCUIT

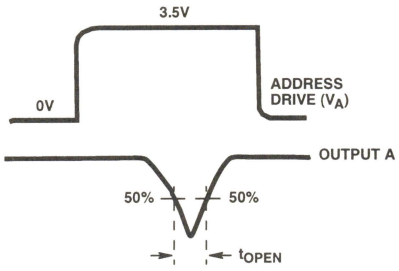


FIGURE 9B. WAVEFORMS

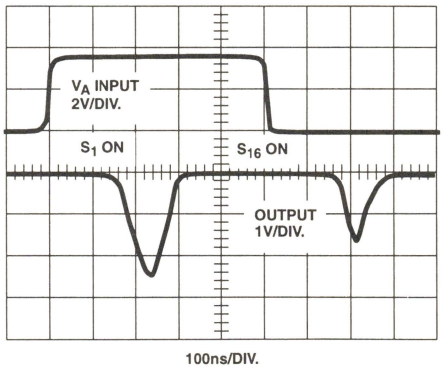
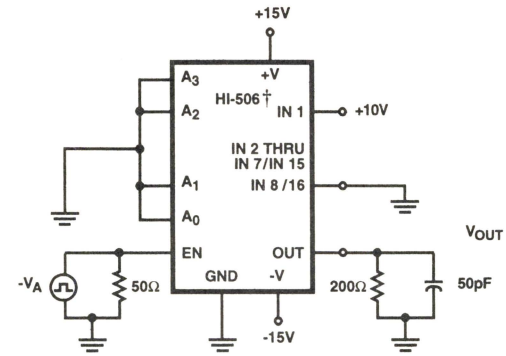


FIGURE 9C. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

FIGURE 9. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

Switching Waveforms (Continued)



†Similar connection for HI-507/HI-508/HI-509

FIGURE 10A. TEST CIRCUIT

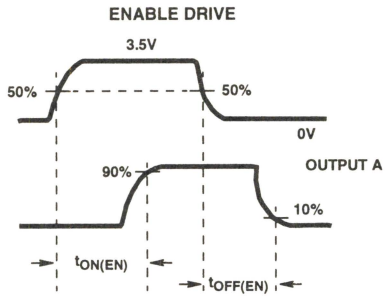


FIGURE 10B. WAVEFORMS

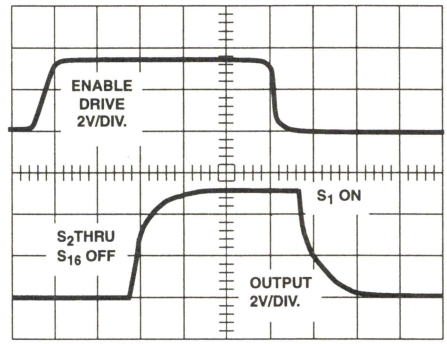


FIGURE 10C. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

FIGURE 10. ENABLE DELAY

Truth Tables

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-508

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Die Characteristics

DIE DIMENSIONS:

129 mils x 82 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride/Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

421

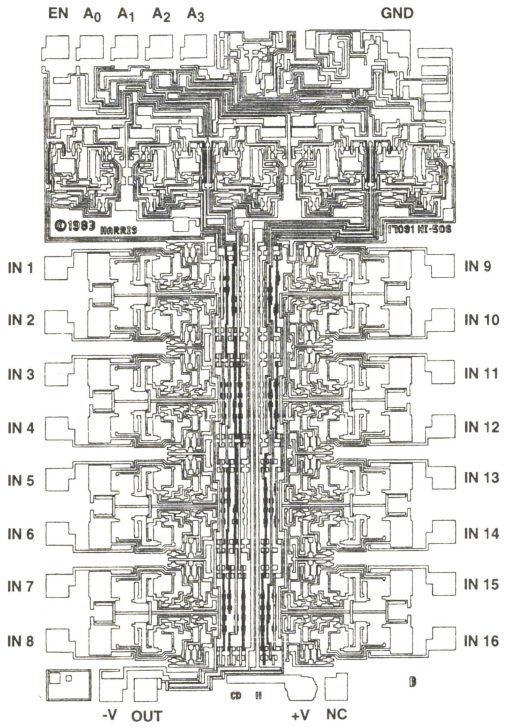
PROCESS:

CMOS-DI

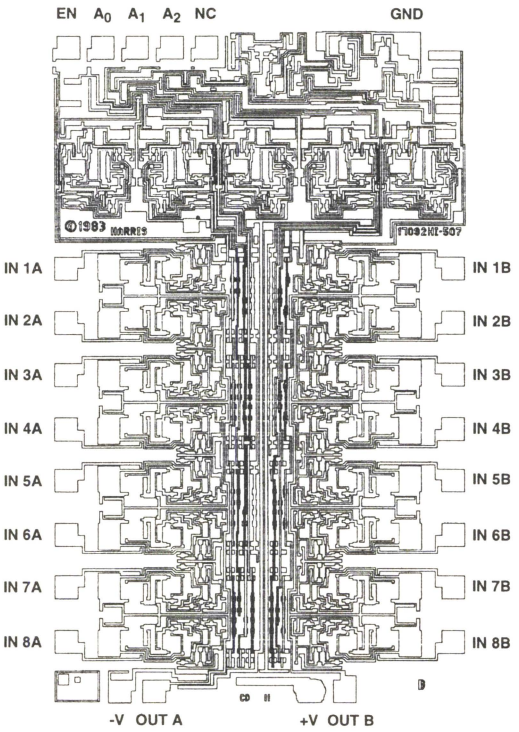
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layout

HI-506



HI-507



NOTE: Pad numbers correspond to DIP pin numbers only.

Die Characteristics

DIE DIMENSIONS:

81.9 mils x 90.2 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride/Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

234

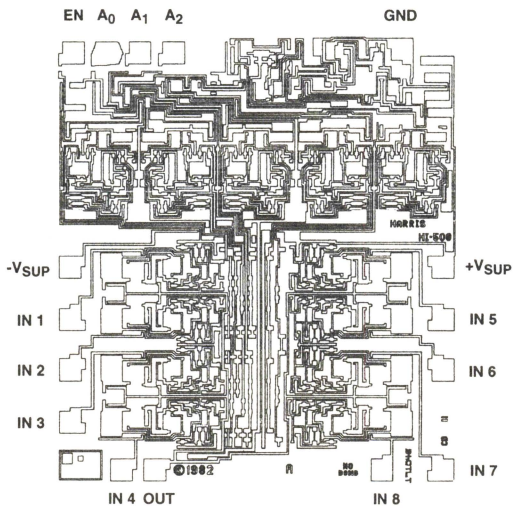
PROCESS:

CMOS-DI

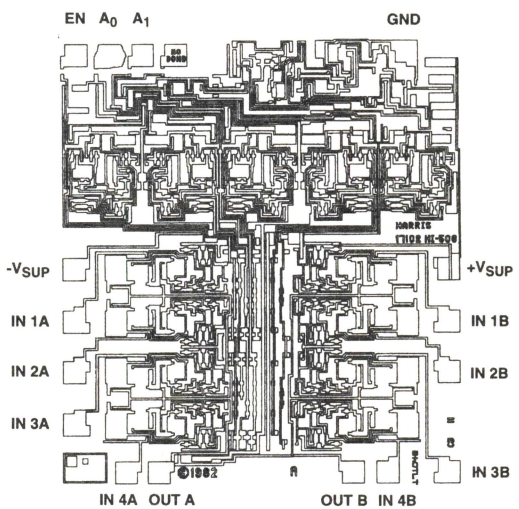
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layout

HI-508



HI-509



NOTE: Pad numbers correspond to DIP pin numbers only.

HARRIS SEMICONDUCTOR

HI-506A, HI-507A HI-508A, HI-509A

16-Channel, 8-Channel, Differential 8-Channel and Differential 4-Channel, CMOS Analog MUXs with Active Overvoltage Protection

August 1997

Features

- Analog Overvoltage ..... $70V_{P-P}$
- No Channel Interaction During Overvoltage
- Maximum Power Supply 44V
- Fail Safe with Power Loss (No Latch-Up)
- Break-Before-Make Switching
- Analog Signal Range..... ±15V
- Access Time 500ns
- Power Dissipation 7.5mW

Applications

- Data Acquisition Systems
- Industrial Controls
- Telemetry

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI1-0506A-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0506A-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0506A-8	-55 to 125 + 160 Hour Burn-In	28 Ld CERDIP	F28.6
HI3-0506A-5	0 to 75	28 Ld PDIP	E28.6
HI1-0507A-8	-55 to 125 + 160 Hour Burn-In	28 Ld CERDIP	F28.6
HI3-0507A-5	0 to 75	28 Ld PDIP	E28.6
HI1-0508A-7	0 to 75 + 96 Hour Burn-In	16 Ld CERDIP	F16.3
HI1-0508A-8	-55 to 125 + 160 Hour Burn-In	16 Ld CERDIP	F16.3
HI3-0508A-5	+0 to 75	16 Ld PDIP	E16.3
HI1-0509A-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0509A-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0509A-7	0 to 75 + 96 Hour Burn-In	16 Ld CERDIP	F16.3
HI1-0509A-8	-55 to 125 + 160 Hour Burn-In	16 Ld CERDIP	F16.3
HI3-0509A-5	0 to 75	16 Ld PDIP	E16.3

Description

The HI-506A, HI-507A, HI-508A and HI-509A are analog multiplexers with active overvoltage protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant $70V_{P-P}$ levels with ±15V supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents 1kΩ of resistance under this condition. These features make the HI-506A, HI-507A, HI-508A and HI-509A ideal for use in systems where the analog inputs originate from external equipment, or separately powered circuitry. All devices are fabricated with 44V dielectrically isolated CMOS technology. The HI-506A is a single 16 channel multiplexer, the HI-507A is an 8-Channel differential multiplexer, the HI-508A is a single 8 channel multiplexer and the HI-509A is a differential 4-Channel multiplexer. If input overvoltage protection is not needed the HI-506/507/508/509 multiplexers are recommended. For further information see Application Notes AN520 and AN521.

The HI-506A/507A devices are available in a 28 lead Plastic or Ceramic DIP and the HI-508A/509A devices are available in a 16 lead Plastic or Ceramic DIP package.

The HI-50XA are offered in industrial/commercial and military grades, additional Hi-Rel screening including 160 hour burn-in is specified by the "8" suffix. For MIL-STD-883 compliant parts, request the HI-546/883, HI-547/883, HI-548/883 or HI-549/883 data sheets.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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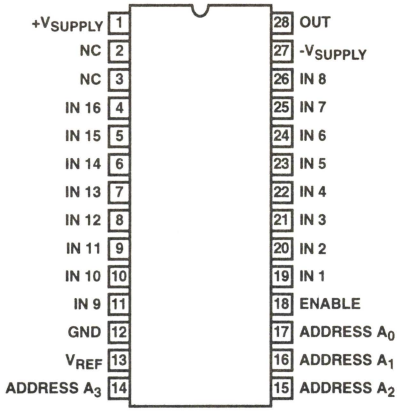
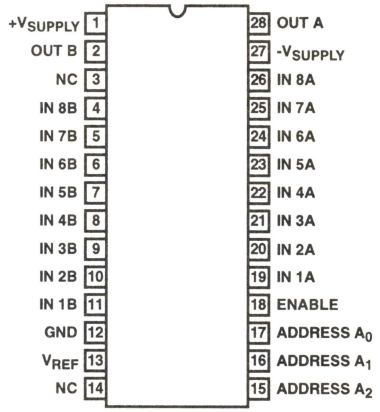
File Number **3143.1**

Pinouts

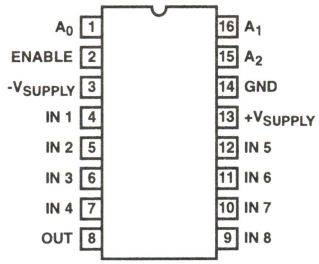
HI1-506A (CERDIP)
HI3-506A (PDIP)
TOP VIEW



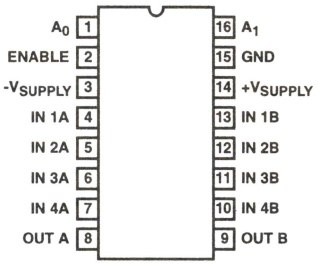
HI1-507A (CERDIP)
HI3-507A (PDIP)
TOP VIEW



HI1-508A (CERDIP)
HI3-508A (PDIP)
TOP VIEW

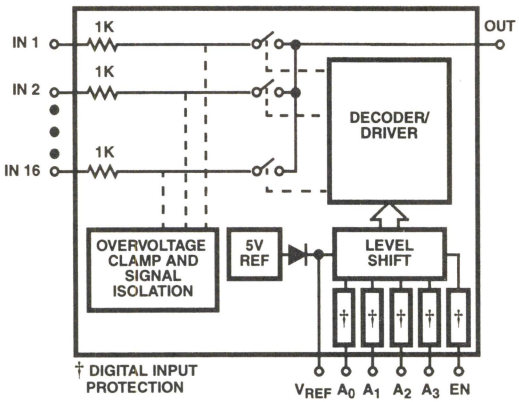


HI1-509A (CERDIP)
HI3-509A (PDIP)
TOP VIEW

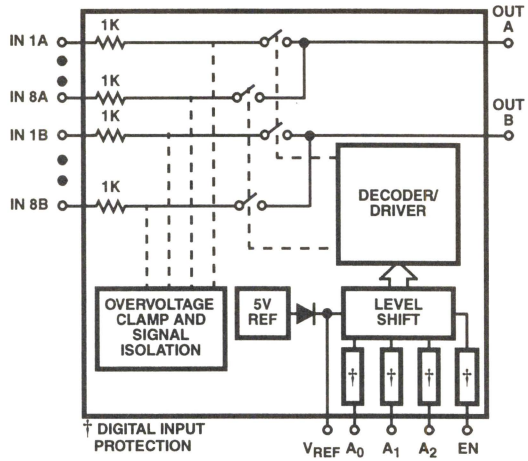


Functional Diagrams

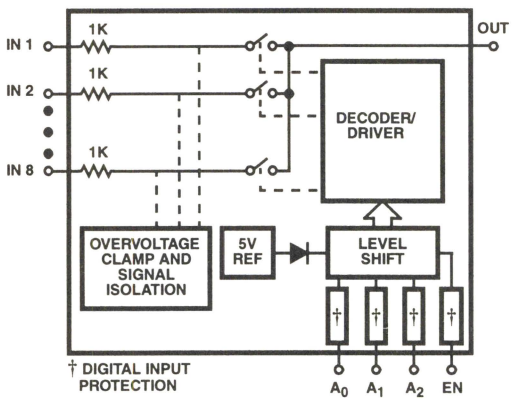
HI-506A



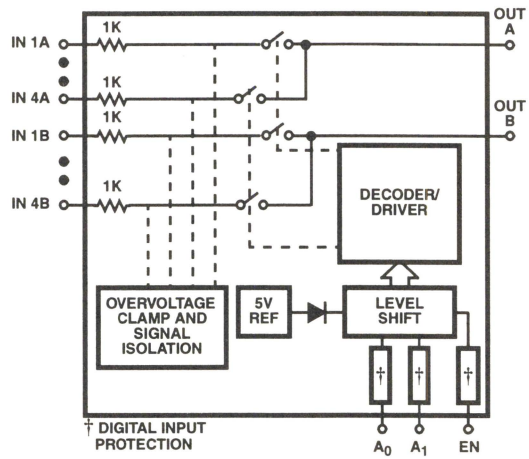
HI-507A



HI-508A

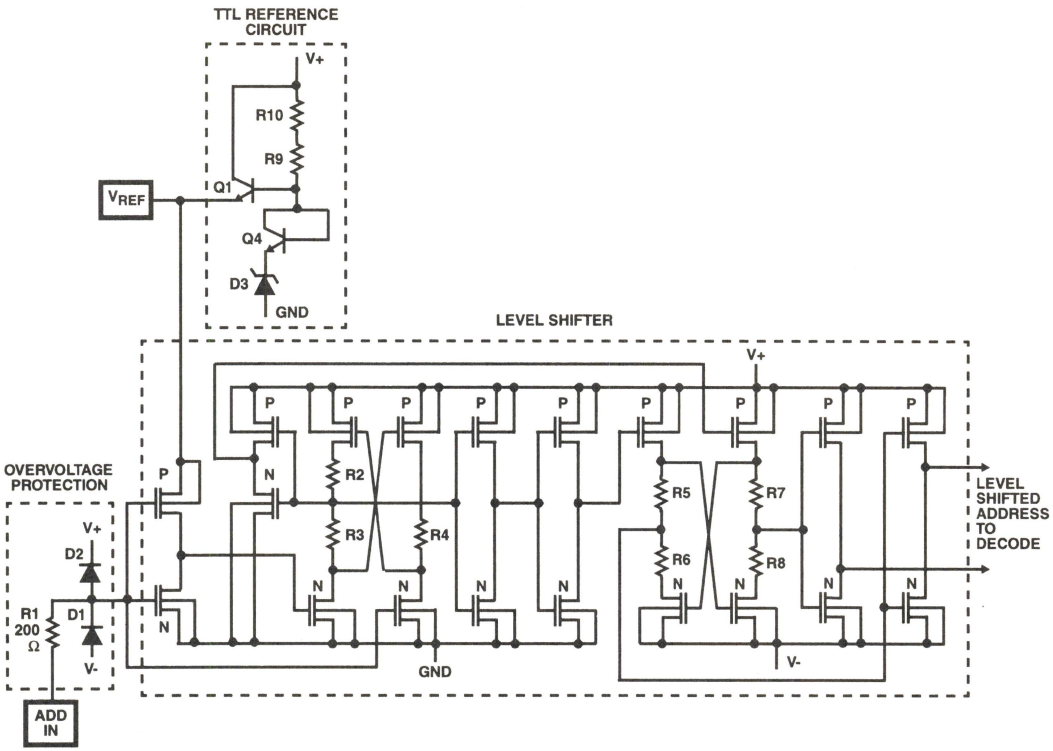


HI-509A

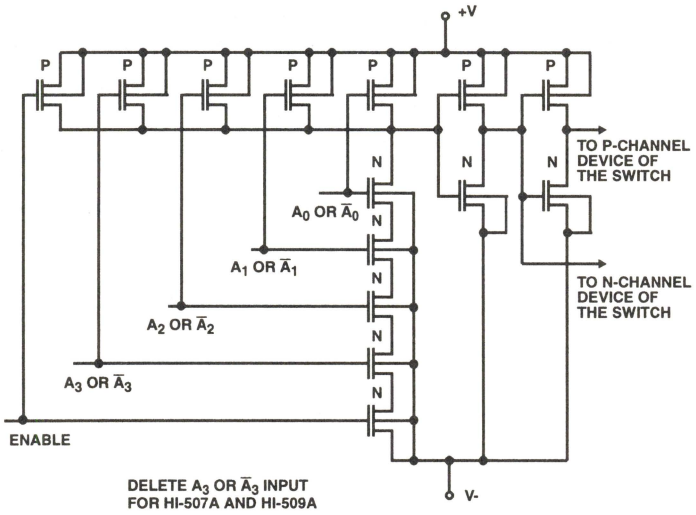


Schematic Diagrams

ADDRESS INPUT BUFFER AND LEVEL SHIFTER

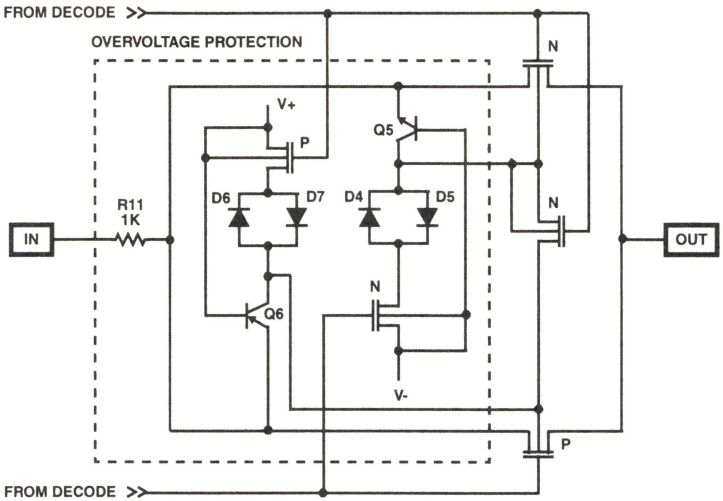


ADDRESS DECODER



Schematic Diagrams (Continued)

MULTIPLEX SWITCH



Absolute Maximum Ratings

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ . . . . . +44V
$V_{SUPPLY(+)}$ to GND . . . . . +22V
$V_{SUPPLY(-)}$ to GND . . . . . +25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ . . . . . $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ . . . . . $-V_{SUPPLY}$ -4V
or 20mA, Whichever Occurs First
Analog Signal Overvoltage
$+V_S$ . . . . . $+V_{SUPPLY}$ +20V
$-V_S$ . . . . . $-V_{SUPPLY}$ -20V
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
Pulsed at 1ms, 10% Duty Cycle (Max)

Operating Conditions

Temperature Ranges
HI-506A/507A/508A/509A-2, -8 . . . . . -55^oC to 125^oC
HI-506A/507A/508A/509A-5, -7 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
28 Ld CERDIP Package (HI-506A, HI-507A)	55	18
16 Ld CERDIP Package (HI-508A, HI-509A)	85	32
28 Ld PDIP Package (HI-506A, HI-507A)	60	N/A
16 Ld PDIP Package (HI-508A, HI-509A)	100	N/A

Maximum Junction Temperature
CERDIP Package . . . . . 175^oC
PDIP Package . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves

PARAMETER	TEMP (^oC)	HI-50XA-2, -8			HI-50XA-5, -7			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS								
Access Time, t_A (Note 2)	25	-	0.5	-	-	0.5	-	µs
	Full	-	-	1.0	-	-	1.0	µs
Break-Before-Make Delay, t_{OPEN} (Note 2)	25	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$ (Note 2)	25	-	300	500	-	300	-	ns
	Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$ (Note 2)	25	-	300	500	-	300	-	ns
	Full	-	-	1000	-	-	1000	ns
Settling Time to 0.1%, t_S (HI-506A and HI-507A)	25	-	1.2	-	-	1.2	-	µs
Settling Time to 0.01%, t_S (HI-506A and HI-507A)	25	-	3.5	-	-	3.5	-	µs
Settling Time to 0.1%, t_S (HI-508A and HI-509A)	25	-	1.2	-	-	1.2	-	µs
Settling Time to 0.01%, t_S (HI-508A and HI-509A)	25	-	3.5	-	-	3.5	-	µs
"Off Isolation" (Note 7)	25	50	68	-	50	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$	25	-	12	-	-	12	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-506A)	25	-	52	-	-	52	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-507A)	25	-	30	-	-	30	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-508A)	25	-	25	-	-	25	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-509A)	25	-	12	-	-	12	-	pF
Digital Input Capacitance, C_A	25	-	10	-	-	10	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$	25	-	0.1	-	-	0.1	-	pF
DIGITAL INPUT CHARACTERISTICS								
Input Low Threshold, TTL Drive, V_{AL} (Note 2)	Full	-	-	+0.8	-	-	+0.8	V
Input High Threshold, V_{AH} (Notes 2, 9)	Full	+4.0	-	-	+4.0	-	-	V

Electrical Specifications Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves **(Continued)**

PARAMETER	TEMP (°C)	HI-50XA-2, -8			HI-50XA-5, -7			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Leakage Current (High or Low), I_A (Notes 2, 6)	Full	-	-	1.0	-	-	1.0	µA
MOS Drive, V_{AL}, HI-506A/HI-507A (Note 10)	25	-	-	0.8	-	-	0.8	V
MOS Drive, V_{AH}, HI-506A/HI-507A (Note 10)	25	6.0	-	-	6.0	-	-	V
ANALOG CHANNEL CHARACTERISTICS								
Analog Signal Range, V_S (Note 2)	Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON}, (Notes 2, 3)	25	-	1.2	1.5	-	1.5	1.8	kΩ
	Full	-	1.5	1.8	-	1.8	2.0	kΩ
Off Input Leakage Current, $I_{S(OFF)}$ (Notes 2, 4)	25	-	0.03	-	-	0.03	-	nA
	Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$ (Notes 2, 4)	25	-	0.1	-	-	0.1	-	nA
HI-506A	Full	-	-	300	-	-	300	nA
HI-507A	Full	-	-	200	-	-	200	nA
HI-508A	Full	-	-	200	-	-	200	nA
HI-509A	Full	-	-	100	-	-	100	nA
With Input Overvoltage Applied, $I_{D(OFF)}$ (Note 5)	25	-	4.0	-	-	4.0	-	nA
	Full	-	-	2.0	-	-	-	µA
On Channel Leakage Current, $I_{D(ON)}$ (Notes 2, 4)	25	-	0.1	-	-	0.1	-	nA
HI-506A	Full	-	-	300	-	-	300	nA
HI-507A	Full	-	-	200	-	-	200	nA
HI-508A	Full	-	-	200	-	-	200	nA
HI-509A	Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current, I_{DIFF}, (HI-507A, HI-509A Only)	Full	-	-	50	-	-	50	nA
POWER REQUIREMENTS								
Current, I+, Pin 1 (Notes 2, 8)	Full	-	1.5	2.0	-	1.5	2.0	mA
Current, I+, HI-508A/HI-509A (Notes 2, 8)	Full	-	1.5	2.4	-	1.5	2.0	mA
Current, I-, Pin 27 (Notes 2, 8)	Full	-	0.02	1.0	-	0.02	1.0	mA
Power Dissipation, P_D	Full	-	7.5	-	-	7.5	-	mW

NOTES:

2. 100% tested for Dash 8. Leakage currents not tested at -55°C.
3. $V_{OUT} = \pm 10V$, $I_{OUT} = \mp 100\mu A$.
4. 10nA is the practical lower limit for high speed measurement in the production test environment.
5. Analog Overvoltage = ±33V.
6. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
7. $V_{EN} = 0.8V$, $R_L = 1K$, $C_L = 15pF$, $V_S = 7V_{RMS}$, f = 100kHz.
8. V_{EN}, $V_A = 0V$ or 4V.
9. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5V supply are recommended.
10. $V_{REF} = +10V$.

Typical Performance Curves and Test Circuits

$T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified

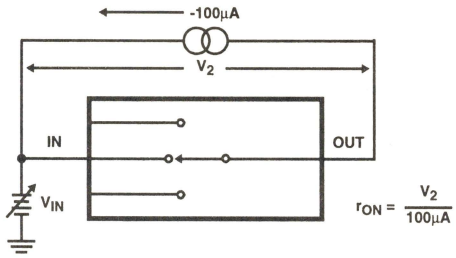


FIGURE 1A. TEST CIRCUIT

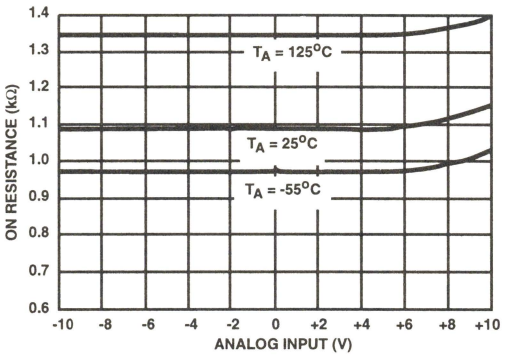


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

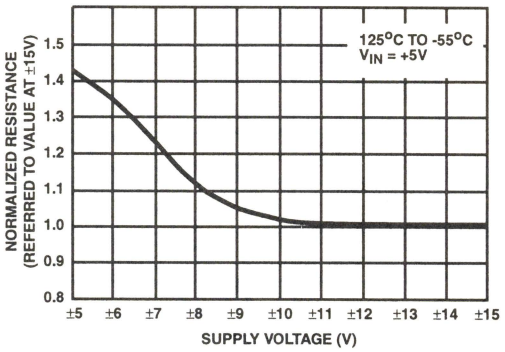


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

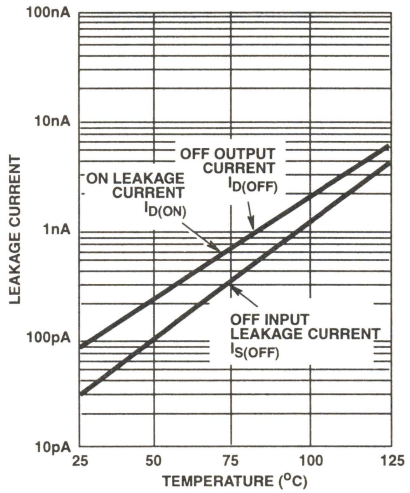


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

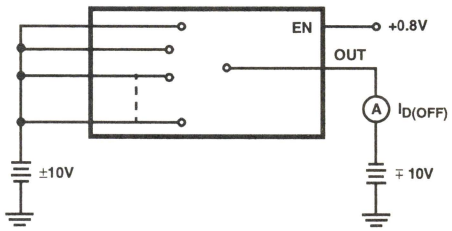


FIGURE 2B. $I_{D(OFF)}$ (NOTE 1)

Typical Performance Curves and Test Circuits

$T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified **(Continued)**

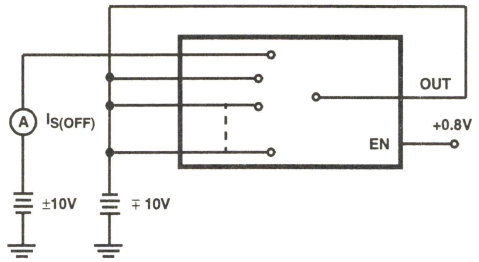


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT (NOTE 1)

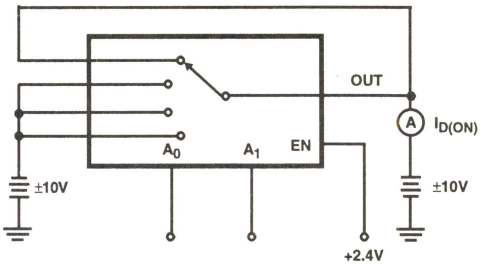


FIGURE 2D. $I_{D(On)}$ TEST CIRCUIT (NOTE 1)

NOTE:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V.)

FIGURE 2. LEAKAGE CURRENTS

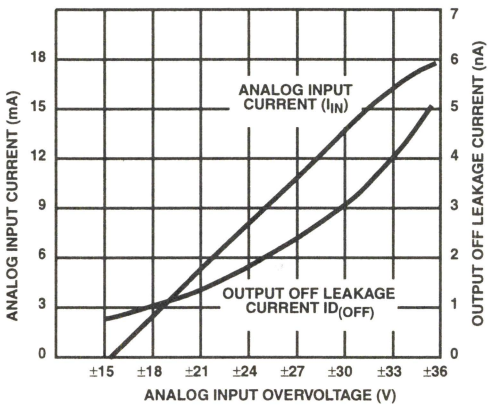


FIGURE 3A. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

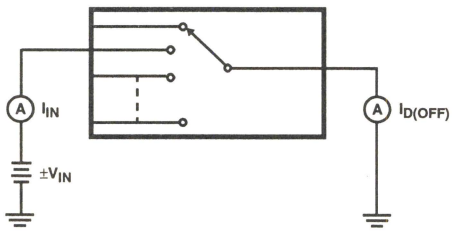


FIGURE 3B. TEST CIRCUIT

FIGURE 3. OVERVOLTAGE CHARACTERISTICS

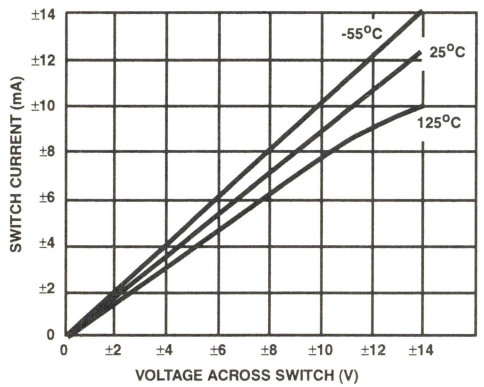


FIGURE 4A. ON CHANNEL CURRENT vs VOLTAGE

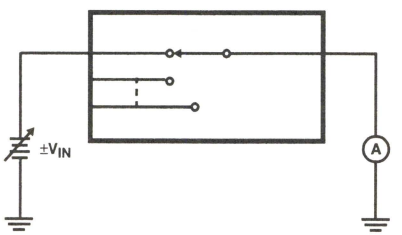


FIGURE 4B. TEST CIRCUIT

FIGURE 4. ON CHANNEL CURRENT

Typical Performance Curves and Test Circuits

$T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified **(Continued)**

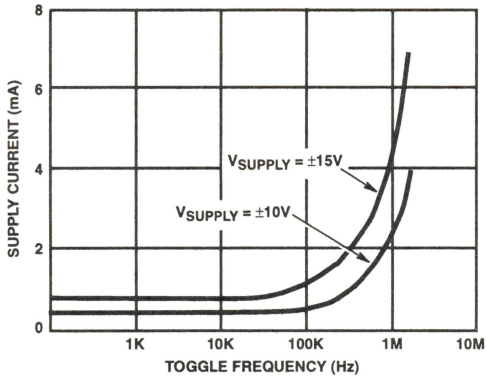
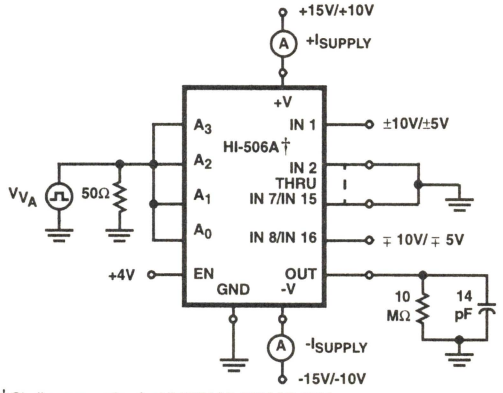


FIGURE 5A. SUPPLY CURRENT vs TOGGLE FREQUENCY



† Similar connection for HI-507A/HI-508A/HI-509A

FIGURE 5B. TEST CIRCUIT

FIGURE 5. SUPPLY CURRENTS

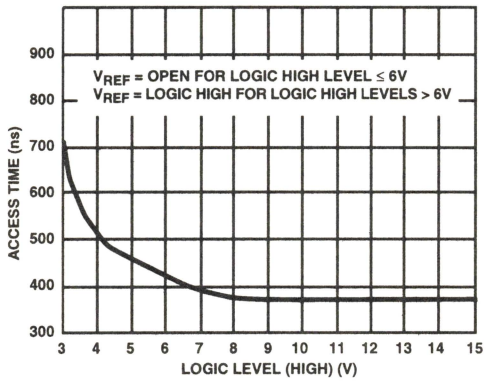
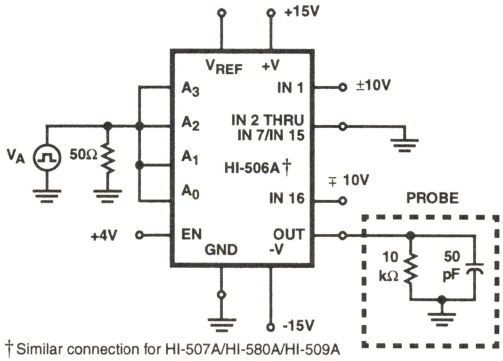


FIGURE 6A. ACCESS TIME vs LOGIC LEVEL (HIGH)



† Similar connection for HI-507A/HI-580A/HI-509A

FIGURE 6B. TEST CIRCUIT

FIGURE 6. ACCESS TIME

Switching Waveforms

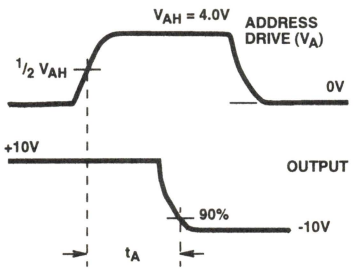


FIGURE 7A.

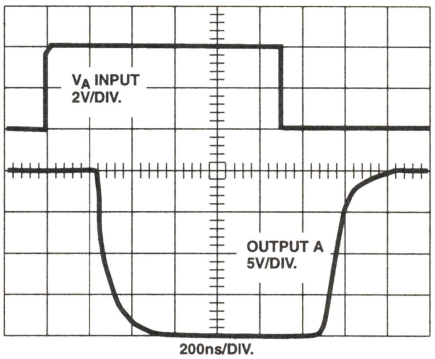
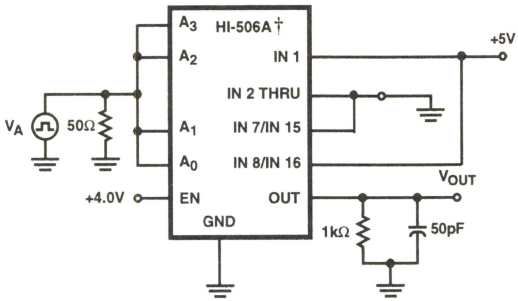


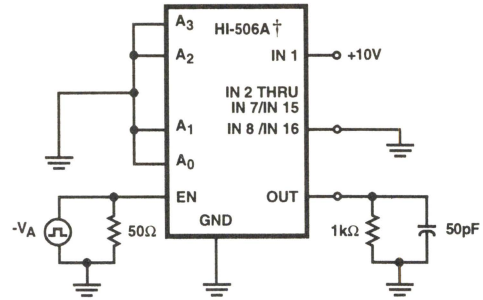
FIGURE 7B.

FIGURE 7. ACCESS TIME



†Similar connection for HI-507A/HI-508A/HI-509A

FIGURE 8A.



†Similar connection for HI-507A//HI-508A/HI-509A

FIGURE 9A.

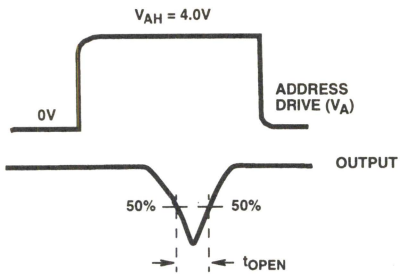


FIGURE 8B.

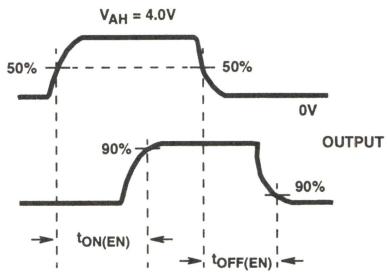


FIGURE 9B.

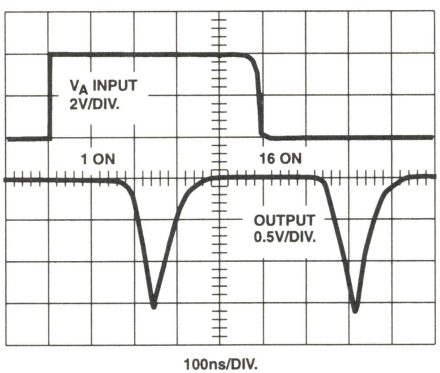


FIGURE 8C.

FIGURE 8. BREAK-BEFORE-MAKE DELAY

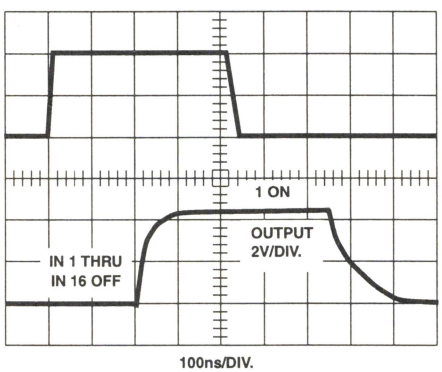


FIGURE 9C.

FIGURE 9. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

Truth Tables

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-508A

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Die Characteristics

DIE DIMENSIONS:

159 mils x 83.9 mils x 19 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Silox: 12kÅ ±2kÅ
Nitride: 3.5kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

485

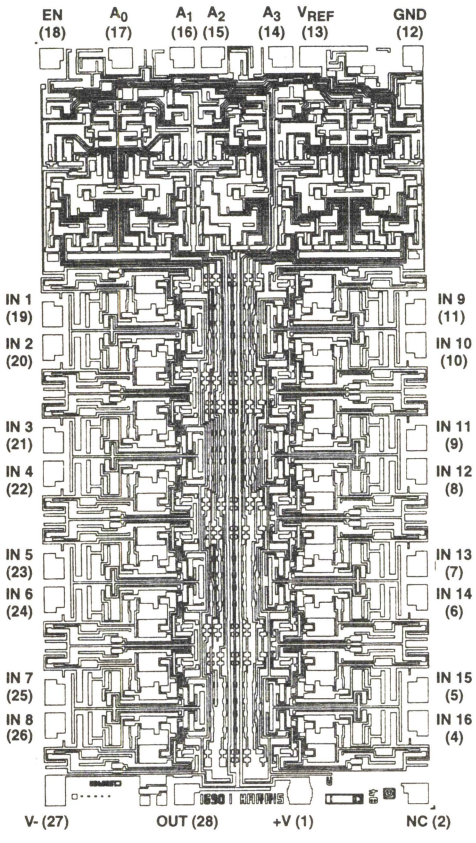
PROCESS:

CMOS-DI

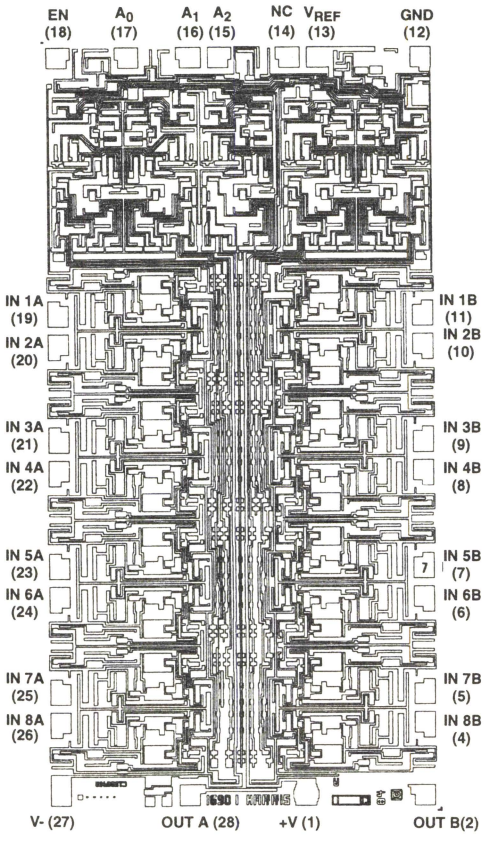
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layouts

HI-506A



HI-507A



Die Characteristics

DIE DIMENSIONS:

108 mils x 83 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Silox: 12kÅ ±2kÅ
Nitride: 3.5kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

253

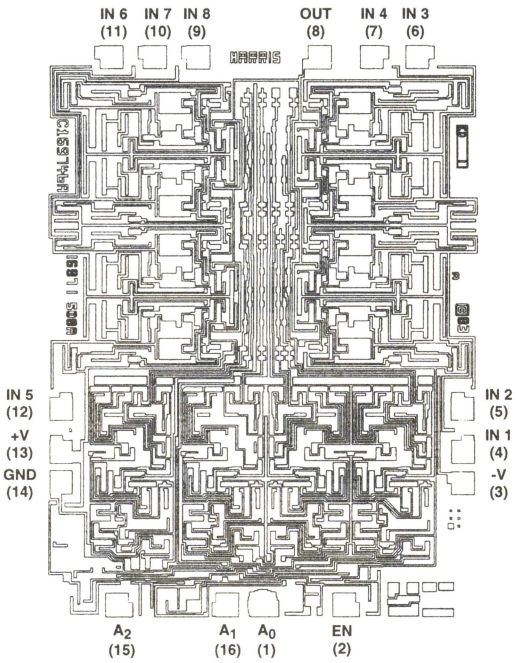
PROCESS:

CMOS-DI

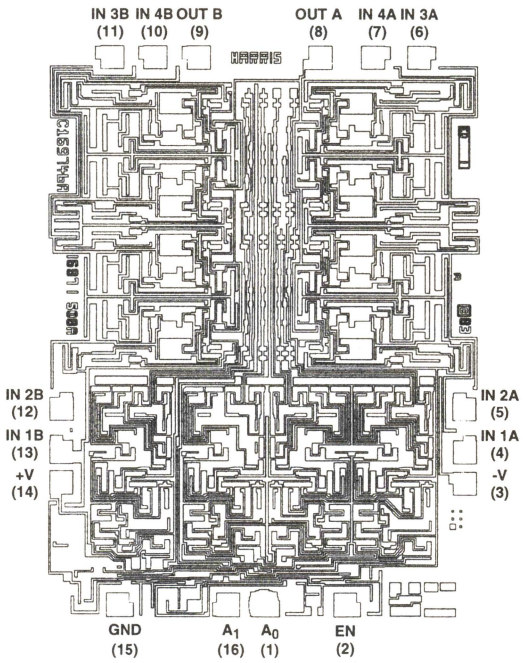
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layouts

HI-508A



HI-509A



HARRIS SEMICONDUCTOR

HI-516

16-Channel/Differential 8-Channel, CMOS High Speed Analog Multiplexer

August 1997

Features

- Access Time (Typical) 130ns
- Settling Time 250ns (0.1%)
- Low Leakage (Typical)
  - $I_{S(OFF)}$ 10pA
  - $I_{D(OFF)}$ 30pA
- Low Capacitance (Max)
  - $C_{S(OFF)}$ 10pF
  - $C_{D(OFF)}$ 25pF
- Off Isolation at 500kHz . . . . . 55dB (Min)
- Low Charge Injection Error 20mV
- Single Ended to Differential Selectable (SDS)
- Logic Level Selectable (LLS)

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Industrial Control

Description

The HI-516 is a monolithic, dielectrically isolated, high-speed, high-performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_3 enables the HI-516 to be user programmed either as a single ended 16-Channel multiplexer by connecting 'out A' to 'out B' and using A_3 as a digital address input, or as an 8-Channel differential multiplexer by connecting A_3 to the V-supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris Dielectric Isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I_{DOFF} < 100pA at 25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

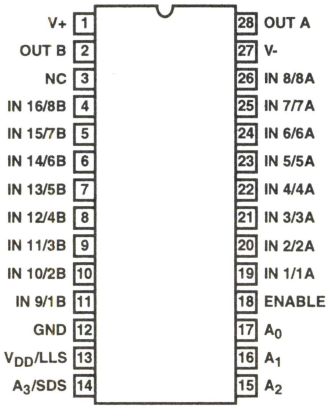
For MIL-STD-883 compliant parts, request the HI-516/883 data sheet.

Ordering Information

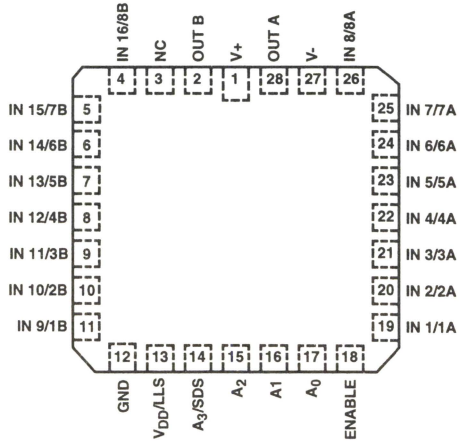
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI4P0516-5	0 to 75	28 Ld PLCC	N28.45
HI3-0516-5	0 to 75	28 Ld PDIP	E28.6
HI1-0516-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0516-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0516-8	-55 to 125	28 Ld CERDIP	F28.6
HI4-0516-8	-55 to 125	28 Ld CLCC	J28.A
HI1-0516/883	-55 to 125	28 Ld CERDIP	F28.6
HI4-0516/883	-55 to 125	28 Ld CLCC	J28.A

Pinouts

HI-516 (CERDIP, PDIP)
TOP VIEW



HI-516 (CLCC, PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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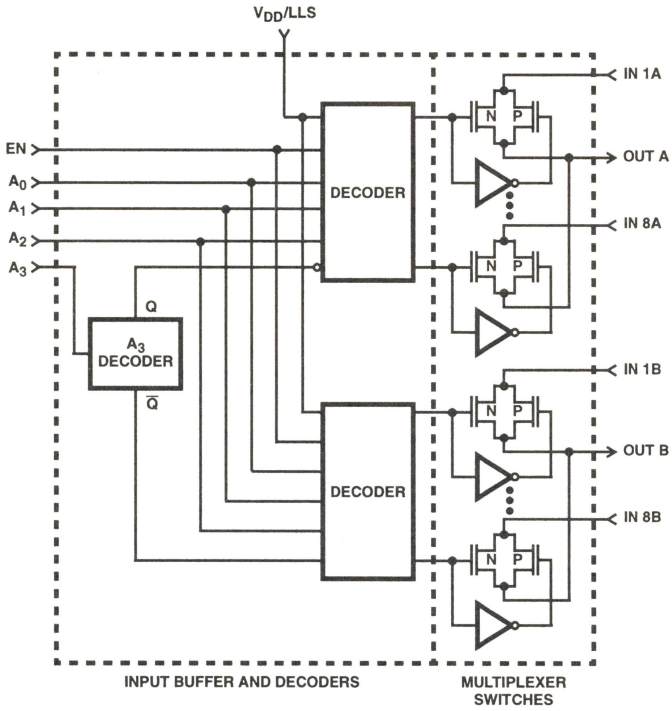
File Number **3146.1**

Functional Block Diagram



A_3 DECODE		
A_3	Q	$\overline{Q}$
H	H	L
L	L	H
V-	L	L

Absolute Maximum Ratings (Note 1)

Voltage Between Supply Pins 33V
Analog Input Voltage
$+V_{IN}$ . . . . . $+V_{SUPPLY}$ +2V
$-V_{IN}$ . . . . . $-V_{SUPPLY}$ -2V
Digital Input Voltage
TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
$+V_A$ . . . . . +6V
$-V_A$ . . . . . -6V
$+A_3$/SDS . . . . . $+V_{SUPPLY}$ +2V
$-A_3$/SDS . . . . . $-V_{SUPPLY}$ -2V
CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
$+V_A$ . . . . . $+V_{SUPPLY}$ +2V
$-V_A$ . . . . . -2V

Operating Conditions

Temperature Ranges
HI-516-2,-8 . . . . . -55°C to 125°C
HI-516-5 . . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	60	N/A
PLCC Package	70	N/A
CERDIP Package	55	18
CLCC Package	70	20

Maximum Junction Temperature
CERDIP, CLCC Packages . . . . . 175°C
PDIP, SOIC, PLCC Packages . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 1) Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-516-2, -8			HI-516-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_I	Note 2	Full	-14	-	+14	-15	-	+15	V
On Resistance, r_{ON}	Note 3	25	-	620	750	-	620	750	Ω
		Full	-	-	1,000	-	-	1,000	Ω
Off Input Leakage Current, $I_{S(OFF)}$		25	-	0.01	-	-	0.01	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$		25	-	0.03	-	-	0.03	-	nA
		Full	-	-	100	-	-	100	nA
On Channel Leakage Current, $I_{D(ON)}$		25	-	0.04	-	-	0.04	-	nA
		Full	-	-	100	-	-	100	nA
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL} (TTL)		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH} (TTL)		Full	2.4	-	-	2.4	-	-	V
Input Low Threshold, V_{AL} (CMOS)		Full		-	$0.3V_{DD}$	-	-	$0.3V_{DD}$	V
Input High Threshold, V_{AH} (CMOS)		Full	$0.7V_{DD}$	-	-	$0.7V_{DD}$	-	-	V
Input Leakage Current, I_{AH} (High)		Full	-	-	1	-	-	1	µA
Current, I_{AL} (Low)		Full	-	-	25	-	-	25	µA
SWITCHING CHARACTERISTICS									
Access Time, t_A		25	-	130	175	-	130	175	ns
		Full	-	-	225	-	-	225	ns
Break-Before-Make Delay, t_{OPEN}		25	10	20	-	10	20	-	ns
Enable Delay (ON), $t_{ON(EN)}$		25	-	120	175	-	120	175	ns
Enable Delay (OFF), $t_{OFF(EN)}$		25	-	140	175	-	140	175	ns
Settling Time									
0.1%		25	-	250	-	-	250	-	ns
0.01%		25	-	800	-	-	800	-	ns

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 1) Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-516-2, -8			HI-516-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Charge Injection Error	Note 4	25	-	-	20	-	-	20	mV
Off Isolation	Note 5	25	55	-	-	55	-	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	-	10	-	-	10	pF
Channel Output Capacitance, $C_{D(OFF)}$		25	-	-	25	-	-	25	pF
Digital Input Capacitance, C_A		25	-	-	10	-	-	10	pF
Input to Output Capacitance, $C_{DS(OFF)}$		25	-	0.02	-	-	0.02	-	pF
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, P_D		Full	-	-	750	-	-	900	mW
I+, Current	Note 6	Full	-	-	25	-	-	30	mA
I-, Current	Note 6	Full	-	-	25	-	-	30	mA

NOTES:
1. V_{DD}/LLS pin = open or grounded for TTL compatibility. V_{DD}/LLS pin = V_{DD} for CMOS compatibility.
2. At temperatures above 90°C, care must be taken to assure V_{IN} remains at least 1V below the V_{SUPPLY} for proper operation.
3. V_{IN} = ±10V, I_{OUT} = -100µA.
4. V_{IN} = 0V, C_L = 100pF, enable input pulse = 3V, f = 500kHz.
5. V_{EN} = 0.8V, V_S = $3V_{RMS}$, f = 500kHz, C_L = 40pF, R_L = 1K, Pin 3 grounded.
6. V_{EN} = +2.4V.

TRUTH TABLE HI-516 Used as a 16-Channel Multiplexer or 8-Channel Differential Multiplexer (Note 1)

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	None	None
H	L	L	L	L	1A	None
H	L	L	L	H	2A	None
H	L	L	H	L	3A	None
H	L	L	H	H	4A	None
H	L	H	L	L	5A	None
H	L	H	L	H	6A	None
H	L	H	H	L	7A	None
H	L	H	H	H	8A	None
H	H	L	L	L	None	1B
H	H	L	L	H	None	2B
H	H	L	H	L	None	3B
H	H	L	H	H	None	4B
H	H	H	L	L	None	5B
H	H	H	L	H	None	6B
H	H	H	H	L	None	7B
H	H	H	H	H	None	8B

NOTE:
1. For 16-channel single-ended function, tie 'out A' to 'out B'; for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

TRUTH TABLE HI-516 Used as a Differential 8-Channel Multiplexer

A_3 CONNECT TO V- SUPPLY				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

Test Circuits and Waveforms

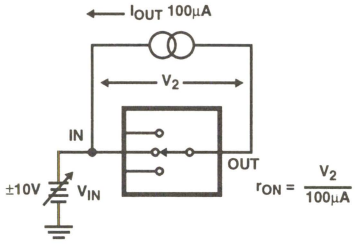


FIGURE 1. ON RESIGTANCE vs INPUT SIGNAL LEVEL

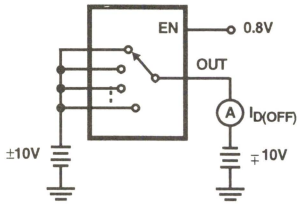


FIGURE 2. $I_{D(OFF)}$ (NOTE 1)

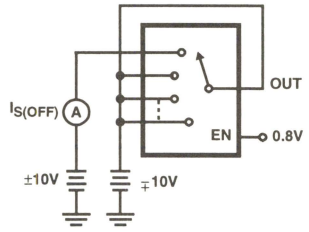


FIGURE 3. $I_{S(OFF)}$ (NOTE 1)

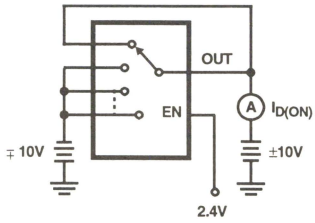


FIGURE 4. $I_{D(ON)}$ (NOTE 1)

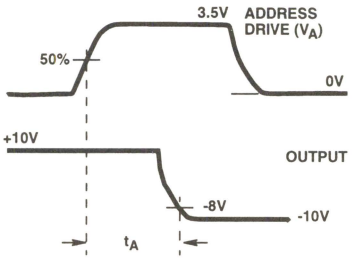


FIGURE 5A.

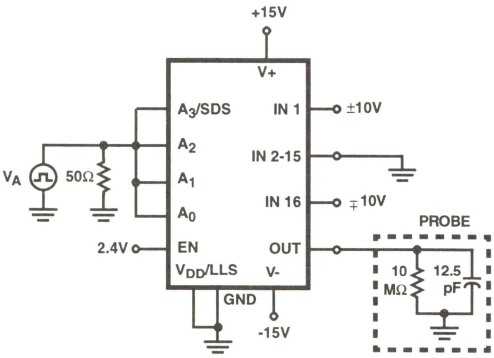


FIGURE 5B.

FIGURE 5. ACCESS TIME

NOTE:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V.)

Test Circuits and Waveforms (Continued)

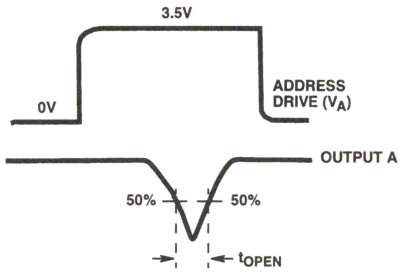


FIGURE 6A. ENABLE DRIVE

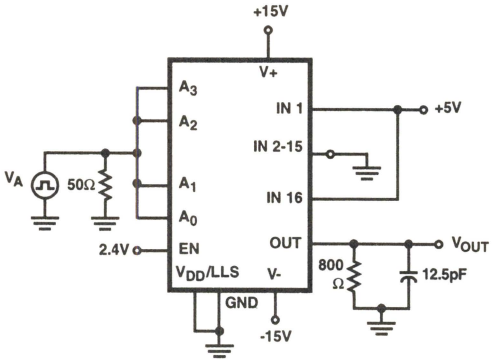


FIGURE 6B.

FIGURE 6. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

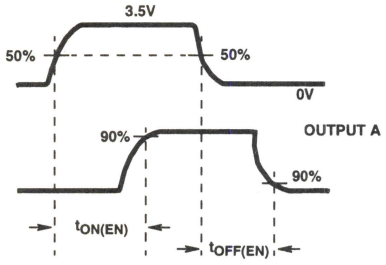


FIGURE 7A. ENABLE DRIVE

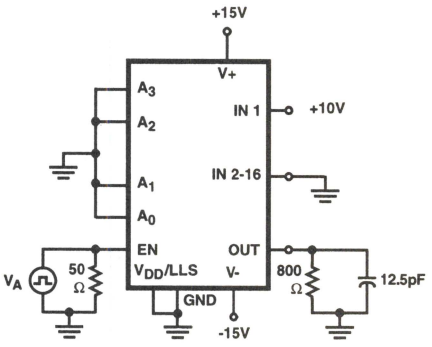


FIGURE 7B.

FIGURE 7. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

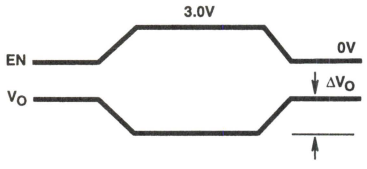


FIGURE 8A.

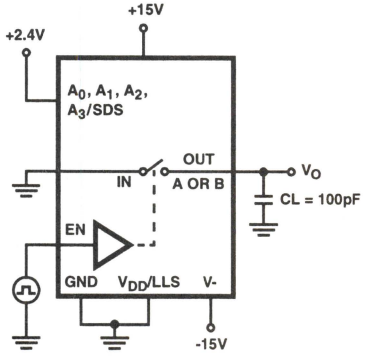


FIGURE 8B.

ΔV_O is the measured voltage error due to charge injection. The error voltage in coulombs is $Q = C_L \times \Delta V_O$.

FIGURE 8. CHARGE INJECTION TEST CIRCUIT

Die Characteristics

DIE DIMENSIONS:

2250µm x 3720µm x 485µm ±25µm

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

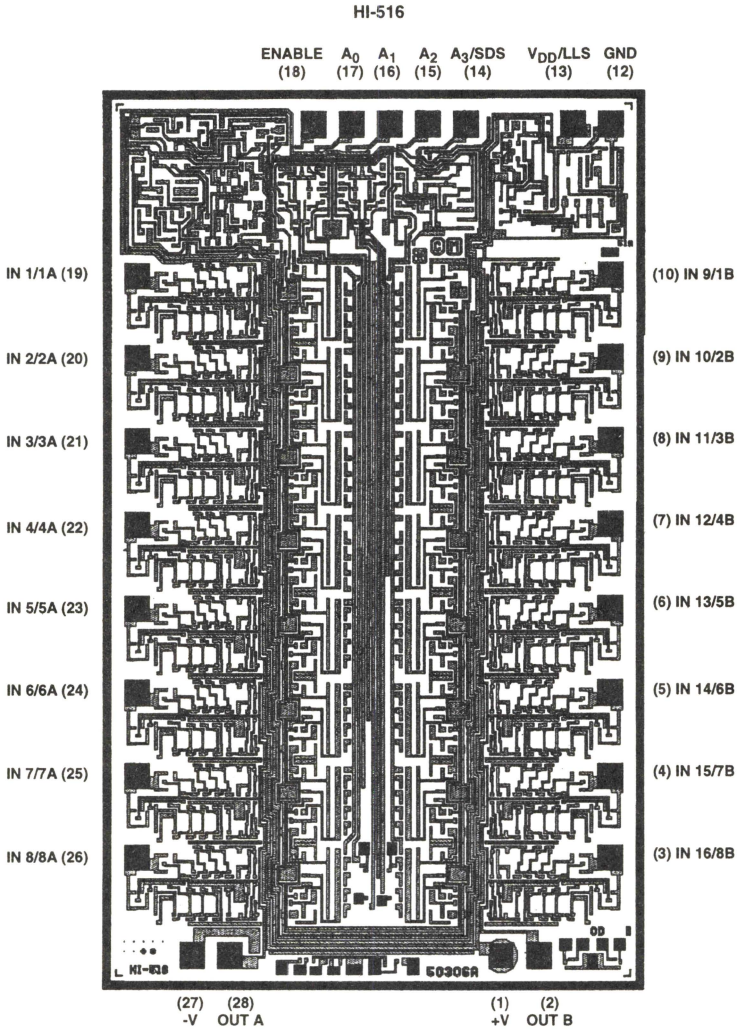
PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.64×10^5 A/cm^2

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HI-518

8-Channel/Differential 4-Channel, CMOS High Speed Analog Multiplexer

August 1997

Features

- Access Time (Typical) 130ns
- Settling Time 250ns (0.1%)
- Low Leakage (Typical)
  - $I_{S(OFF)}$ 10pA
  - $I_{D(OFF)}$ 15pA
- Low Capacitance (Max)
  - $C_{S(OFF)}$ 5pF
  - $C_{D(OFF)}$ 10pF
- Off Isolation at 500kHz . . . . . 45dB (Min)
- Low Charge Injection Error 25mV
- Single Ended to Differential Selectable (SDS)
- Logic Level Selectable (LLS)

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Industrial Control

Description

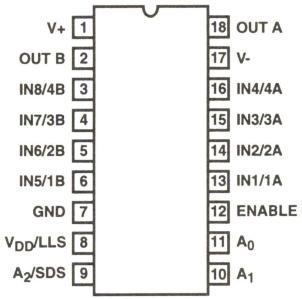
The HI-518 is a monolithic, dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_2 enables the HI-518 to be user programmed either as a single ended 8-Channel multiplexer by connecting 'Out A' to 'Out B' and using A_2 as a digital address input, or as a 4-Channel differential multiplexer by connecting A_2 to the V- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris Dielectric Isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I_{DOFF} < 100pA at 25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

Ordering Information

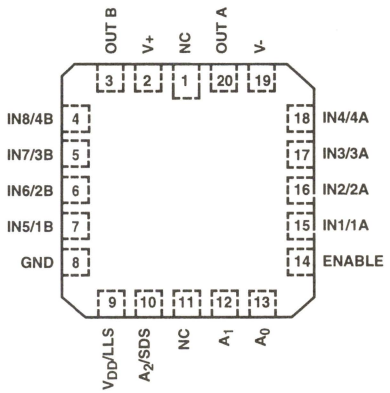
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3-0518-5	0 to 75	18 Ld PDIP	E18.3
HI1-0518-5	0 to 75	18 Ld CERDIP	F18.3
HI1-0518-2	-55 to 125	18 Ld CERDIP	F18.3
HI1-0518-8	-55 to 125	18 Ld CERDIP	F18.3
HI4P0518-5	0 to 75	20 Ld PLCC	N20.35
HI4-0518-8	-55 to 125	20 Ld CLCC	J20.A

Pinouts

HI-518 (CERDIP, PDIP)
TOP VIEW



HI-518 (CLCC, PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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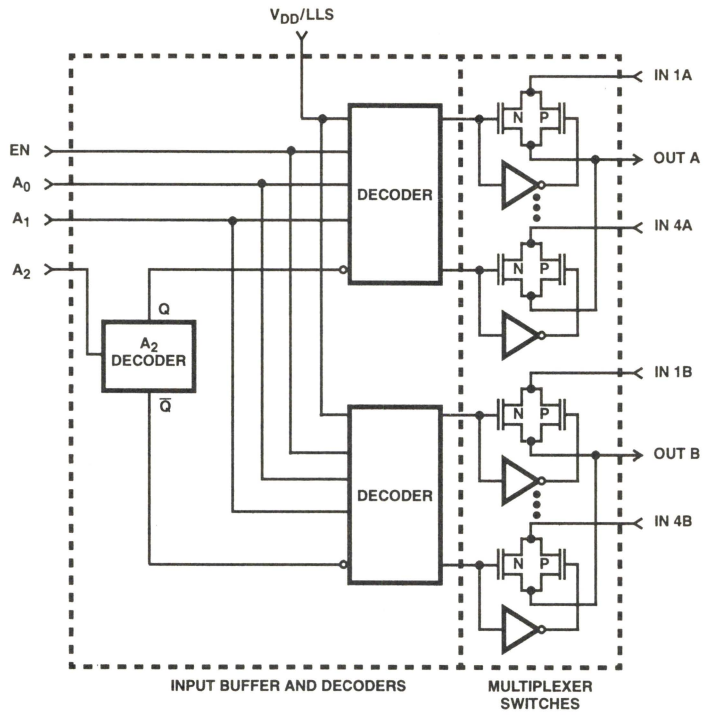
File Number **3147.1**

Functional Block Diagram



A_2 DECODE		
A_2	Q	$\overline{Q}$
H	H	L
L	L	H
V-	L	L

Absolute Maximum Ratings (Note 1)

V+ to V- 33V
Analog Input Voltage
$+V_{IN}$ . . . . . (V+) +2V
$-V_{IN}$ . . . . . (V-) -2V
Digital Input Voltage
TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
$+V_A$ . . . . . +6V
$-V_A$ . . . . . -6V
$+A_2$/SDS . . . . . (V+) +2V
$-A_2$/SDS . . . . . (V-) -2V
CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
$+V_A$ . . . . . (V+) +2V
$-V_A$ . . . . . -2V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	90	N/A
PLCC Package	80	N/A
CERDIP Package	70	18
CLCC Package	65	14

Maximum Junction Temperature
CERDIP, CLCC Packages . . . . . 175°C
PDIP, PLCC, SOIC Packages . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC - Lead Tips Only)

Operating Conditions

Temperature Ranges
HI-518-2,-8 . . . . . -55°C to 125°C
HI-518-5 . . . . . 0°C to 75°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND (Note 1), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-518-2, -8			HI-518-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, t_A		25	-	130	175	-	130	175	ns
		Full	-	-	225	-	-	225	ns
Break-Before-Make Delay, t_{OPEN}		25	10	20	-	10	20	-	ns
Enable Delay (ON), $t_{ON(EN)}$		25	-	120	175		120	175	ns
Enable Delay (OFF), $t_{OFF(EN)}$		25	-	140	175		140	175	ns
Settling Time									
0.1%		25	-	250	-	-	250	-	ns
0.01%		25	-	800	-	-	800	-	ns
Charge Injection Error	Note 4	25	-	-	25	-	-	25	mV
Off Isolation	Note 5	25	45	-	-	45	-	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	-	5	-	-	5	pF
Channel Output Capacitance, $C_{D(OFF)}$		25	-	-	10	-	-	10	pF
Digital Input Capacitance, C_A		25	-	-	5	-	-	5	pF
Input to Output Capacitance, $C_{DS(OFF)}$		25	-	0.02		-	0.02	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL} (TTL)		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH} (TTL)		Full	2.4	-	-	2.4	-	-	V
Input Low Threshold, V_{AL} (CMOS)		Full	-	-	$0.3V_{DD}$	-	-	$0.3V_{DD}$	V
Input High Threshold, V_{AH} (CMOS)		Full	$0.7V_{DD}$	-	-	$0.7V_{DD}$	-	-	V

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND (Note 1), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-518-2, -8			HI-518-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Leakage Current, I_{AH} (High)		Full	-	-	1	-	-	1	µA
Input Leakage Current, I_{AL} (Low)		Full	-	-	20	-	-	20	µA
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_{IN}	Note 2	Full	-14		+14	-15	-	+15	V
On Resistance, r_{ON}	Note 3	25	-	480	750	-	480	750	Ω
		Full	-	-	1,000	-	-	1,000	Ω
Off Input Leakage Current, $I_{S(OFF)}$		25	-	0.01	-	-	0.01	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$		25	-	0.015	-	-	0.015	-	nA
		Full	-	-	50	-	-	50	nA
On Channel Leakage Current, $I_{D(ON)}$		25	-	0.015	-	-	0.015	-	nA
		Full	-	-	50	-	-	50	nA
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, P_D		Full	-	-	450	-	-	540	mW
I+, Current	Note 6	Full	-	-	15	-	-	18	mA
I-, Current	Note 6	Full	-	-	15	-	-	18	mA

NOTES:

1. V_{DD}/LLS pin = open or grounded for TTL compatibility. V_{DD}/LLS pin = V_{DD} for CMOS compatibility.
2. At temperatures above 90°C, care must be taken to assure V_{IN} remains at least 1.0V below the V_{SUPPLY} for proper operation.
3. V_{IN} = ±10V, I_{OUT} = -100µA.
4. V_{IN} = 0V, C_L = 100pF, enable input pulse = 3V, f = 500kHz.
5. C_L = 40pF, R_L = 1K. Due to the pin to pin capacitance between IN 8/4B and OUT B, channel 8/4B exhibits 60dB of OFF isolation under the above test conditions.
6. V_{EN} = +2.4V.

TRUTH TABLE HI-518 Used as an 8-Channel Multiplexer or 4-Channel Differential Multiplexer

USE A_2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	None
H	L	L	H	2A	None
H	L	H	L	3A	None
H	L	H	H	4A	None
H	H	L	L	None	1B
H	H	L	H	None	2B
H	H	H	L	None	3B
H	H	H	H	None	4B

TRUTH TABLE HI-518 Used as a DIfferential 4-Channel Multiplexer

A_2 CONNECT TO V- SUPPLY			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	None	None
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

Test Circuits and Waveforms

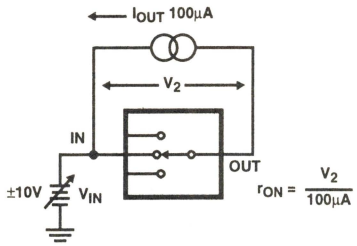


FIGURE 1. ON RESIGTANCE vs INPUT SIGNAL LEVEL

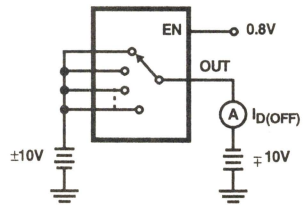


FIGURE 2. $I_{D(OFF)}$ (NOTE 1)

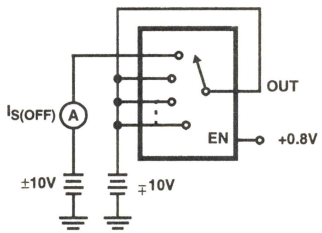


FIGURE 3. $I_{S(OFF)}$ (NOTE 1)

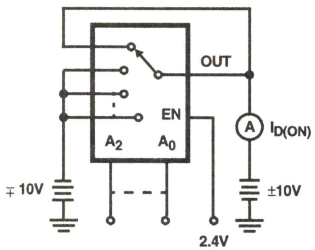


FIGURE 4. $I_{D(ON)}$ (NOTE 1)

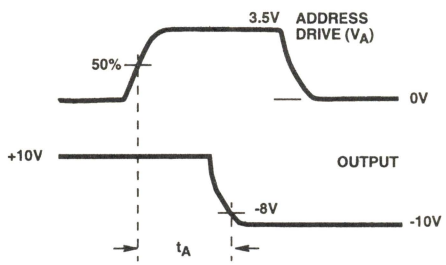


FIGURE 5A.

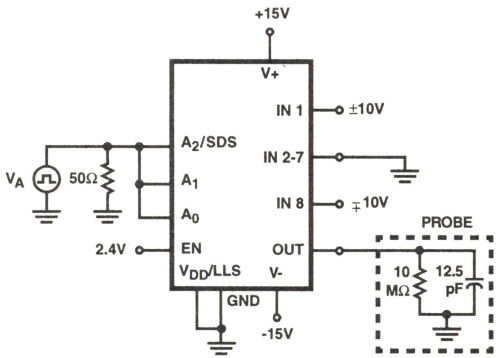


FIGURE 5B.

FIGURE 5. ACCESS TIME

NOTE:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V.)

Test Circuits and Waveforms (Continued)

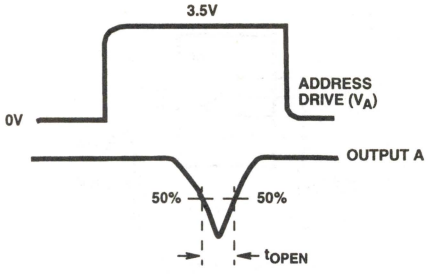


FIGURE 6A.

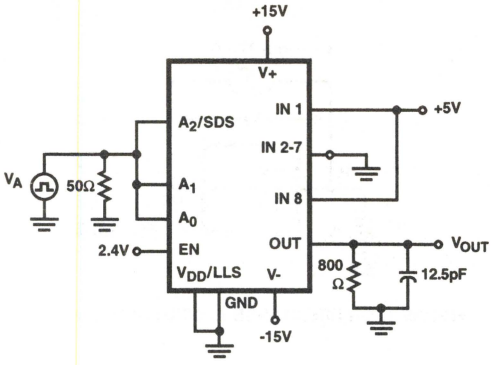


FIGURE 6B.

FIGURE 6. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

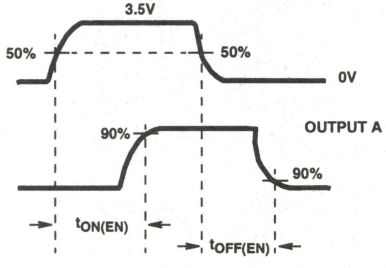


FIGURE 7A.

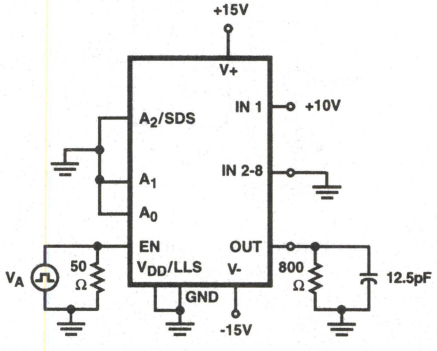


FIGURE 7B.

FIGURE 7. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

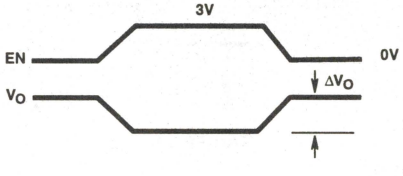


FIGURE 8A.

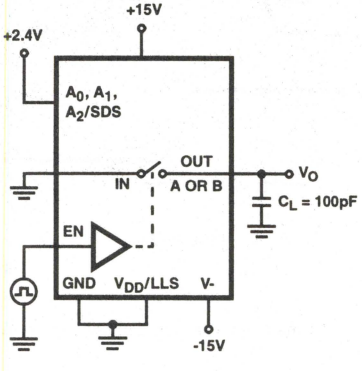


FIGURE 8B.

ΔV_O is the measured voltage error due to charge injection. The error voltage in coulombs is $Q = C_L \times \Delta V_O$.

FIGURE 8. CHARGE INJECTION TEST CIRCUIT

Die Characteristics

DIE DIMENSIONS:

89 mils x 93 mils

METALLIZATION:

Type: AlCu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1.0kÅ
Silox Thickness: 12kÅ ±2.0kÅ

WORST CASE CURRENT DENSITY:

1.43×10^5 A/cm^2

TRANSISTOR COUNT:

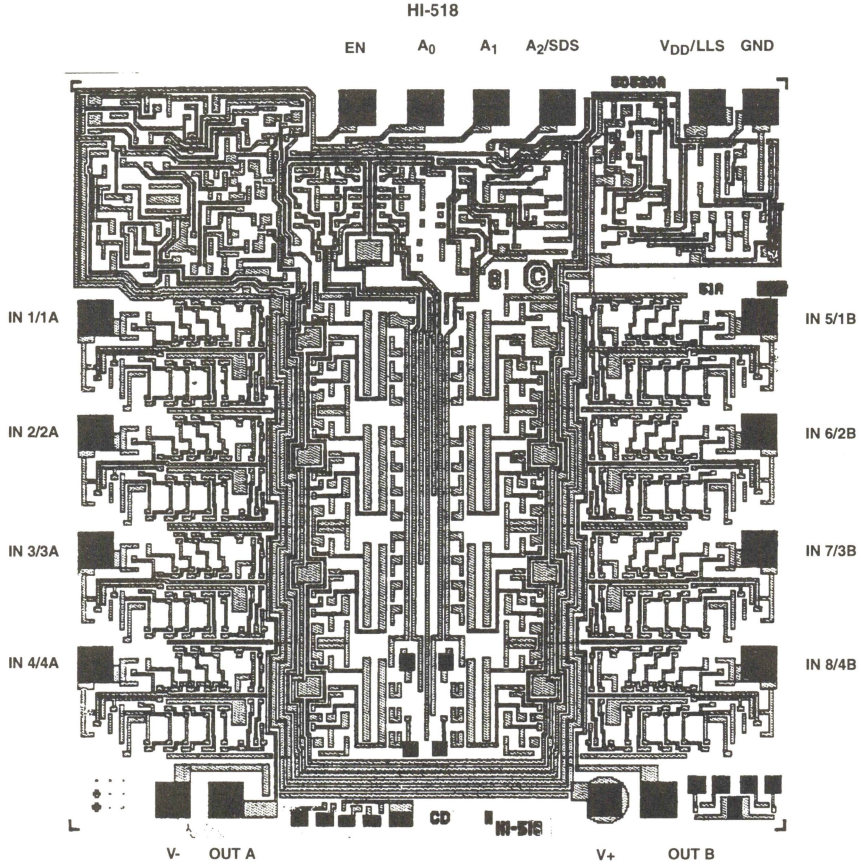
356

PROCESS:

CMOS-DI

NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HI-524

August 1997

4-Channel Wideband and Video Multiplexer

Features

- Crosstalk (10MHz) ..... <-60dB
- Fast Access Time 150ns
- Fast Settling Time 200ns
- TTL Compatible

Applications

- Wideband Switching
- Radar
- TV Video
- ECM

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0524-5	0 to 75	18 Ld CERDIP	F18.3
HI1-0524-2	-55 to 125	18 Ld CERDIP	F18.3
HI4P0524-5	0 to 75	20 Ld PLCC	N20.35
HI3-0524-5	0 to 75	18 Ld PDIP	E18.3
HI1-0524-8	-55 to 125	18 Ld CERDIP	F18.3
HI1-0524/883	-55 to 125	18 Ld CERDIP	F18.3
HI4-0524/883	-55 to 125	20 Ld CLCC	J20.A

Description

The HI-524 is a 4-Channel CMOS analog multiplexer designed to process single-ended signals with bandwidths up to 10MHz. The chip includes a 1 of 4 decoder for channel selection and an enable input to inhibit all channels (chip select).

Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure the Crosstalk is less than -60dB at 10MHz.

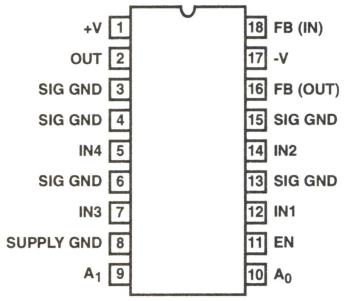
The HI-524 is designed to operate into a wideband buffer amplifier such as the Harris HA-2541. The multiplexer chip includes two "ON" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel r_{ON} resistance, to minimize the amplifier V_{OS} and its variation with temperature.

The HI-524 is well suited to the rapid switching of video and other wideband signals in telemetry, instrumentation, radar and video systems.

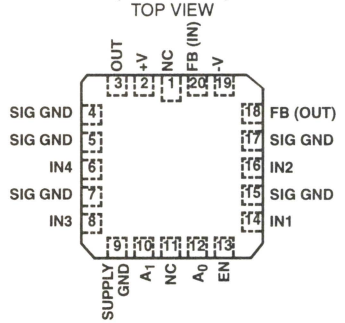
For MIL-STD-883 compliant parts, request the HI-524/883 data sheet.

Pinouts

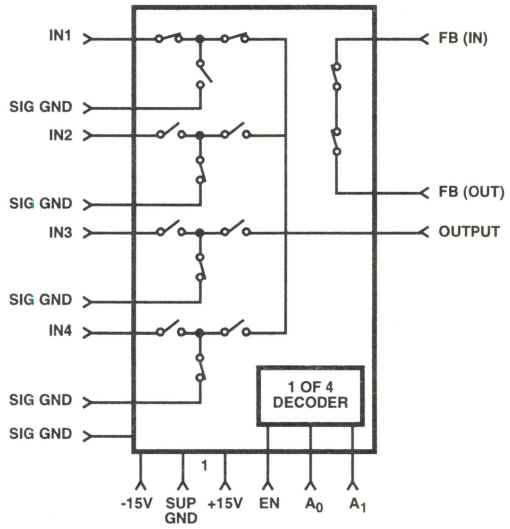
(CERDIP, PDIP)
TOP VIEW



(CLCC, PLCC)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3148.1**

Absolute Maximum Ratings

Voltage Between Supplies 33V
Digital Input Voltage
$+V_A$ . . . . . +6V
$-V_A$ . . . . . -6V
Analog Input Voltage
$+V_{IN}$ . . . . . $+V_{SUPPLY}$ +2.0V
$-V_{IN}$ . . . . . $-V_{SUPPLY}$ -2.0V
Either Supply to Ground 16.5V

Operating Conditions

Temperature Range
HI-524-2, -8 . . . . . -55^oC to 125^oC
HI-524-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	70	18
CLCC Package	65	16
PDIP Package	90	N/A
PLCC Package	80	N/A

Maximum Junction Temperature . . . . . 175^oC
CERDIP, CLCC Packages . . . . . 175^oC
PLCC, PDIP Packages . . . . . 150^oC
Maximum Storage Temperature
(CERDIP, CLCC) . . . . . -65^oC to 150^oC
(PLCC) . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC
(PLCC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} = (Logic Level Low) = +0.5V; V_{EN} = +2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	HI-524-2/-8			HI-524-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, t_A	(Note 5)	25	-	150	300	-	150	300	ns
Break-Before-Make Delay, t_{OPEN}	(Note 5)	25	-	20	-	-	20	-	ns
Enable Delay (ON), $R_L = 500\Omega$, $t_{ON\ (EN)}$		25	-	180	300	-	180	-	ns
Enable Delay (OFF), $R_L = 500\Omega$, $t_{OFF\ (EN)}$		25	-	180	250	-	180	-	ns
Settling Time (0.1%)	(Note 5)	25	-	200	-	-	200	-	ns
(0.01%)		25	-	600	-	-	600	-	ns
Crosstalk	(Note 6)	25	-	-65	-	-	-65	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	4	-	-	4	-	pF
Channel Output Capacitance, $C_{D(OFF)}$		25	-	10	-	-	10	-	pF
Digital Input Capacitance, C_A		25	-	5	-	-	5	-	pF
DIGITAL INPUT SPECIFICATIONS									
Input Low Threshold (TTL), V_{AL}		Full	-	-	0.8	-	-	0.8	V
Input High Threshold (TTL), V_{AH}		Full	2.4	-	-	2.4	-	-	V
Input Leakage Current (High), I_{AH}		Full	-	0.05	1	-	0.05	1	µA
Current (Low), A_L		Full	-	-	25	-	-	25	µA
ANALOG CHANNEL SPECIFICATIONS									
Analog Signal Range, V_{IN}		Full	-10	-	+10	-10	-	+10	V
On Resistance, r_{ON}	(Note 2)	25	-	700	-	-	700	-	Ω
		Full	-	-	1.5	-	-	1.5	KΩ
Off Input Leakage Current, $I_{S\ (OFF)}$	(Note 3)	25	-	0.2	-	-	0.2	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D\ (OFF)}$	(Note 3)	25	-	0.2	-	-	0.2	-	nA
		Full	-	-	50	-	-	50	nA
On Channel Leakage Current, $I_{D\ (ON)}$	(Note 3)	25	-	0.7	-	-	0.7	-	nA
		Full	-	-	50	-	-	50	nA

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} = (Logic Level Low) = +0.5V; V_{EN} = +2.4V, Unless Otherwise Specified **(Continued)**

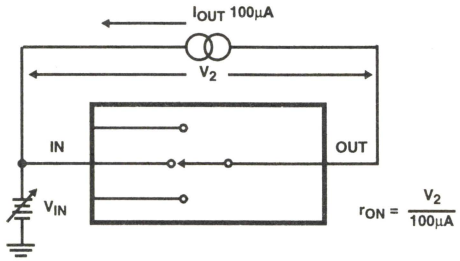
PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-524-2/-8			HI-524-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
3dB Bandwidth	(Note 4)	25	-	8	-	-	8	-	MHz
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, P_D		Full	-	-	750	-	-	750	mW
Current, I+	(Note 7)	Full	-	-	25	-	-	25	mA
Current, I-	(Note 7)	Full	-	-	25	-	-	25	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{IN} = 0V; I_{OUT} = 100µA (See Test Circuit 1).
3. V_O = ±10V; V_{IN} = ±10V. (See Test Circuits 2, 3, 4.)
4. MUX output is buffered with HA-5033 amplifier.
5. 6V Step, ±3V to ±3V, See Test Circuit 5.
6. V_{IN} = 10MHz, $3V_{P-P}$ on one channel, with any other channel selected. (Worst case is channel 3 selected with input on channel 4.) MUX output is buffered with HA-2541 as shown in Applications section. Terminate all channels with 75Ω.
7. Supply currents vary less than 0.5mA for switching rates from DC to 2MHz.

Typical Performance Curves and Test Circuits

T_A = 25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified



TEST CIRCUIT 1. ON RESISTANCE

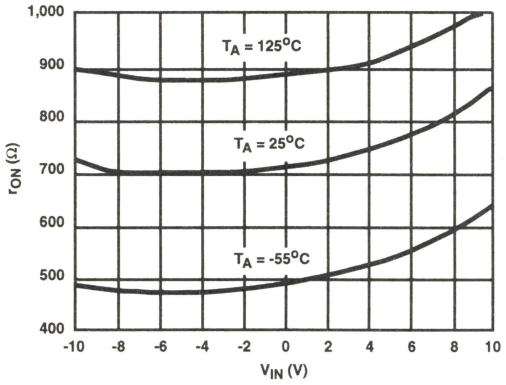


FIGURE 1. ON RESISTANCE vs ANALOG INPUT VOLTAGE

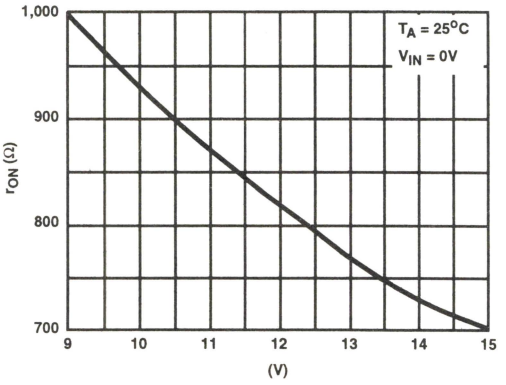


FIGURE 2. ON RESISTANCE vs SUPPLY VOLTAGE

Typical Performance Curves and Test Circuits

$T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$, Unless Otherwise Specified **(Continued)**

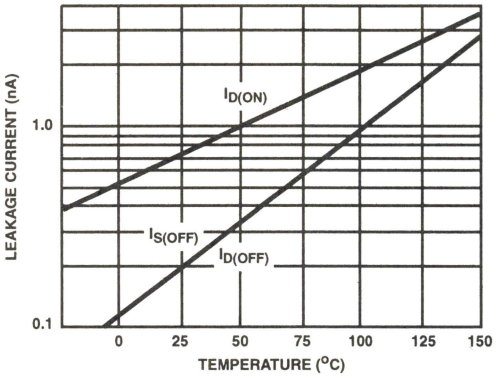
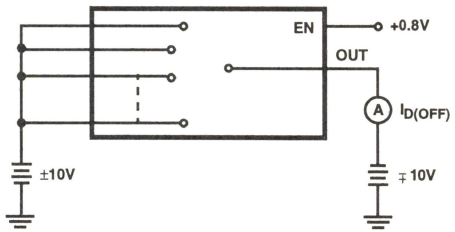
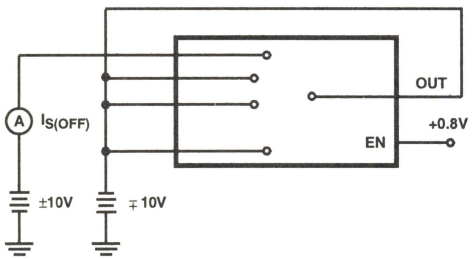


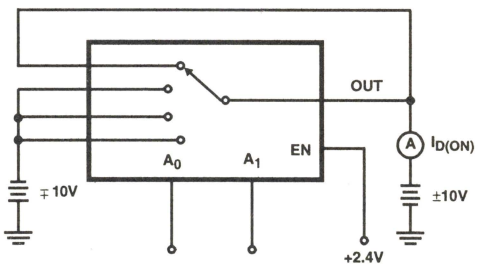
FIGURE 3. LEAKAGE CURRENT vs TEMPERATURE



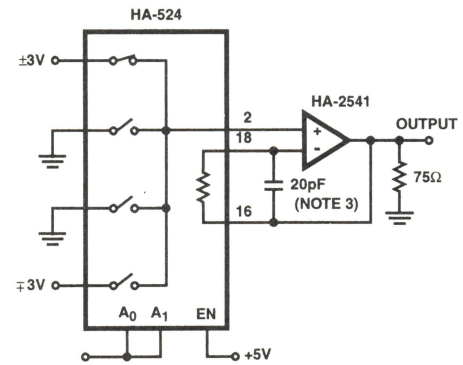
TEST CIRCUIT 2. LEAKAGE CURRENT (NOTE 1)



TEST CIRCUIT 3. LEAKAGE CURRENT (NOTE 1)



TEST CIRCUIT 4. LEAKAGE CURRENT (NOTE 1)



TEST CIRCUIT 5. SETTLING TIME, ACCESS TIME, BREAK-BEFORE-MAKE DELAY (NOTE 2)

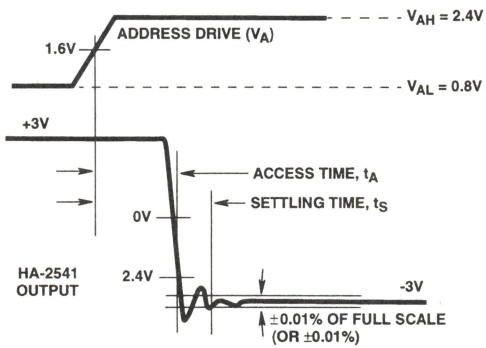


FIGURE 4. POWER SUPPLY CURRENT vs TEMPERATURE

NOTES:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V.)
2. This test requires channel inputs 1 and 4 at the same level.
3. Capacitor value may be selected to optimize AC performance.

Typical Performance Curves and Test Circuits $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$, Unless Otherwise Specified **(Continued)**

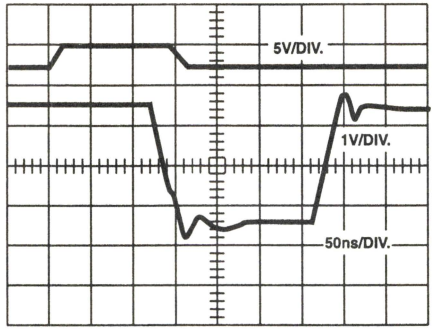


FIGURE 5. ACCESS TIME

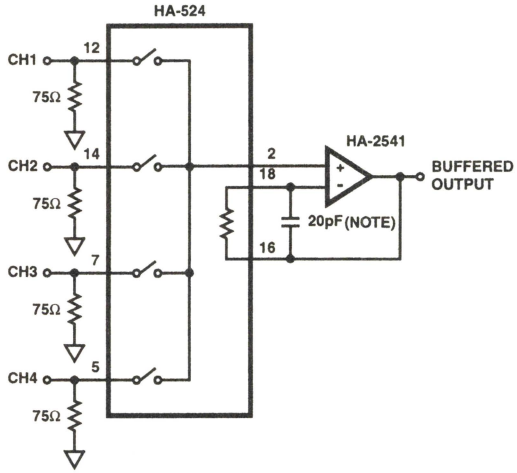
TABLE 1. TRUTH TABLE

A_1	A_0	EN	ON CHANNEL
X	X	L	None
L	L	H	1 (Note)
L	H	H	2
H	L	H	3
H	H	H	4

NOTE: Channel 1 is shown selected in the Functional Diagram.

Typical Applications

Often it is desirable to buffer the HI-524 output, to avoid loading errors due to the channel "ON" resistance:



NOTE: Capacitor value may be selected to optimize AC performance.

The buffer amplifier should offer sufficient bandwidth and slew rate to avoid degradation of the anticipated signals. For video switching, the HA-5033 and HA-2542 offer good performance plus ±100mA output current for driving coaxial cables. For general wideband applications, the HA-2541 offers the convenience of unity gain stability plus 90ns settling (to ±0.1%) and ±10V output swing. Also, the HI-524 includes a feedback resistance for use with the HA-2541. This resistance matches and tracks the channel "ON" resistance, to minimize offset voltage due to the buffer's bias currents.

Note that the on-chip feedback element between pins 16 and 18 includes two switches in series, to simulate a channel resistance. These switches open for V_{EN} = Low. This allows two or more HI-524s to operate into one HA-2541, with their feedback elements connected in parallel. Thus, only the selected multiplexer provides feedback, and the amplifier remains stable.

All HI-524 DIP package pins labeled 'SIG GND' (pins 3, 4, 6, 13, 15) should be externally connected to signal ground for best crosstalk performance.

Bypass capacitors (0.1µF to 1µF) are recommended from each HI-524 supply pin to power ground (pins 1 and 17 to pin 8 DIP package). Locate the buffer amplifier near the HI-524 so the two capacitors may bypass both devices.

If an analog input 1V or greater is present when supplies are off, a low resistance is seen from that input to a supply line. (For example, the resistance is approximately 160Ω for an input of -3V.) Current flow may be blocked by a diode in each supply line, or limited by a resistor in series with each channel. The best solution, of course, is to arrange that no digital or analog inputs are present when the power supplies are off.

Die Characteristics

DIE DIMENSIONS:

2250µm x 3720µm x 485µm ±25µm

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

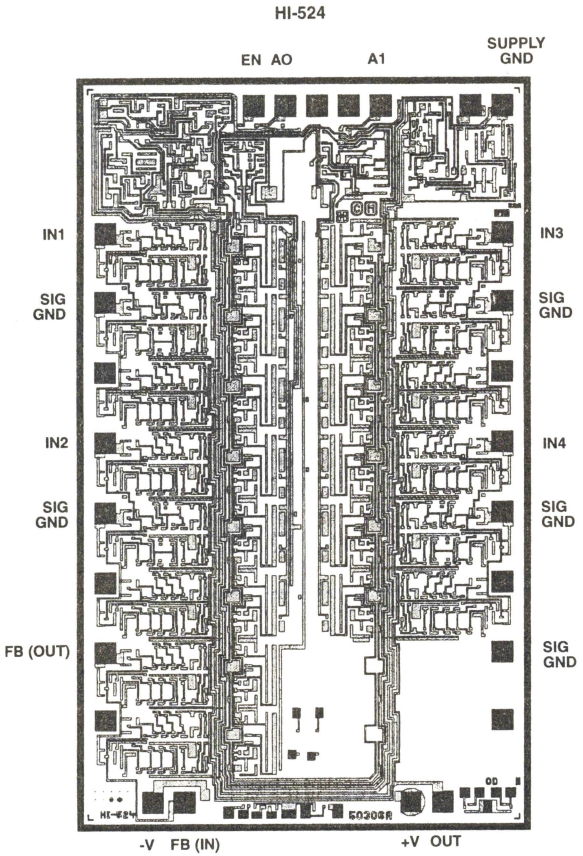
PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.58×10^5 A/cm^2

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HI-539

Monolithic, 4-Channel, Low-Level, Differential Multiplexer

August 1997

Features

- Differential Performance, Typical:
  - Low Δr_{ON}, 125°C 5.5Ω
  - Low $\Delta I_{D(ON)}$, 125°C 0.6nA
  - Low Δ(Charge Injection) 0.1pC
  - Low Crosstalk . . . . . -124dB
- Settling Time, ±0.01% 900ns
- Wide Supply Range . . . . . ±5V to ±18V
- Break-Before-Make Switching
- No Latch-Up

Applications

- Low Level Data Acquisition
- Precision Instrumentation
- Test Systems

Description

The Harris HI-539 is a monolithic, 4-Channel, differential multiplexer. Two digital inputs are provided for channel selection, plus an Enable input to disconnect all channels.

Performance is guaranteed for each channel over the voltage range ±10V, but is optimized for low level differential signals. Leakage current, for example, which varies slightly with input voltage, has its distribution centered at zero input volts.

In most monolithic multiplexers, the net differential offset due to thermal effects becomes significant for low level signals. This problem is minimized in the HI-539 by symmetrical placement of critical circuitry with respect to the few heat producing devices.

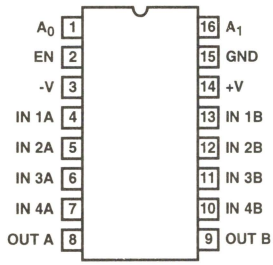
Supply voltages are ±15V and power consumption is only 2.5mW.

Ordering Information

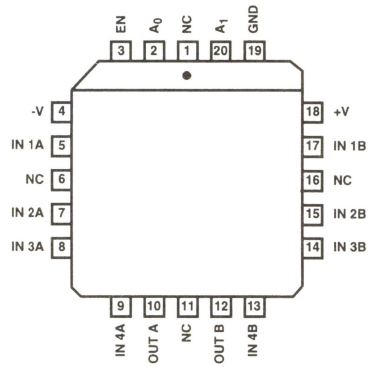
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI4P0539-5	0 to 75	20 Ld PLCC	N20.35
HI1-0539-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-0539-5	0 to 75	16 Ld PDIP	E16.3
HI1-0539-4	-25 to 85	16 Ld CERDIP	F16.3
HI1-0539-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0539-8	-55 to 125	16 Ld CERDIP	F16.3

Pinouts

HI1-539 (CERDIP)
HI3-539 (PDIP)
TOP VIEW



HI4P539 (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3149.1**

Absolute Maximum Ratings

Voltage Between Supply Pins (+V, -V) 40V
Voltage From Either Supply to GND 20V
Analog Input Voltage, V_{IN} . . . . . $-V \le V_{IN} \le +V$
Digital Input Voltage . . . . . $-V \le V_A \le +V$
Current (Source or Drain) 20mA

Operating Conditions

Temperature Range
HI-539-2, -8 . . . . . -55°C to 125°C
HI-539-4 . . . . . -25°C to 85°C
HI-539-5 . . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	85	32
PDIP Package	100	N/A
PLCC Package	80	N/A

Maximum Junction Temperature
CERDIP Package . . . . . 175°C
PDIP, PLCC Package . . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = ±15V. V_{EN} = +4V. V_{AH} (Logic Level High) = +4V, V_{AL} (Logic Level Low) = +0.8V. See the "Performance Curves". Selected parameters are defined in "Definitions", Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-539-2, -4, -8,		HI-539 -5		UNITS
			TYP	MAX (MIN)	TYP	MAX (MIN)	
SWITCHING CHARACTERISTICS							
Access Time, t_A		25	250	750	250	750	ns
		Full	-	1,000	-	1,000	ns
Break-Before-Make Delay, t_{OPEN}		25	85	(30)	85	(30)	ns
		Full	-	(30)	-	(30)	ns
Enable Delay On, $t_{ON(EN)}$		25	250	750	250	750	ns
		Full	-	1,000	-	1,000	ns
Enable Delay Off, $t_{OFF(EN)}$		25	160	650	160	650	ns
		Full	-	900	-	900	ns
Settling Time, to ±0.01%		25	0.9	-	0.9	-	µs
Charge Injection (Output)		Full	3	-	3	-	pC
Δ Charge Injection (Output)		Full	0.1	-	0.1	-	pC
Charge Injection (Input)		Full	10	-	10	-	pC
Differential Crosstalk	Note 3	25	124	-	124	-	dB
Single Ended Crosstalk	Note 3	25	100	-	100	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		Full	5	-	5	-	pF
Channel Output Capacitance, $C_{D(OFF)}$		Full	7	-	7	-	pF
Channel On Output Capacitance, $C_{D(ON)}$		Full	17	-	17	-	pF
Input to Output Capacitance, C_{DS}	Note 4	Full	0.08	-	0.08	-	pF
Digital Input Capacitance, C_A		Full	3	-	3	-	pF
DIGITAL INPUT CHARACTERISTICS							
Input Low Threshold, V_{AL}		Full	-	0.8	-	0.8	V
Input High Threshold, V_{AH}		Full	-	(4.0)	-	(4.0)	V
Input Leakage Current (High), I_{AH}		Full	-	1	-	1	µA
Input Leakage Current (Low), I_{AL}		Full	-	1	-	1	µA
ANALOG CHANNEL CHARACTERISTICS							
Analog Signal Range, V_{IN}		Full	-	(-10)/+10	-	(-10)/+10	V
On Resistance, r_{ON}	V_{IN} = 0V	25	650	850	650	850	Ω
	V_{IN} = ±10V	25	700	900	700	900	Ω
	V_{IN} = 0V	Full	950	1.3K	800	1K	Ω
	V_{IN} = ±10V	Full	1.1K	1.4K	900	1.1K	Ω

Electrical Specifications Supplies = ±15V. V_{EN} = +4V. V_{AH} (Logic Level High) = +4V, V_{AL} (Logic Level Low) = +0.8V. See the "Performance Curves". Selected parameters are defined in "Definitions", Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-539-2, -4, -8,		HI-539 -5		UNITS
			TYP	MAX (MIN)	TYP	MAX (MIN)	
(Side A-Side B), Δr_{ON}	V_{IN} = 0V	25	4.0	24	4.0	24	Ω
	V_{IN} = ±10V	25	4.5	27	4.5	27	Ω
	V_{IN} = 0V	Full	4.75	28	4.0	24	Ω
	V_{IN} = ±10V	Full	5.5	33	4.5	27	Ω
Off Input Leakage Current, $I_{S(OFF)}$	Condition 0V (Note 1)	25	30	-	30	-	pA
	Condition ±10V (Note 1)	25	100	-	100	-	pA
	Condition 0V (Note 1)	Full	2	10	0.2	1	nA
	Condition ±10V (Note 1)	Full	5	25	0.5	2.5	nA
(Side A-Side B), $\Delta I_{S(OFF)}$	Condition 0V	25	3	-	3	-	pA
	Condition ±10V	25	10	-	10	-	pA
	Condition 0V	Full	0.2	2	0.02	0.2	nA
	Condition ±10V	Full	0.5	5	0.05	0.5	nA
Off Output Leakage Current, $I_{D(OFF)}$	Condition 0V (Note 1)	25	30	-	30	-	pA
	Condition ±10V (Note 1)	25	100	-	100	-	pA
	Condition 0V (Note 1)	Full	2	10	0.2	1	nA
	Condition ±10V (Note 1)	Full	5	25	0.5	2.5	nA
(Side A-Side B), $\Delta I_{D(OFF)}$	Condition 0V	25	3	-	3	-	pA
	Condition ±10V	25	10	-	10	-	pA
	Condition 0V	Full	0.2	2	0.02	0.2	nA
	Condition ±10V	Full	0.5	5	0.05	0.5	nA
On Channel Leakage Current, $I_{D(ON)}$	Condition 0V (Note 1)	25	50	-	50	-	pA
	Condition ±10V (Note 1)	25	150	-	150	-	pA
	Condition 0V (Note 1)	Full	5	25	0.5	2.5	nA
	Condition ±10V (Note 1)	Full	6	40	0.8	4.0	nA
(Side A-Side B), $\Delta I_{D(ON)}$	Condition 0V	25	10	-	10	-	pA
	Condition ±10V	25	30	-	30	-	pA
	Condition 0V	Full	0.5	5	0.05	0.5	nA
	Condition ±10V	Full	0.6	6	0.08	0.8	nA
Differential Offset Voltage, ΔV_{OS}	Note 2	25	0.02	-	0.02	-	µV
		Full	0.70	-	0.08	-	µV
POWER REQUIREMENTS							
Power Dissipation, P_D		25	2.3	-	2.3	-	mW
		Full	-	45	-	45	mW
Current, I+		25	0.150	-	0.150	-	mA
		Full	-	2.0	-	2.0	mA
Current, I-		25	0.001	-	0.001	-	mA
		Full	-	1.0	-	1.0	mA
Supply Voltage Range, ±V		Full	±15	(±5)/±18	±15	(±5)/ ±18	V

NOTES:

1. See Figures 2B, 2C, 2D. The condition ±10V means:
   $I_{S(OFF)}$ and $I_{D(OFF)}$:
   (V_S = +10V, V_D = -10V), then
   (V_S = -10V, V_D = +10V)
   $I_{D(ON)}$: (+10V, then -10V)
2. ΔV_{OS} (Exclusive of thermocouple effects) = $r_{ON} \Delta I_{D(ON)} + I_{D(ON)} \Delta r_{ON}$. See Applications section for discussion of additional V_{OS} error.
3. V_{IN} = 1kHz, $15V_{P-P}$ on all but the selected channel. See Figure 7.
4. Calculated from typical Single-Ended Crosstalk performance.

Typical Performance Curves

Unless Otherwise Specified $T_A = 25^oC$, V+ = +15V, V- = -15V, V_{AH} = +4V and V_{AL} = +0.8V

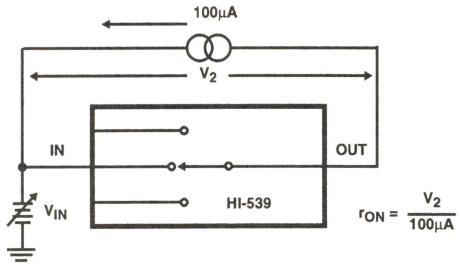


FIGURE 1A. ON RESISTANCE TEST CIRCUIT

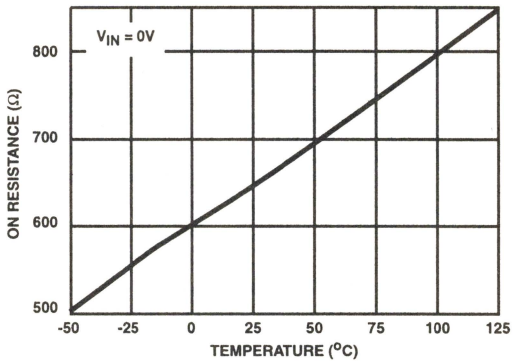


FIGURE 1B. ON RESISTANCE vs TEMPERATURE

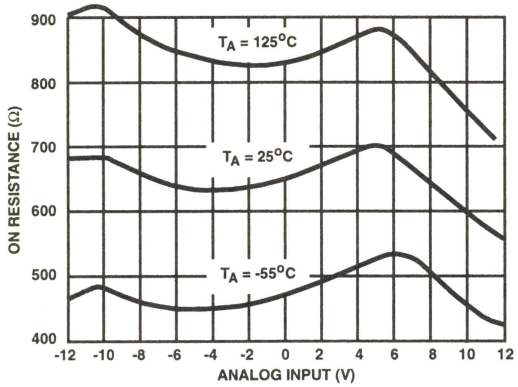


FIGURE 1C. ON RESISTANCE vs ANALOG INPUT VOLTAGE

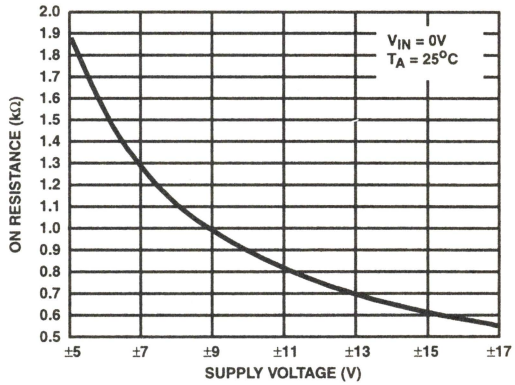


FIGURE 1D. ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

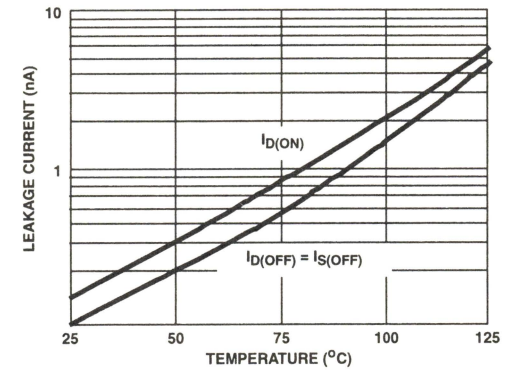
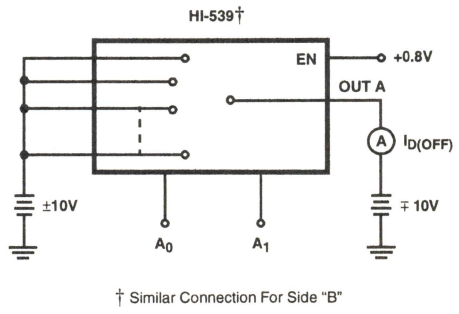


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

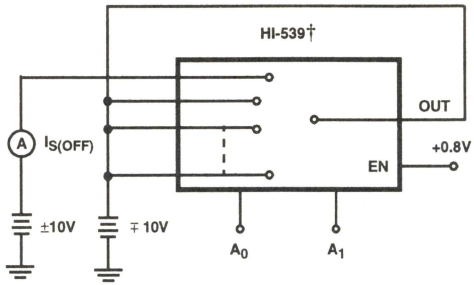


† Similar Connection For Side "B"

FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT (NOTE 1)

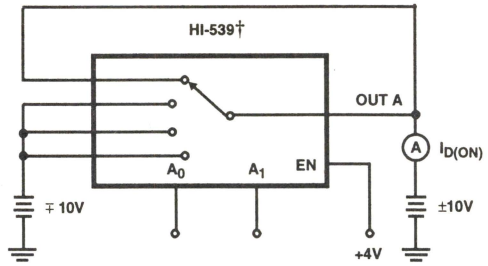
Typical Performance Curves (Continued)

Unless Otherwise Specified $T_A = 25^oC$, V+ = +15V, V- = -15V, V_{AH} = +4V and V_{AL} = +0.8V



† Similar Connection For Side "B"

FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT (NOTE 1)



†Similar Connection For Side "B"

FIGURE 2D. $I_{D(ON)}$ TEST CIRCUIT (NOTE 1)

NOTE:

1. Three measurements = +10V/-10V, -10V/+10V, and 0V.

FIGURE 2. LEAKAGE CURRENT

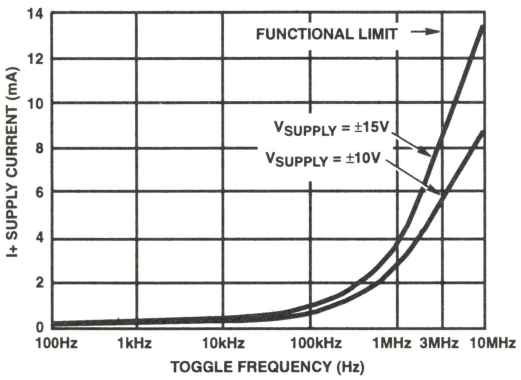
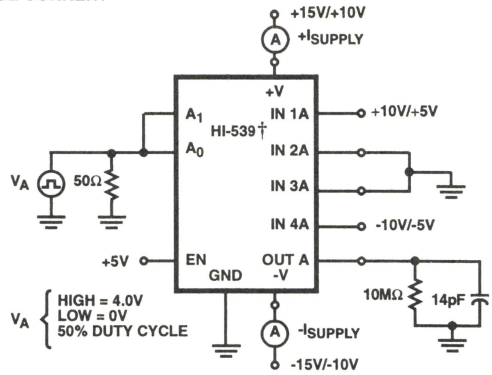


FIGURE 3A. SUPPLY CURRENT vs TOGGLE FREQUENCY



†Similar Connection For Side "B"

FIGURE 3B. SUPPLY CURRENT TEST CIRCUIT

FIGURE 3. SUPPLY CURRENT

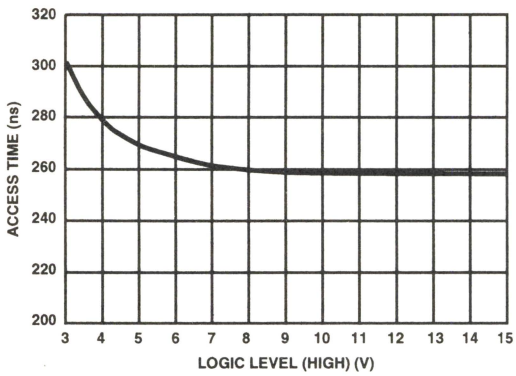


FIGURE 4A. ACCESS TIME vs LOGIC LEVEL (HIGH)

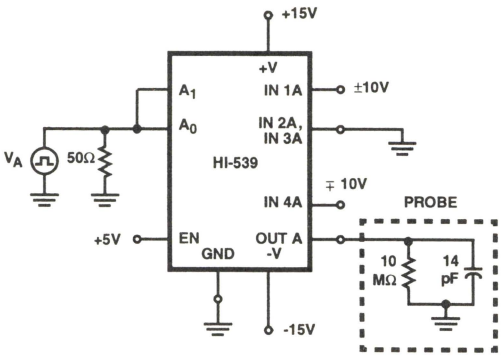


FIGURE 4B. ACCESS TIME TEST CIRCUIT

Typical Performance Curves Unless Otherwise Specified $T_A = 25^oC$, V+ = +15V, V- = -15V, V_{AH} = +4V and V_{AL} = +0.8V (Continued)

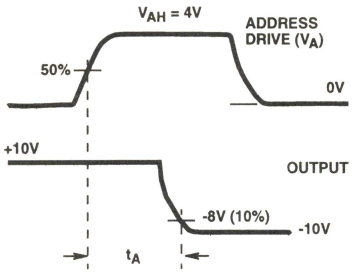


FIGURE 4C. ACCESS TIME MEASUREMENT

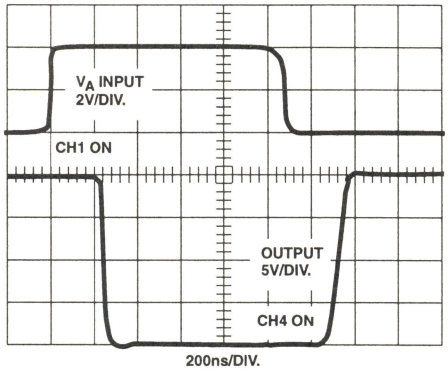


FIGURE 4D. ACCESS TIME WAVEFORMS

FIGURE 4. ACCESS TIME

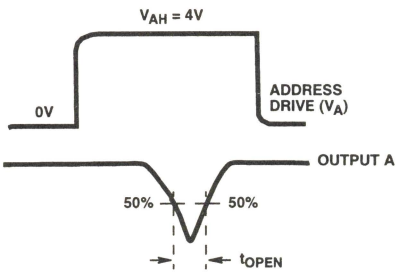


FIGURE 5A. t_{OPEN} MEASUREMENT

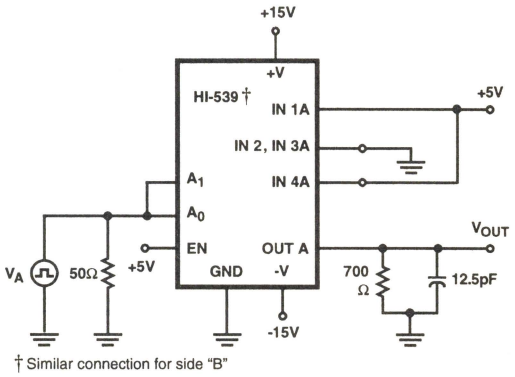


FIGURE 5B. t_{OPEN} TEST CIRCUIT

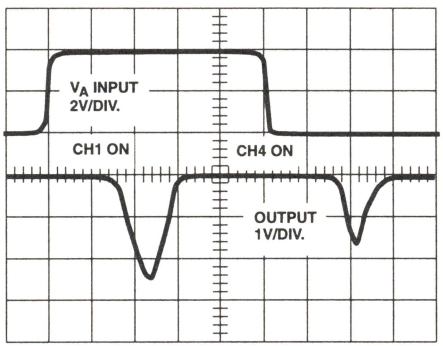


FIGURE 5. t_{OPEN} WAVEFORMS

FIGURE 5. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

Typical Performance Curves (Continued)

Unless Otherwise Specified $T_A = 25^oC$, V+ = +15V, V- = -15V, V_{AH} = +4V and V_{AL} = +0.8V

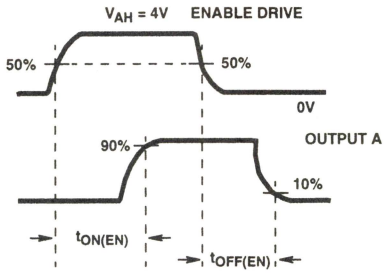
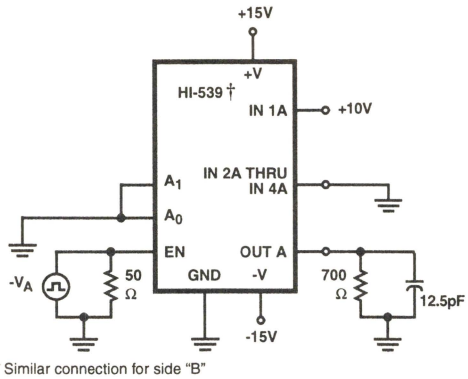


FIGURE 6A. $t_{ON(EN)}$, $t_{OFF(EN)}$ MEASUREMENT



† Similar connection for side "B"

FIGURE 6B. $t_{ON(EN)}$, $t_{OFF(EN)}$ TEST CIRCUIT

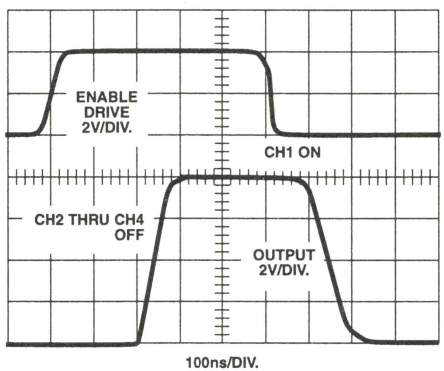
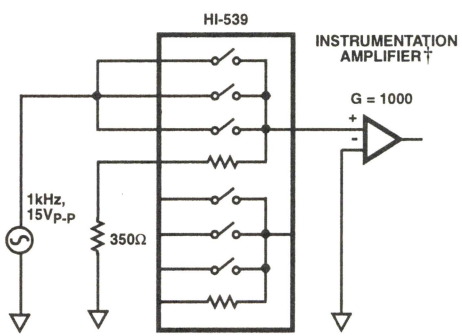


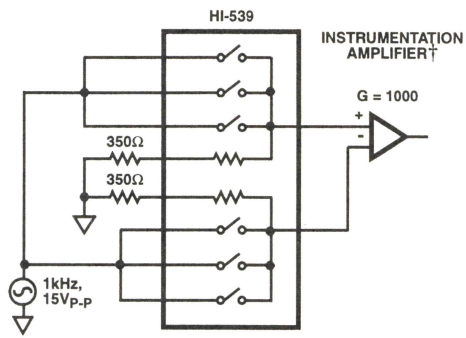
FIGURE 6C. $t_{ON(EN)}$, $t_{OFF(EN)}$ WAVEFORMS

FIGURE 6. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



† AD606 or BB3630, for Example

FIGURE 7A. SINGLE-ENDED CROSSTALK TEST CIRCUIT



† AD606 or BB3630, for example

FIGURE 7B. DIFFERENTIAL CROSSTALK TEST CIRCUIT

FIGURE 7. CROSSTALK

Typical Applications

General

The HI-539 accepts inputs in the range -15V to +15V, with performance guaranteed over the ±10V range. At these higher levels of analog input voltage it is comparable to the HI-509, and is plug-in compatible with that device (as well as the HI-509A). However, as mentioned earlier, the HI-539 was designed to introduce minimum error when switching low level inputs.

Special care is required in working with these low level signals. The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded differential signal path is essential to maintain a noise level below $50\mu V_{RMS}$.

Low Level Signal Transmission

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only $^1/_{10}$ as much leakage capacitance to ground per foot. A key requirement for the transmission cable is that it presents a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in phase to both conductors, and may be rejected as common-mode voltage by a differential amplifier connected to the multiplexer output.

Coaxial cable is not suitable for low level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

Watch Small ΔV Errors

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12 bits or more.

Table 1 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values of inductance.)

As an example, suppose the HI-539 is feeding a 12-bit converter system with an allowable error of $\pm^1/_2$ LSB (±1.22mV). If the interface logic draws 100mA from the 5V supply, this current will produce 1.28mV across 6 inches of #24 wire; more than the error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

TABLE 1.

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 oz. Cu)	DC RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				60Hz	10kHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.37μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

Provide Path For I_{BIAS}

The input bias current for any DC-coupled amplifier must have an external path back to the amplifier's power supply. No such path exists in Figure 8A, and consequently the amplifier output will remain in saturation.

A single large resistor (1MΩ to 10MΩ) from either signal line to power supply common will provide the required path, but a resistor on each line is necessary to preserve accuracy. A single pair of these bias current resistors on the HI-539 output may be used if their loading effect can be tolerated (each forms a voltage divider with r_{ON}). Otherwise, a resistor pair on each input channel of the multiplexer is required.

The use of bias current resistors is acceptable only if one is confident that the sum of signal plus common-mode voltage will remain within the input range of the multiplexer/amplifier combination.

Another solution is to simply run a third wire from the low side of the signal source, as in Figure 8B. This wire assures a low common-mode voltage as well as providing the path for bias currents. Making the connection near the multiplexer will save wire, but it will also unbalance the line and reduce the amplifier's common-mode rejection.

Differential Offset, ΔV_{OS}

There are two major sources of ΔV_{OS}. That part due to the expression ($r_{ON}\,\Delta I_{D(ON)} + I_{D(ON)}\,\Delta r_{ON}$) becomes significant with increasing temperature, as shown in the Electrical Specifications tables. The other source of offset is the thermocouple effects due to dissimilar materials in the signal path. These include silicon, aluminum, tin, nickel-iron and (often) gold, just to exit the package.

For the thermocouple effects in the package alone, the constraint on ΔV_{OS} may be stated in terms of a limit on the difference in temperature for package pins leading to any channel of the HI-539. For example, a difference of $0.13^{o}C$ produces a 5μV offset. Obviously, this ΔT effect can dominate the ΔV_{OS} parameter at any temperature unless care is taken in mounting the HI-539 package.

Temperature gradients across the HI-539 package should be held to a minimum in critical applications. Locate the HI-539 far from heat producing components, with any air currents flowing lengthwise across the package.

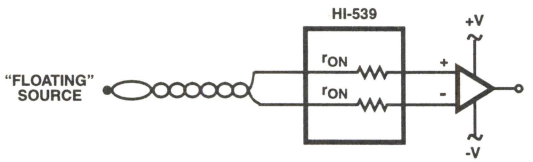
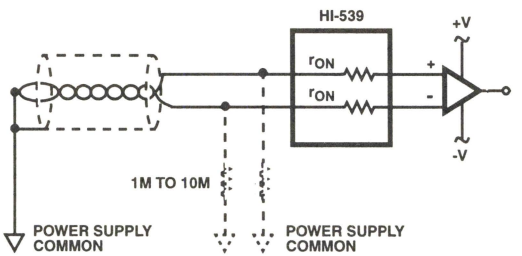


FIGURE 8A.



NOTE: The amplifier in Figure 8A is unusable because its bias currents cannot return to the power supply. Figure 8B shows two alternative paths for these bias currents: either a pair of resistors, or (better) a third wire from the low side of the signal source.

FIGURE 8B.

Die Characteristics

DIE DIMENSIONS:

92 mils x 100 mils

METALLIZATION:

Type: AlCu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2.0kÅ

WORST CASE CURRENT DENSITY:

2.54×10^5 A/cm^2 at 20mA

TRANSISTOR COUNT:

236

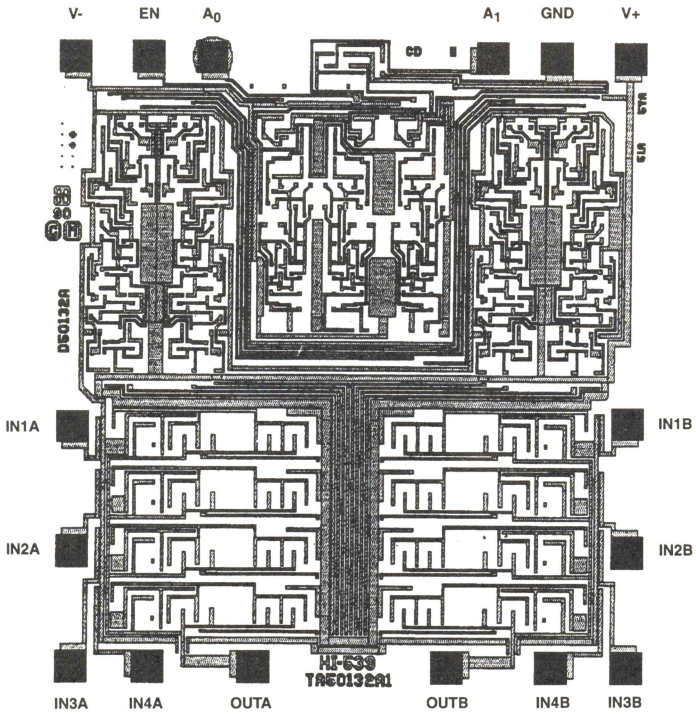
PROCESS:

CMOS-DI

NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layout

HI-539



HARRIS SEMICONDUCTOR

HI-546, HI-547, HI-548, HI-549

Single 16 and 8, Differential 8-Channel and 4-Channel CMOS Analog MUXs with Active Overvoltage Protection

August 1997

Features

- Analog Overvoltage Protection ..... $70V_{P-P}$
- No Channel Interaction During Overvoltage
- Guaranteed r_{ON} Matching
- 44V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range..... ±15V
- Access Time (Typical)..... 500ns
- Standby Power (Typical) 7.5mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Description

The HI-546, HI-547, HI-548 and HI-549 are analog multiplexers with active overvoltage protection and guaranteed r_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers.

Analog inputs can withstand constant $70V_{P-P}$ levels with ±15V supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents 1kΩ of resistance under this condition. These features make the HI-546, HI-547, HI-548 and HI-549 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. All devices are fabricated with 44V Dielectrically Isolated CMOS technology. The HI-546 is a single 16-Channel, the HI-547 is an 8-Channel differential, the HI-548 is a single 8-Channel and the HI-549 is a 4-Channel differential device. If input overvoltage protection is not needed the HI-506/507/508/509 multiplexers are recommended. For further information see Application Notes AN520 and AN521. The HI-546 and HI-547 devices are available in a 28 lead Plastic or Ceramic DIP and a 28 pad Ceramic LCC package. The HI-548/549 devices are available in a 16 lead Plastic or Ceramic DIP and a 20 pad Ceramic LCC package.

The HI-546, HI-547, HI-548 and HI-549 are offered in industrial/commercial and military grades. Additional Hi-Rel screening including 160 hour Burn-In is specified by the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-546/883, HI-547/883, HI-548/883 and HI-549/883 datasheets.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0546-4	-25 to 85	28 Ld CERDIP	F28.6
HI1-0546-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0546-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0546/883	-55 to 125	28 Ld CERDIP	F28.6
HI3-0546-5	0 to 75	28 Ld PDIP	E28.6
HI3-0546-9	-40 to 85	28 Ld PDIP	E28.6
HI4-0546/883	-55 to 125	28 Ld CLCC	J28.A
HI4P0546-5	0 to 75	28 Ld PLCC	N28.45
HI9P0546-5	0 to 75	28 Ld SOIC	M28.3
HI9P0546-9	-40 to 85	28 Ld SOIC	M28.3
HI1-0547-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0547-4	-25 to 85	28 Ld CERDIP	F28.6
HI1-0547-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0547/883	-55 to 125	28 Ld CERDIP	F28.6
HI3-0547-5	0 to 75	28 Ld PDIP	E28.6
HI4-0547/883	-55 to 125	28 Ld CLCC	J28.A
HI4P0547-5	0 to 75	28 Ld PLCC	N28.45
HI9P0547-5	0to 75	28 Ld SOIC	M28.3
HI9P0547-9	-40 to 85	28 Ld SOIC	M28.3

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0548-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0548-4	-25 to 85	16 Ld CERDIP	F16.3
HI1-0548-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0548/883	-55 to 125	16 Ld CERDIP	F16.3
HI3-0548-5	0 to 75	16 Ld PDIP	E16.3
HI4-0548/883	-55 to 125	20 Ld CLCC	J20.A
HI4P0548-5	0 to 75	20 Ld PLCC	N20.35
HI9P0548-5	0 to 75	16 Ld SOIC	M16.15
HI9P0548-9	-40 to 85	16 Ld SOIC	M16.15
HI1-0549-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0549-4	-25 to 85	16 Ld CERDIP	F16.3
HI1-0549-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0549/883	-55 to 125	16 Ld CERDIP	F16.3
HI3-0549-5	0 to 75	16 Ld PDIP	E16.3
HI3-0549-9	-40 to 85	16 Ld PDIP	E16.3
HI4-0549/883	-55 to 125	20 Ld CLCC	J20.A
HI4P0549-5	0 to 75	20 Ld PLCC	N20.35
HI9P0549-5	0 to 75	16 Ld SOIC	M16.15
HI9P0549-9	-40 to 85	16 Ld SOIC	M16.15

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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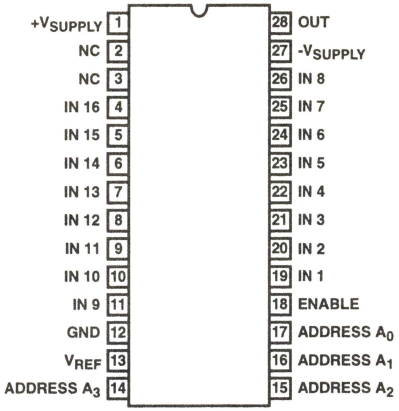
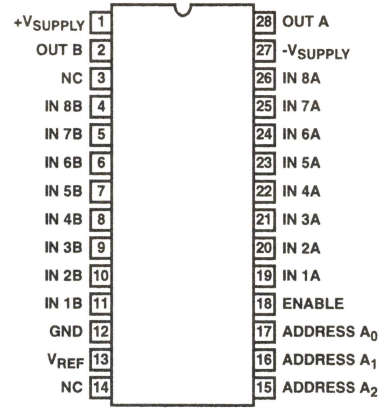
File Number **3150.1**

Pinouts

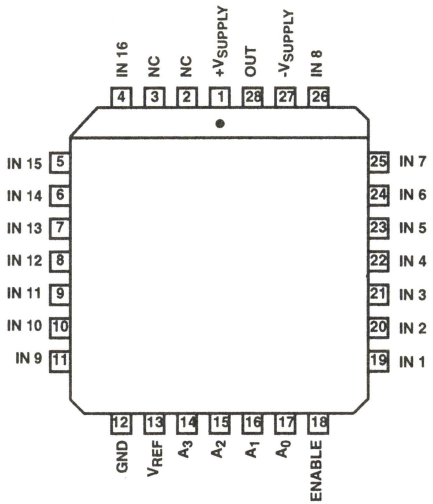
HI1-0546 (CERDIP), HI3-0546 (PDIP), HI9P0546 (SOIC)
TOP VIEW



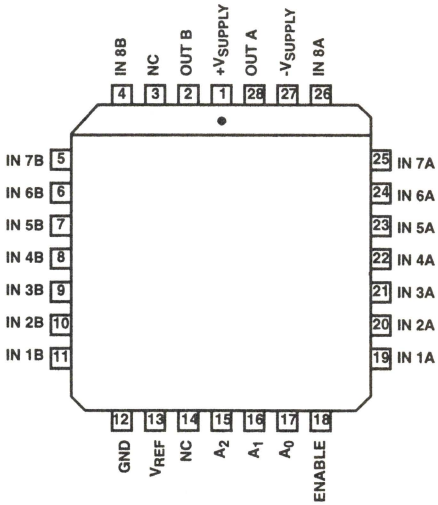
HI1-0547 (CERDIP), HI3-0547 (PDIP), HI9P0547 (SOIC)
TOP VIEW



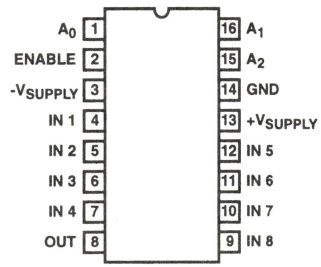
H14-0546 (CLCC
HI4P0546 (PLCC)
TOP VIEW



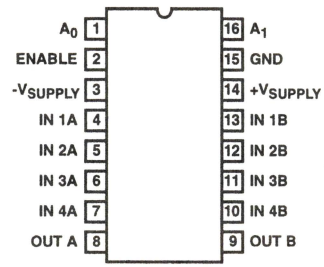
H14-0547 (CLCC
HI4P0547 (PLCC)
TOP VIEW



HI1-0548 (CERDIP), HI3-0548 (PDIP), HI9P0548 (SOIC)
TOP VIEW

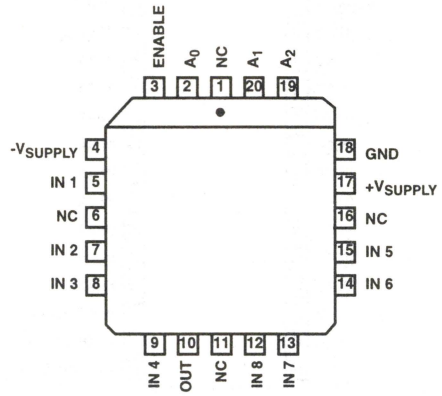


HI1-0549 (CERDIP), HI3-0549 (PDIP), HI9P0549 (SOIC)
TOP VIEW

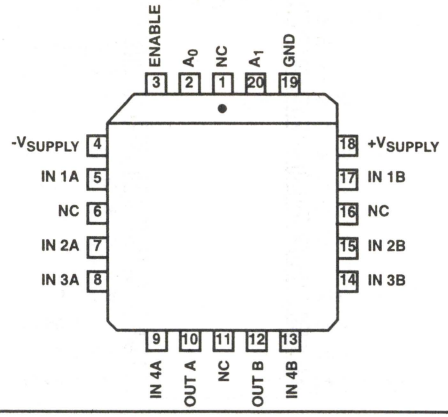


Pinouts (Continued)

HI14-0548 (CLCC)
HI4P0548 (PLCC)
TOP VIEW

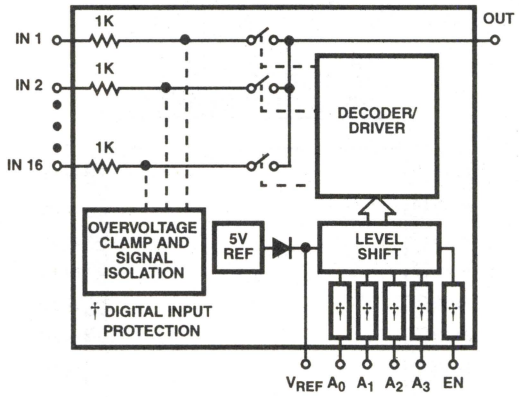


HI4-0549 (CLCC)
HI4P0549 (PLCC)
TOP VIEW

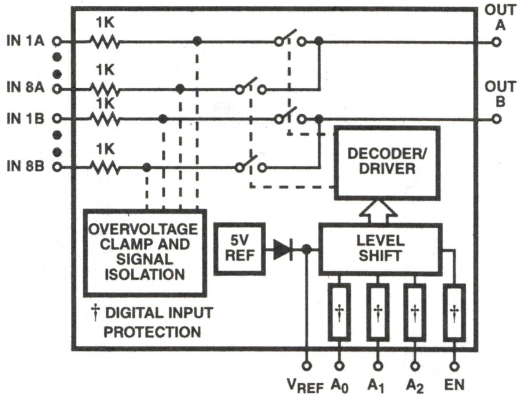


Functional Diagrams

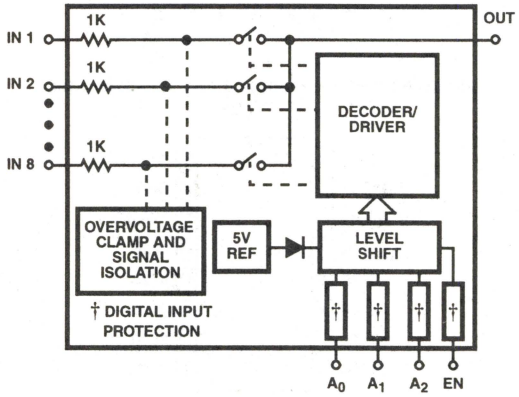
HI-546



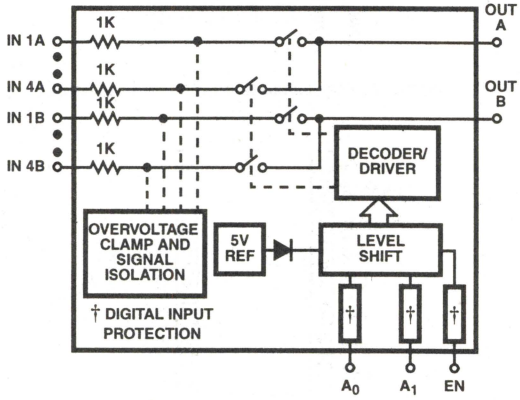
HI-547



HI-548

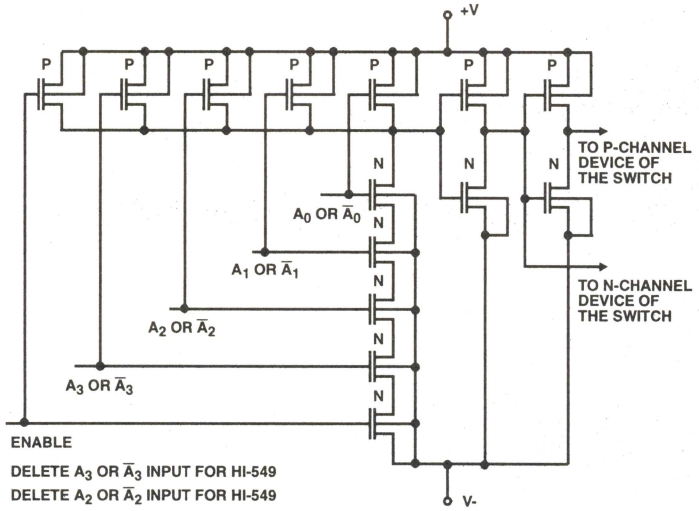


HI-549

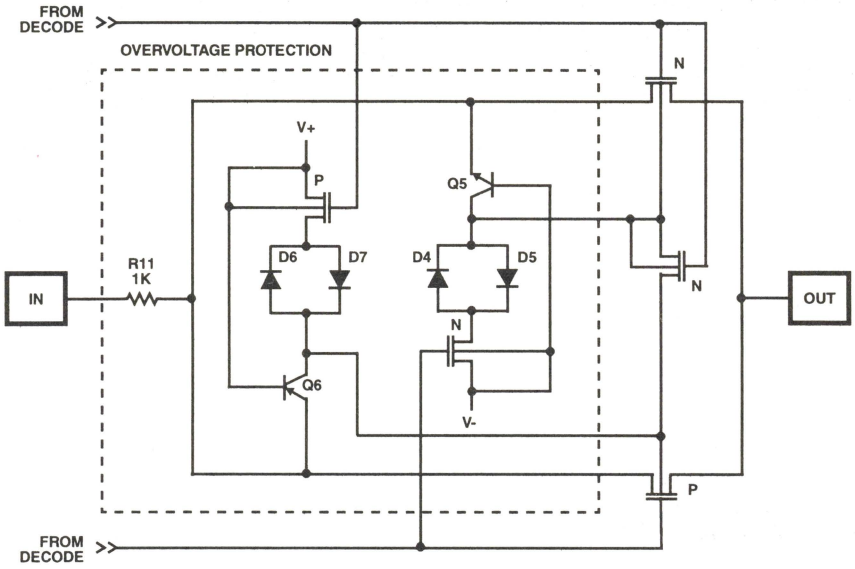


Schematic Diagrams

ADDRESS DECODER

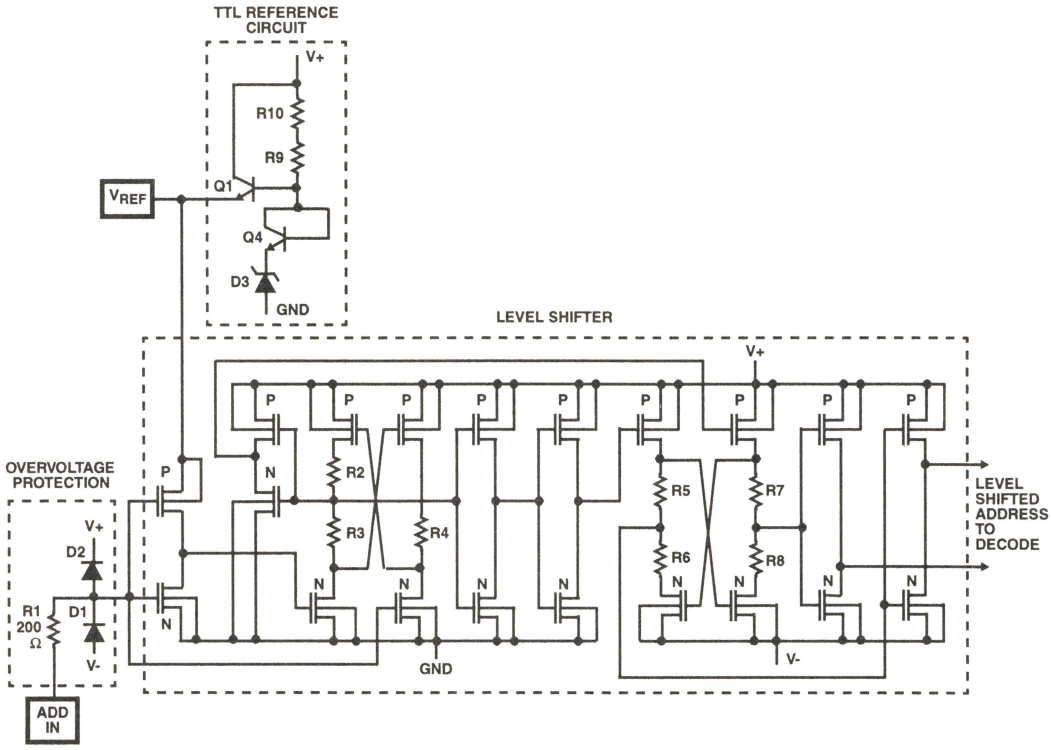


MULTIPLEX SWITCH



Schematic Diagrams (Continued)

ADDRESS INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ . . . . . +44V
$V_{SUPPLY(+)}$ to GND . . . . . +22V
$V_{SUPPLY(-)}$ to GND. . . . . -25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ . . . . . $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ . . . . . $-V_{SUPPLY}$ -4V
or 20mA, Whichever Occurs First
Analog Signal Overvoltage (Note 6)
$+V_S$ . . . . . $+V_{SUPPLY}$ +20V
$-V_S$ . . . . . $-V_{SUPPLY}$ -20V
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed at 1ms, 10% Duty Cycle Max)

Operating Conditions

Operating Temperature Ranges
HI-546/547/548/549-2. . . . . -55°C to 125°C
HI-546/547/548/549-4. . . . . -25°C to 85°C
HI-546/547/548/549-5. . . . . 0°C to 75°C
HI-546/547/548/549-9. . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld CERDIP Package	85	32
28 Ld CERDIP Package	55	18
20 Ld CLCC Package	80	28
28 Ld CLCC Package	70	20
28 Ld PDIP Package	60	N/A
16 Ld PDIP Package	100	N/A
28 Ld PLCC Package	70	N/A
20 Ld PLCC Package	80	N/A
28 Ld SOIC Package	70	N/A
16 Ld SOIC Package	100	N/A

Maximum Junction Temperature
Ceramic Package . . . . . 175°C
Plastic Package . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC, SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4V; V_{AL} (Logic Level Low) = +0.8V; Unless Otherwise Specified. For Test Conditions, Consult Performance Curves

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-54X-2			HI-54X-4, -5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, t_A		25	-	0.5	-	-	0.5	-	µs
		Full	-	-	1.0	-	-	1.0	µs
Break-Before Make Delay, t_{OPEN}		25	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$		25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$		25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Settling Time (0.1%)		25	-	1.2	-	-	1.2	-	µs
(0.01%)		25	-	3.5	-	-	3.5	-	µs
"Off Isolation"	Note 5	25	50	68	-	50	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	5	-	-	5	-	pF
Channel Output Capacitance $C_{D(OFF)}$									
HI-546		25	-	52	-	-	52	-	pF
HI-547		25	-	30	-	-	30	-	pF
HI-548		25	-	25	-	-	25	-	pF
HI-549		25	-	12	-	-	12	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$		25	-	0.1	-	-	0.1	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, TTL Drive, V_{AL}		Full	-	-	0.8	-	-	0.8	V

Electrical Specifications Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4V; V_{AL} (Logic Level Low) = +0.8V; Unless Otherwise Specified. For Test Conditions, Consult Performance Curves **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-54X-2			HI-54X-4, -5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input High Threshold, V_{AH}	Note 7	Full	4.0	-	-	4.0	-	-	V
MOS Drive (HI-546/547 Only), V_{AL}	Note 8	25	-	-	0.8	-	-	0.8	V
MOS Drive (HI-546/547 Only), V_{AH}	Note 8	25	6.0	-	-	6.0	-	-	V
Input Leakage Current (High or Low), I_A	Note 4	Full	-	-	1.0	-	-	1.0	µA
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_S		Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON}	Note 1	25	-	1.2	1.5	-	1.5	1.8	kΩ
		Full	-	1.5	1.8	-	1.8	2.0	kΩ
Δr_{ON}, (Any Two Channels)		25	-	-	7.0	-	-	7.0	%
Off Input Leakage Current, $I_{S(OFF)}$	Note 2	25	-	0.03	-	-	0.03	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$	Note 2	25	-	0.1	-	-	0.1	-	nA
HI-546		Full	-	-	300	-	-	300	nA
HI-547		Full	-	-	200	-	-	200	nA
HI-548		Full	-	-	200	-	-	200	nA
HI-549		Full	-	-	100	-	-	100	nA
With Input Overvoltage Applied, $I_{D(OFF)}$	Note 3	25	-	4.0	-	-	4.0	-	nA
		Full	-	-	2.0	-	-	-	µA
On Channel Leakage Current, $I_{D(ON)}$	Note 2	25	-	0.1	-	-	0.1	-	nA
HI-546		Full	-	-	300	-	-	300	nA
HI-547		Full	-	-	200	-	-	200	nA
HI-548		Full	-	-	200	-	-	200	nA
HI-549		Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current (HI-547, HI-549 Only), I_{DIFF}		Full	-	-	50	-	-	50	nA
POWER REQUIREMENTS									
Power Dissipation, P_D		Full	-	7.5	-	-	7.5	-	mW
Current, I+	Note 6	Full	-	0.5	2.0	-	0.5	2.0	mA
Current, I-	Note 6	Full	-	0.02	1.0	-	0.02	1.0	mA

NOTES:

1. $V_{OUT} = \pm 10V$, $I_{OUT} = \mp 100\mu A$.
2. 10nA is the practical lower limit for high speed measurement in the production test environments.
3. Analog Overvoltage = ±33V.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
5. $V_{EN} = 0.8V$, $R_L = 1K$, $C_L = 15pF$, $V_S = 7V_{RMS}$, f = 100kHz.
6. V_{EN}, V_A = 0V or 4V.
7. To drive from DTL/TTLCircuits, 1kΩ pull-up resistors to $+5V_{SUPPLY}$ are recommended.
8. $V_{REF} = +10V$.

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified

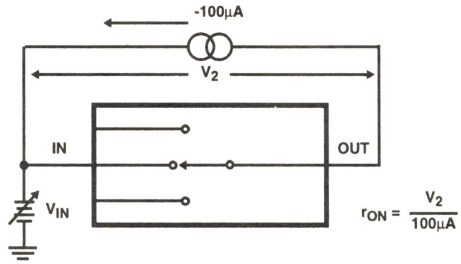


FIGURE 1A. ON RESISTANCE TEST CIRCUIT

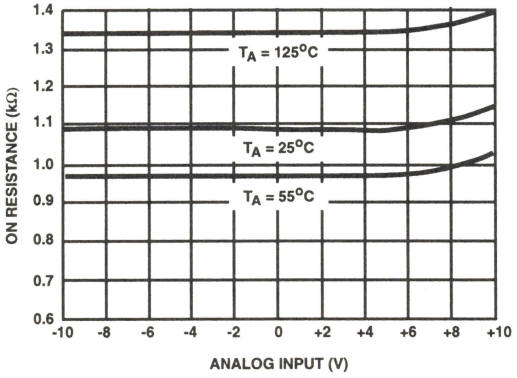


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

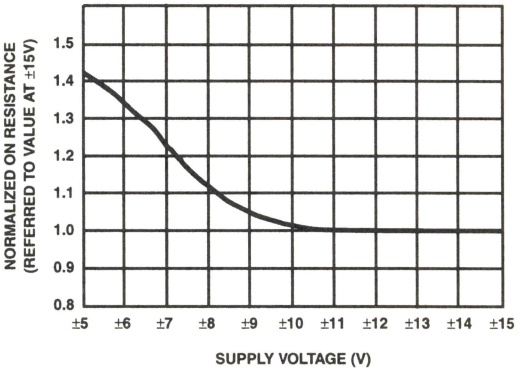


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

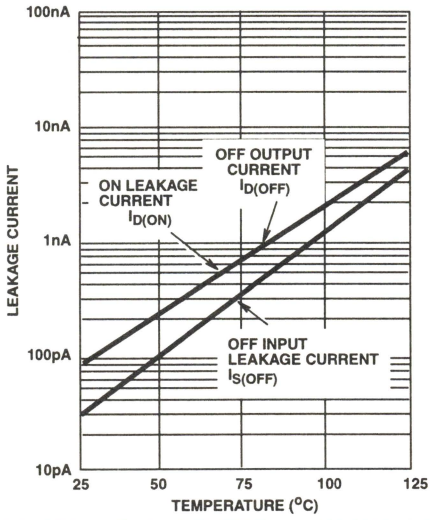


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

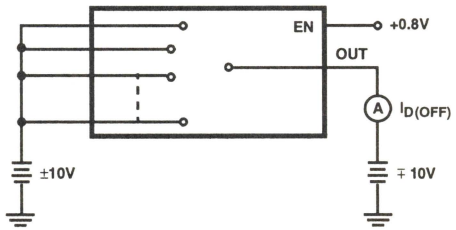


FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT

Typical Performance Curves (Continued)

$T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified

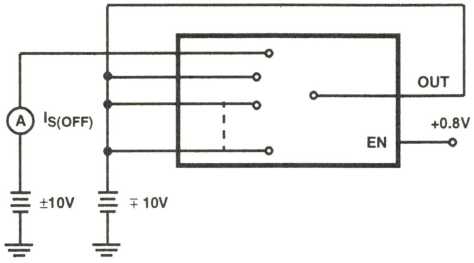


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT

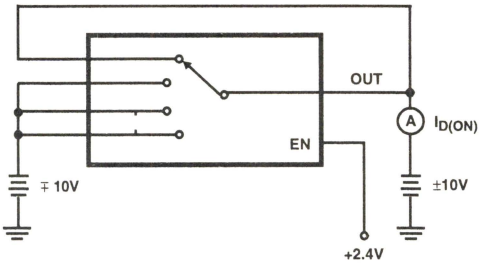


FIGURE 2D. $I_{D(ON)}$ TEST CIRCUIT

NOTE:

1. Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V.)

FIGURE 2. LEAKAGE CURRENT

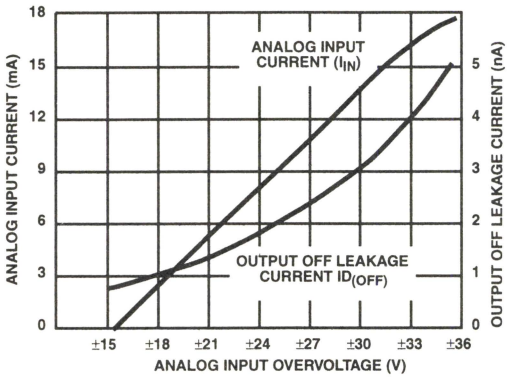


FIGURE 3A. ANALOG INPUT CURRENT AND OUTPUT OFF LEAKAGE CURRENT vs ANALOG INPUT OVER-VOLTAGE

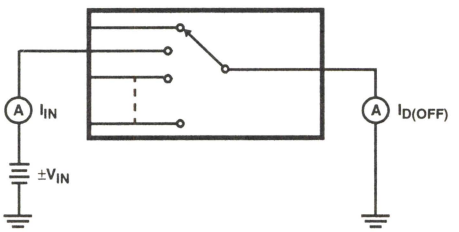


FIGURE 3B. ANALOG INPUT OVERVOLTAGE TEST CIRCUIT

FIGURE 3. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

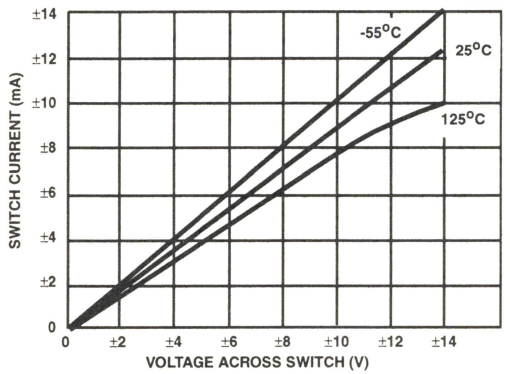


FIGURE 4A. ON CHANNEL CURRENT vs VOLTAGE

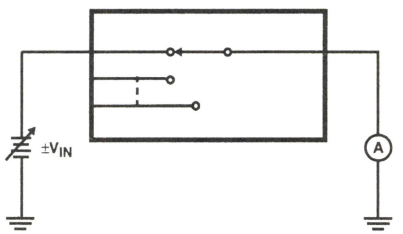


FIGURE 4B. ON CHANNEL CURRENT TEST CIRCUIT

FIGURE 4. ON CHANNEL CURRENT

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified (Continued)

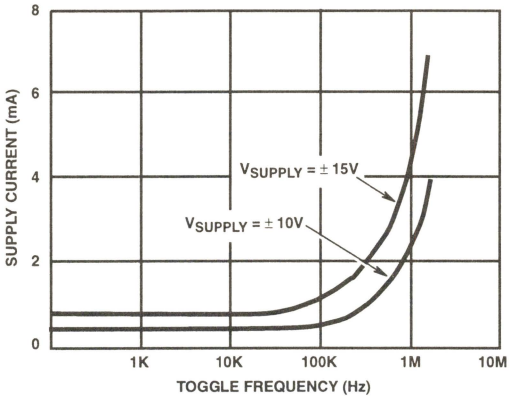
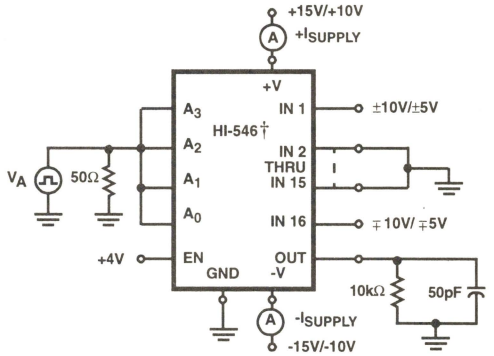


FIGURE 5A. SUPPLY CURRENT vs TOGGLE FREQUENCY



†Similar connection for HI-547/HI-548/HI-549.

FIGURE 5B. SUPPLY CURRENT vs TOGGLE FREQUENCY

FIGURE 5. SUPPLY CURRENT

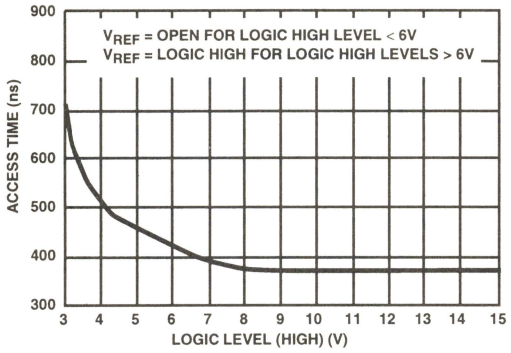
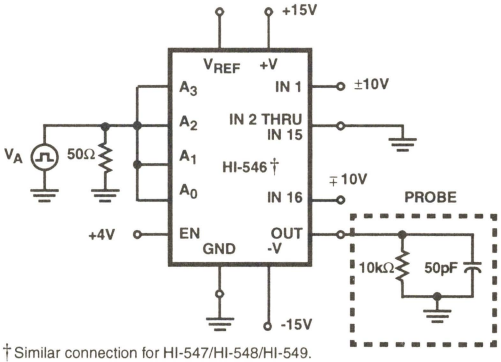


FIGURE 6A. ACCESS TIME vs LOGIC LEVEL (HIGH)



†Similar connection for HI-547/HI-548/HI-549.

FIGURE 6B. ACCESS TIME TEST CIRCUIT

FIGURE 6. ACCESS TIME

Switching Waveforms

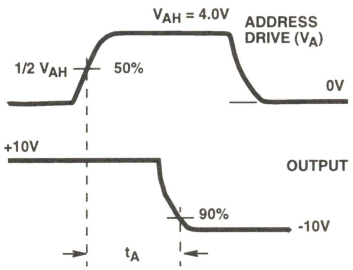


FIGURE 7A. ACCESS TIME MEASUREMENT

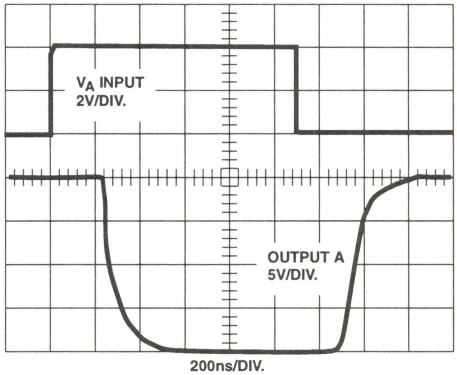
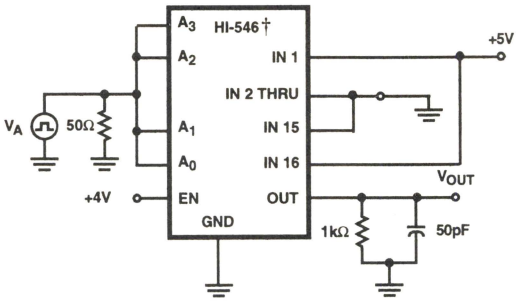


FIGURE 7B. ACCESS TIME WAVEFORMS

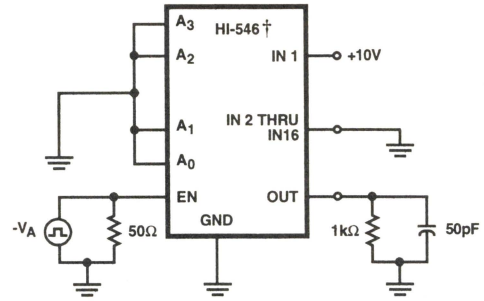
FIGURE 7. ACCESS TIME (Refer to Figure 6B for Test Circuit)

Switching Waveforms (Continued)



† Similar connection for HI-547/HI-548/HI-549

FIGURE 8A. BREAK-BEFORE-MAKE DELAY TEST CIRCUIT



† Similar connection for HI-547/HI-548/HI-549

FIGURE 9A. ENABLE DELAY TEST CIRCUIT

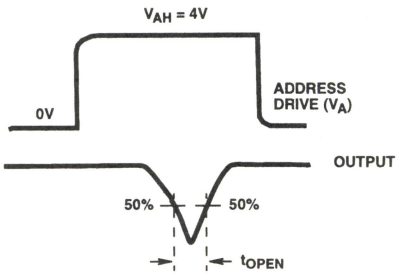


FIGURE 8B. BREAK-BEFORE-MAKE DELAY MEASUREMENT

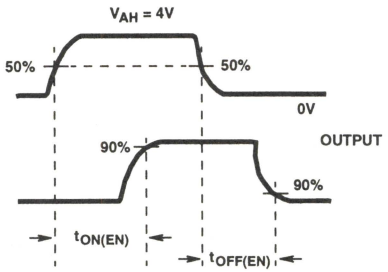


FIGURE 9B. ENABLE DELAY MEASUREMENTS

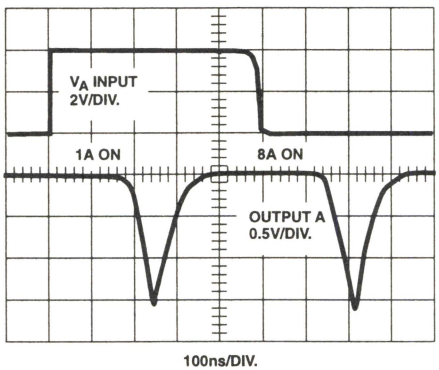


FIGURE 8C. BREAK-BEFORE-MAKE DELAY WAVEFORMS

FIGURE 8. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

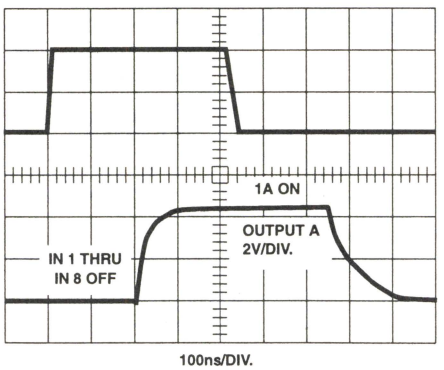


FIGURE 9C. ENABLE DELAY WAVEFORMS

FIGURE 9. ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

Truth Tables

HI-546

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-547

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-548

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-549

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Die Characteristics

DIE DIMENSIONS:

83.9 mils x 159 mils x 19 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

HI-546: 485
HI-547: 485

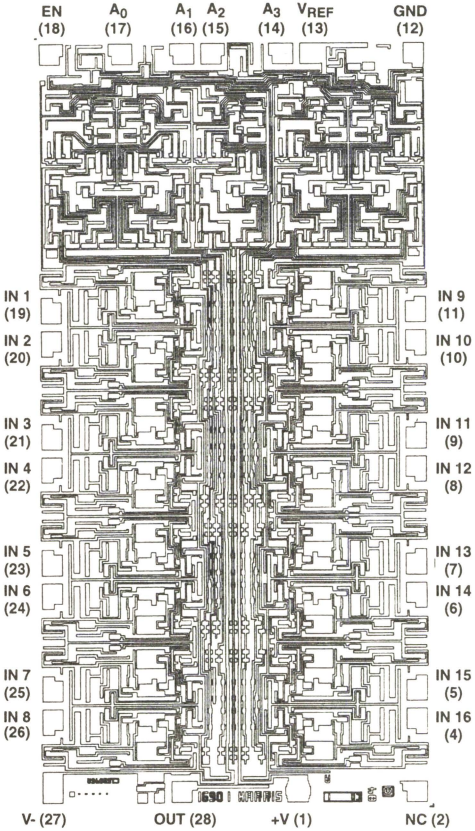
PROCESS:

CMOS-DI

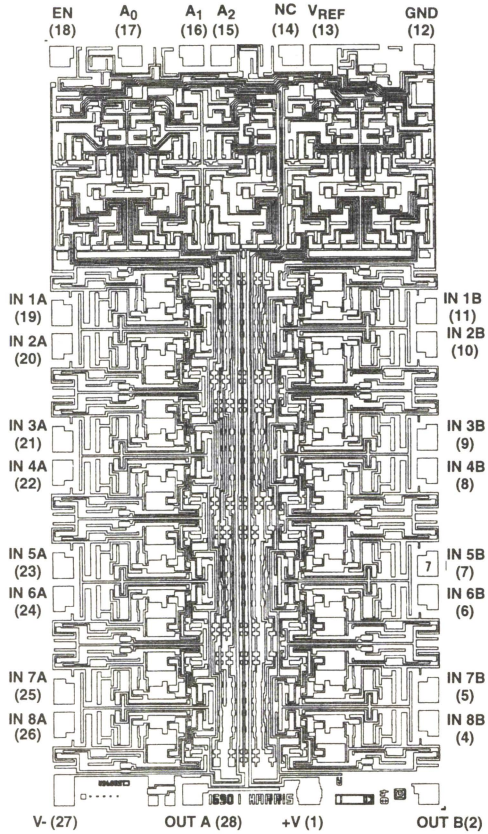
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layouts

HI-546



HI-547



Die Characteristics

DIE DIMENSIONS:

83 mils x 108 mils x 19 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm

TRANSISTOR COUNT:

HI-548: 253
HI-549: 253

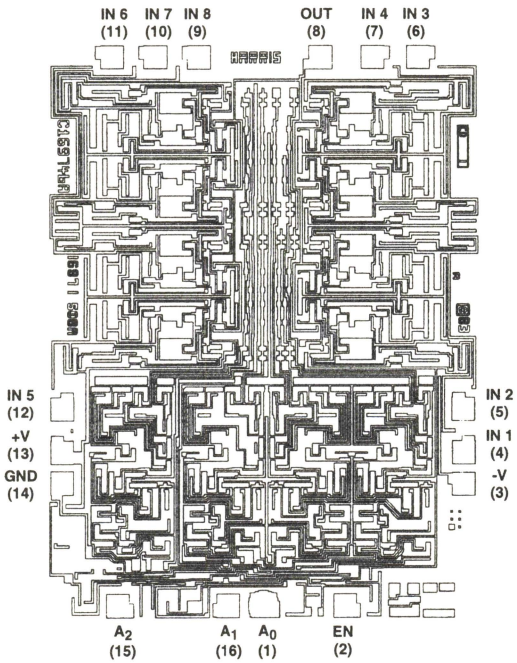
PROCESS:

CMOS-DI

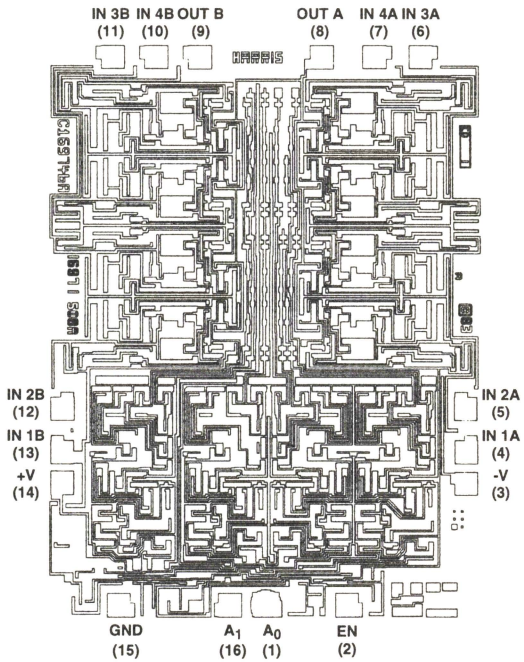
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layouts

HI-548



HI-549



DATA ACQUISITION 12

SPECIAL PURPOSE

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Special Purpose Data Sheets

AD590 2-Wire, Current Output Temperature Transducer 12-3

ICL8069 Low Voltage Reference 12-4

ICM7170 Microprocessor-Compatible, Real-Time Clock 12-5

Selection Guide

REAL-TIME CLOCKS

TYPE	COMMENTS AND APPLICATIONS	NUMBER OF PINS	µP INTERFACE					OSCILLATOR				TIME KEEPING FUNCTIONS							ALARM FUNCTIONS			POWER DOWN MODES			
			STANDARD µP INTERFACE	MUX BUS OPTION	PROGRAMMABLE SQUARE WAVE OUTPUT SIGNAL	INTERRUPTS	BYTES OF GENERAL PURPOSE RAM	ON BOARD OSCILLATOR	60Hz LINE	4.197MHz, 1.049MHz, 32.768kHz XTAL	2.097MHz XTAL	READS SEC., MIN., HR., DAY, MONTH	READS YEAR, DATE	DAYLIGHT SAVINGS TIME	AUTOMATIC END OF MONTH RECOGNITION	AUTOMATIC LEAP YEAR COMPENSATION	12 OR 24 HOUR CLOCK WITH AM/PM	BCD FORMAT AVAILABLE	1/10s, 1/100s ALARM	SEC., MIN., HR. ALARM	DAY, MONTH, YEAR, DATE ALARM	POWER SENSE INPUT/DETECTION	BATTERY INPUT PIN	STANDBY TIME KEEPING	POWER DOWN MODE (µA)
GENERAL																									
ICM7170	Real-Time Clock-Time Keeping and Date Stamping for Personal Computers, Communica-tions, Robotics, Auto, etc.	24	•	•		•		•		•	•	•	•		•	•	•		•	•	•	•	•	•	5

AD590

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

2-Wire, Current Output Temperature Transducer

Features

- Linear Current Output . . . . . 1μA/°K
- Wide Temperature Range . . . . . -55°C to 150°C
- Two-Terminal Device Voltage In/Current Out
- Wide Power Supply Range . . . . . +4V to +30V
- Sensor Isolation From Case
- Low Cost

Ordering Information

PART NUMBER	NON-LINEARITY (°C)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
AD590IH	±3.0	-55 to 150	3 Ld Metal Can (TO-52)	T3.A
AD590JH	±1.5	-55 to 150	3 Ld Metal Can (TO-52)	T3.A

Description

The AD590 is an integrated-circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance constant current regulator, passing 1μA/°K for supply voltages between +4V and +30V. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2°K (25°C).

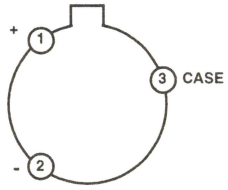
The AD590 should be used in any temperature-sensing application between -55°C to 150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590. In the simplest application, a resistor, a power source and any voltmeter can be used to measure temperature.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, and biasing proportional to absolute temperature.

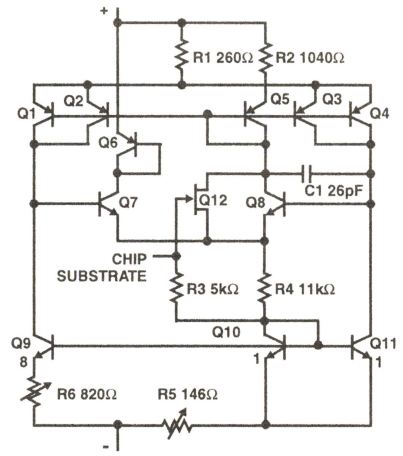
The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high-impedance current output. Any well insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

Pinout

AD590
(METAL CAN)



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **3171.1**

HARRIS SEMICONDUCTOR

ICL8069

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

Low Voltage Reference

Features

- Low Bias Current (Min) 50µA
- Low Dynamic Impedance
- Low Reverse Voltage
- Low Cost

Description

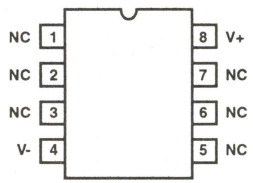
The ICL8069 is a 1.2V temperature-compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50µA. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

Ordering Information

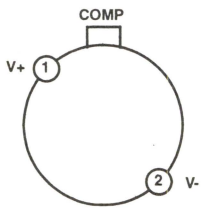
PART NUMBER	MAXIMUM TEMPCO	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICL8069CCZR	0.005%/^{o}C	0 to 70	SIP Package (TO-92)	Z3.05
ICL8069CCSQ	0.005%/^{o}C	0 to 70	Metal Can Package (TO-52)	T2.A
ICL8069DCZR	0.01%/^{o}C	0 to 70	SIP Package (TO-92)	Z3.05
ICL8069DCSQ	0.01%/^{o}C	0 to 70	Metal Can Package (TO-52)	T2.A
ICL8069CCBA	0.005%/^{o}C	0 to 70	8 Ld SOIC	M8.15
ICL8069DCBA	0.01%/^{o}C	0 to 70	8 Ld SOIC	M8.15
ICL8069CMSQ	0.005%/^{o}C	-55 to 125	Metal Can Package (TO-52)	T2.A
ICL8069DMSQ	0.01%/^{o}C	-55 to 125	Metal Can Package (TO-52)	T2.A

Pinouts

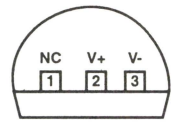
ICL8069 (SOIC) TOP VIEW



ICL8069 (METAL CAN TO-52) TOP VIEW



ICL8069 (SIP TO-92) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3172.1**

ICM7170

August 1997

Microprocessor-Compatible, Real-Time Clock

Features

- 8-Bit, µP Bus Compatible
  - Multiplexed or Direct Addressing
- Regulated Oscillator Supply Ensures Frequency Stability and Low Power
- Time From 1/100 Seconds to 99 Years
- Software Selectable 12/24 Hour Format
- Latched Time Data Ensures No Roll Over During Read
- Full Calendar with Automatic Leap Year Correction
- On-Chip Battery Backup Switchover Circuit
- Access Time Less than 300ns
- 4 Programmable Crystal Oscillator Frequencies Over Industrial Temperature Range
- 3 Programmable Crystal Oscillator Frequencies Over Military Temperature Range
- On-Chip Alarm Comparator and RAM
- Interrupts from Alarm and 6 Selectable Periodic Intervals
- Standby Micro-Power Operation: 1.2µA Typical at 3.0V and 32kHz Crystal

Applications

- Portable and Personal Computers
- Data Logging
- Industrial Control Systems
- Point Of Sale

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICM7170IPG	-40 to 85	24 Ld PDIP	E24.6
ICM7170IDG	-40 to 85	24 Ld SBDIP	D24.6
ICM7170IBG	-40 to 85	24 Ld SOIC	M24.3
ICM7170MDG	-55 to 125	24 Ld SBDIP	D24.6
ICM7170AIPG	-40 to 85	24 Ld PDIP	E24.6
ICM7170AIDG	-40 to 85	24 Ld SBDIP	D24.6
ICM7170AIBG	-40 to 85	24 Ld SOIC	M24.3
ICM7170AMDG	-55 to 125	24 Ld SBDIP	D24.6

NOTE: "A" Parts Screened to <5µA I_{STBY} at 32kHz.

Description

The ICM7170 real time clock is a microprocessor bus compatible peripheral, fabricated using Harris' silicon gate CMOS LSI process. An 8-bit bidirectional bus is used for the data I/O circuitry. The clock is set or read by accessing the 8 internal separately addressable and programmable counters from $^1/_{100}$ seconds to years. The counters are controlled by a pulse train divided down from a crystal oscillator circuit, and the frequency of the crystal is selectable with the on-chip command register. An extremely stable oscillator frequency is achieved through the use of an on-chip regulated power supply.

The device access time (t_{ACC}) of 300ns eliminates the need for wait states or software overhead with most microprocessors. Furthermore, an ALE (Address Latch Enable) input is provided for interfacing to microprocessors with a multiplexed address/data bus. With these two special features, the ICM7170 can be easily interfaced to any available microprocessor.

The ICM7170 generates two types of interrupts, periodic and alarm. The periodic interrupt (100Hz, 10Hz, etc.) can be programmed by the internal interrupt control register to provide 6 different output signals. The alarm interrupt is set by loading an on-chip 51-bit RAM that activates an interrupt output through a comparator. The alarm interrupt occurs when the real time counter and alarm RAM time are equal. A status register is available to indicate the interrupt source.

An on-chip Power Down Detector eliminates the need for external components to support the battery back-up function. When a power down or power failure occurs, internal logic switches the on-chip counters to battery back-up operation. Read/write functions become disabled and operation is limited to time-keeping and interrupt generation, resulting in low power consumption.

Internal latches prevent clock roll-over during a read cycle. Counter data is latched on the chip by reading the 100th-seconds counter and is held indefinitely until the counter is read again, assuring a stable and reliable time value.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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DATA ACQUISITION 13

SWITCHES

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SINGLE POLE SINGLE THROW SWITCH (SPST, FIGURE 1)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
HI1-5040	-2, -5, -7	Y	75	2.4	0.8	36V CMOS-DI	0.8	370	280	

DUAL SINGLE POLE SINGLE THROW SWITCH (2 x SPST, FIGURE 2)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
DG200	AA, AK BA, BK CJ	Y	100	2.4	0.8	36V CMOS-JI	2.0	1000	500	TTL Inputs
DG300A	CA, AA, AK BA, BK CK, CJ	Y	50	4.0	0.8	44V CMOS-JI	0.1	150	130	TTL/CMOS Inputs
DG401	DJ, DY, EJ, EY	Y	45	2.4	0.8	44V CMOS-JI	-0.01	100	60	Very Low $r_{DS(ON)}$
HI1-0200	-2, -4, -5, -7	Y	80	0.8	2.4	44V CMOS-DI	1.0	240	500 (-5) 330 (-2)	
HI2-0200	-2, -4, -5, -7	Y								
HI3-0200	-5									
HI9P0200	-5, -9									
HI-0222	-5, -9	Y	35	2.0	0.8	36V CMOS-DI	0.1	100	70	Video Switch
HI1-0222	-5, -9									
HI3-0222	-5									
HI4-0222		Y								
HI4P0222	-5									
HI1-0300	-2, -5	Y	50	4.0	0.8	44V CMOS-DI	0.04	210	160	TTL/5V CMOS Logic Very Low Leakage
HI2-0300	-2, -5	Y								
HI3-0300	-5									
HI9P0300	-5, -9									
HI1-0304	-2, -5	Y	50	11.0	3.5	44V CMOS-DI	0.04	160	100	15V CMOS Logic Very Low Leakage
HI2-0304	-2, -5	Y								
HI3-0304	-5									
HI9P0304	-5, -9									
HI1-0381	-2, -5	Y	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Very Low Leakage
HI2-0381	-2, -5	Y								
HI3-0381	-5									
HI9P0381	-5, -9									

DUAL SINGLE POLE SINGLE THROW SWITCH (2 x SPST, FIGURE 2) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
HI1-5041	-2, -5, -7, -8	Y	75	2.4	0.8	36V CMOS-DI	0.8	370	280	10Ω $r_{DS(ON)}$ Matching
HI3-5041	-5									
HI1-5048	-2, -5, -7	Y	45	2.4	0.8	36V CMOS-DI	0.8	370	280	5Ω $r_{DS(ON)}$ Matching
HI3-5048	-5									
IH5341	CPD, ITW, MTW	Y	75	2.4	0.8	36V CMOS-JI	1.0	150	80	RF Video T-Switch

QUAD SINGLE POLE SINGLE THROW SWITCH (4 x SPST, FIGURE 3)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
DG201	AK, BK, CJ	Y	125	2.4	0.8	36V CMOS-JI	±5.0	1000	500	
DG201A	AK, BK, CJ, CK, BY, CY	Y	175	0.8	2.4	44V CMOS-JI	0.01	480	370	Very Low Leakage
DG202	AK, BK, CJ, CK	Y	175	2.4	0.8	44V CMOS-JI	0.01	480	370	Very Low Leakage
DG211	CJ, CY		175	0.8	2.4	44V CMOS-JI	0.01	460	360	Low Cost
DG212	CJ, CY		175	2.4	0.8	44V CMOS-JI	0.01	460	360	Low Cost
DG308A	AK, BK CJ, CK, CY	Y	60 Typ	11.0	3.5	44V CMOS-JI	0.1	130	90	CMOS Logic, Single or Dual Supply Operation
DG309	AK, BK, CJ, CK, CY	Y	60 Typ	3.5	11.0	44V CMOS-JI	0.1	130	90	CMOS Logic, Single or Dual Supply Operation
DG411	DJ, DY, EJ, EY	Y	35	0.8	2.4	44V CMOS-JI	-0.1	110	100	Very Low $r_{DS(ON)}$
DG412	DJ, DY EJ, EY	Y	35	2.4	0.8	44V CMOS-JI	-0.1	110	100	Very Low $r_{DS(ON)}$
DG413	DJ, DY EJ, EY	Y	35	2.4	0.8	44V CMOS-JI	-0.1	110	100	Very Low $r_{DS(ON)}$ Channel 1, 4 "ON" Channel 2, 3 "OFF"
DG441	DJ, DY EJ, EY	Y	85	0.8	2.4	44V CMOS-JI	0.01	150	90	Low $r_{DS(ON)}$, Low Leakage
DG442	DJ, DY EJ, EY	Y	85	2.4	0.8	44V CMOS-JI	0.01	150	110	Low $r_{DS(ON)}$, Low Leakage
DG444	DJ, DY		85	0.8	2.4	44V CMOS-JI	0.01	150	90	Low $r_{DS(ON)}$, Low Leakage
DG445	DJ, DY		85	2.4	0.8	44V CMOS-JI	0.01	150	110	Low $r_{DS(ON)}$, Low Leakage

QUAD SINGLE POLE SINGLE THROW SWITCH (4 x SPST, FIGURE 3) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
HI1-0201	-2, -4, -5, -7, -8	Y	80	2.4	0.8	44V CMOS-DI	2.0	185	220	
HI3-0201	-5									
HI4P0201	-5									
HI9P0201	-5, -9									
HI4-0201/883		Y								
HI1-0201HS	-2, -4, -5, -7, -8	Y	50	2.4	0.8	36V CMOS-DI	0.3	30	40	High Speed, Low $r_{DS(ON)}$
HI3-0201HS	-4, -5									
HI4P0201HS	-5									
HI9P0201HS	-5, -9									
HI4-0201HS/883		Y								
IH5052	CDE, MDE		100	2.4	0.8	36V CMOS-JI	5.0	1000	500	Low Power
IH5053	CDE, MDE		100	2.4	0.8	36V CMOS-JI	5.0	1000	500	Low Power
IH5352	CPE, IJE, MJE, CBP, IBP	Y	75	2.4	0.8	36V CMOS-JI	2.0	150	80	RF Video T-Switch

FOUR POLE SINGLE THROW SWITCH (4PST, FIGURE 4)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
HI1-5047	-2, -5, -7	Y	75	2.4	0.8	36V CMOS-JI	0.8	370	280	10Ω Max $r_{DS(ON)}$ Matching
HI3-5047	-5									
HI1-5047A	-2, -5, -7, -8	Y	45	2.4	0.8	36V CMOS-JI	0.8	370	280	5Ω Max $r_{DS(ON)}$ Matching
HI3-5047A	-5									
HI4P5047A	-5									

SINGLE POLE DOUBLE THROW SWITCH (SPDT, FIGURE 5)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
DG301A	AA, AK BA, BK CA, CJ, CK	Y	50	4.0	0.8	44V CMOS-JI	0.1	150	130	Channel 1 "ON", Channel 2 "OFF", TTL Inputs

SINGLE POLE DOUBLE THROW SWITCH (SPDT, FIGURE 5) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
HI1-0301	-2, -5, -7	Y	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Very Low Leakage, TTL Inputs Channel 1 "ON" Channel 2 "OFF"
HI2-0301	-2, -5	Y								
HI3-0301	-5									
HI9P0301	-5, -9									
HI1-0305	-2, -5	Y	50	11.0	3.5	44V CMOS-DI	0.04	160	100	15V CMOS Logic Very Low Leakage Channel 1 "ON" Channel 2 "OFF"
HI2-0305	-2, -5	Y								
HI3-0305	-5									
HI9P0305	-5, -9									
HI1-0387	-2, -5	Y	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Channel 1 "ON", Channel 2 "OFF", Very Low Leakage
HI2-0387	-2, -5	Y								
HI3-0387	-5									
HI9P0387	-5, -9									
HI1-5042	-2, -5, -7	Y	75	2.4	0.8	36V CMOS-DI	0.8	370	280	Channel 1 "ON", Channel 2 "OFF", 10Ω Max $r_{DS(ON)}$ Matching
HI3-5042	-5									
HI1-5050	-2, -5, -7	Y	45	2.4	0.8	36V CMOS-DI	0.8	370	280	Channel 1 "ON", Channel 2 "OFF", 5Ω Max $r_{DS(ON)}$ Matching
HI3-5050	-5									

DUAL SINGLE POLE DOUBLE THROW SWITCH (2 x SPDT, FIGURE 6)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
DG303A	CY, AK, BK, CK, CJ, BY	Y	50	4.0	0.8	44VCMOS-JI	0.1	150	130	TTL and CMOS Compatible
DG403	DJ, DY, EJ, EY	Y	45	2.4	0.8	44V CMOS-JI	-0.01	100	60	
HI1-0303	-2, -5	Y	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Switch 1, 2 "ON", Switch 3, 4 "OFF", Very Low Leakage, TTL Inputs
HI3-0303	-5									
HI9P0303	-5, -9									
HI1-0307	-2, -5, -7	Y	50	11.0	3.5	44V CMOS-DI	0.04	160	100	Switch 1, 2 "ON", Switch 3, 4 "OFF", Very Low Leakage
HI3-0307	-5									
HI9P0307	-5, -9									

DUAL SINGLE POLE DOUBLE THROW SWITCH (2 x SPDT, FIGURE 6) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
HI1-0390	-2, -5	Y	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Switch 1, 2 "ON", Switch 3, 4 "OFF", Very Low Leakage
HI3-0390	-5									
HI9P0390	-5, -9									
HI1-5043	-2, -5 -8	Y	75	2.4	0.8	36V CMOS-DI	0.8	370	280	Switch 1, 2 "ON", Switch 3, 4 "OFF", 10Ω Max $r_{DS(ON)}$ Matching
HI3-5043	-5									
HI9P5043	-5, -9									
HI1-5051	-2, -5, -7, -8	Y	45	2.4	0.8	36V CMOS-DI	0.8	370	280	Switch 1, 2 "ON", Switch 3, 4 "OFF", 5Ω Max $r_{DS(ON)}$ Matching
HI3-5051	-5									
HI4P5051	-5									
HI9P5051	-5, -9									
IH5043	CJE, CPE, CY, MJE	Y	130	2.4	0.8	36V CMOS-JI	5.0	1000	500	Switch 1 "ON" Switch 2 "OFF", Low Power
IH5151	CJE, CPE, MJE	Y	50	2.4	0.8	36V CMOS-JI	1.0	250	200	

DOUBLE POLE SINGLE THROW SWITCH (DPST, FIGURE 7)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
HI1-5044	-2, -5, -7	Y	75	2.4	0.8	36V CMOS-DI	0.8	370	280	10Ω Max $r_{DS(ON)}$ Matching
HI3-5044	-5									

DUAL DOUBLE POLE SINGLE THROW SWITCH (2 x DPST, FIGURE 8)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
DG302A	AK, BK, CK, CJ	Y	50	4.0	0.8	44V CMOS-JI	0.1	150	130	TTL/CMOS Inputs
DG405	DJ, DY, EJ, EY	Y	45	2.4	0.8	44V CMOS-JI	-0.01	100	60	Very Low $r_{DS(ON)}$
HI1-0302	-2, -5	Y	50	4.0	0.8	44V CMOS-DI	0.1	210	160	TTL/5V CMOS Inputs
HI3-0302	-5									
HI9P0302	-5, -9									

DUAL DOUBLE POLE SINGLE THROW SWITCH (2 x DPST, FIGURE 8) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
HI1-0306	-2, -5	Y	50	11.0	3.5	44V CMOS-DI	0.1	160	100	15V CMOS Logic
HI3-0306	-5									
HI9P0306	-5, -9									
HI1-0384	-2, -5	Y	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Very Low Leakage
HI3-0384	-5									
HI9P0384	-5, -9									
HI1-5045	-2, -5, -7	Y	75	2.4	0.8	36V CMOS-DI	0.8	370	280	10Ω Max $r_{DS(ON)}$ Matching
HI3-5045	-5									
HI4-5045/883		Y								
HI9P5045	-5, -9									
HI1-5049	-2, -5, -7	Y	45	2.4	0.8	36V CMOS-DI	0.8	370	280	5Ω $r_{DS(ON)}$ Matching
HI3-5049	-5									
HI9P5049	-5, -9									

DUAL DOUBLE POLE DOUBLE THROW SWITCH (2 x DPDT, FIGURE 9)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
HI1-5046	-2, -5, -7	Y	75	0.8	2.4	36V CMOS-DI	0.8	370	280	Switch 1 and 4 "ON" Switch 2 and 3 "OFF" 10Ω Max $r_{DS(ON)}$ Matching
HI3-5046	-5									
HI9P5046	-5, -9									
HI1-5046A	-2, -5, -7	Y	45	0.8	2.4	36V CMOS-DI	0.8	370	280	Switch 1 and 4 "ON" Switch 2 and 3 "OFF" 5Ω Max $r_{DS(ON)}$ Matching
HI3-5046A	-5									

RF/VIDEO "T" SWITCHES ("T" SWITCH, FIGURE 10 and 11)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $r_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	t_{ON} (ns) TYP	t_{OFF} (ns) TYP	FEATURES
IH5341	ITW, MTW, CPD	Y	75	2.4	0.8	36V CMOS-JI	1.0	150	80	Dual SPST
IH5352	MJE	Y	75	2.4	0.8	36V CMOS-JI	1.0	150	80	Quad SPST
IH5352	IJE, CPE, CBP, IBP		75	2.4	0.8	36V CMOS-JI	2.0	150	80	Quad SPST

NOTES:

1. The $r_{DS(ON)}$ of a CMOS switch varies as a function of supply voltage, analog signal voltage, and temperature. Values shown are maximum (unless noted "Typ" = typical) at 25°C.
   SWITCH "ON" V: Digital Threshold to "CLOSE" a particular switch. (Minimum if greater than "OFF". Maximum if less than "OFF".)
   SWITCH "OFF" V: Digital Threshold to "OPEN" a particular switch. (Minimum if greater than "ON". Maximum if less than "ON".)
   V_{INL}: Digital Threshold to represent a "Low" select signal. (Maximum, voltage levels greater than this value are not guaranteed to produce a "LOW".)
   V_{INH}: Digital Threshold to represent a "HIGH" select signal. (Minimum, voltage levels less than this value are not guaranteed to produce a "HIGH".)
2. Package codes:
   DG Types - SUFFIX:
   - A 10 Lead TO-100
   - J Plastic DIP
   - K CERDIP
   - P SBDIP
   - Y Plastic SOIC

   IH Types - Middle SUFFIX Letter:
   - J CERDIP
   - P Plastic DIP
   - T TO-100 Can
   - B SOIC

   HI Types - PREFIX:
   - HI1 CERDIP
   - HI2 Metal Can
   - HI3 Plastic DIP
   - HI4 Ceramic LCC
   - HI4P PLCC
   - HI9P SOIC
3. Temperature Code Suffix:
   - -1: 0° to 200°C
   - -2, A, or M: -55°C to 125°C
   - -4 or B: -25°C to 85°C
   - -5: 0°C to 75°C
   - C: 0°C to 70°C
   - -7: 0°C to 75°C with Burn-In
   - -8: -55°C to 125°C with Burn-In
   - -9: -40°C to 85°C
   - /883: MIL-STD-883, Class B, -55°C to 125°C with Burn-In
   - D: -40°C to 85°C
   - E: -40°C to 85°C with Extended Processing Flow
   - I: Industrial, -25°C or -40°C to 85°C, see data sheet

Double Throw switches have one switch ON and the other switch OFF for each input state. See data sheet.

SWITCH CONFIGURATIONS

FIGURE 1. FSPST

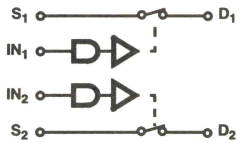


FIGURE 2. DUAL SPST

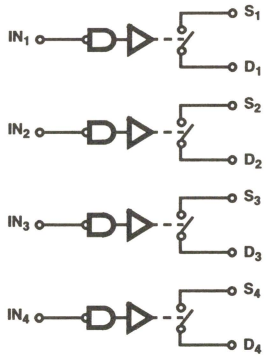


FIGURE 3. QUAD SPST

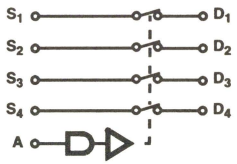


FIGURE 4. 4PST

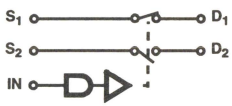


FIGURE 5. SPDT

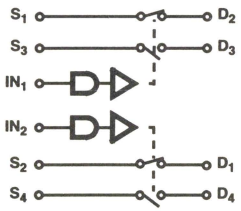


FIGURE 6. DUAL SPDT

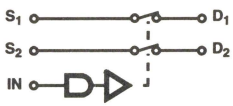


FIGURE 7. DPST

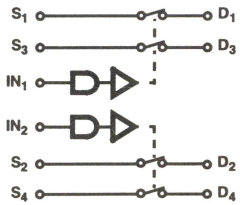


FIGURE 8. DUAL DPST

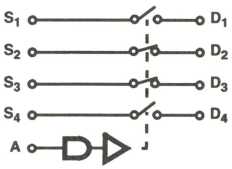


FIGURE 9. DPDT

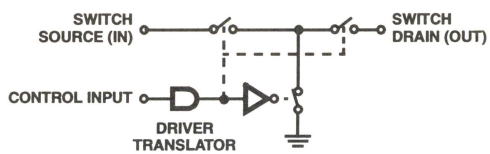


FIGURE 10. "T" SCHEMATIC

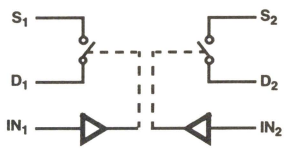


FIGURE 11. "T" SWITCH

HARRIS SEMICONDUCTOR

DG200, DG201

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

CMOS Dual/Quad SPST Analog Switches

Features

- Switches Greater than $28V_{P-P}$ Signals with ±15V Supplies
- Break-Before-Make Switching (Typ)
  - t_{OFF} 250ns
  - t_{ON} 700ns
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching with Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG200, DG201)

Applications

- Data Acquisition
- Sample and Hold Circuits
- Operational Amplifier Gain Switching Networks

Description

The DG200 and DG201 solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates has been eliminated by Harris' CMOS technology.

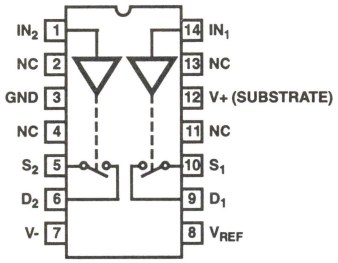
The DG200 and DG201 are completely specification and pinout compatible with the industry standard devices.

Ordering Information

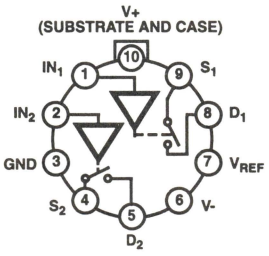
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG200AA	-55 to 125	10 Pin Metal Can	T10.B
DG200AK	-55 to 125	14 Ld CERDIP	F14.3
DG200BA	-25 to 85	10 Pin Metal Can	T10.B
DG200BK	-25 to 85	14 Ld CERDIP	F14.3
DG200CJ	0 to 70	14 Ld PDIP	E14.3
DG200AA/883B	-55 to 125	10 Pin Metal Can	T10.B
DG200AK/883B	-55 to 125	14 Ld CERDIP	F14.3
DG201AK	-55 to 125	16 Ld CERDIP	F16.3
DG201BK	-25 to 85	16 Ld CERDIP	F16.3
DG201CJ	0 to 70	16 Ld PDIP	E16.3
DG201AK/883B	-55 to 125	16 Ld CERDIP	F16.3

Pinouts

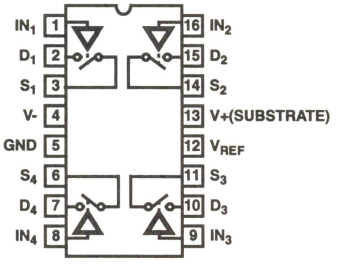
DG200
(CERDIP, PDIP)
TOP VIEW



DG200
(METAL CAN)
TOP VIEW



DG201
(CERDIP, PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **3115.2**

HARRIS SEMICONDUCTOR

DG201A, DG202

August 1997

Quad SPST, CMOS Analog Switches

Features

- Input Signal Range ..... ±15V
- Low $r_{DS(ON)}$ ..... ≤175Ω
- TTL, CMOS Compatible
- Latch Proof
- True Second Source
- Maximum Supply Ratings 44V
- Logic Inputs Accept Negative Voltages

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
DG201AAK	-55 to 125	16 Ld CERDIP	F16.3
DG201ABK	-25 to 85	16 Ld CERDIP	F16.3
DG201AAK/883B	-55 to 125	16 Ld CERDIP	F16.3
DG201ACK	0 to 70	16 Ld CERDIP	F16.3
DG201ACJ	0 to 70	16 Ld PDIP	E16.3
DG201ACY	0 to 70	16 Ld SOIC	M16.3
DG202AK	-55 to 125	16 Ld CERDIP	F16.3
DG202AK/883B	-55 to 125	16 Ld CERDIP	F16.3
DG202BK	-25 to 85	16 Ld CERDIP	F16.3
DG202CJ	0 to 70	16 Ld PDIP	E16.3

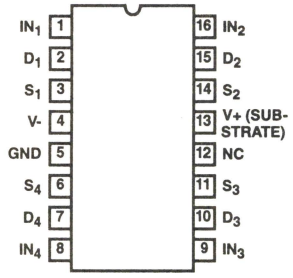
Description

The DG201A (normally open) and DG202 (normally closed) quad SPST analog switches are designed using Harris' 44V CMOS process. These bidirectional switches are latch-proof and feature break-before-make switching. Designed to block signals up to $30V_{P-P}$ in the OFF state, the DG201A and DG202 offer the advantages of low ON resistance (≤175Ω), wide input signal range (±15V) and provide both TTL and CMOS compatibility.

The DG201A and DG202 are specification and pinout compatible with the industry standard devices.

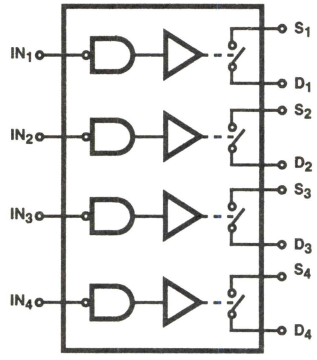
Pinout

DG201A, DG202
(CERDIP, PDIP, SOIC)
TOP VIEW

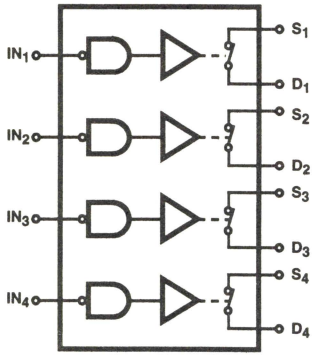


Functional Block Diagrams

DG201A



DG202



NOTES:

1. Four SPST switches per package.
2. Switches shown for logic "1" input.

TRUTH TABLE

LOGIC	DG201A	DG202
0	ON	OFF
1	OFF	ON

Logic "0" ≤0.8V, Logic "1" ≥ 2.4V

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3117.1**

Absolute Maximum Ratings

V+ to V- 44V
V- to Ground . . . . . -25V
V_{IN} to Ground (Note 1) . . . . . (V- -2V), (V+ +2V)
V_S or V_D to V+ (Note 1) . . . . . +2, (V- -2V)
V_S or V_D to V- (Note 1) . . . . . -2, (V+ +2V)
Current, any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max) 70mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	20
PDIP Package	100	N/A
SOIC Package	100	N/A

Maximum Junction Temperature
CERDIP Package . . . . . 175°C
PDIP Package . . . . . 150°C
Maximum Storage Temperature Range
C Suffix . . . . . -65°C to 125°C
A and B Suffix . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on V_S, V_D, or V_{IN} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V+ = 15V, V- = -15V, GND = 0V, T_A = 25°C

PARAMETER	TEST CONDITIONS		DG201AA/DG202A MIN	DG201AA/DG202A (NOTE 3) TYP	DG201AA/DG202A MAX	DG201AB, C/DG202B, C MIN	DG201AB, C/DG202B, C (NOTE 3) TYP	DG201AB, C/DG202B, C MAX	UNITS
DYNAMIC CHARACTERISTICS									
Turn-On Time, t_{ON}	See Figure 1		-	480	600	-	480	-	ns
Turn-Off Time, t_{OFF}	See Figure 1		-	370	450	-	370	-	ns
Charge Injection, Q	C_L = 1000pF, R_S = 0, V_S = 0V		-	20	-	-	20	-	pC
Source OFF Capacitance, $C_{S(OFF)}$	f = 140kHz, V_{IN} = 5V, V_S = 0V		-	5.0	-	-	5.0	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	f = 140kHz, V_{IN} = 5V, V_D = 0V		-	5.0	-	-	5.0	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$	f = 140kHz, V_{IN} = 5V, V_S = V_D = 0V		-	16	-	-	16	-	pF
OFF Isolation, OIRR	V_{IN} = 5V, Z_L = 75Ω, V_S = 2.0V, f = 100kHz		-	70	-	-	70	-	dB
Crosstalk (Channel to Channel), CCRR			-	90	-	-	90	-	dB
INPUT									
Input Current with Voltage High, I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004	-	-1.0	-0.0004	-	µA
	V_{IN} = 15V		-	0.003	1.0	-	0.003	1.0	µA
Input Current with Voltage Low, I_{INL}	V_{IN} = 0V		-1.0	-0.0004	-	-1.0	-0.0004	-	µA
SWITCH									
Analog Signal Range, V_{ANALOG}			-15	-	15	-15	-	15	V
Drain Source On Resistance, $r_{DS(ON)}$	V_D = ±10V, V_{IN} = 0.8V (DG201A) I_S = 1mA, V_{IN} = 2.4V (DG202)		-	115	175	-	115	200	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 2.4V (DG201A) V_{IN} = 0.8V (DG202)	V_S = 14V, V_D = -14V	-	0.01	1.0	-	0.01	5.0	nA
		V_S = -14V, V_D = 14V	-1.0	-0.02	-	-5.0	-0.02	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	0.01	1.0	-	0.01	5.0	nA
		V_S = 14V, V_D = -14V	-1.0	-0.02	-	-5.0	-0.02	-	nA

Electrical Specifications V+ = 15V, V- = -15V, GND = 0V, T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS		DG201AA/DG202A MIN	DG201AA/DG202A (NOTE 3) TYP	DG201AA/DG202A MAX	DG201AB, C/DG202B, C MIN	DG201AB, C/DG202B, C (NOTE 3) TYP	DG201AB, C/DG202B, C MAX	UNITS
Drain ON Leakage Current, $I_{D(ON)}$ (Note 5)	V_{IN} = 0.8V (DG201A) V_{IN} = 2.4V (DG202)	$V_D = V_S$ = 14V	-	0.1	1.0	-	0.1	5.0	µA
		$V_D = V_S$ = -14V	-1.0	-0.15	-	-5.0	-0.15	-	µA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I+	All Channels ON or OFF		-	0.9	2	-	0.9	2	mA
Negative Supply Current, I-			-1	-0.3	-	-1	-0.3	-	mA

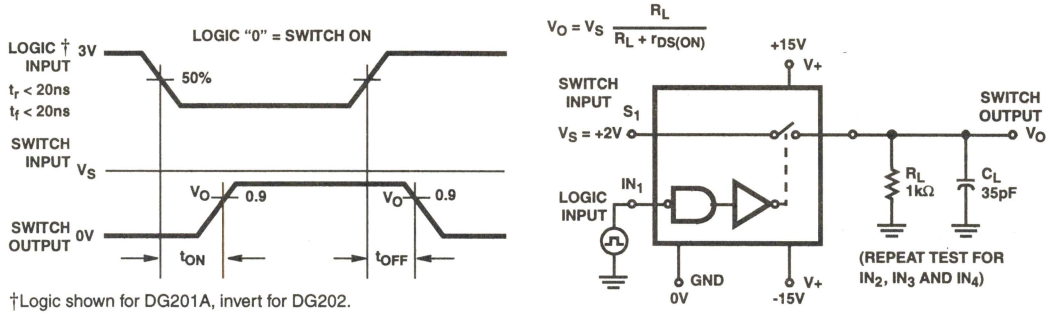
Electrical Specifications V+ = 15V, V- = -15V, GND = 0V, T_A Over Operating Temperature Range

PARAMETER	TEST CONDITIONS		DG201AA/DG202A MIN	DG201AA/DG202A (NOTE 3) TYP	DG201AA/DG202A MAX	DG201AB, C/DG202B, C MIN	DG201AB, C/DG202B, C (NOTE 3) TYP	DG201AB, C/DG202B, C MAX	UNITS
INPUT									
Input Current with Voltage High, I_{INH}	V_{IN} = 2.4V		-10	-	-	-	-	-	µA
	V_{IN} = 15V		-	-	10	-	-	-	µA
Input Current with Voltage Low, I_{INL}	V_{IN} = 0V		-10	-	-	-	-	-	µA
SWITCH									
Analog Signal Range, V_{ANALOG}			-15	-	15	-	-	-	V
Drain Source On Resistance, $r_{DS(ON)}$	V_D = ±10V, V_{IN} = 0.8V (DG201A) I_S = 1mA, V_{IN} = 2.4V (DG202)		-	-	250	-	-	-	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 2.4V (DG201A) V_{IN} = 0.8V (DG202)	V_S = 14V, V_D = -14V	-	-	100	-	-	-	nA
		V_S = -14V, V_D = 14V	-100	-	-	-	-	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	-	100	-	-	-	nA
		V_S = 14V, V_D = -14V	-100	-	-	-	-	-	nA
Drain ON Leakage Current, $I_{D(ON)}$ (Note 5)	V_{IN} = 0.8V (DG201A) V_{IN} = 2.4V (DG202)	$V_D = V_S$ = 14V	-	-	200	-	-	-	µA
		$V_D = V_S$ = -14V	-200	-	-	-	-	-	µA

NOTES:

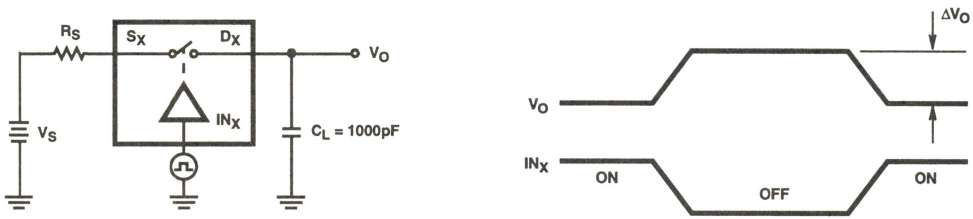
3. Typical values are for design aid only, not guaranteed and not subject to production testing.
4. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
5. $I_{D(ON)}$ is leakage from driver into ON switch.

Test Circuits and Waveforms



†Logic shown for DG201A, invert for DG202.

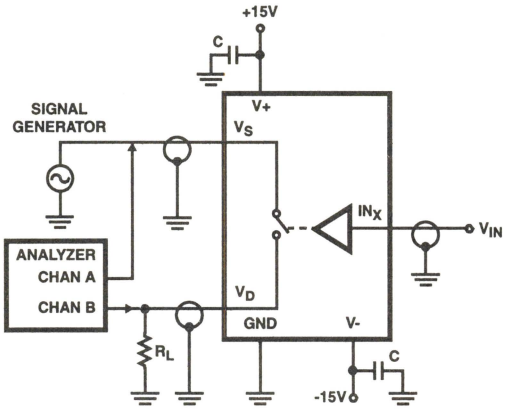
FIGURE 1. t_{ON} AND t_{OFF} SWITCHING TEST CIRCUIT AND WAVEFORM



NOTES:

6. ΔV_O = Measured voltage error due to charge injection.
7. The error voltage in coulombs is $\Delta Q = C_L \times \Delta V_O$.

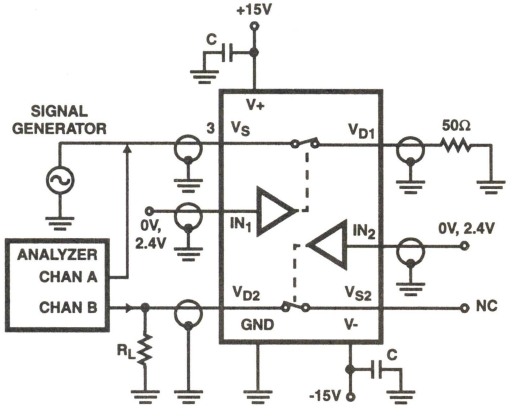
FIGURE 2. CHARGE INJECTION TEST CIRCUIT AND WAVEFORM



C = 0.001µF / / 0.1µF
Chip Capacitors

$$OIRR = 20 \text{ Log} \left| \frac{V_S}{V_D} \right|$$

FIGURE 3. OFF ISOLATION TEST CIRCUIT



C = 0.001µF / / 0.1µF
Chip Capacitors

$$CCRR = 20 \text{ Log} \left| \frac{V_{S1}}{V_{D2}} \right|$$

FIGURE 4. CHANNEL TO CHANNEL CROSSTALK TEST CIRCUIT

HARRIS SEMICONDUCTOR

DG211, DG212

August 1997

SPST 4-Channel Analog Switches

Features

- Switches ±15V Analog Signals
- TTL Compatibility
- Logic Inputs Accept Negative Voltages
- r_{ON} ..... ≤175Ω

Ordering Information

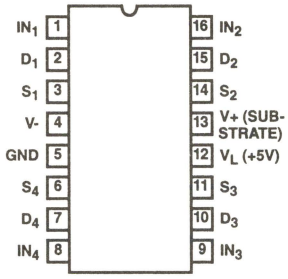
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG211CJ	0 to 70	16 Ld PDIP	E16.3
DG212CJ	0 to 70	16 Ld PDIP	E16.3
DG211CY	0 to 70	16 Ld SOIC	M16.15
DG212CY	0 to 70	16 Ld SOIC	M16.15

Description

The DG211 and DG212 are low cost, CMOS monolithic, Quad SPST analog switches. These can be used in general purpose switching applications for communications, instrumentation, process control and computer peripheral equipment. Both devices provide true bidirectional performance in the ON condition and will block signals to $30V_{P-P}$ in the OFF condition. The DG211 and DG212 differ only in that the digital control logic is inverted, as shown in the truth table.

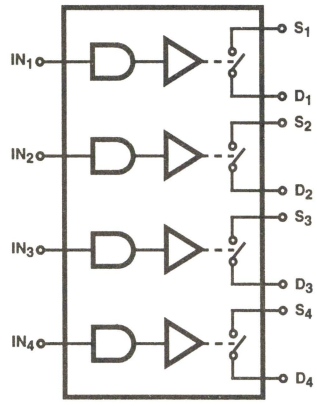
Pinout

DG211, DG212
(PDIP, SOIC)
TOP VIEW

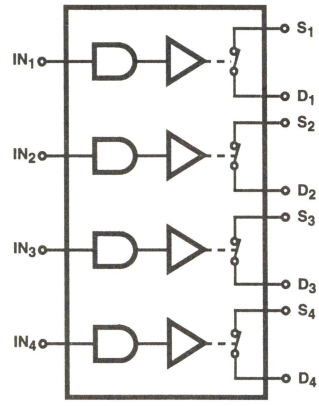


Functional Block Diagrams

DG211



DG212



NOTES:
1. Four SPST switches per package.
2. Switches shown for logic "1" input.

TRUTH TABLE

LOGIC	DG211	DG212
0	ON	OFF
1	OFF	ON

Logic "0" ≤0.8V, Logic "1" ≥ 2.4V

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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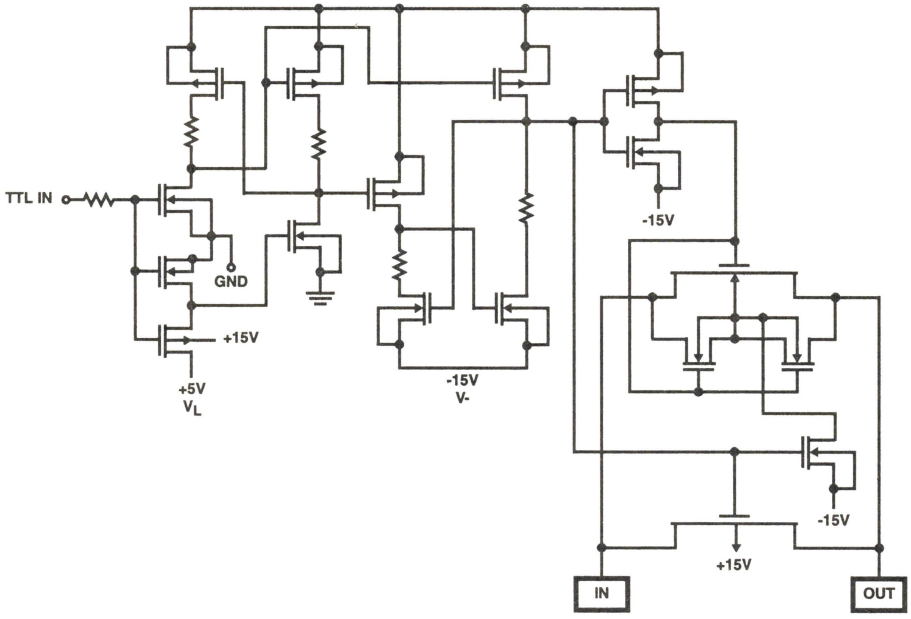
File Number **3118.1**

Schematic Diagram

DG211 ($^1/_4$ AS SHOWN)



Absolute Maximum Ratings

V+ to V- 44V
V_{IN} to Ground . . . . . .V-, V+
V_L to Ground . . . . . -0.3V, 25V
V_S or V_D to V+ . . . . . .0, -36V
V_S or V_D to V- 0, 36V
V+ to Ground 25V
V- to Ground . . . . . .-25V
Current, any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max). . . . 70mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	100
SOIC Package	120

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . .-65°C to 125°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . .0°C to 70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V+ = +15V$, $V- = -15V$, $V_L = +5V$, GND, $T_A = 25°C$

PARAMETER	TEST CONDITIONS		(NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-On Time, t_{ON}	See Figure 1 $V_S = 10V$, $R_L = 1k\Omega$, $C_L = 35pF$		-	460	-	ns
Turn-Off Time, t_{OFF1}			-	360	-	ns
t_{OFF2}			-	450	-	ns
Source OFF Capacitance, $C_{S(OFF)}$	$V_S = 0V$, $V_{IN} = 5V$, f = 1MHz (Note 2)		-	5	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	$V_D = 0V$, $V_{IN} = 5V$, f = 1MHz (Note 2)		-	5	-	pF
Channel ON Capacitance, $C_{D + S(ON)}$	$V_D = V_S = 0V$, $V_{IN} = 0V$, f = 1MHz (Note 2)		-	16	-	pF
OFF Isolation, OIRR (Note 4)	$V_{IN} = 5V$, $R_L = 1k\Omega$, $C_L = 15pF$, $V_S = 1V_{RMS}$, f = 100kHz (Note 2)		-	70	-	dB
Crosstalk (Channel to Channel), CCRR			-	90	-	dB
INPUT						
Input Current with Voltage High, I_{INH}	$V_{IN} = 2.4V$		-1.0	-0.0004	-	µA
	$V_{IN} = 15V$		-	0.003	1.0	µA
Input Current with Voltage Low, I_{INL}	$V_{IN} = 0V$		-1.0	-0.0004	-	µA
SWITCH						
Analog Signal Range, V_{ANALOG}	V- = -15V, $V_L = +5V$		-15	-	15	V
Drain Source On Resistance, $r_{DS(ON)}$	$V_D = \pm10V$, $V_{IN} = 2.4V$ (DG212) $I_S = 1mA$, $V_{IN} = 0.8V$ (DG211)		-	150	175	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	$V_{IN} = 2.4V$ (DG211) $V_{IN} = 0.8V$ (DG212)	$V_S = 14V$, $V_D = -14V$	-	0.01	5.0	nA
		$V_S = -14V$, $V_D = 14V$	-5.0	-0.02	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		$V_S = -14V$, $V_D = 14V$	-	0.01	5.0	nA
		$V_S = 14V$, $V_D = -14V$	-5.0	-0.02	-	nA

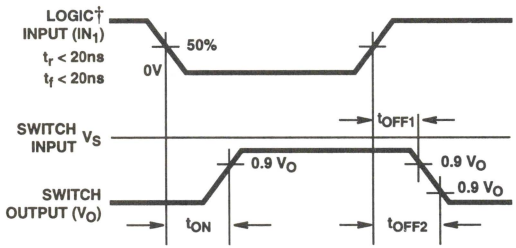
Electrical Specifications V+ = +15V, V- = -15V, V_L = +5V, GND, T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
Drain ON Leakage Current, $I_{D(ON)}$ (Note 3)	$V_S = V_D$ = -14V, V_{IN} = 0.8V (DG211) V_{IN} = 2.4V (DG212)	-	0.1	5.0	nA
		-5.0	-0.15	-	nA
POWER SUPPLY CHARACTERISTICS					
Positive Supply Current, I+	V_{IN} = 0V and 2.4V	-	0.1	10	µA
Negative Supply Current, I-		-	0.1	10	µA
Logic Supply Current, I_L		-	0.1	10	µA

NOTES:
1. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
2. For design reference only, not 100% tested.
3. $I_{D(ON)}$ is leakage from driver into ON switch.
4. OFF Isolation = $20\log\frac{V_S}{V_D}$, V_S = Input to OFF switch, V_D = output.
5. Switching times only sampled.

Test Circuits and Waveforms

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note the V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



† Logic shown for DG211. Invert for DG212.

FIGURE 1. SWITCHING TIME TEST WAVEFORMS

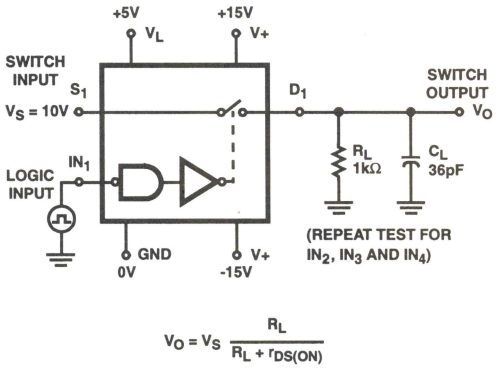


FIGURE 2. SWITCHING TIME TEST CIRCUIT

Die Characteristics

DIE DIMENSIONS:

2159µm x 2235µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

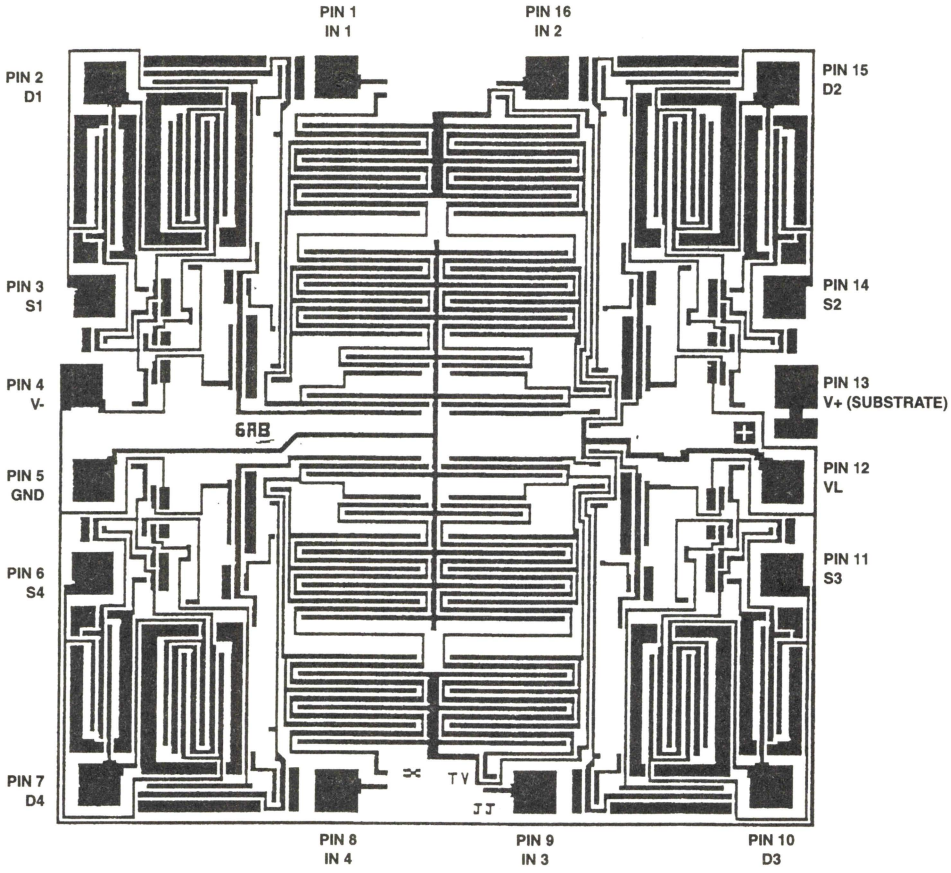
Type: PSG/Nitride
PSG Thickness: 7kÅ ±1.4kÅ
Nitride Thickness: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG211, DG212



HARRIS SEMICONDUCTOR

DG300A, DG301A, DG302A, DG303A

TTL-Compatible, CMOS Analog Switches

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

Features

- Low Power Consumption
- Break-Before-Make Switching (Typ)
  - t_{OFF} 130ns
  - t_{ON} 150ns
- TTL, CMOS Compatible
- Low $r_{DS(ON)}$ . . . . . ≤ 50Ω
- Single Supply Operation
- True Second Source

Description

The DG300A through DG303A family of monolithic CMOS switches are truly compatible second source of the original manufacturer. The switches are latch-proof and are designed to block signals up to $30V_{P-P}$ when OFF. Featuring low leakage and low power consumption, these switches are ideally suited for precision application in instrumentation, communication, data acquisition and battery powered applications. Other key features include Break-Before-Make switching, TTL and CMOS compatibility, and low ON resistance. Single supply operation (for positive switch voltages) is possible by connecting V- to 0V.

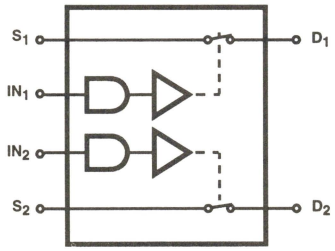
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG300AAK	-55 to 125	14 Ld CERDIP	F14.3
DG301AAK	-55 to 125	14 Ld CERDIP	F14.3
DG302AAK	-55 to 125	14 Ld CERDIP	F14.3
DG303AAK	-55 to 125	14 Ld CERDIP	F14.3
DG300ABK	-25 to 85	14 Ld CERDIP	F14.3
DG301ABK	-25 to 85	14 Ld CERDIP	F14.3
DG302ABK	-25 to 85	14 Ld CERDIP	F14.3
DG303ABK	-25 to 85	14 Ld CERDIP	F14.3
DG300ACK	0 to 70	14 Ld CERDIP	F14.3
DG301ACK	0 to 70	14 Ld CERDIP	F14.3
DG303ACK	0 to 70	14 Ld CERDIP	F14.3
DG300ACJ	0 to 70	14 Ld PDIP	E14.3

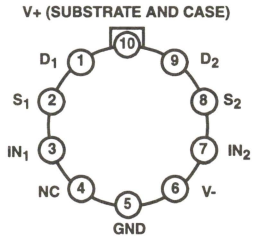
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG301ACJ	0 to 70	14 Ld PDIP	E14.3
DG302ACJ	0 to 70	14 Ld PDIP	E14.3
DG303ACJ	0 to 70	14 Ld PDIP	E14.3
DG300AAA	-55 to 125	10 Pin Metal Can	T10.B
DG301AAA	-55 to 125	10 Pin Metal Can	T10.B
DG303ACY	0 to 70	16 Ld SOIC	M16.3
DG300AAA/883B	-55 to 125	10 Pin Metal Can	T10.B
DG300AAK/883B	-55 to 125	14 Ld CERDIP	F14.3
DG301AAA/883B	-55 to 125	10 Pin Metal Can	T10.B
DG301AAK/883B	-55 to 125	14 Ld CERDIP	F14.3
DG302AAK/883B	-55 to 125	14 Ld CERDIP	F14.3
DG303AAK/883B	-55 to 125	14 Ld CERDIP	F14.3

Functional Diagrams and Pinouts

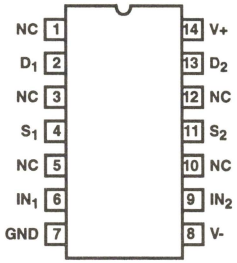
DG300A



DG300A (METAL CAN)
TOP VIEW



DG300A (CERDIP, PDIP)
TOP VIEW



TRUTH TABLE

LOGIC	SWITCH
0	OFF
1	ON

Logic "0" ≤ 0.8V, Logic "1" ≥ 4.0V; Two SPST switches per package (switches shown for Logic "1" input)

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3119.1**

DG308A, DG309

HARRIS SEMICONDUCTOR

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

Quad Monolithic SPST, CMOS Analog Switches

Features

- **Low Power Consumption**
- **CMOS Compatible**
- **±15V Analog Signal Range**
- **Single or Dual Supply Capability**
- **Alternate Source**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG308ACJ	0 to 70	16 Ld PDIP	E16.3
DG308ACY	0 to 70	16 Ld SOIC	M16.15
DG308AAK/883B	-55 to 125	16 Ld CERDIP	F16.3
DG309AK	-55 to 125	16 Ld CERDIP	F16.3
DG309CJ	0 to 70	16 Ld PDIP	E16.3
DG309CY	0 to 70	16 Ld SOIC	M16.15
DG309AK/883B	-55 to 125	16 Ld CERDIP	F16.3

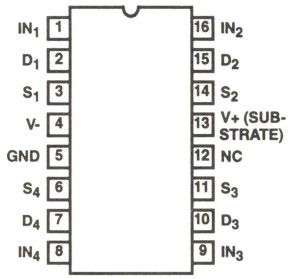
Description

The DG308A and DG309 quad monolithic SPST, CMOS switches are latch proof and are designed to block signals up to $30V_{P-P}$ when OFF. Featuring low ON resistance, low power consumption, and rail-to-rail analog signal range, these switches are ideally suited for high speed switching applications in communications, instrumentation and process control. The DG308A "normally-closed" and DG309 "normally-open" switches have single and dual supply capability. The input thresholds are CMOS compatible.

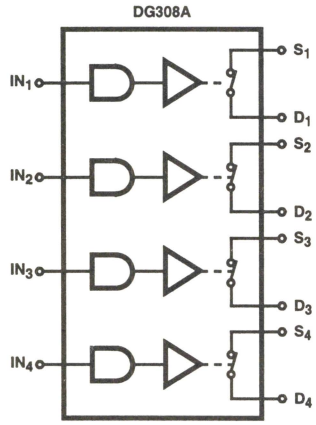
The DG308A and DG309 switches are available over commercial, and military temperature ranges.

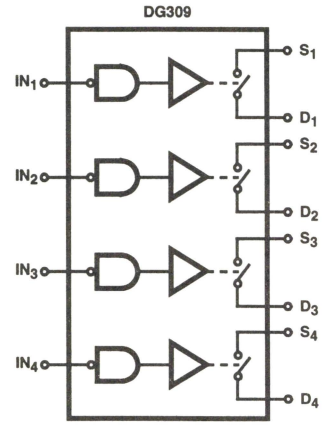
Pinout

DG201A, DG202
(CERDIP, PDIP, SOIC)
TOP VIEW



Functional Block Diagrams





NOTES:

1. Four SPST switches per package.
2. Switches shown for logic "1" input.

TRUTH TABLE

LOGIC	DG201A	DG202
0	ON	OFF
1	OFF	ON

Logic "0" ≤0.8V, Logic "1" ≥ 2.4V

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number **3120.1**

DG401, DG403, DG405

August 1997

Monolithic CMOS Analog Switches

Features

- ON-Resistance . . . . . <35Ω
- Low Power Consumption (P_D) . . . . . <35µW
- Fast Switching Action
  - t_{ON} . . . . . <150ns
  - t_{OFF} . . . . . <100ns
- Low Charge Injection
- DG401 Dual SPST; Same Pinout as HI-5041
- DG403 Dual SPDT; DG190, IH5043, IH5151, HI-5051
- DG405 Dual DPST; DG184, HI-5045, IH5145
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG401, DG403 and DG405 monolithic CMOS analog switches have TTL and CMOS compatible digital inputs.

These switches feature low analog ON resistance (<35Ω) and fast switch time (t_{ON} < 150ns). Low charge injection simplifies sample and hold applications.

The improvements in the DG401/403/405 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V_{P-P} signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±17V.

The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±15V analog input range. The three different devices provide the equivalent of two SPST (DG401), two SPDT (DG403) or two DPST (DG405) relay switch contacts with CMOS or TTL level activation. The pinout is similar, permitting a standard layout to be used, choosing the switch function as needed.

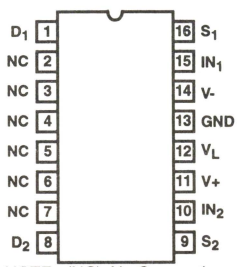
Ordering Information

PART NUMBER		TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG401AK/883	(Note 2)	-55 to 125	16 Ld CERDIP	F16.3
DG401DJ		-40 to 85	16 Ld PDIP	E16.3
DG401DY		-40 to 85	16 Ld SOIC	M16.15
DG401EJ	(Note 1)	-40 to 85	16 Ld PDIP	E16.3
DG401EY	(Note 1)	-40 to 85	16 Ld SOIC	M16.15
DG403AK/883	(Note 2)	-55 to 125	16 Ld CERDIP	F16.3
DG403DJ		-40 to 85	16 Ld PDIP	E16.3
DG403DY		-40 to 85	16 Ld SOIC	M16.15
DG403EJ	(Note 1)	-40 to 85	16 Ld PDIP	E16.3
DG403EY	(Note 1)	-40 to 85	16 Ld SOIC	M16.15
DG405AK/883	(Note 2)	-55 to 125	16 Ld CERDIP	F16.3
DG405DJ		-40 to 85	16 Ld PDIP	E16.3
DG405DY		-40 to 85	16 Ld SOIC	M16.15
DG405EJ	(Note 1)	-40 to 85	16 Ld PDIP	E16.3
DG405EY	(Note 1)	-40 to 85	16 Ld SOIC	M16.15

NOTES:
1. Extended Processing Flow.
2. Refer to Military data sheet for complete specifications.

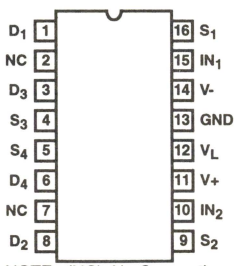
Pinouts

DG401 (CERDIP, PDIP, SOIC)
TOP VIEW



NOTE: (NC) No Connection

DG403, DG405 (CERDIP, PDIP, SOIC)
TOP VIEW



NOTE: (NC) No Connection

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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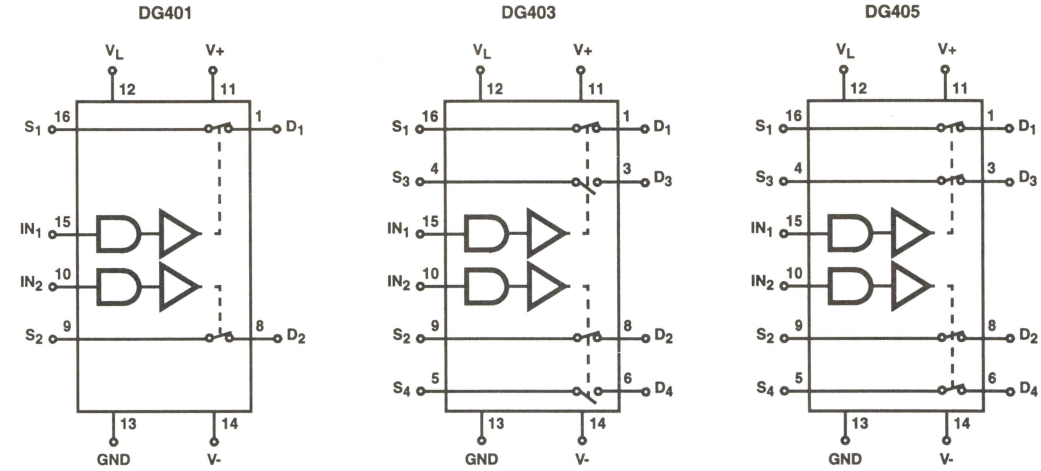
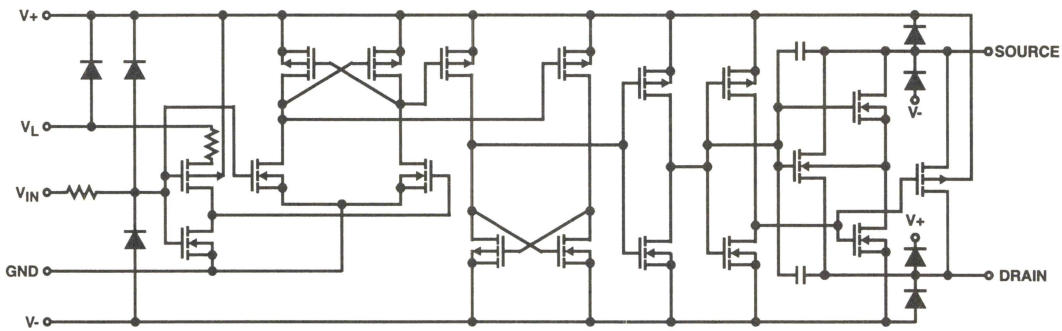
File Number **3284.5**

Functional Diagrams



Schematic Diagram



Truth Table

LOGIC	DG401	DG403		DG405
	SWITCH	SWITCH 1, 2	SWITCH 3, 4	SWITCH
0	OFF	OFF	ON	OFF
1	ON	ON	OFF	ON

NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V.

Absolute Maximum Ratings

V+ to V- . . . . . +44.0V
GND to V- 25V
VL . . . . . (GND - 0.3V) to (VC+) +0.3V
Digital Inputs (Note 1), V_S, V_D . . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous (Any Terminal) Current, (Note 1) . . . . . ±30mA
Peak Current, S or D (Note 1) . . . . . ±100mA
(Pulsed 1ms, 10% Duty Cycle)

Operating Conditions

Temperature (D and E Suffix) . . . . . -40°C to 85°C
Voltage Range . . . . . ±20V (Max)
Temperature Range . . . . . -55°C to 125°C
Input Low Voltage . . . . . 0.8V (Max)
Input High Voltage . . . . . 2.4V (Min)
Input Rise and Fall Time 20ns

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	90	N/A
SOIC Package	115	N/A
CERDIP Package	75	22

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Junction Temperature (Hermetic Package) . . . . . 175°C
Maximum Storage Temperature Range
(D and E Suffix) . . . . . -65°C to 125°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, V_L = 5V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 300Ω, C_L = 35pF	Room	-	100	150	ns
Turn-OFF Time, t_{OFF}		Room	-	60	100	ns
Break-Before-Make, Time Delay (DG403), t_D	R_L = 300Ω, C_L = 35pF	Room	5	12	-	ns
Charge Injection, Q	C_L = 10,000pF, V_{GEN} = 0V, R_{GEN} = 0Ω	Room	-	60	-	pC
OFF Isolation Reject Ratio, OIRR	R_L = 100Ω, C_L = 5pF, f = 1MHz	Room	-	72	-	dB
Crosstalk (Channel-to-Channel), CCRR	R_L = 100Ω, C_L = 5pF, f = 1MHz	Room	-	90	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz, V_S = 0V	Room	-	12	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	f = 1MHz, V_S = 0V	Room	-	12	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$	f = 1MHz, V_S = 0V	Room	-	39	-	pF
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, I_S = ∓10mA, V_D = ±10V	Room	-	20	45	Ω
		Full	-	-	55	Ω
Drain-Source ON Resistance, $\Delta r_{DS(ON)}$	V+ = 16.5V, V- = -16.5V, I_S = -10mA, V_D = 5, 0, -5V	Room	-	3	3	Ω
		Full	-	-	5	Ω
Switch OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5 V_D = ±15.5V, V_S = ∓15.5V	Room	-0.5	-0.01	0.5	nA
		Full	-5	-	5	nA
Switch OFF Leakage Current, $I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	Room	-0.5	-0.01	0.5	nA
		Full	-5	-	5	nA

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, V_L = 5V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
Channel ON Leakage Current, $I_{D(ON)}$	V± = ±16.5V, V_D = V_S = ±15.5V	Room	-1	-0.04	1	nA
		Full	-10	-	10	nA
DIGITAL CONTROL						
Input Current with V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-1	0.005	1	µA
Input Current with V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-1	0.005	1	µA
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	Room	-	0.01	1	µA
		Full	-	-	5	µA
Negative Supply Current, I-		Room	-1	-0.01	-	µA
		Full	-5	-	-	µA
Logic Supply Current, I_L		Room	-	0.01	1	µA
		Full	-	-	5	µA
Ground Current, I_{GND}		Room	-1	-0.01	-	µA
		Full	-5	-	-	µA

NOTES:

3. V_{IN} = input voltage to perform proper function.
4. Hot = as determined by the operating temperature suffix.
5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Typical Performance Curves

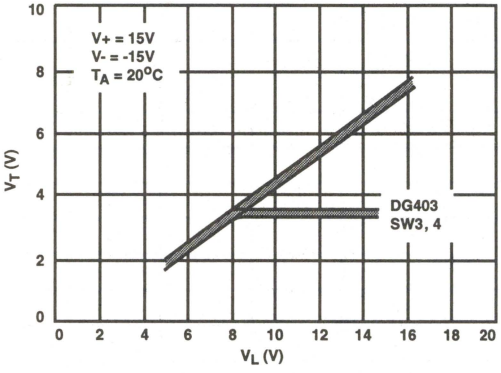


FIGURE 1. INPUT SWITCHING THRESHOLD vs LOGIC SUPPLY VOLTAGE

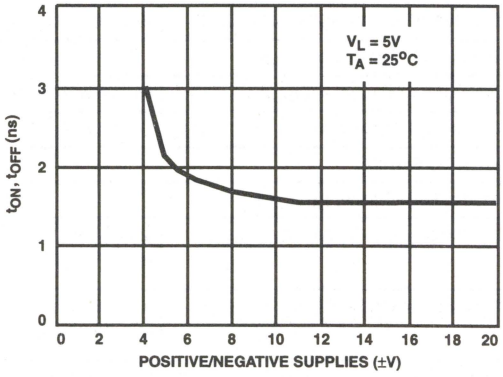


FIGURE 2. INPUT SWITCHING THRESHOLD vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

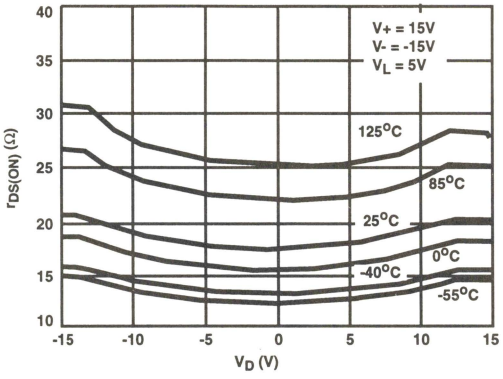


FIGURE 3. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

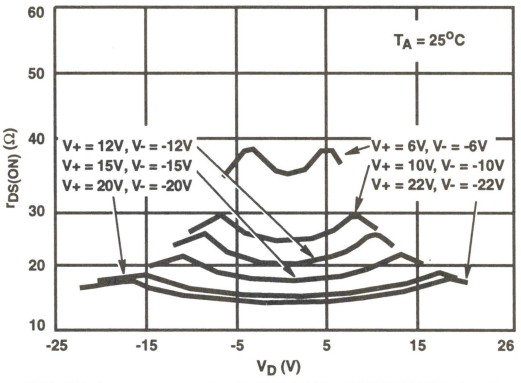


FIGURE 4. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

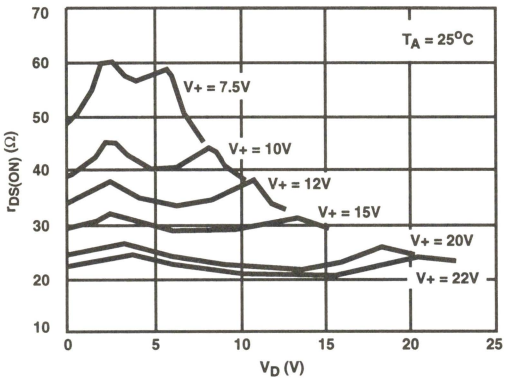


FIGURE 5. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE, V- = -0V

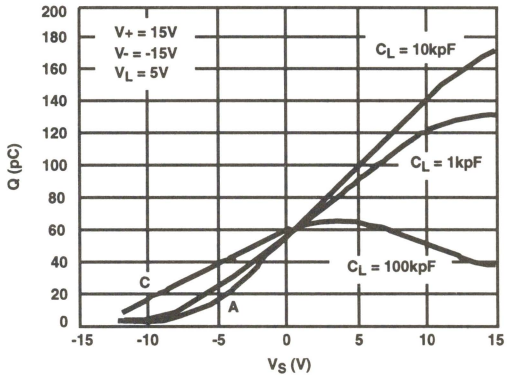


FIGURE 6. CHARGE INJECTION vs ANALOG VOLTAGE (V_S)

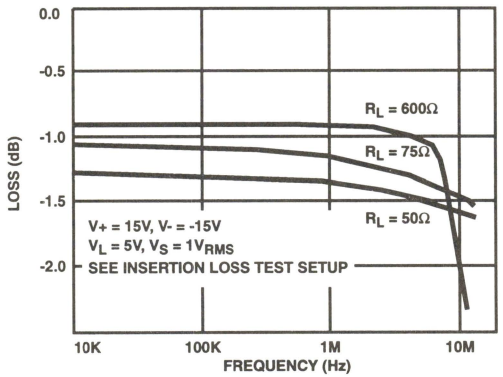


FIGURE 7. INSERTION LOSS vs FREQUENCY

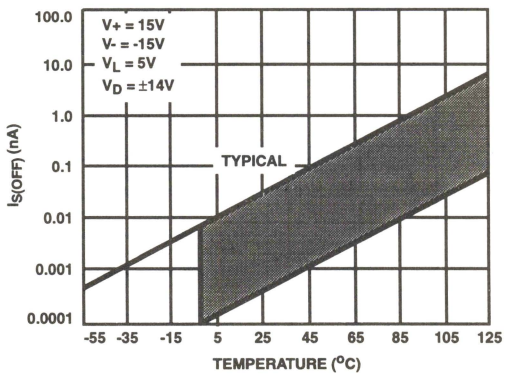


FIGURE 8. $I_{S(OFF)}$ vs TEMPERATURE

Typical Performance Curves (Continued)

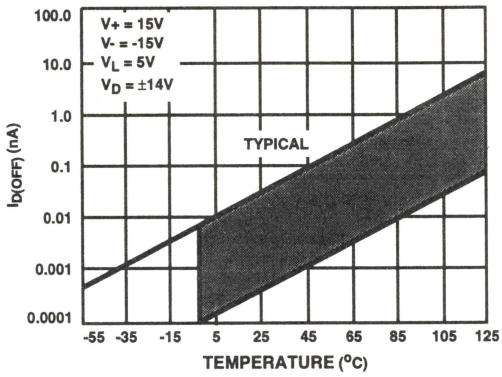


FIGURE 9. $I_{D(OFF)}$ vs TEMPERATURE

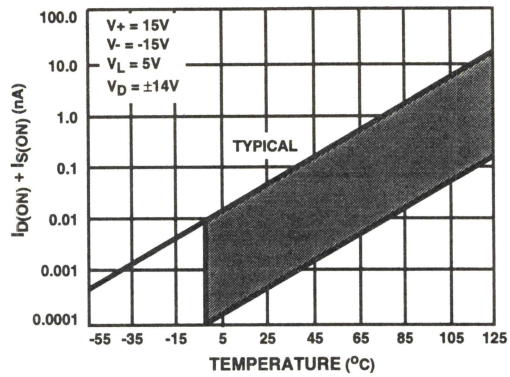


FIGURE 10. $I_{D(ON)} + I_{S(ON)}$ vs TEMPERATURE

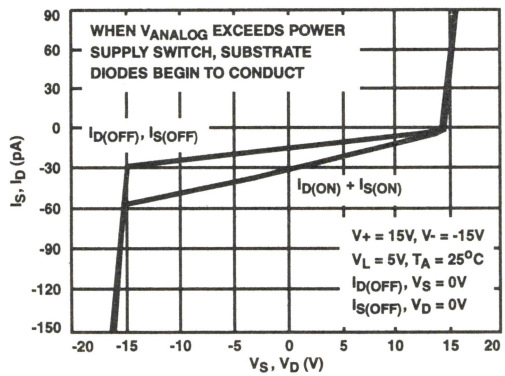


FIGURE 11. LEAKAGE CURRENT vs ANALOG VOLTAGE

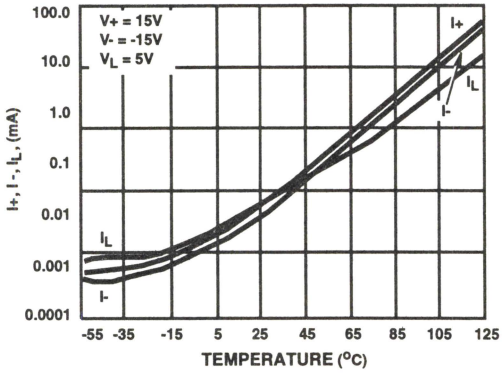


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

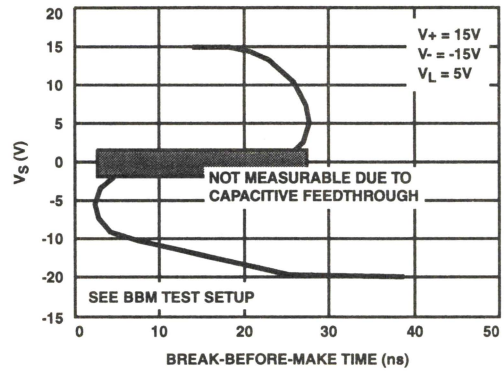


FIGURE 13. BREAK-BEFORE-MAKE vs ANALOG VOLTAGE

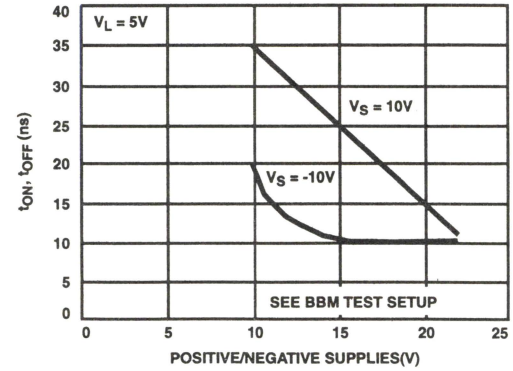


FIGURE 14. BREAK-BEFORE-MAKE vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

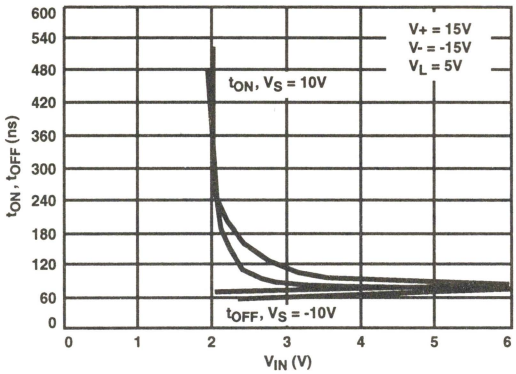


FIGURE 15. SWITCHING TIME vs INPUT LOGIC VOLTAGE (V_{IN}) (NOTE 1)

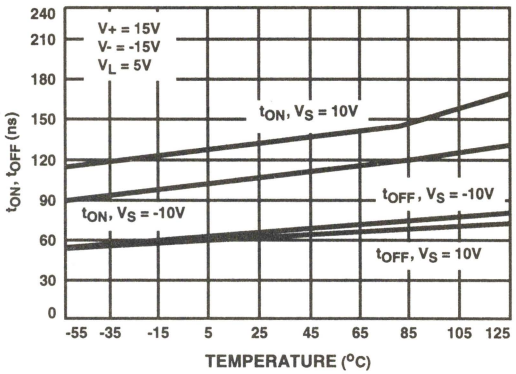


FIGURE 16. SWITCHING TIME vs TEMPERATURE (NOTE 1)

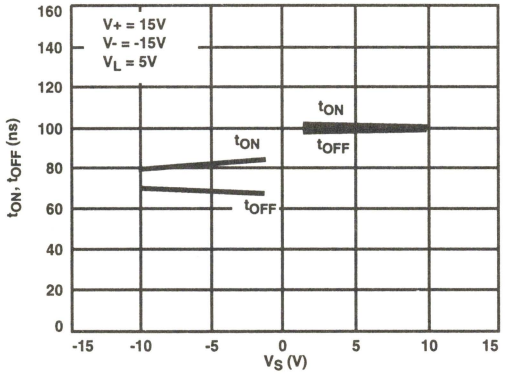


FIGURE 17. SWITCHING TIME vs ANALOG VOLTAGE (NOTE 1)

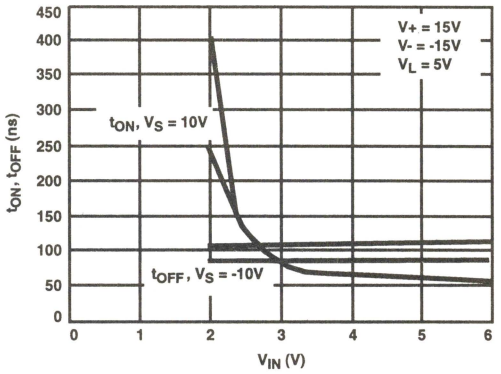


FIGURE 18. SWITCHING TIME vs INPUT LOGIC VOLTAGE (V_{IN}) (NOTE 1)

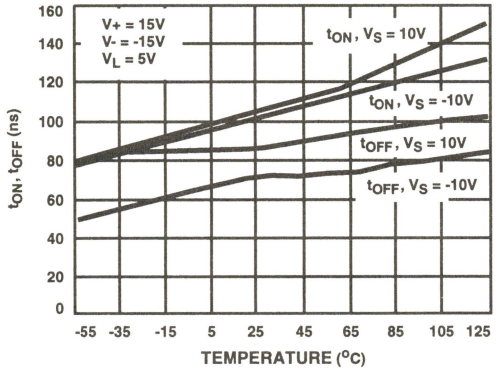


FIGURE 19. SWITCHING TIME vs TEMPERATURE (NOTE 1)

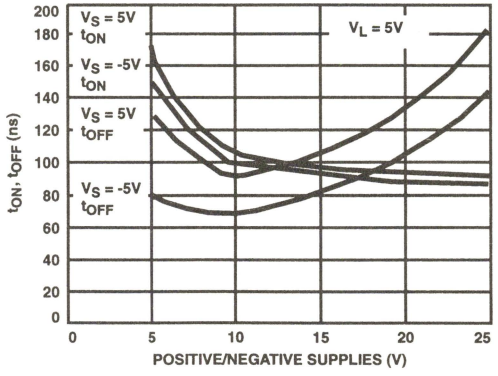


FIGURE 20. SWITCHING TIME vs POWER SUPPLY VOLTAGE (NOTE 1)

Typical Performance Curves (Continued)

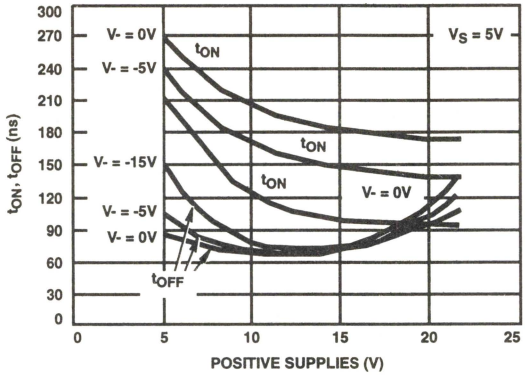


FIGURE 21. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

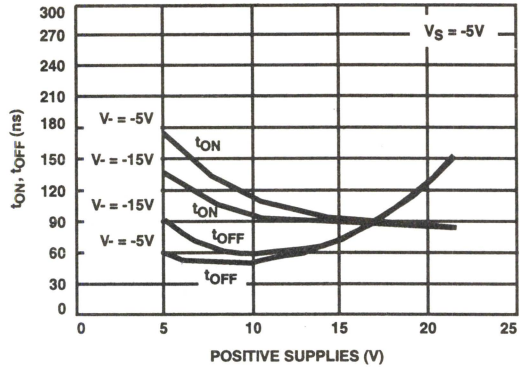


FIGURE 22. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

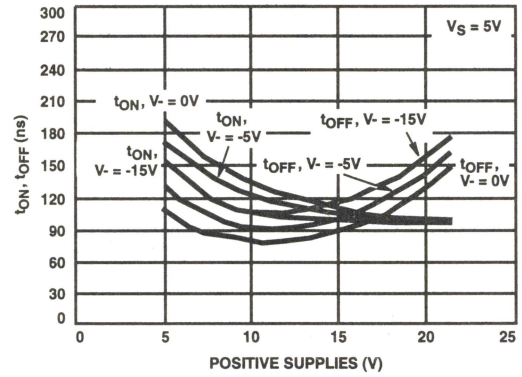


FIGURE 23. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

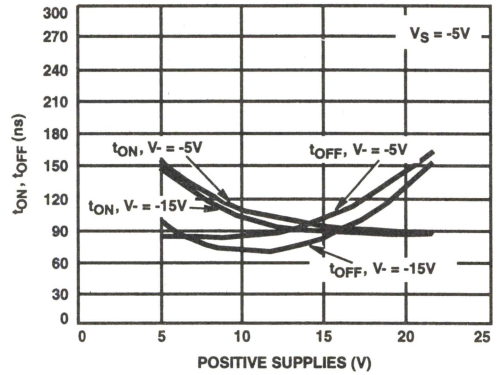
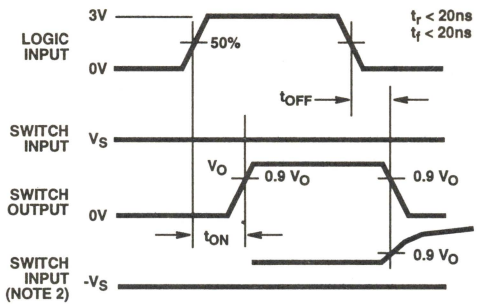


FIGURE 24. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

NOTE:

1. Refer to Figure 1 for test conditions.

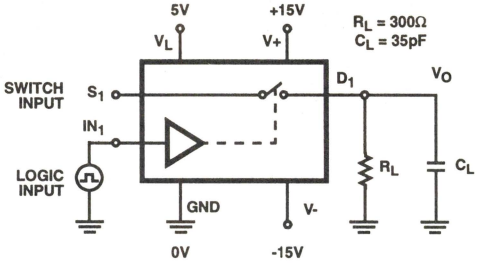
Test Circuits and Waveforms



NOTES:

1. Logic input waveform is inverted for switches that have the opposite logic sense.
2. V_S = 10V for t_{ON}, V_S = -10V for t_{OFF}.

FIGURE 25A.



Repeat test for IN_2 and S_2.
For load conditions, see Specifications. C_L (includes fixture and stray capacitance).

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 25B.

FIGURE 25. SWITCHING TIME

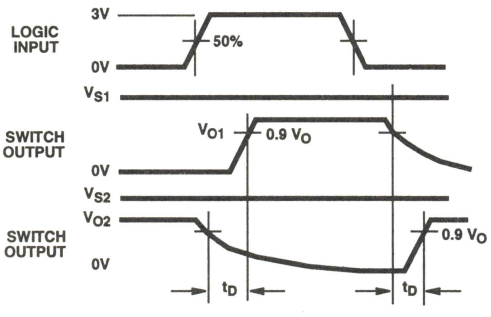
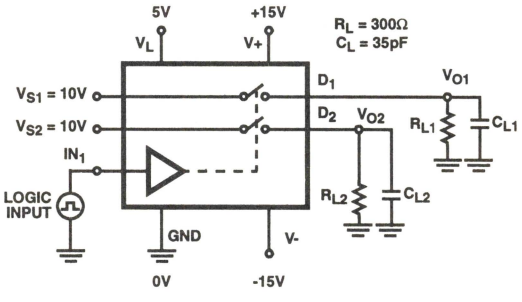


FIGURE 26A.



C_L (includes fixture and stray capacitance).

FIGURE 26B.

FIGURE 26. BREAK-BEFORE-MAKE

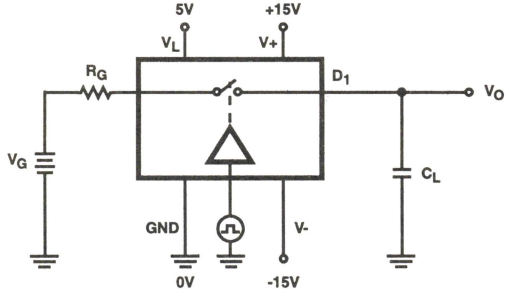
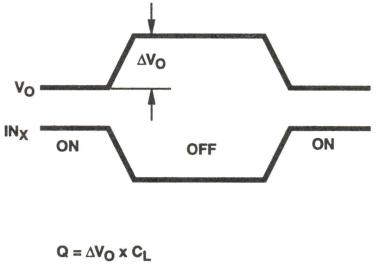


FIGURE 27A.



$Q = \Delta V_O \times C_L$

FIGURE 27B.

FIGURE 27. CHARGE INJECTION

Test Circuits and Waveforms (Continued)

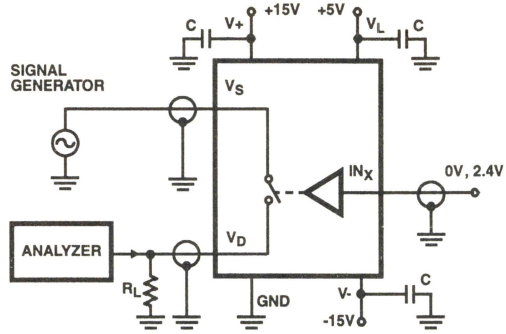


FIGURE 28. OFF ISOLATION

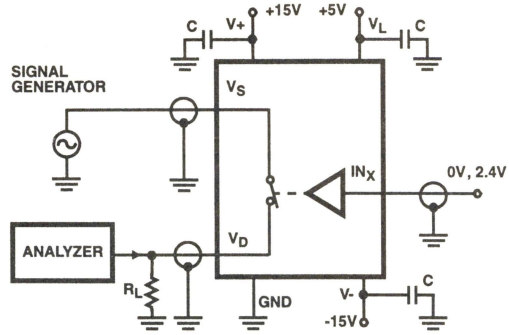


FIGURE 29. INSERTION LOSS

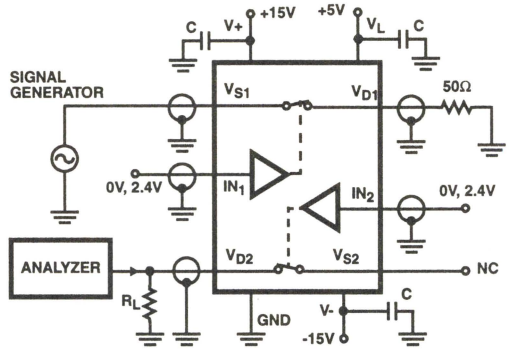


FIGURE 30. CROSSTALK

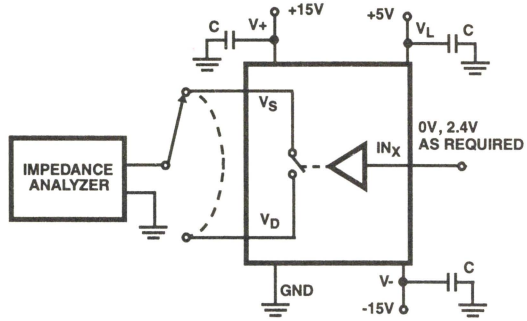


FIGURE 31. CAPACITANCES

Dual Slope Integrators

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2. Another one selects e_{IN} or discharges the capacitor in preparation for the next integration cycle.

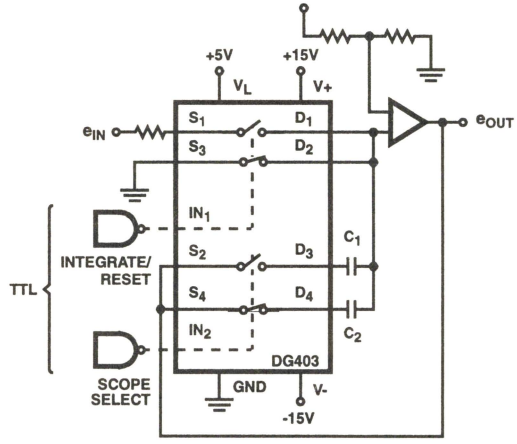


FIGURE 32. DUAL SLOPE INTEGRATOR

Peak Detector

A_3 acting as a comparator provides the logic drive for operating SW_1. the output of A_2 is fed back to A_3 and compared to the analog input e_{IN}. If $e_{IN} > e_{OUT}$ the output of A_3 is high keeping SW_1 closed. This allows C_1 to charge up to the analog input voltage. When e_{IN} goes below e_{OUT} of A_3 goes negative, turning SW_1 off. the system will therefore store the most positive analog input experienced.

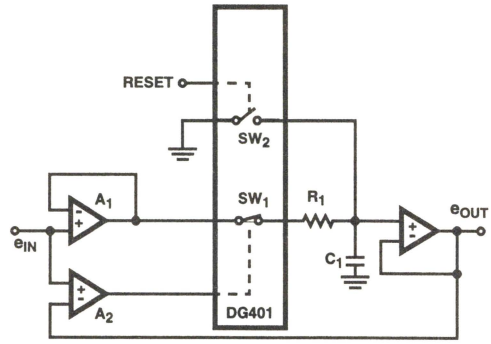


FIGURE 33. POSITIVE PEAK DETECTOR

HARRIS SEMICONDUCTOR

DG411, DG412, DG413

Monolithic Quad SPST, CMOS Analog Switches

August 1997

Features

- ON-Resistance . . . . . <35Ω Max
- Low Power Consumption (P_D) . . . . . <35µW
- Fast Switching Action
  - t_{ON} . . . . . <175ns
  - t_{OFF} . . . . . <145ns
- Low Charge Injection
- Upgrade from DG211/DG212
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG411 series monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole throw (SPST) analog switches, and TTL and CMOS compatible digital inputs.

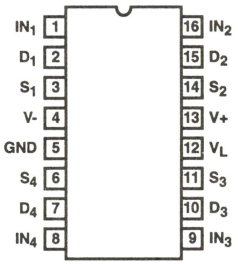
These switches feature lower analog ON resistance (<35Ω) and faster switch time (t_{ON} < 175ns) compared to the DG211 or DG212. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG411 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling $40V_{P-P}$ signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a 15V analog input range. The switches in the DG411 and DG412 are identical, differing only in the polarity of the selection logic. Two of the switches in the DG413 (#1 and #4) use the logic of the DG211 and DG411 (i.e., a logic "0" turns the switch ON) and the other two switches use DG212 and DG412 positive logic. This permits independent control of turn-on and turn-off times for SPDT configurations, permitting "break-before-make" or "make-before-break" operation with a minimum of external logic.

Pinout

DG411, DG412, DG413
(CERDIP, PDIP, SOIC)
TOP VIEW



Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG411AK/883	-55 to 125	16 Ld CERDIP	F16.3
DG411DJ	-40 to 85	16 Ld PDIP	E16.3
DG411DY	-40 to 85	16 Ld SOIC	M16.15
DG411EJ (Note)	-40 to 85	16 Ld PDIP	E16.3
DG411EY (Note)	-40 to 85	16 Ld SOIC	M16.15
DG412AK/883	-55 to 125	16 Ld CERDIP	F16.3
DG412DJ	-40 to 85	16 Ld PDIP	E16.3
DG412DY	-40 to 85	16 Ld SOIC	M16.15
DG412EJ (Note)	-40 to 85	16 Ld PDIP	E16.3
DG412EY (Note)	-40 to 85	16 Ld SOIC	M16.15
DG413AK/883	-55 to 125	16 Ld CERDIP	F16.3
DG413DJ	-40 to 85	16 Ld PDIP	E16.3
DG413DY	-40 to 85	16 Ld SOIC	M16.15
DG413EJ (Note)	-40 to 85	16 Ld PDIP	E16.3
DG413EY (Note)	-40 to 85	16 Ld SOIC	M16.15

NOTE: Extended Processing Flow

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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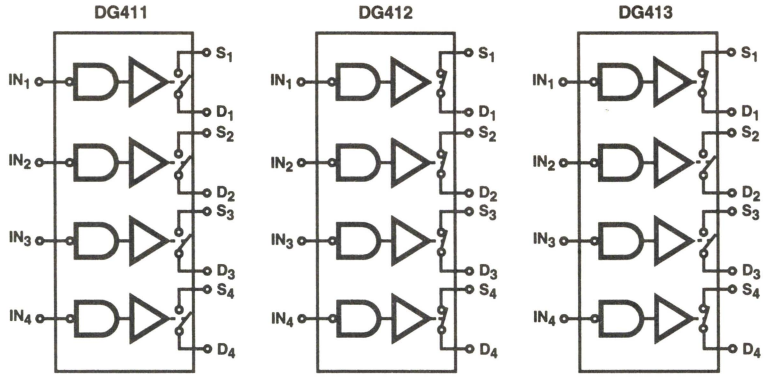
File Number **3282.4**

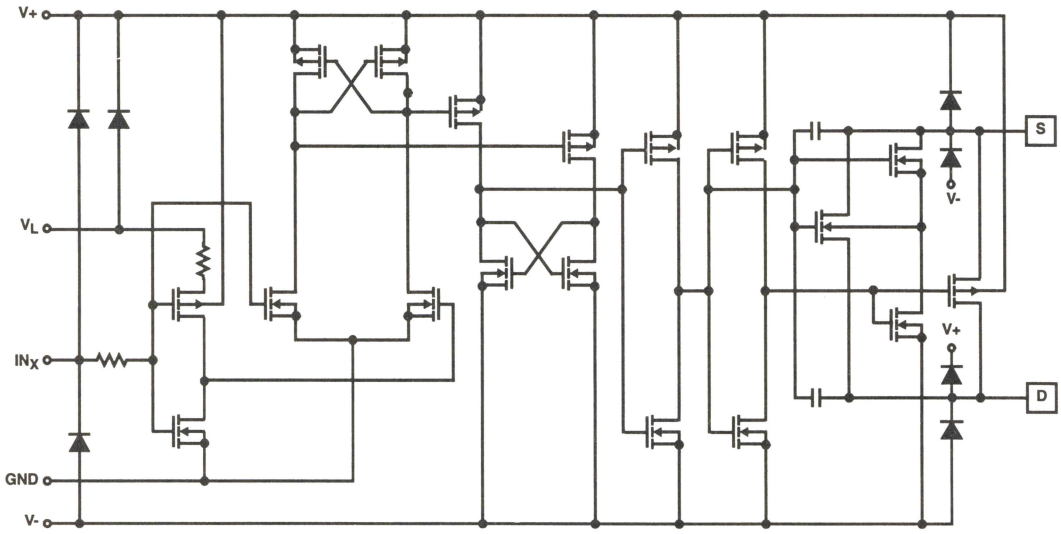
Functional Diagrams

Four SPST Switches per Package Switches Shown for Logic "1" Input



Typical Schematic Diagram

(Typical Channel)



Absolute Maximum Ratings

V+ to V- 44V
GND to V- 25V
V_L . . . . . (GND -0.3V) to (V+) +0.3V
Digital Inputs, V_S, V_D (Note 1) . . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Current, S or D (Pulsed 1ms, 10% Duty Cycle) 100mA

Operating Conditions

Operating Voltage Range . . . . . ±20V (Max)
Operating Temperature Range . . . . . -40°C to 85°C
Input Low Voltage . . . . . 0.8V (Max)
Input High Voltage . . . . . 2.4V (Min)
Input Rise and Fall Time . . . . . ≤20ns
Operating Temperature
(D Suffix) . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	100	N/A
SOIC Package	115	N/A
CERDIP Package	75	20

Maximum Junction Temperature (Plastic Packages) . . . . . 150°C
Maximum Junction Temperature (Ceramic Package) . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 125°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:
1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS		(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS							
Turn-ON Time, t_{ON}	R_L = 300Ω, C_L = 35pF, V_S = ±10V, (See Figure 7)		25	-	110	175	ns
			Hot	-	-	220	ns
Turn-OFF Time, t_{OFF}			25	-	100	145	ns
			Hot	-	-	160	ns
Break-Before-Make Time Delay	DG413 Only, R_L = 300Ω, C_L = 35pF		25	-	25	-	ns
Charge Injection, Q	C_L = 10nF, V_G = 0V, R_G = 0Ω		25	-	5	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz		25	-	68	-	dB
Crosstalk (Channel-to-Channel)			25	-	85	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz		25	-	9	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$			25	-	9	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$			25	-	35	-	pF
DIGITAL CONTROL							
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V		Full	-0.5	0.005	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V		Full	-0.5	0.005	0.5	µA
ANALOG SWITCH							
Analog Signal Range, V_{ANALOG}	I_S = ∓10mA		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = -10mA, V_D = ±8.5, V+ = 13.5V, V- = -13.5V		25	-	25	35	Ω
			Full	-	-	45	Ω
Switch OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V	V_D = ±15.5V, V_S = ∓15.5V	25	-0.25	±0.1	0.25	nA
			Full	-5	-	+5	nA
Switch OFF Leakage Current, $I_{D(OFF)}$		V_D = ±15.5V, V_S = ∓15.5V	25	-0.25	±0.1	0.25	nA
			Full	-5	-	+5	nA
Channel ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$		$V_S = V_D$ = ±15.5V	25	-0.4	±0.1	0.4	nA
			Full	-10	-	+10	nA

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V V_{IN} = 0V or 5V	25	-	0.0001	1	µA
		Hot		-	5	µA
Negative Supply Current, I-		25	-1	-0.0001	-	µA
		Hot	-5	-	-	µA
Logic Supply Current, I_L		25	-	0.0001	1	µA
		Hot	-	-	5	µA
Ground Current, I_{GND}		25	-1	-0.0001	-	µA
		Hot	-5	-	-	µA

Electrical Specifications (Unipolar Supplies) Test Conditions: V+ = +12V, V- = 0V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 300Ω, C_L = 35pF, V_S = ±8V, (See Figure 7)	25	-	175	250	ns
		Hot	-	-	315	ns
Turn-OFF Time, t_{OFF}		25	-	95	125	ns
		Hot	-	-	140	ns
Break-Before-Make Time Delay	DG413 Only, R_L = 300Ω, C_L = 35pF, V_S = 8V	25	-	25	-	ns
Charge Injection, Q	C_L = 10nF, V_G = 6.0V, R_G = 0Ω	25	-	25	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = -10mA, V_D = 3V, 8V V+ = 10.8V	25	-	40	80	Ω
		Full	-	-	100	Ω
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 13.2V, V- = 0V V_{IN} = 0V or 5V	25	-	0.0001	1	µA
		Hot		-	5	µA
Negative Supply Current, I-		25	-1	-0.0001	-	µA
		Hot	-5	-	-	µA
Logic Supply Current, I_L		25	-	0.0001	1	µA
		Hot	-	-	5	µA
Ground Current, I_{GND}		25	-1	-0.0001	-	µA
		Hot	-5	-	-	µA

NOTES:

3. V_{IN} = input voltage to perform proper function.
4. Hot = as determined by the operating temperature suffix.
5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Typical Performance Curves

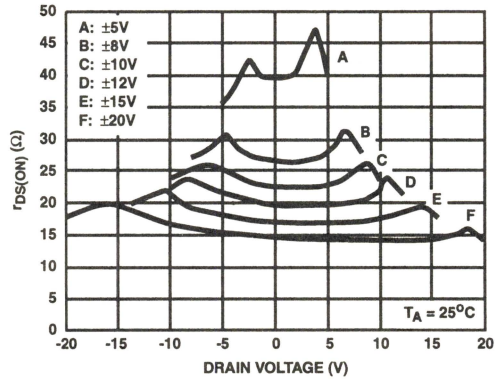


FIGURE 1. ON-RESISTANCE vs V_D AND POWER SUPPLY VOLTAGE

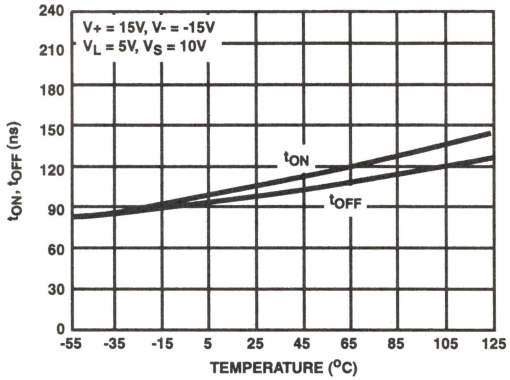


FIGURE 2. SWITCHING TIME vs TEMPERATURE

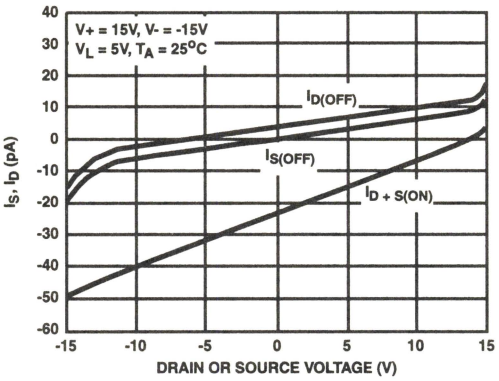


FIGURE 3. LEAKAGE CURRENT vs ANALOG VOLTAGE

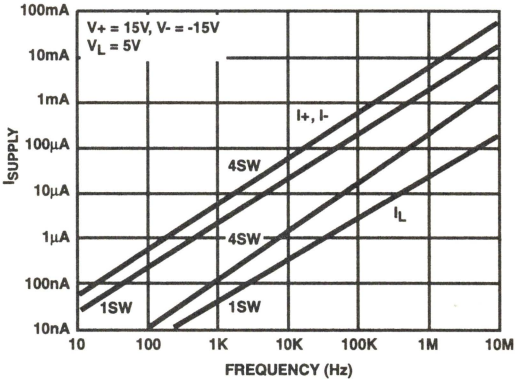


FIGURE 4. SUPPLY CURRENT vs INPUT SWITCHING FREQUENCY

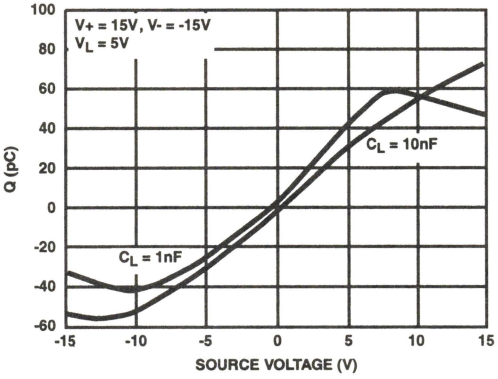


FIGURE 5. CHARGE INJECTION vs ANALOG VOLTAGE (V_D)

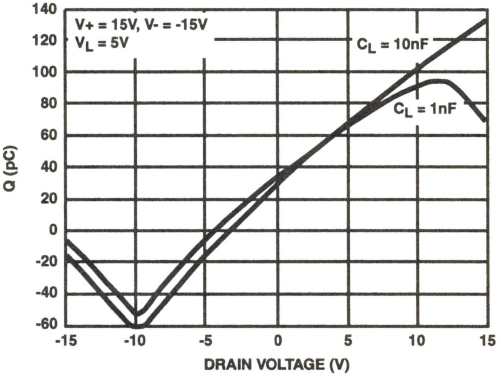


FIGURE 6. CHARGE INJECTION vs ANALOG VOLTAGE (V_S)

Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic Control for Switch 1.
2	D_1	Drain (Output) Terminal for Switch 1.
3	S_1	Source (Input) Terminal for Switch 1.
4	V-	Negative Power Supply Terminal.
5	GND	Ground Terminal (Logic Common).
6	S_4	Source (Input) Terminal for Switch 4.
7	D_4	Drain (Output) Terminal for Switch 4.
8	IN_4	Logic Control for Switch 4.
9	IN_3	Logic Control for Switch 3.
10	D_3	Drain (Output) Terminal for Switch 3.
11	S_3	Source (Input) Terminal for Switch 3.
12	V_L	Logic Reference Voltage.
13	V+	Positive Power Supply Terminal (Substrate).
14	S_2	Source (Input) Terminal for Switch 2.
15	D_2	Drain (Output) Terminal for Switch 2.
16	IN_2	Logic Control for Switch 2.

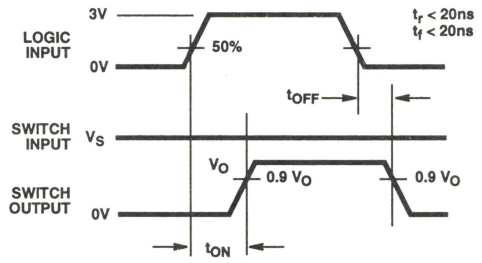
TRUTH TABLE

LOGIC	DG411 SWITCH	DG412 SWITCH	DG413 SWITCH 1, 4	DG413 SWITCH 2, 3
0	ON	OFF	OFF	ON
1	OFF	ON	ON	OFF

NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V.

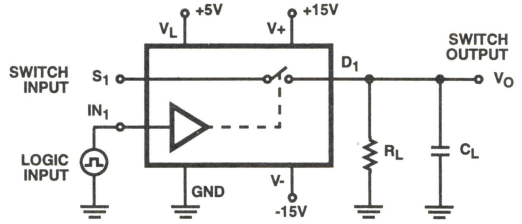
Test Circuits and Waveforms

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 7A.



Repeat test for all IN and S.
For load conditions, see Specifications C_L (includes fixture and stray capacitance).

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 7B.

FIGURE 7. SWITCHING TIME

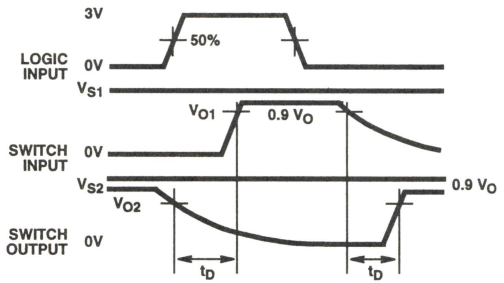


FIGURE 8A.

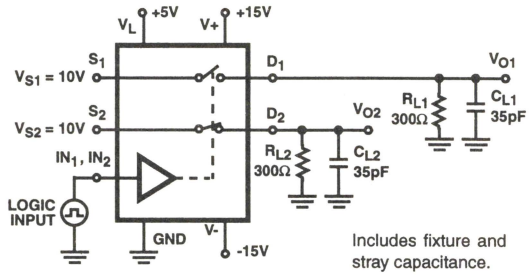


FIGURE 8B.

FIGURE 8. BREAK-BEFORE-MAKE

Test Circuits and Waveforms (Continued)

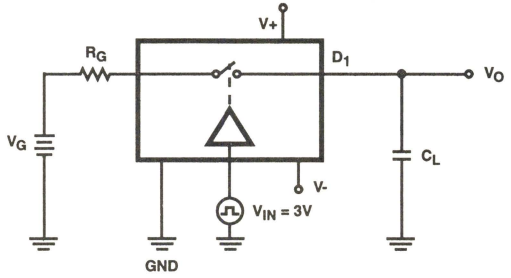
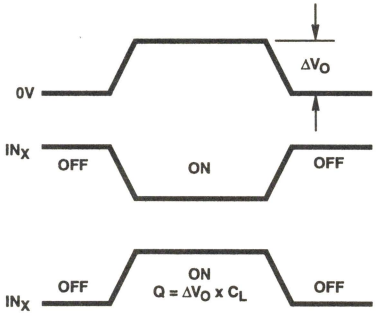


FIGURE 9A.



NOTE: IN_X dependent on switch configuration input polarity determined by sense of switch.

FIGURE 9B.

FIGURE 9. CHARGE INJECTION

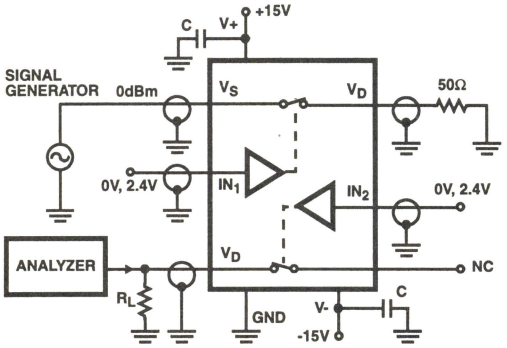


FIGURE 10. CROSSTALK

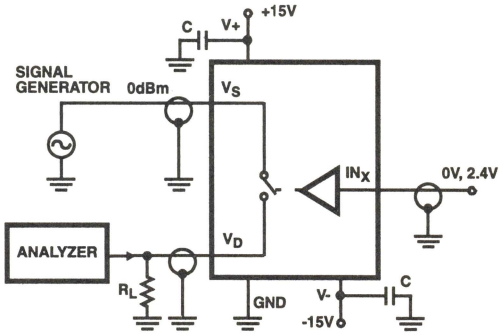


FIGURE 11. OFF ISOLATION

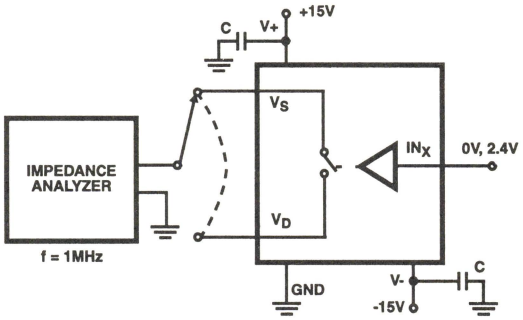


FIGURE 12. SOURCE/DRAIN CAPACITANCES

Typical Applications

Single Supply Operation

The DG411, DG412, DG413 can be operated with unipolar supplies from 5V to 44V. These devices are characterized and tested for unipolar supply operation at 12V to facilitate the majority of applications. To function properly, 12V are tied to Pin 13 and 0V are tied to Pin 4.

NOTE: Pin 12 still requires 5V for TTL compatible switching.

Summing Amplifier

When driving a high impedance, high capacitance load such as shown in Figure 9, where the inputs to the summing amplifier have some noise filtering, it is necessary to have shunt switches for rapid discharge of the filter capacitor, thus preventing offsets from occurring at the output.

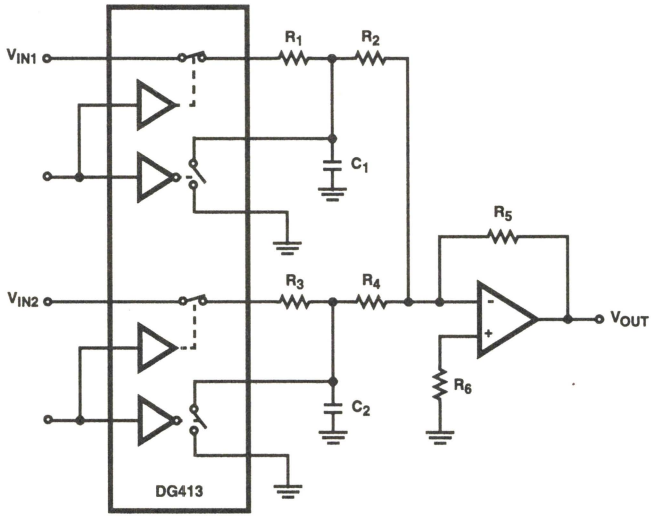


FIGURE 13. SUMMING AMPLIFIER

Die Characteristics

DIE DIMENSIONS:

2760µm x 1780µm x 485µm ±25µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

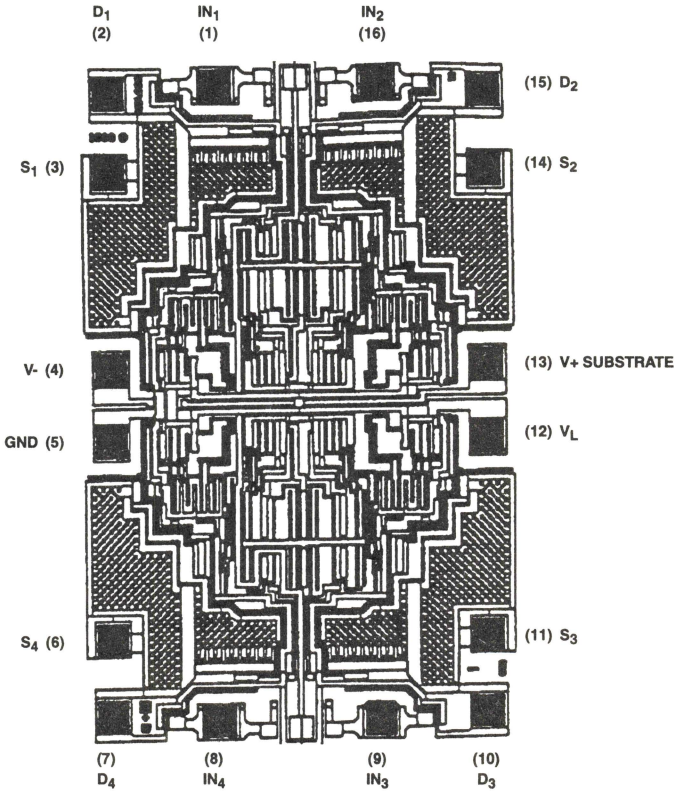
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

1.5×10^5 A/cm^2

Metallization Mask Layout

DG411, DG412, DG413



HARRIS SEMICONDUCTOR

DG441, DG442

Monolithic, Quad SPST, CMOS Analog Switches

August 1997

Features

- ON-Resistance (Max) 85Ω
- Low Power Consumption (P_D <1.6mW)
- Fast Switching Action
  - t_{ON} . . . . . <250ns
  - t_{OFF} . . . . . <120ns (DG441)
- Low Charge Injection
- Upgrade from DG201A/DG202
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG441 and DG442 monolithic CMOS analog switches are drop-in replacements for the popular DG201A and DG202 series devices. They include four independent single pole single throw (SPST) analog switches, TTL and CMOS compatible digital inputs, and a voltage reference for logic thresholds.

These switches feature lower analog ON resistance (<85Ω) and faster switch time (t_{ON} < 250ns) compared to the DG201A and DG202. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG441 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling $40V_{P-P}$ signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range. The switches in the DG441 and DG442 are identical, differing only in the polarity of the selection logic.

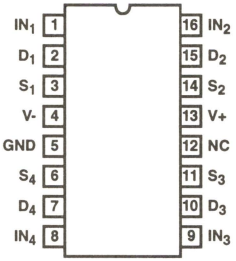
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG441AK/883 (Note 2)	-55 to 125	16 Ld CERDIP	F16.3
DG441DJ	-40 to 85	16 Ld PDIP	E16.3
DG441DY	-40 to 85	16 Ld SOIC	M16.15
DG441EJ (Note 1)	-40 to 85	16 Ld PDIP	E16.3
DG441EY (Note 1)	-40 to 85	16 Ld SOIC	M16.15
DG442AK/883 (Note 2)	-55 to 125	16 Ld CERDIP	F16.3
DG442DJ	-40 to 85	16 Ld PDIP	E16.3
DG442DY	-40 to 85	16 Ld SOIC	M16.15
DG442EJ (Note 1)	-40 to 85	16 Ld PDIP	E16.3
DG442EY (Note 1)	-40 to 85	16 Ld SOIC	M16.15

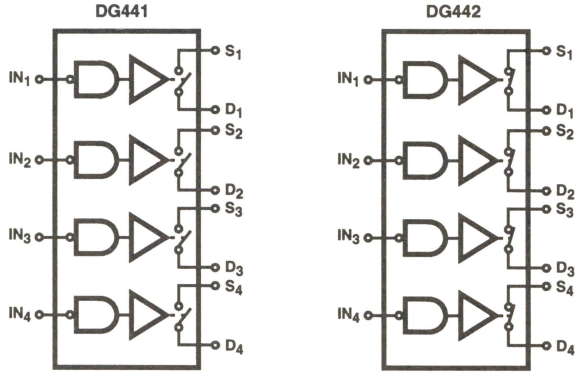
NOTES:
1. Extended Processing Flow
2. Refer to military data sheets for complete specifications.

Pinout

DG441, DG442
(PDIP, CERDIP, SOIC)
TOP VIEW



Functional Diagrams



SWITCHES SHOWN FOR LOGIC "1" INPUT

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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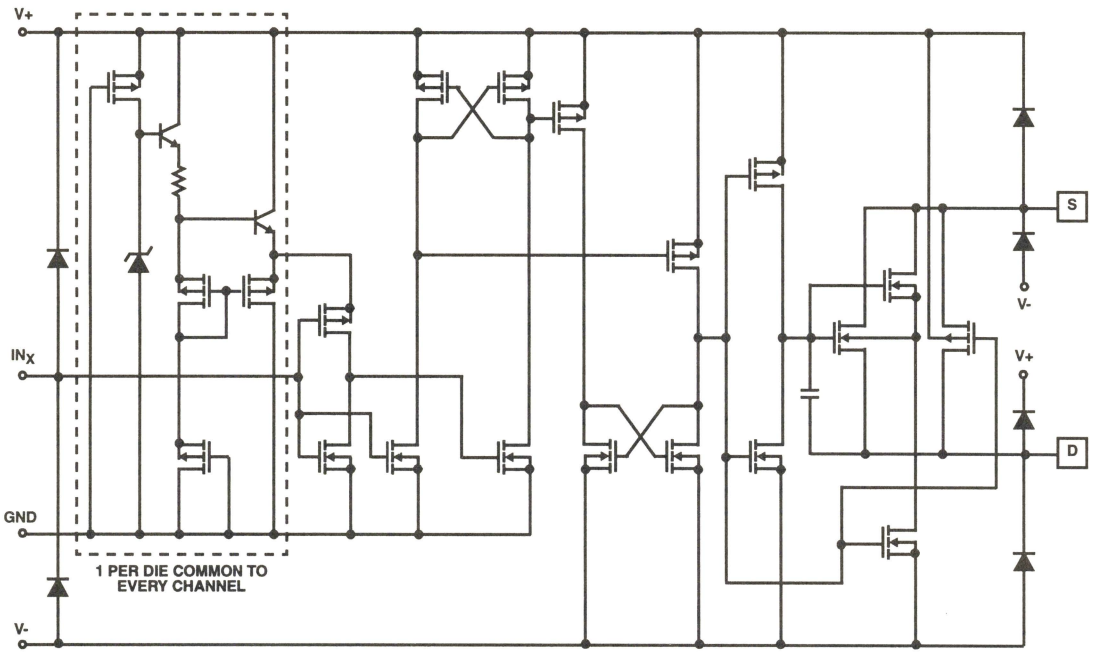
File Number **3281.4**

Schematic Diagram (One Channel)



Absolute Maximum Ratings

V+ to V- . . . . . +44.0V
GND to V- 25V
Digital Inputs (Note 1) . . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current, S or D (Note 1) . . . . . ±30mA
Peak Current, S or D (Note 1) . . . . . ±100mA
(Pulsed 1ms, 10% Duty Cycle)

Operating Conditions

Temperature Range (D Suffix) . . . . . -40°C to 85°C
Voltage Range . . . . . ±20V (Max)
Temperature Range . . . . . -55°C to 125°C
Input Low Voltage . . . . . 0.8V (Max)
Input High Voltage . . . . . 2.4V (Min)
Input Rise and Fall Time . . . . . ≤20ns

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	100	N/A
SOIC Package	115	N/A
CERDIP Package	75	22

Maximum Junction Temperature (Ceramic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Packages) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on SX, DX or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

(Dual Supply) Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, $V_{ANALOG} = V_S$, V_D, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEMP (°C)	D SUFFIX -40°C TO 85°C MIN	(NOTE 4) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_1 = 1kΩ, C_L = 35pF, V_S = ±10V, See Figure 18	25	-	150	250	ns
Turn-OFF Time, t_{OFF}		25				
DG441			-	90	120	ns
DG442			-	110	210	ns
Charge Injection, Q	C_L = 1nF, V_S = 0V, V_{GEN} = 0V, R_{GEN} = 0Ω	25	-	-1	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	60	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	-100	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz	25	-	4	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	f = 1MHz	25	-	4	-	pF
Channel ON Capacitance, $C_{D(ON)}$ + $C_{S(ON)}$	V_{ANALOG} = 0	25	-	16	-	pF
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = ∓10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V	25	-	50	85	Ω
		Hot	-	-	100	Ω
Switch OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	25	-0.5	0.01	0.5	nA
		Hot	-5	-	5	nA
Switch OFF Leakage Current, $I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	25	-0.5	0.01	0.5	nA
		Hot	-5	-	5	nA

Electrical Specifications (Dual Supply) Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, V_{ANALOG} = V_S, V_D, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEMP (°C)	D SUFFIX -40°C TO 85°C MIN	(NOTE 4) TYP	MAX	UNITS
Channel ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, $V_S = V_D = \pm 15.5V$	25	-0.5	0.08	0.5	nA
		Hot	-10	-	10	nA
DIGITAL CONTROL						
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-0.5	-0.00001	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-0.5	0.00001	0.5	µA
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	Full	-	15	100	µA
Negative Supply Current, I-		25	-1	-0.0001	-	µA
		Full	-5	-	-	µA
Ground Current, I_{GND}		Full	-100	-15	-	µA

Electrical Specifications (Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_{IN} = 2.4V, 0.8V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEMP (°C)	D SUFFIX -40°C TO 85°C MIN	(NOTE 4) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 1kΩ, C_L = 35pF, See Test Circuit, V_S = 8V	25	-	300	450	ns
Turn-OFF Time, t_{OFF}		25	-	60	200	ns
Charge Injection, Q	C_L = 1nF, V_{GEN} = 6V, R_{GEN} = 0Ω	25	-	2	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON-Resistance, $r_{DS(ON)}$	I_S = 10mA, V_D = 3V, 8V V+ = 10.8V	25	-	100	160	Ω
		Full	-	-	200	Ω
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5V	Full	-	15	100	µA
Negative Supply Current, I-		25	-1	-0.0001	-	µA
		Full	-100	-0.0001	-	µA
Ground Current, I_{GND}		Full	-100	-15	-	µA

NOTES:

3. Room: 25°C. Cold: D suffix -40°C. Hot: D suffix 85°C.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor production tested.

Typical Performance Curves

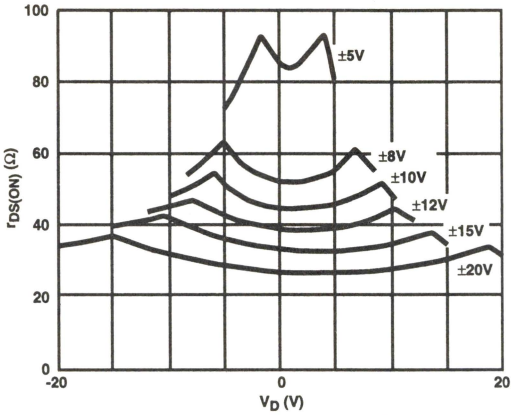


FIGURE 1. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

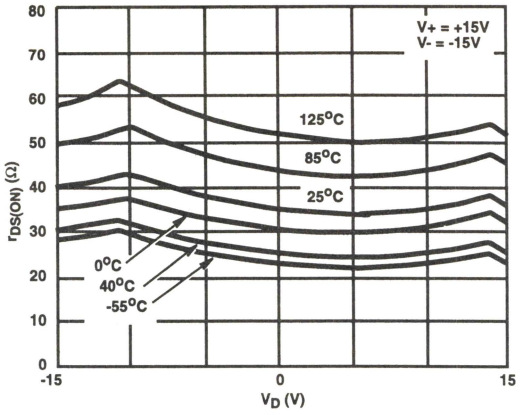


FIGURE 2. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

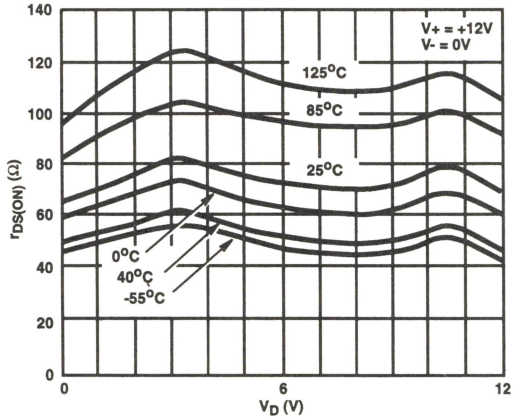


FIGURE 3. $r_{DS(ON)}$ vs V_D AND TEMPERATURE (SINGLE 12V SUPPLY)

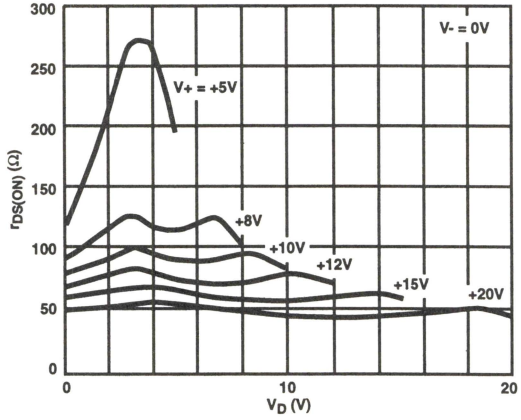


FIGURE 4. $r_{DS(ON)}$ vs V_D AND UNIPOLAR POWER SUPPLY VOLTAGE

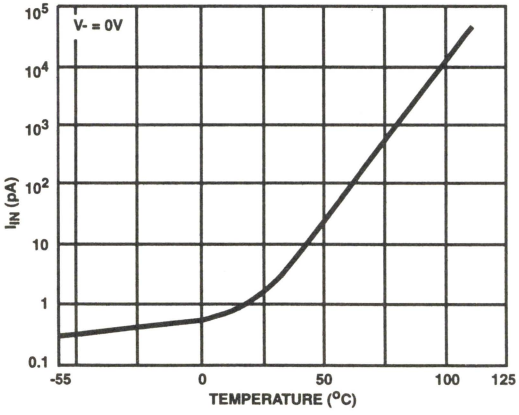


FIGURE 5. INPUT CURRENT vs TEMPERATURE

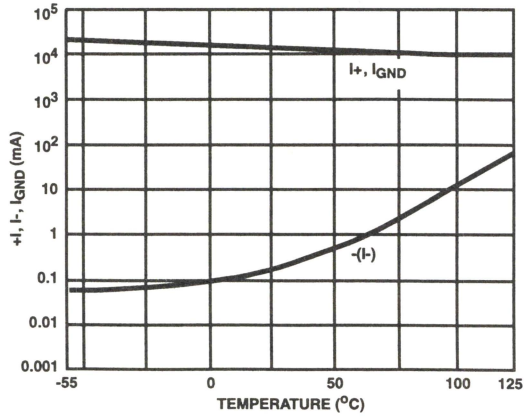


FIGURE 6. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

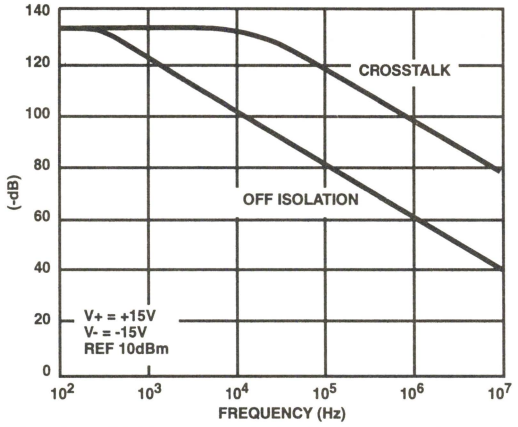


FIGURE 7. CROSSTALK AND OFF ISOLATION vs FREQUENCY

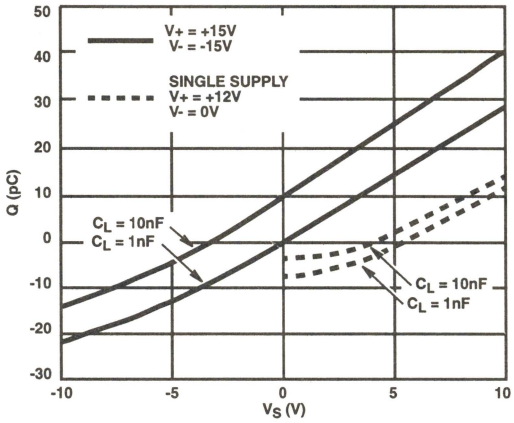


FIGURE 8. CHARGE INJECTION vs SOURCE VOLTAGE

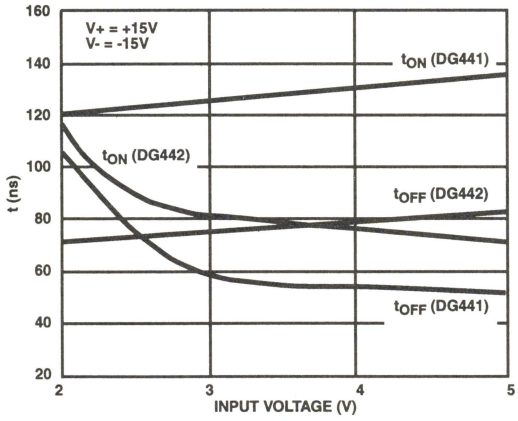


FIGURE 9. SWITCHING TIMES vs INPUT VOLTAGE

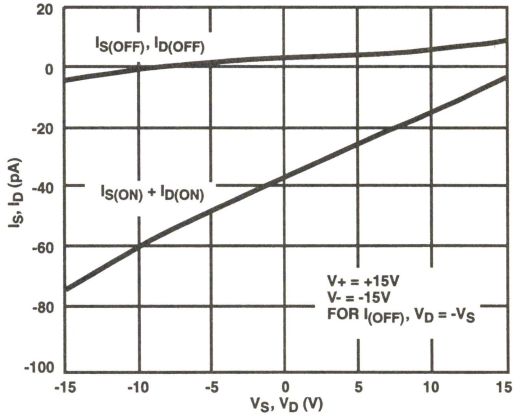


FIGURE 10. SOURCE/DRAIN LEAKAGE CURRENTS

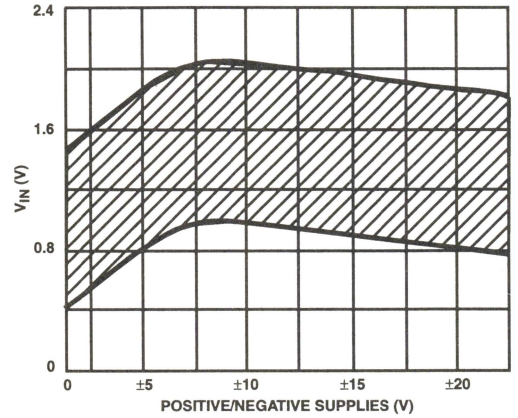


FIGURE 11. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

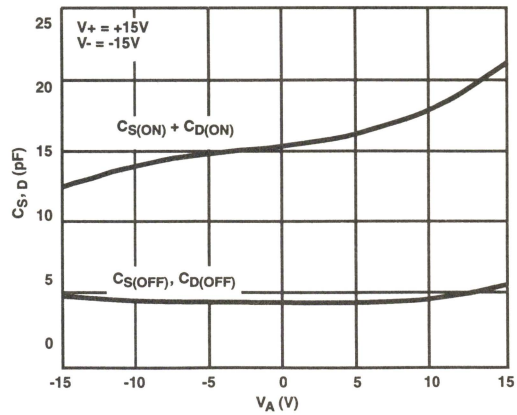


FIGURE 12. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

Typical Performance Curves (Continued)

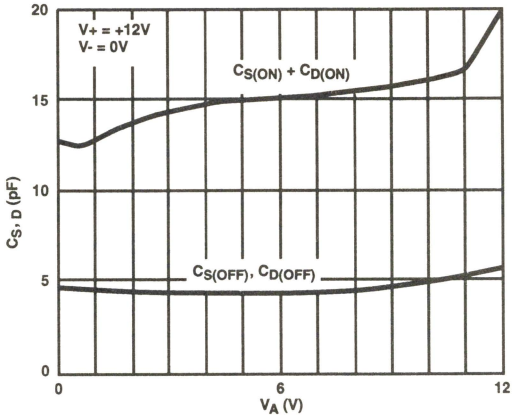


FIGURE 13. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

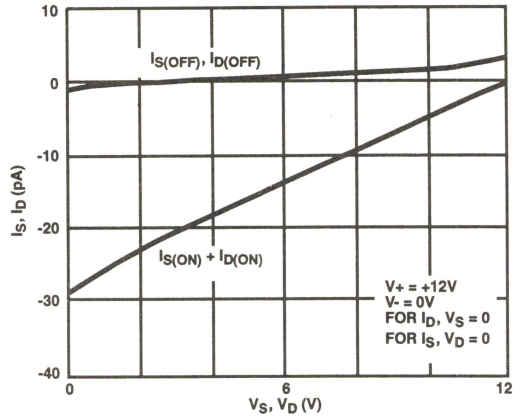


FIGURE 14. SOURCE/DRAIN LEAKAGE CURRENTS (SINGLE 12V SUPPLY)

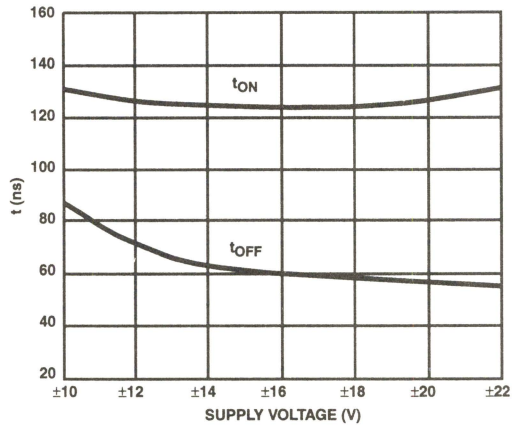


FIGURE 15. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG441)

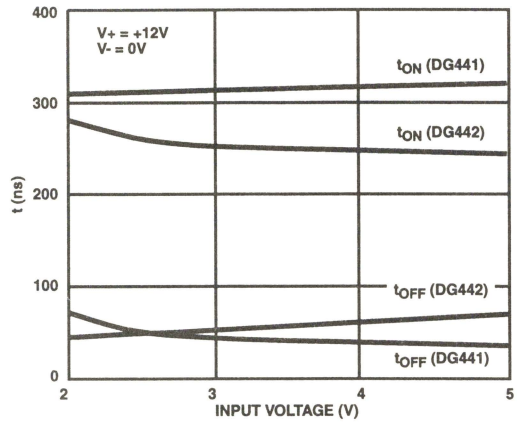


FIGURE 16. SWITCHING TIMES vs INPUT VOLTAGE

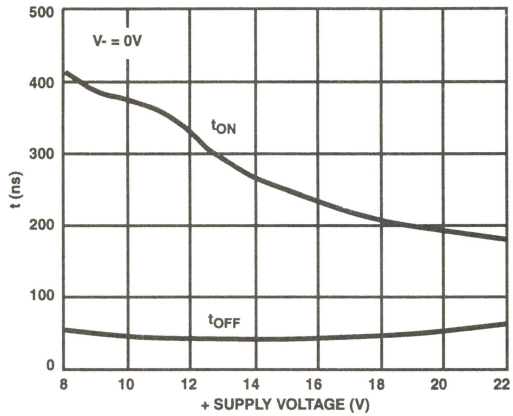


FIGURE 17. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG441)

Pin Descriptions

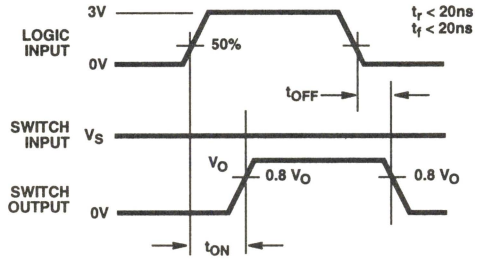
PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic Control for Switch 1
2	D_1	Drain (Output) Terminal for Switch 1
3	S_1	Source (Input) Terminal for Switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S_4	Source (Input) Terminal for Switch 4
7	D_4	Drain (Output) Terminal for Switch 4
8	IN_4	Logic Control for Switch 4
9	IN_3	Logic Control for Switch 3
10	D_3	Drain (Output) Terminal for Switch 3
11	S_3	Source (Input) Terminal for Switch 3
12	NC	No Internal Connection
13	V+	Positive Power Supply Terminal (Substrate)
14	S_2	Source (Input) Terminal for Switch 2
15	D_2	Drain (Output) Terminal for Switch 2
16	IN_2	Logic Control for Switch 2

TRUTH TABLE

LOGIC	V_{IN}	DG441	DG442
0	≤0.8V	ON	OFF
1	≥2.4V	OFF	ON

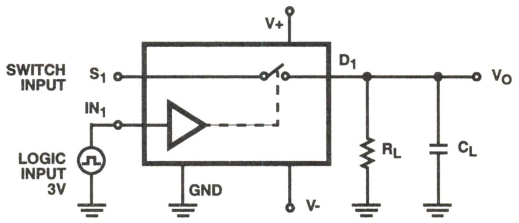
Test Circuits and Waveforms

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 18A.



Repeat test for Channels 2, 3 and 4.
For load conditions, see Specifications C_L (includes fixture and stray capacitance).

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 18B.

FIGURE 18. SWITCHING TIME

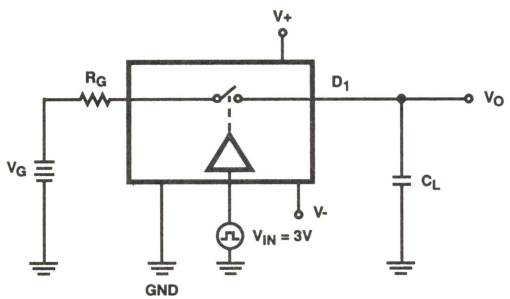


FIGURE 19A.

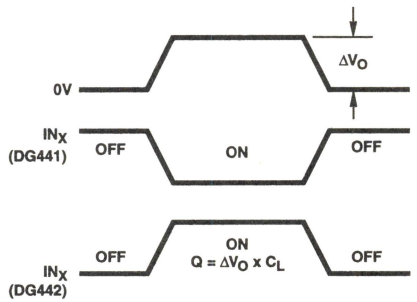


FIGURE 19B.

FIGURE 19. CHARGE INJECTION

Test Circuits (Continued)

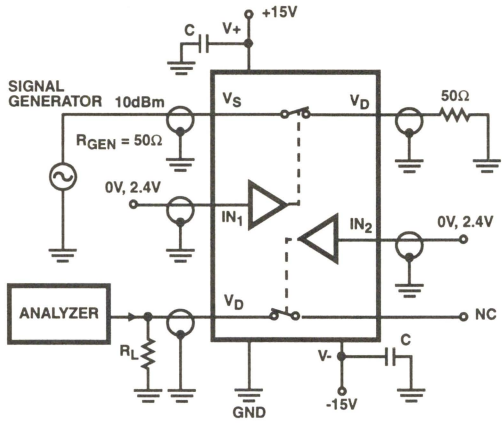


FIGURE 20. CROSSTALK

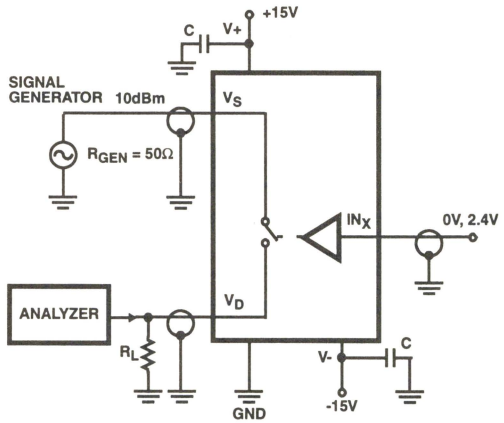


FIGURE 21. OFF ISOLATION

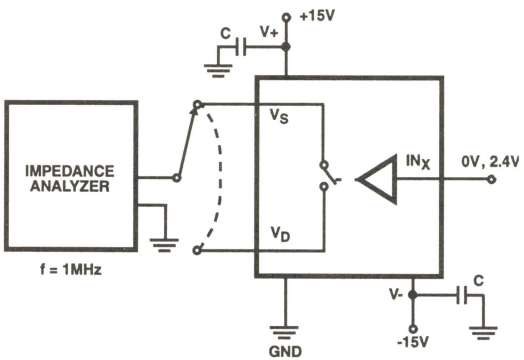
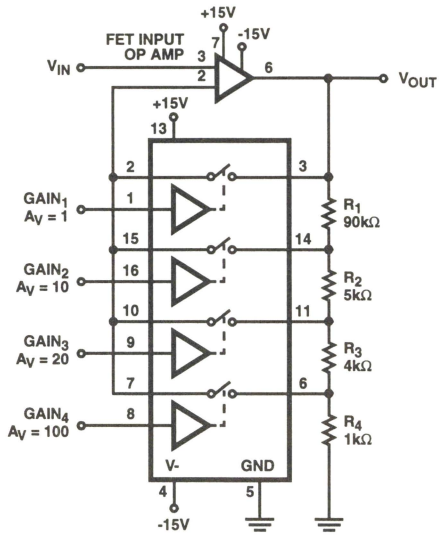


FIGURE 22. SOURCE/DRAIN CAPACITANCES

Applications

GAIN ERROR IS DETERMINED ONLY BY THE RESISTOR TOLERANCE. OP AMP OFFSET AND CMRR WILL LIMIT ACCURACY OF CIRCUIT



$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

WITH SW_4 CLOSED

FIGURE 23. PRECISION WEIGHTED RESISTOR PROGRAMMABLE GAIN AMPLIFIER

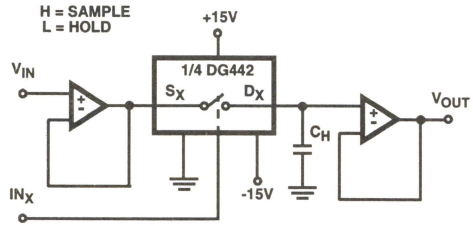


FIGURE 24. OPEN LOOP SAMPLE AND HOLD

Die Characteristics

DIE DIMENSIONS:

2160µm x 1760µm x 485µm ±25µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

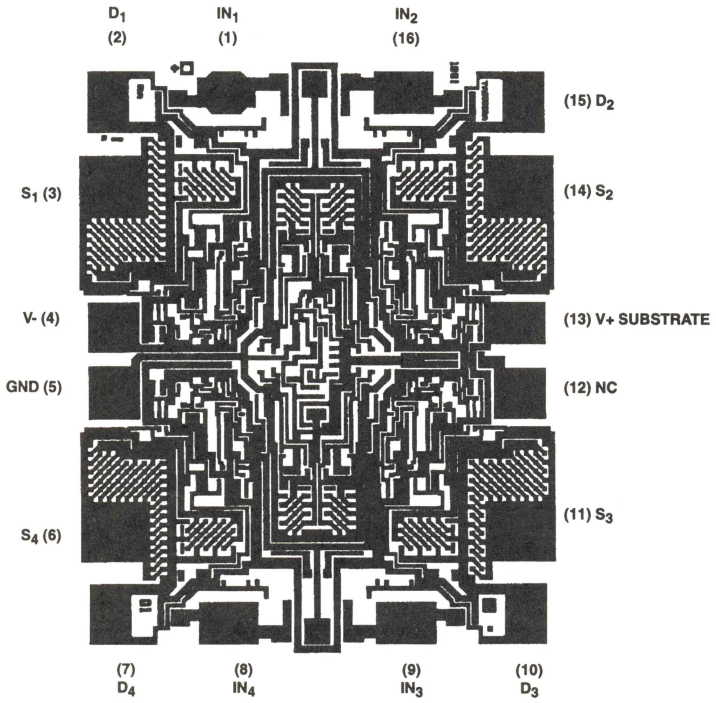
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG441, DG442



HARRIS SEMICONDUCTOR

DG444, DG445

Monolithic, Quad SPST, CMOS Analog Switches

August 1997

Features

- ON-Resistance (Max) 85Ω
- Low Power Consumption (P_D) . . . . . <35µW)
- Fast Switching Action
  - t_{ON} . . . . . <250ns
  - t_{OFF} (DG444) . . . . . <120ns
- Low Charge Injection
- Upgrade from DG211/DG212
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG444 and DG445 monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole single throw (SPST) analog switches and TTL and CMOS compatible digital inputs.

These switches feature lower analog ON resistance (<85Ω) and faster switch time (t_{ON} <250ns) compared to the DG211 and DG212. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG444 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling ±20V signals when operating with ±20V power supplies.

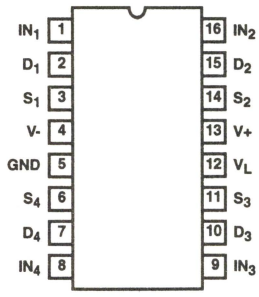
The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range. The switches in the DG444 and DG445 are identical, differing only in the polarity of the selection logic.

Ordering Information

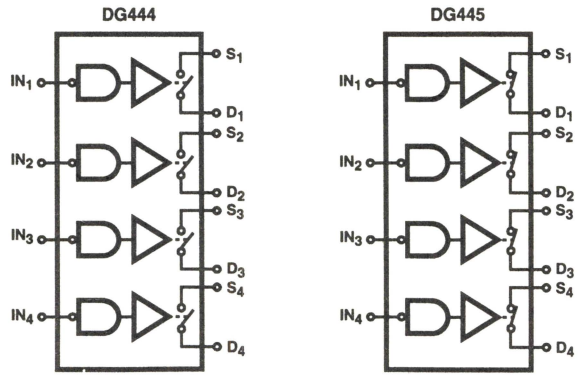
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG444DJ	-40 to 85	16 Ld PDIP	E16.3
DG444DY	-40 to 85	16 Ld SOIC	M16.15
DG445DJ	-40 to 85	16 Ld PDIP	E16.3
DG445DY	-40 to 85	16 Ld SOIC	M16.15

Pinout

DG444, DG445
(PDIP, SOIC)
TOP VIEW



Functional Diagrams

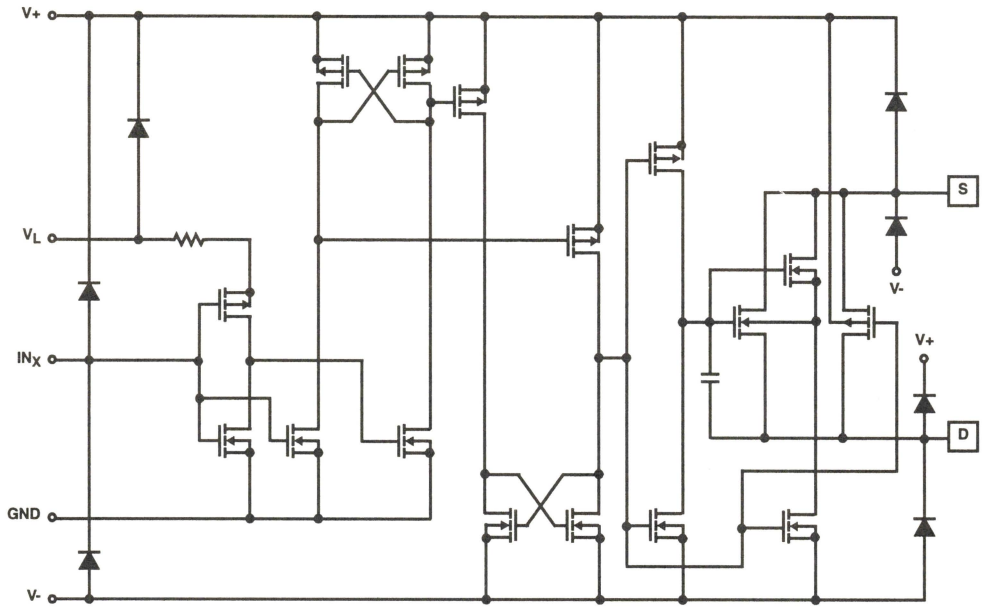


SWITCHES SHOWN FOR LOGIC "1" INPUT

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

File Number **3586.4**

Typical Schematic Diagram (One Channel)



Absolute Maximum Ratings

V+ to V- 44V
GND to V- 25V
V_L . . . . . (GND - 0.3V) to (V+) + 0.3V
Digital Inputs, V_S, V_D (Note 1) . . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Current, S or D (Pulsed 1ms, 10% Duty Cycle) 100mA

Operating Conditions

Temperature (D Suffix) . . . . . -40^oC to 85^oC
Voltage Range . . . . . ±20V (Max)
Temperature Range . . . . . -55^oC to 125^oC
Input Low Voltage . . . . . 0.8V (Max)
Input High Voltage . . . . . 2.4V (Min)
Input Rise and Fall Time . . . . . ≤20ns

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	100
SOIC Package	115

Maximum Junction Temperature (PDIP, SOIC) . . . . . 150^oC
Maximum Storage Temperature Range (D Suffix) . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:
1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (^oC)	D SUFFIX -40^oC TO 85^oC (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = ±10V, (See Figure 18)	25	-	120	250	ns
Turn-OFF Time, t_{OFF}						
DG444		25	-	110	140	ns
DG445		25	-	160	210	ns
Charge Injection, Q	C_L = 1nF, V_S = 0V, V_{GEN} = 0V, R_{GEN} = 0Ω	25	-	-1	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	60	-	dB
Crosstalk (Channel-to-Channel)	Any Other Channel Switches R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	100	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz	25	-	4	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	f = 1MHz	25	-	4	-	pF
Channel ON Capacitance, $C_{D(ON)}$ + $C_{S(ON)}$	V_{ANALOG} = 0	25	-	16	-	pF
DIGITAL CONTROL						
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-0.5	-0.00001	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-0.5	0.00001	0.5	µA
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = ∓10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V	25	-	50	85	Ω
		Full	-	-	100	Ω
Switch OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	25	-0.5	0.01	0.5	nA
		Hot	-5	-	5	nA
Switch OFF Leakage Current, $I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	25	-0.5	0.01	0.5	nA
		Hot	-5	-	5	nA

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
Channel ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$	V+ = 16.5V, V- = -16.5V $V_S = V_D = \pm 15.5V$	25	-0.5	0.08	0.5	nA
		Hot	-10	-	10	nA
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	25	-	0.001	1	µA
		Hot	-	-	5	µA
Negative Supply Current, I-		25	-1	-0.0001	-	µA
		Hot	-5	-	-	µA
Logic Supply Current, I_L		25	-	0.001	1	µA
		Hot	-	-	5	µA
Ground Current, I_{GND}		25	-1	-0.001	-	µA
		Hot	-5	-	-	µA

Electrical Specifications (Unipolar Supplies) Test Conditions: V+ = +12V, V- = 0V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = 8V, (See Figure 18)	25	-	300	450	ns
Turn-OFF Time, t_{OFF}		25	-	60	200	ns
Charge Injection, Q	C_L = 1nF, V_{GEN} = 6V, R_{GEN} = 0Ω	25	-	2	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = -10mA, V_D = 3V, 8V V+ = 10.8V, V_L = 5.25V	25	-	100	160	Ω
		Full	-	-	200	Ω
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 13.2V, V_{IN} = 0V or 5V	25	-	0.001	1	µA
		Full	-	-	5	µA
Negative Supply Current, I-	V_{IN} = 0V or 5V	25	-1	-0.0001	-	µA
		Full	-5	-	-	µA
Logic Supply Current, I_L	V_L = 5.25V, V_{IN} = 0V or 5V	25	-	0.001	1	µA
		Full	-	-	5	µA
Ground Current, I_{GND}	V_{IN} = 0V or 5V	25	-1	-0.001	-	µA
		Full	-5	-	-	µA

NOTES:

3. V_{IN} = input voltage to perform proper function.
4. Hot = as determined by the operating temperature suffix.
5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Typical Performance Curves

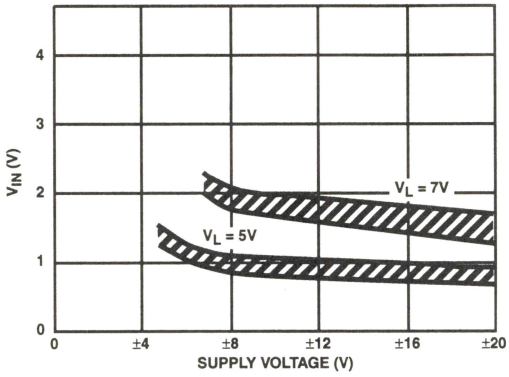


FIGURE 1. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

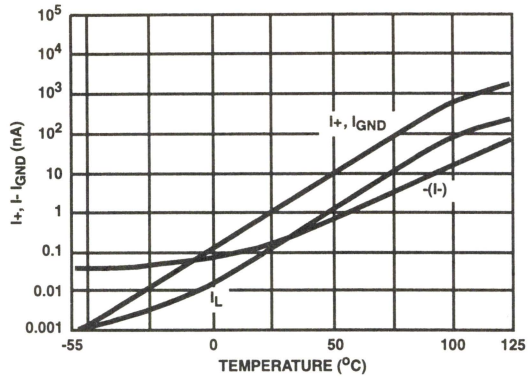


FIGURE 2. SUPPLY CURRENT vs TEMPERATURE

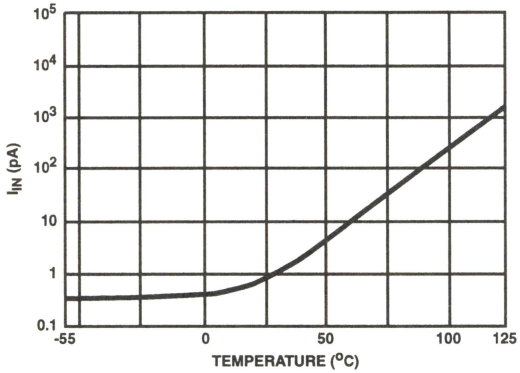


FIGURE 3. INPUT CURRENT vs TEMPERATURE

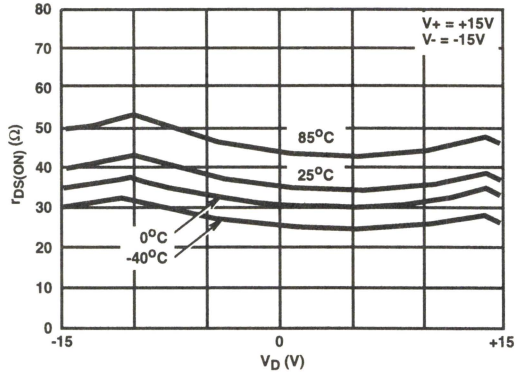


FIGURE 4. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

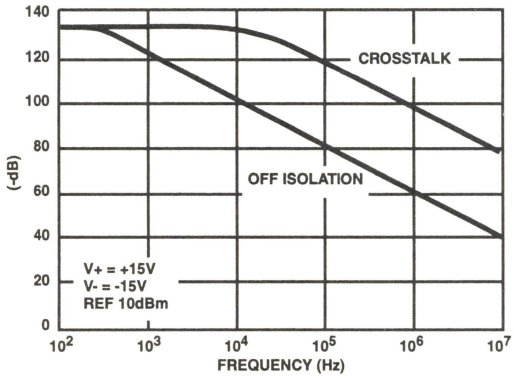


FIGURE 5. CROSSTALK AND OFF ISOLATION vs FREQUENCY

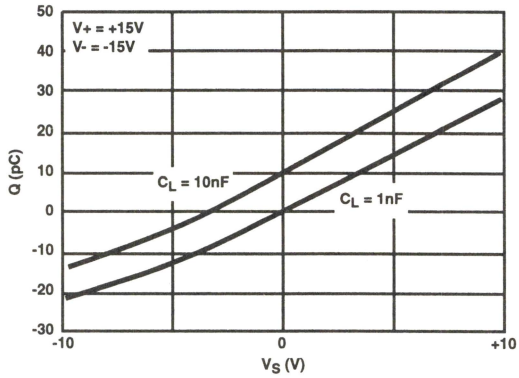


FIGURE 6. CHARGE INJECTION vs SOURCE VOLTAGE

Typical Performance Curves (Continued)

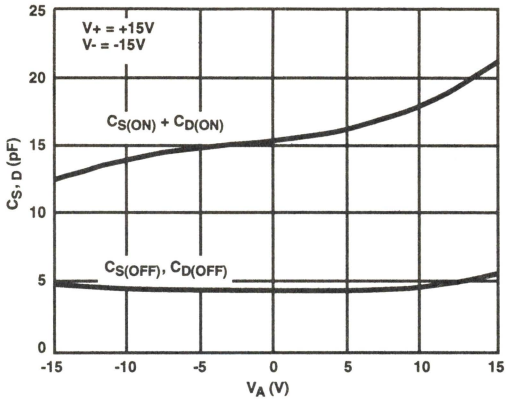


FIGURE 7. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

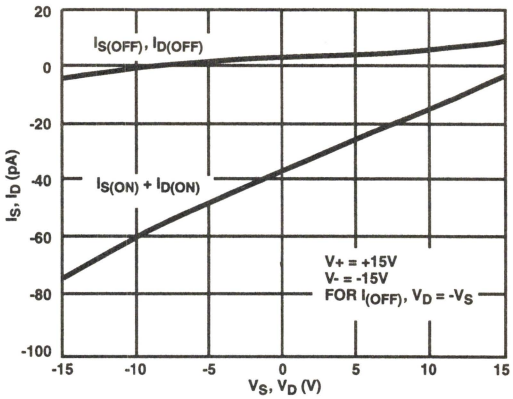


FIGURE 8. SOURCE/DRAIN LEAKAGE CURRENTS

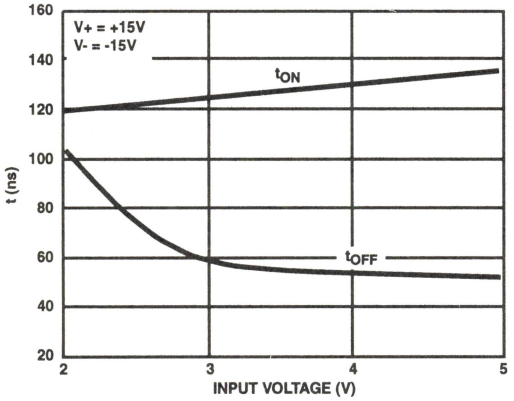


FIGURE 9. SWITCHING TIME vs INPUT VOLTAGE

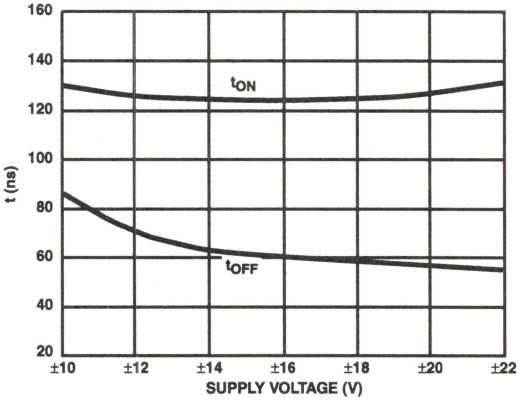


FIGURE 10. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG444)

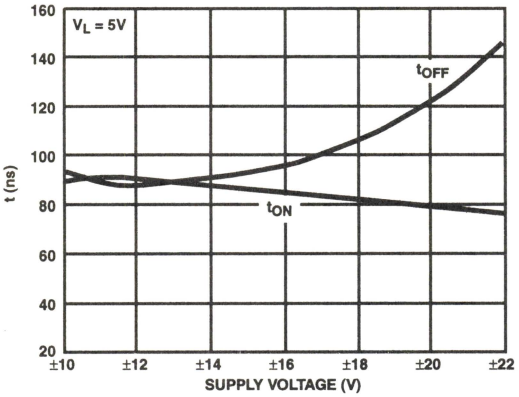


FIGURE 11. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG445)

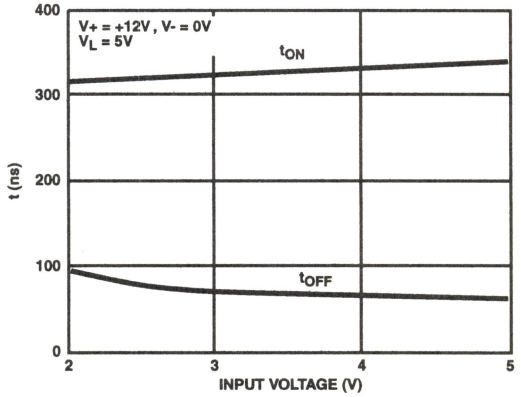


FIGURE 12. SWITCHING TIME vs INPUT VOLTAGE (DG444)

Typical Performance Curves (Continued)

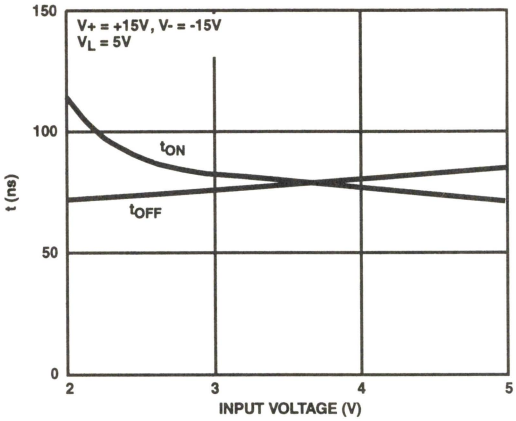


FIGURE 13. SWITCHING TIME vs INPUT VOLTAGE (DG445)

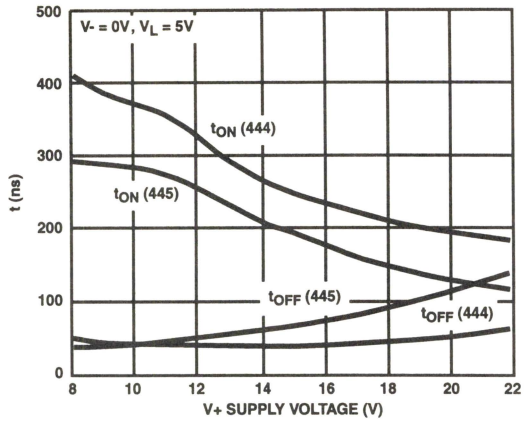


FIGURE 14. SWITCHING TIMES vs POWER SUPPLY VOLTAGE

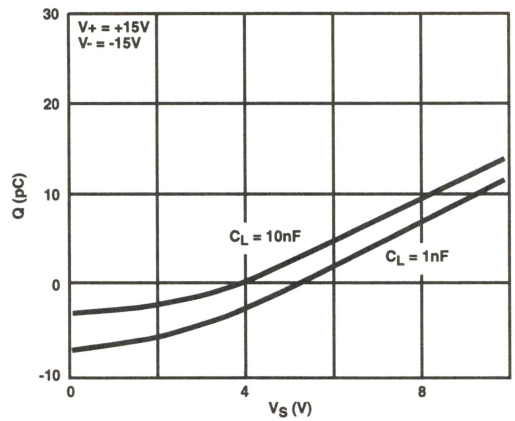


FIGURE 15. CHARGE INJECTION vs SOURCE VOLTAGE (SINGLE 12V SUPPLY)

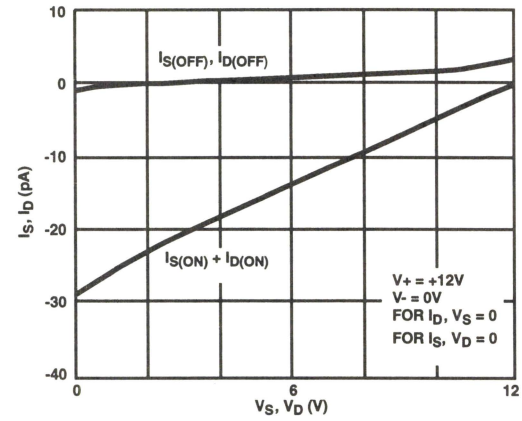


FIGURE 16. SOURCE/DRAIN LEAKAGE CURRENTS (SINGLE 12V SUPPLY)

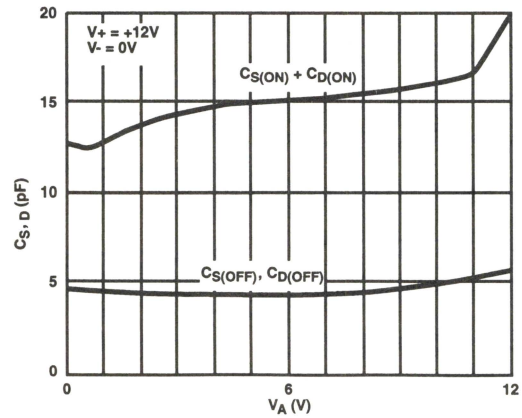


FIGURE 17. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

Pin Descriptions

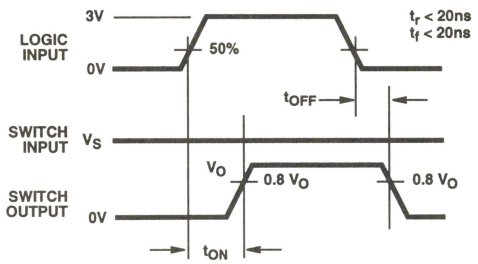
PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic Control for Switch 1
2	D_1	Drain (Output) Terminal for Switch 1
3	S_1	Source (Input) Terminal for Switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S_4	Source (Input) Terminal for Switch 4
7	D_4	Drain (Output) Terminal for Switch 4
8	IN_4	Logic Control for Switch 4
9	IN_3	Logic Control for Switch 3
10	D_3	Drain (Output) Terminal for Switch 3
11	S_3	Source (Input) Terminal for Switch 3
12	V_L	Logic Reference Voltage.
13	V+	Positive Power Supply Terminal (Substrate)
14	S_2	Source (Input) Terminal for Switch 2
15	D_2	Drain (Output) Terminal for Switch 2
16	IN_2	Logic Control for Switch 2

TRUTH TABLE

LOGIC	V_{IN}	DG444	DG445
0	≤0.8V	ON	OFF
1	≥2.4V	OFF	ON

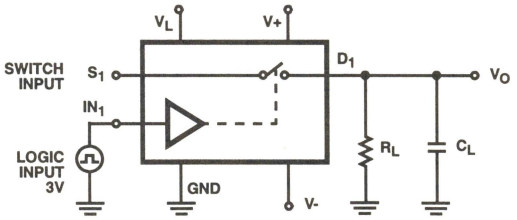
Test Circuits and Waveforms

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 18A.



Repeat test for Channels 2, 3 and 4.
For load conditions, see Specifications C_L (includes fixture and stray capacitance).

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 18B.

FIGURE 18. SWITCHING TIME

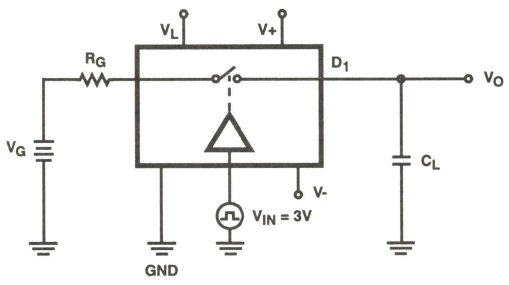


FIGURE 19A.

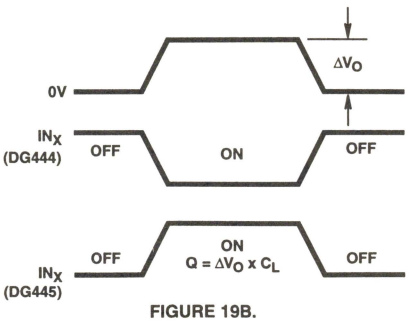


FIGURE 19B.

FIGURE 19. CHARGE INJECTION

Test Circuits and Waveforms (Continued)

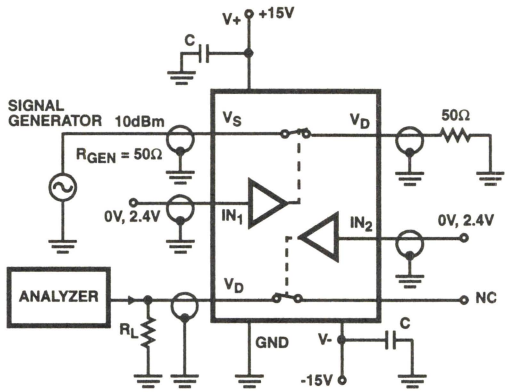


FIGURE 20. CROSSTALK

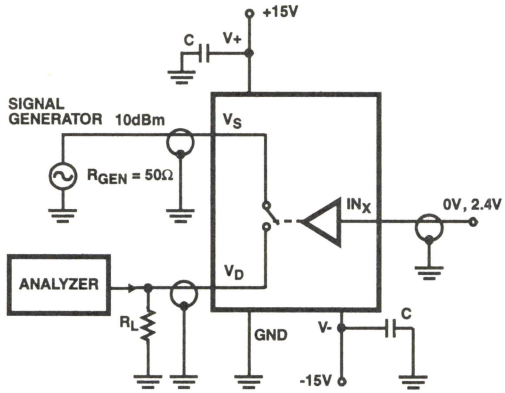


FIGURE 21. OFF ISOLATION

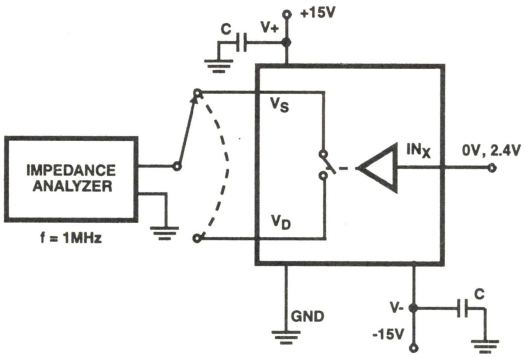
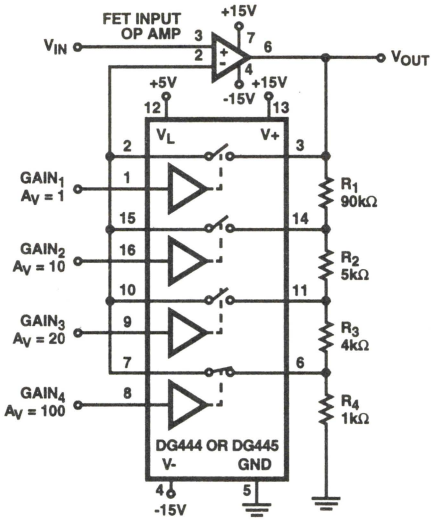


FIGURE 22. SOURCE/DRAIN CAPACITANCES

Typical Applications



GAIN ERROR IS DETERMINED ONLY BY THE RESISTOR TOLERANCE, OP AMP OFFSET AND CMRR WILL LIMIT ACCURACY OR CIRCUIT

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

WITH SW_4 CLOSED

FIGURE 23. PRECISION WEIGHTED RESISTOR PROGRAMMABLE GAIN AMPLIFIER

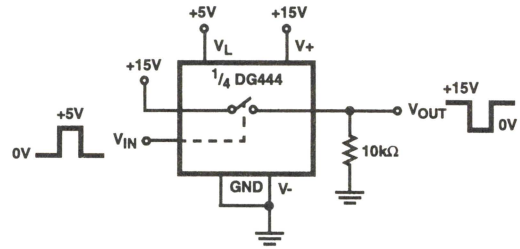


FIGURE 24. LEVEL SHIFTER

Die Characteristics

DIE DIMENSIONS:

2160µm x 1760µm x 485 ±25µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

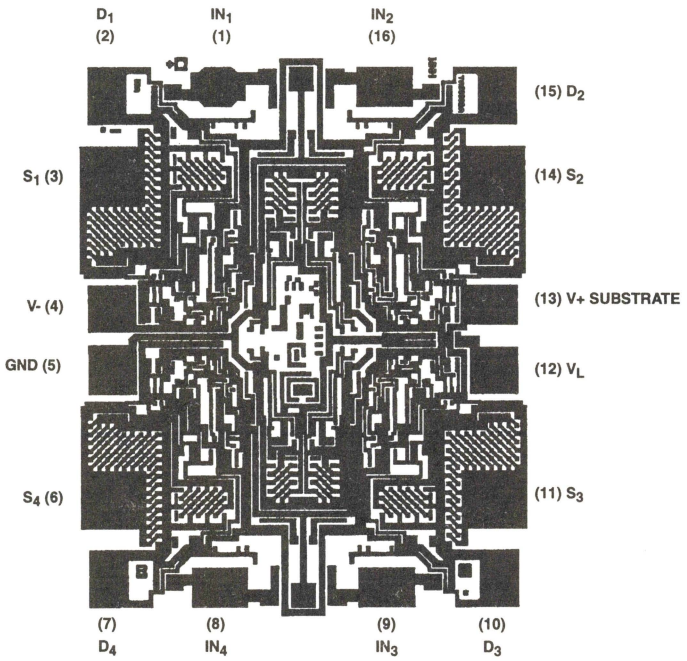
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG444, DG445



HARRIS SEMICONDUCTOR

HI-200, HI-201

August 1997

Dual/Quad SPST, CMOS Analog Switches

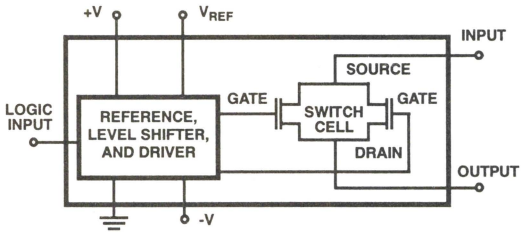
Features

- Analog Voltage Range . . . . . ±15V
- Analog Current Range 80mA
- Turn-On Time 240ns
- Low r_{ON} 55Ω
- Low Power Dissipation 15mW
- TTL/CMOS Compatible

Applications

- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks

Functional Diagram



Description

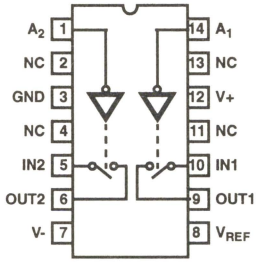
HI-200/HI-201 are monolithic devices comprising independently selectable SPST switches which feature fast switching speeds (HI-200 240ns, and HI-201 185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltage up to the supply rails and for signal current up to 80mA. Rugged DI construction eliminates latch-up and substrate SCR failure modes.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200/HI-201 are ideal components for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and operational amplifier gain switching networks.

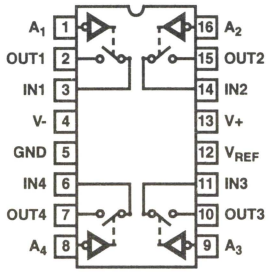
HI-200 is a dual SPST CMOS analog switch available in DIP and (TO-99) metal cans and is pin compatible with other available "200 series" switches. For MIL-STD-883 compliant parts, request the HI-200/883 data sheet.

Pinouts

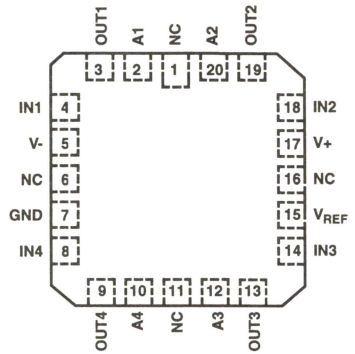
HI-200 (CERDIP, PDIP, SOIC)
TOP VIEW



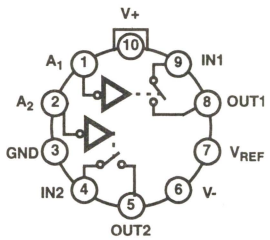
HI-201 (CERDIP, PDIP, SOIC)
TOP VIEW



HI-201 (PLCC, CLCC)
TOP VIEW



HI-200 (METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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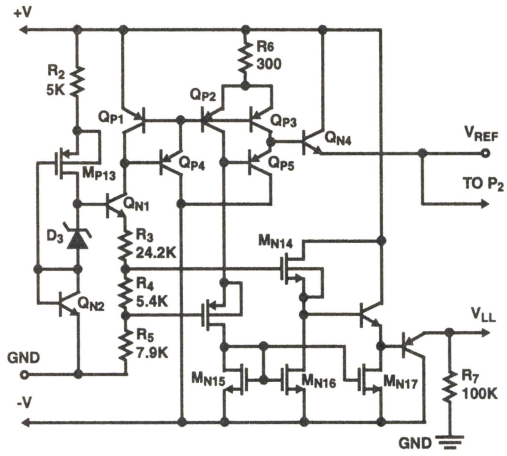
File Number **3121.2**

Ordering Information

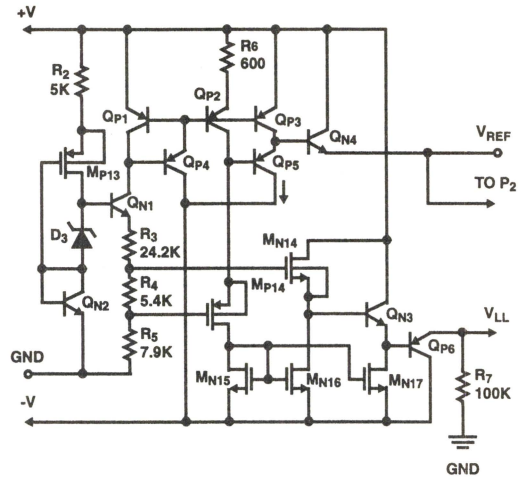
PART NUMBER	TEMPERATURE RANGE (°C)	PACKAGE	PKG. NO.
HI2-0200-5	0 to 75	10 Pin Metal Can	T10.B
HI1-0200-5	0 to 75	14 Ld CERDIP	F14.3
HI2-0200-4	-25 to 85	10 Pin Metal Can	T10.B
HI3-0200-5	0 to 75	14 Ld PDIP	E14.3
HI1-0200-7	0 to 75 + 96 Hr. Burn-In	14 Ld CERDIP	F14.3
HI1-0200-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0200-4	-25 to 85	14 Ld CERDIP	F14.3
HI2-0200-2	-55 to 125	10 Pin Metal Can	T10.B
HI9P0200-5	0 to 75	14 Ld SOIC	M14.15
HI1-0200/883	-55 to 125	14 Ld CERDIP	F14.3
HI2-0200/883	-55 to 125	10 Pin Metal Can	T10.B
HI1-0201-7	0 to 75 + 96 Hr. Burn-In	16 Ld CERDIP	F16.3
HI1-0201-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0201-4	-25 to 85	16 Ld CERDIP	F16.3
HI4P0201-5	0 to 75	20 Ld PLCC	N20.35
HI9P0201-5	0 to 75	16 Ld SOIC	M16.15
HI9P0201-9	-40 to 85	16 Ld SOIC	M16.15
HI1-0201-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-0201-5	0 to 75	16 Ld PDIP	E16.3
HI1-0201/883	-55 to 125	16 Ld CERDIP	F16.3
HI4-0201/883	-55 to 125	20 Ld CLCC	J20.A

Schematic Diagrams

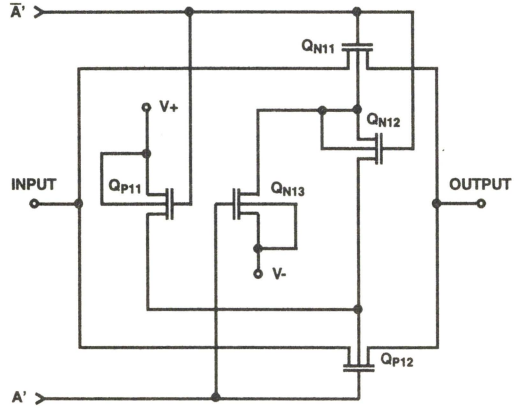
TTL/CMOS REFERENCE CIRCUIT V_{REF} CELL
HI-200



TTL/CMOS REFERENCE CIRCUIT V_{REF} CELL
HI-201

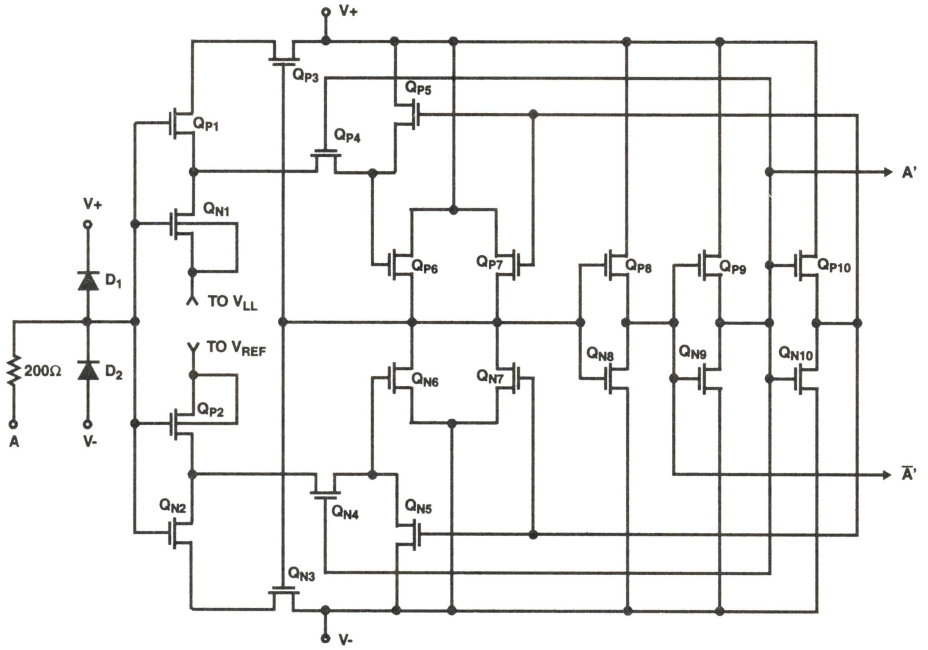


SWITCH CELL



Schematic Diagrams (Continued)

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

Supply Voltage . . . . . 44V (±22)
V_{REF} to Ground . . . . . 20V, -5V
Digital Input Voltage . . . . . $+V_{SUPPLY}$ 4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage (One Switch). . . . . $+V_{SUPPLY}$ 2.0V
$-V_{SUPPLY}$ -2.0V

Operating Conditions

Temperature Ranges
HI-200-2, HI-201-2 . . . . . -55°C to 125°C
HI-200-4, HI-201-4 . . . . . -25°C to 85°C
HI-200-5, HI-201-5 . . . . . 0°C to 75°C
HI200-9, HI201-9 . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld CERDIP Package (/883 Versions)	80	24
14 Ld CERDIP Package (Non /883 Versions)	95	40
16 Ld CERDIP Package (/883 Versions)	75	20
16 Ld CERDIP Package (Non /883 Versions)	90	35
PLCC Package	80	N/A
PDIP Package	100	N/A
14 Ld SOIC Package	120	N/A
16 Ld SOIC Package	115	N/A
10 Pin Metal Can Package (HI-200 Only)	160	75
20 Ld CLCC Package (HI-201 Only)	65	13

Maximum Storage Temperature . . . . . -65°C to 150°C
Maximum Junction Temperature (Hermetic) . . . . . 175°C
Maximum Junction Temperature (Plastic) . . . . . 150°C
Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C
(PLCC and SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Characteristics

Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-200, HI-201-2/883			HI-200, HI201 -4, -5, -7, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Switch On Time, t_{ON}									
HI-200		25	-	240	500	-	240	-	ns
HI-201		25	-	185	500	-	185	-	ns
		Full	-	1000	-	-	1000	-	ns
Switch Off Time, t_{OFF}									
HI-200		25	-	330	500	-	500	-	ns
HI-201		25	-	220	500	-	220	-	ns
		Full	-	1000	-	-	1000	-	ns
"Off Isolation"	(Note 4)								
HI-200		25	-	70	-	-	70	-	dB
HI-201		25	-	80	-	-	80	-	dB
Input Switch Capacitance, $C_{S(OFF)}$		25	-	5.5	-	-	5.5	-	pF
Output Switch Capacitance, $C_{D(OFF)}$		25	-	5.5	-	-	5.5	-	pF
Output Switch Capacitance, $C_{D(ON)}$		25	-	11	-	-	11	-	pF
Digital Input Capacitance, C_A		25	-	5	-	-	5	-	pF
Drain-to-Source Capacitance, $C_{DS(OFF)}$		25	-	0.5	-	-	0.5	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL}		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH}		Full	2.4	-	-	2.4	-	-	V
Input Leakage Current (High or Low), I_A	(Note 2)	Full	-	-	1.0	-	-	1.0	µA
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range, V_S		Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON}	(Note 1)	25	-	55	70	-	55	80	Ω
		Full	-	80	100	-	72	100	Ω

Electrical Characteristics Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-200, HI-201-2/883			HI-200, HI201 -4, -5, -7, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Off Input Leakage Current, $I_{S(OFF)}$	(Note 6)	25	-	1	5	-	1	50	nA
HI-200		Full	-	100	500	-	10	500	nA
Off Output Leakage Current, $I_{D(OFF)}$	(Note 6)	25	-	1	5	-	1	50	nA
HI-200		Full	-	100	500	-	10	500	nA
On Leakage Current, $I_{D(ON)}$	(Note 6)	25	-	1	5	-	1	50	nA
HI-200		Full	-	100	500	-	10	500	nA
$I_{S(OFF)}$		25	-	2	5	-	2	50	nA
HI-201		Full	-	-	500	-	-	250	nA
$I_{D(OFF)}$		25	-	2	5	-	2	50	nA
HI-201		Full	-	35	500	-	35	250	nA
$I_{D(ON)}$		25	-	2	5	-	2	50	nA
HI-201		Full	-	-	500	-	-	250	nA
POWER REQUIREMENTS (Note 5)									
Power Dissipation, P_D		25	-	15	-	-	15	-	mW
		Full	-	-	60	-	-	60	mW
Current, I+		25	-	0.5	-	-	0.5	-	mA
		Full	-	-	2.0	-	-	2.0	mA
Current, I-		25	-	0.5	-	-	0.5	-	mA
		Full	-	-	2.0	-	-	2.0	mA

NOTES:

2. V_{OUT} = ±10V, I_{OUT} = 1mA.
3. Digital Inputs are MOS gates: typical leakage is < 1nA.
4. V_{AH} = 4V.
5. V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = $3V_{RMS}$, f = 100kHz.
6. V_A = +3V or V_A = 0V for Both Switches.
7. Refer to Leakage Current Measurements (Figure 4).

Performance Curves and Test Circuits T_A = 25°C, V_{SUPPLY} = 15V, V_{AH} = 2.4V, V_{AL} = 0.8V and V_{REF} = Open

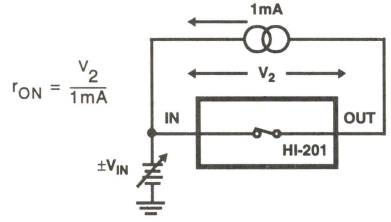


FIGURE 1. ON RESISTANCE vs ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE

Performance Curves and Test Circuits $T_A = 25^oC$, $V_{SUPPLY} = 15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$ and V_{REF} = Open (Continued)

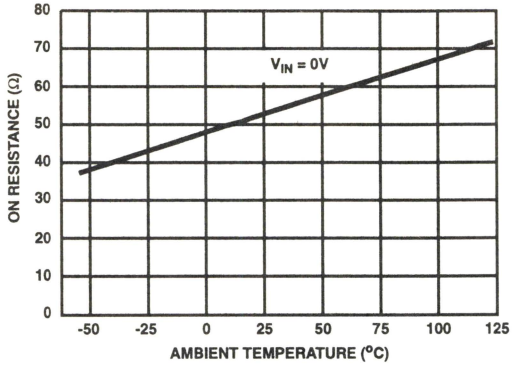


FIGURE 2. ON RESISTANCE vs TEMPERATURE

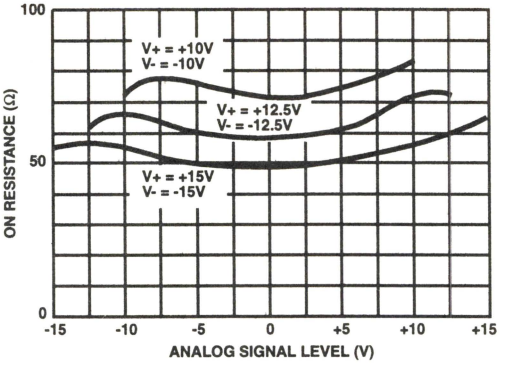


FIGURE 3. HI-201 ON RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

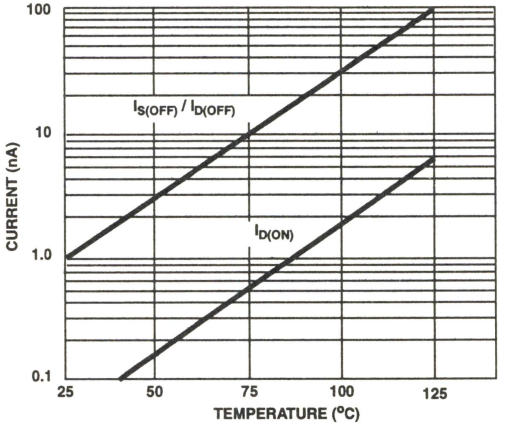


FIGURE 4A. HI-201 SWITCH LEAKAGE CURRENT vs TEMPERATURE

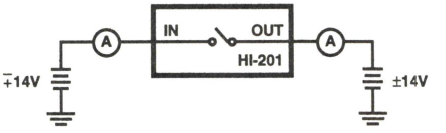


FIGURE 4B. OFF LEAKAGE CURRENT vs TEMPERATURE

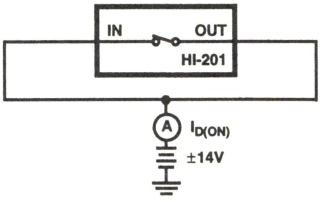


FIGURE 4C. ON LEAKAGE CURRENT vs TEMPERATURE

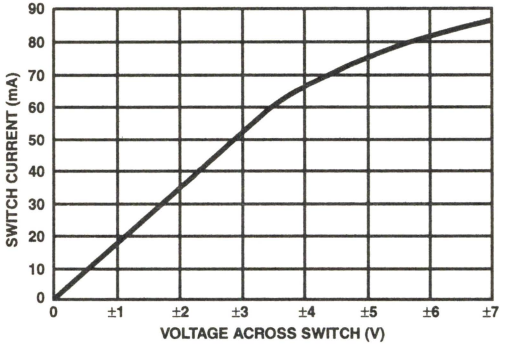


FIGURE 5A.

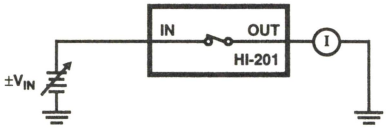


FIGURE 5B.

FIGURE 5. SWITCH CURRENT vs VOLTAGE

Switching Waveforms

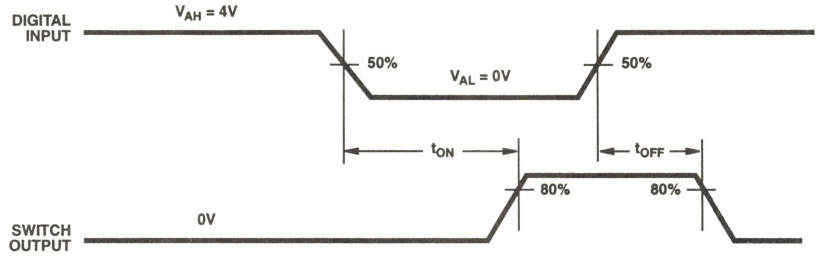
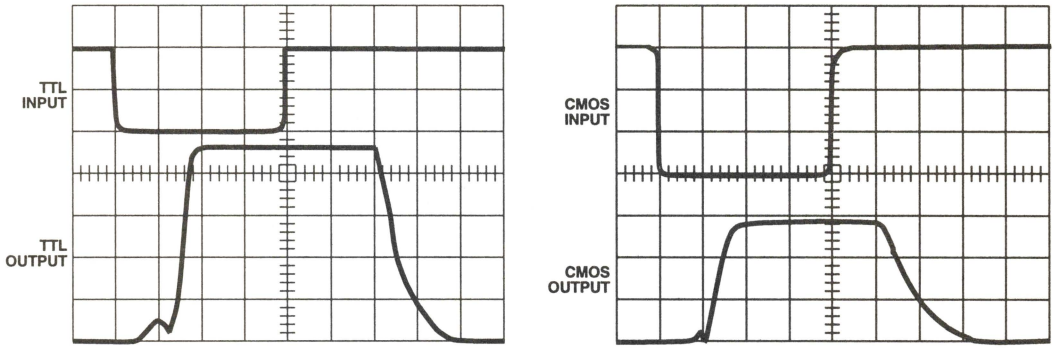


FIGURE 6. LOGIC "0" = SWITCH ON



t_{ON}, t_{OFF} (TTL INPUT), V_{IN} = +4V
Vertical: 2V/Div.
Horizontal: 100ns/Div.

t_{ON}, t_{OFF} (TTL INPUT), V_{IN} = +15V
Vertical: 5V/Div.
Horizontal: 100ns/Div.

FIGURE 7. TTL INPUT

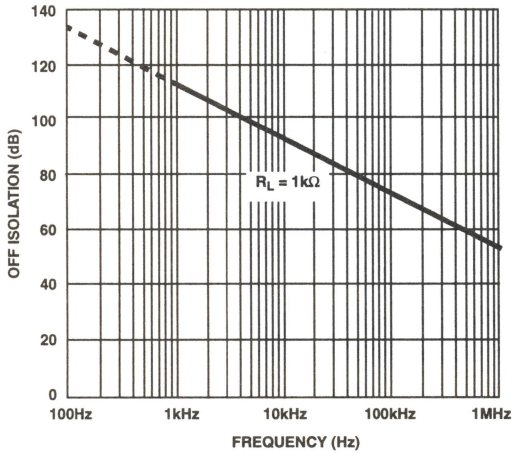


FIGURE 8. OFF ISOLATION vs FREQUENCY

For more information see Application Notes AN520, AN521, AN531, AN532 and AN557.

Single Supply

The switch operation of the HI-200/201 is dependent upon an internally generated switching threshold voltage optimized for ±15V power supplies. The HI-200/201 does not provide the necessary internal switching threshold in a single supply system. Therefore, if single supply operation is required, the HI-300 series of switches is recommended. The HI-300 series will remain operational to a minimum +5V single supply.

Switch performance will degrade as power supply voltage is reduced from optimum levels (±15V). So it is recommended that a single supply design be thoroughly evaluated to ensure that the switch will meet the requirements of the application.

For further information see Application Notes AN520, AN521, AN531, AN532, AN543 and AN557.

Die Characteristics

DIE DIMENSIONS:

54 mils x 79 mils x 19 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

PASSIVATION:

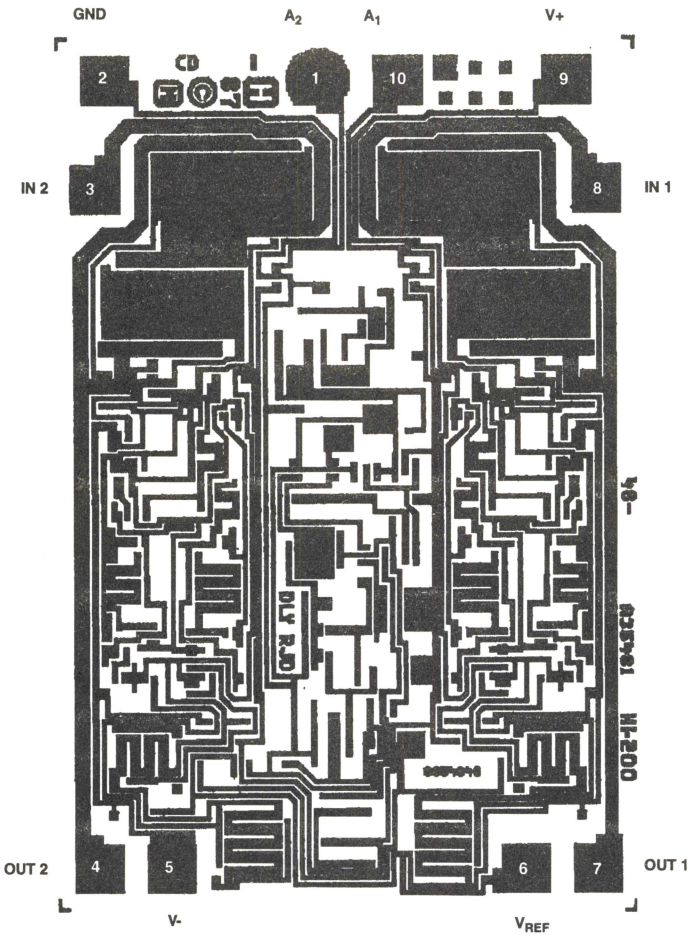
Type: Nitride over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

2×10^5 A/cm^2 at 25mA

Metallization Mask Layout

HI-200



Die Characteristics

DIE DIMENSIONS:

81 mils x 85 mils x 19 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

PASSIVATION:

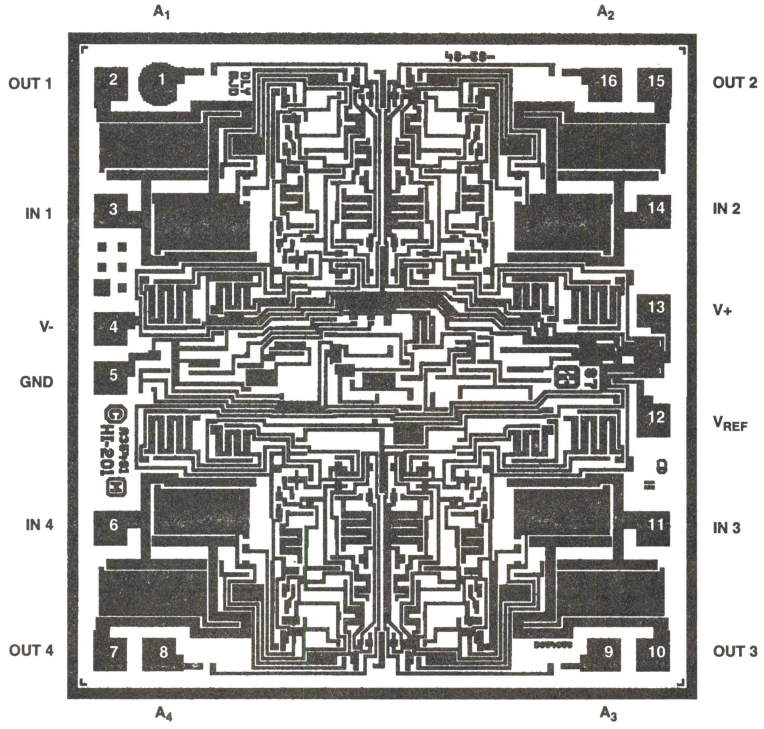
Type: Nitride over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

2×10^5 A/cm^2 at 25mA

Metallization Mask Layout

HI-201



HARRIS SEMICONDUCTOR

HI-201HS

High Speed, Quad SPST, CMOS Analog Switch

August 1997

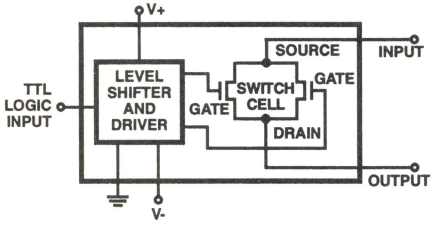
Features

- Fast Switching Times
  - t_{ON} 30ns
  - t_{OFF} 40ns
- Low "ON" Resistance 30Ω
- Pin Compatible with Standard HI-201
- Wide Analog Voltage Range (±15V Supplies) ..... ±15V
- Low Charge Injection (±15V Supplies) 10pC
- TTL Compatible
- Symmetrical Switching Analog Current Range .. 80mA

Applications

- High Speed Multiplexing
- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks
- Integrator Reset Circuits

Functional Diagram



LOGIC	SWITCH
0	ON
1	OFF

Description

The HI-201HS is a monolithic CMOS Analog Switch featuring very fast switching speeds and low ON resistance. The integrated circuit consists of four independently selectable SPST switches and is pin compatible with the industry standard HI-201 switch.

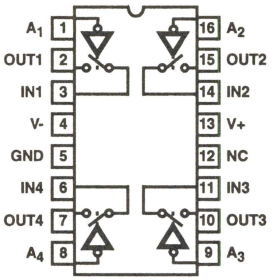
Fabricated using silicon-gate technology and the Harris Dielectric Isolation process, this TTL compatible device offers improved performance over previously available CMOS analog switches. Featuring maximum switching times of 50ns, low ON resistance of 50Ω maximum, and a wide analog signal range, the HI-201HS is designed for any application where improved switching performance, particularly switching speed, is required. (A more detailed discussion on the design and application of the HI-201HS can be found in Application Note AN543.)

Ordering Information

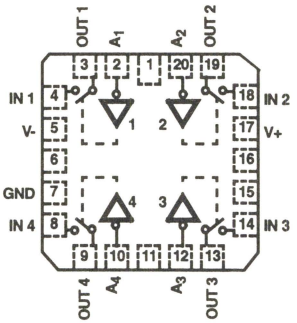
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0201HS-5	0 to 75	16 Ld CERDIP	F16.3
HI3-0201HS-4	-25 to 85	16 Ld PDIP	E16.3
HI1-0201HS-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0201HS-4	-25 to 85	16 Ld CERDIP	F16.3
HI4P0201HS-5	0 to 75	20 Ld PLCC	N20.35
HI3-0201HS-5	0 to 75	16 Ld PDIP	E16.3
HI1-0201HS-7	0 to 75	16 Ld CERDIP	F16.3
HI4-0201HS/883	-55 to 125	20 Ld CLCC	J20.A
HI9P0201HS-5	0 to 75	16 Ld SOIC	M16.3
HI9P0201HS-9	-40 to 85	16 Ld SOIC	M16.3
HI1-0201HS/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-0201HS-8	-55 to 125	16 Ld CERDIP	F16.3

Pinouts

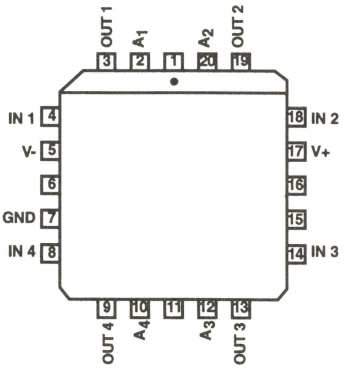
HI-201HS (CERDIP, PDIP, SOIC)
TOP VIEW



HI201HS (CLCC)
TOP VIEW



HI201HS (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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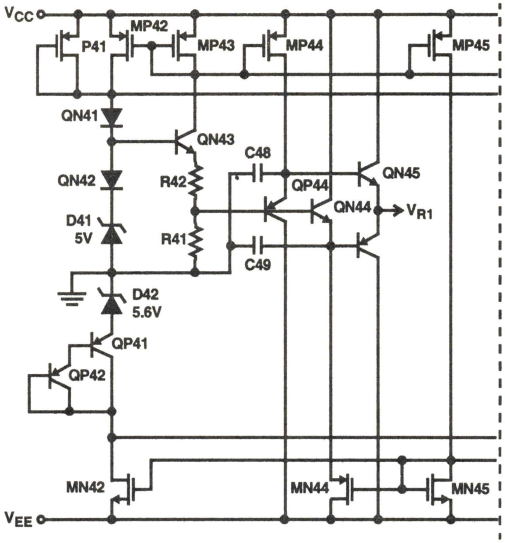
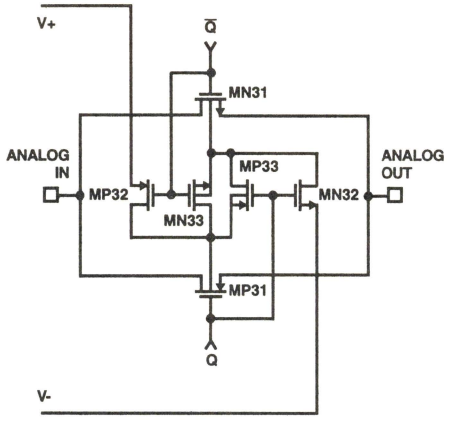
File Number **3123.1**

Schematic Diagrams

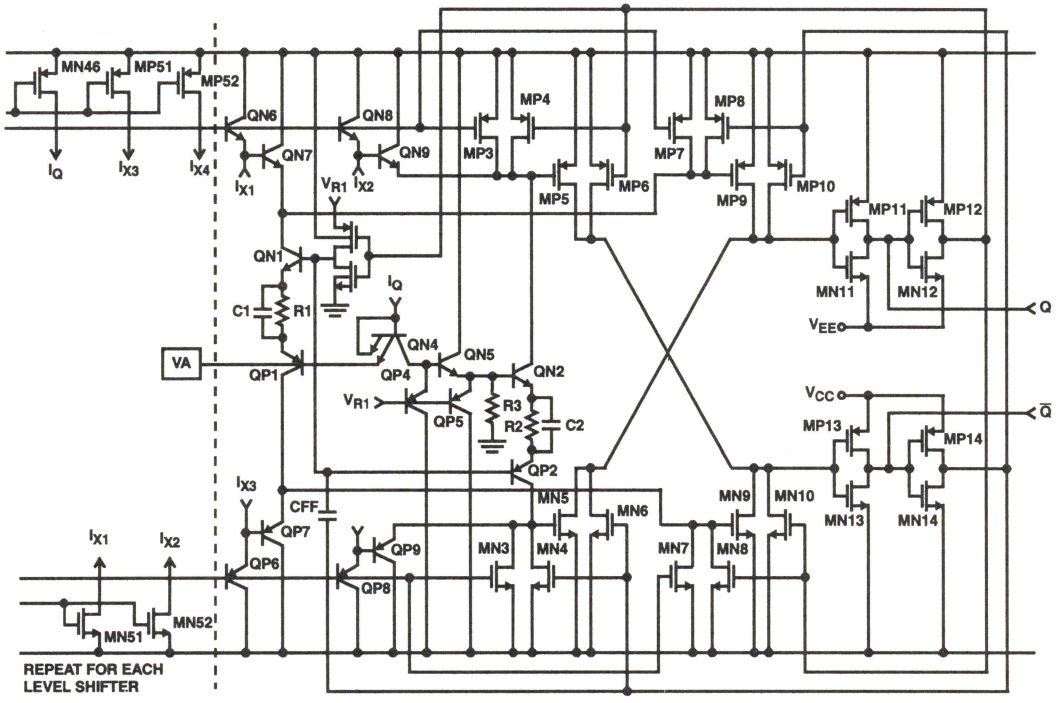
TTL/CMOS REFERENCE CIRCUIT



SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

Supply Voltage (Between Pins 4 and 13) 36V
Digital Input Voltage (Pins 1, 8, 9, 16) . . . . . (V+) +4V, (V-) -4V
Analog Input Voltage (One Switch) . . . . . (V+) +2.0V
Pins 2, 3, 6, 7, 10, 11, 14, 15 . . . . . (V-) -2.0V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 50mA
Continuous Current Any Terminal (Except S or D) 25mA

Operating Conditions

Temperature Ranges
HI-201HS-2,-8 . . . . . $-55^{o}C$ to $125^{o}C$
HI-201HS-4 . . . . . $-25^{o}C$ to $85^{o}C$
HI-201HS-5,-7 . . . . . $0^{o}C$ to $75^{o}C$
HI-201HS-9 . . . . . $-40^{o}C$ to $85^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{o}C/W$)	θ_{JC} ($^{o}C/W$)
CERDIP Package	80	30
CLCC Package	65	14
PDIP Package	100	N/A
PLCC Package	80	N/A
SOIC Package	100	N/A

Maximum Junction Temperature
Ceramic Package . . . . . $175^{o}C$
Plastic Package . . . . . $150^{o}C$
Maximum Storage Temperature . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(SOIC, PLCC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, GND = 0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	HI-201HS-2/-8			HI-201HS-5/-4/-9/-7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
t_{ON}, Switch On Time	(Note 3)	25	-	30	50	-	30	50	ns
t_{OFF1}, Switch Off Time	(Note 3)	25	-	40	50	-	40	50	ns
t_{OFF2}, Switch Off Time	(Note 3)	25	-	150	-	-	150	-	ns
Output Settling Time 0.1%		25	-	180	-	-	180	-	ns
"Off Isolation"	(Note 4)	25	-	72	-	-	72	-	dB
Crosstalk	(Note 5)	25	-	86	-	-	86	-	dB
Charge Injection	(Note 6)	25	-	10	-	-	10	-	pC
$C_{S(OFF)}$, Input Switch Capacitance		25	-	10	-	-	10	-	pF
$C_{D(OFF)}$, Output Switch Capacitance		25	-	10	-	-	10	-	pF
$C_{D(ON)}$, Output Switch Capacitance		25	-	30	-	-	30	-	pF
C_A, Digital Input Capacitance		25	-	18	-	-	18	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance		25	-	0.5	-	-	0.5	-	pF
DIGITAL INPUT CHARACTERISTICS									
V_{AL}, Input Low Threshold		Full	-	-	0.8	-	-	0.8	V
V_{AH}, Input High Threshold		25	2.0	-	-	2.0	-	-	V
		Full	2.4	-	-	2.4	-	-	V
I_{AL}, Input Leakage Current (Low)		25	-	-200	-	-	-200	-	µA
		Full	-	-	-500	-	-	-500	µA
I_{AH}, Input Leakage Current (High)	V_{AH} = 4.0V	25	-	20	-	-	20	-	µA
		Full	-	-	+40	-	-	+40	µA
ANALOG SWITCH CHARACTERISTICS									
V_S, Analog Signal Range		Full	-15	-	+15	-15	-	+15	V
r_{ON}, On Resistance	(Note 2)	25	-	30	50	-	30	50	Ω
		Full	-	-	75	-	-	75	Ω
r_{ON}, Match		25	-	3	-	-	3	-	%

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, GND = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-201HS-2/-8			HI-201HS-5/-4/-9/-7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{S(OFF)}$, Off Input Leakage Current		25	-	0.3	10	-	0.3	10	nA
		Full	-	-	100	-	-	50	nA
$I_{D(OFF)}$, Off Output Leakage Current		25	-	0.3	10	-	0.3	10	nA
		Full	-	-	100	-	-	50	nA
$I_{D(ON)}$, On Leakage Current		25	-	0.1	10	-	0.1	10	nA
		Full	-	-	100	-	-	50	nA
POWER SUPPLY CHARACTERISTICS (Note 7)									
P_D, Power Dissipation		25	-	120	-	-	120	-	mW
		Full	-	-	240	-	-	240	mW
I+, Current (Pin 13)		25	-	4.5	-	-	4.5	-	mA
		Full	-	-	10.0	-	-	10.0	mA
I-, Current (Pin 4)		25	-	3.5	-	-	3.5	-	mA
		Full	-	-	6	-	-	6	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = 1mA.
3. R_L = 1kΩ, C_L = 35pF, V_{IN} = +10V, V_A = +3V. (See Switching Waveforms).
4. V_A = 3V, R_L = 1kΩ, C_L = 10pF, V_{IN} = $3V_{RMS}$, f = 100kHz.
5. V_A = 3V, R_L = 1kΩ, V_{IN} = $3V_{RMS}$, f = 100kHz.
6. C_L = 1000pF, V_{IN} = 0V, R_{IN} = 0V, $\Delta Q = C_L \times \Delta V_O$.
7. V_A = 3V or V_A = 0 for all switches.

Switching Waveforms

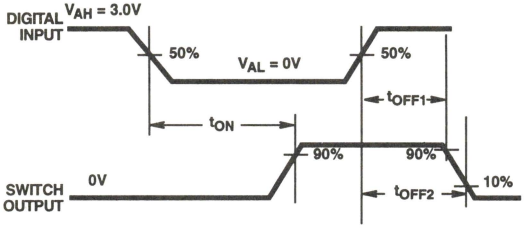
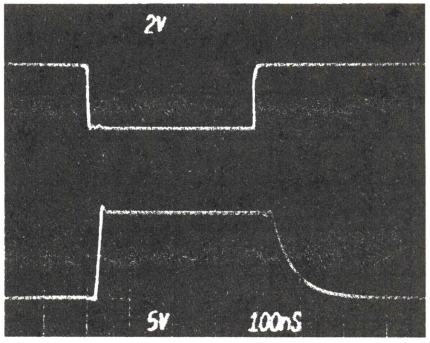


FIGURE 1A.



TOP: TTL Input (2V/Div.) BOTTOM: Output (5V/Div.)
HORIZONTAL: 100ns/Div.

FIGURE 1B.

FIGURE 1. SWITCH t_{ON} AND t_{OFF} TIMES

Typical Performance Curves

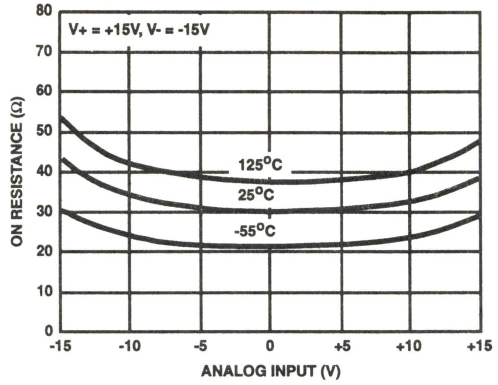


FIGURE 2. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL AND TEMPERATURE

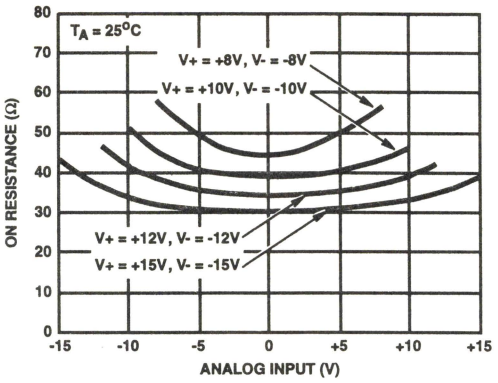


FIGURE 3. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

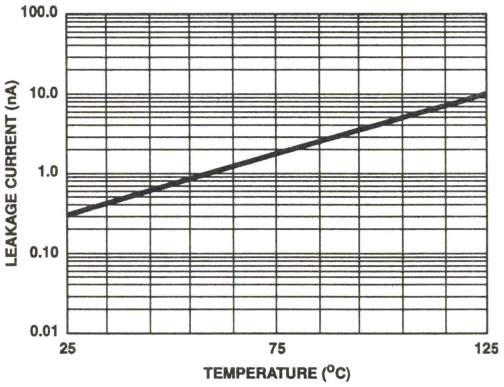


FIGURE 4. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE†

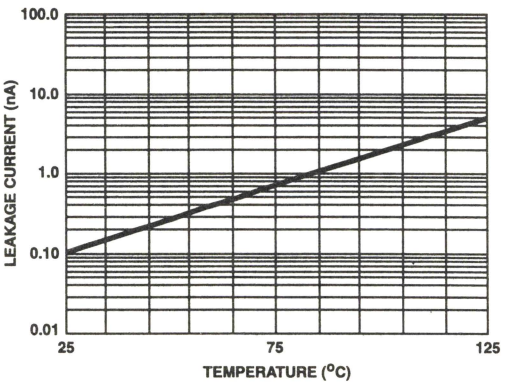


FIGURE 5. $I_{D(ON)}$ vs TEMPERATURE†

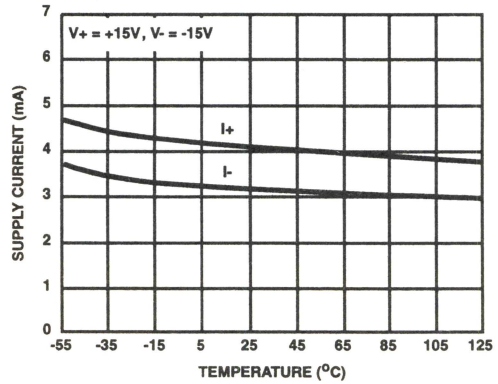


FIGURE 6. SUPPLY CURRENT vs TEMPERATURE

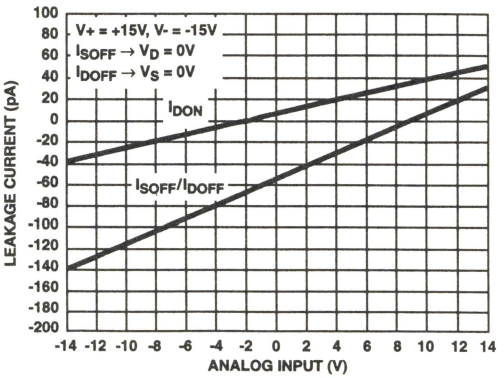


FIGURE 7. LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE

† Theoretically, leakage current will continue to decrease below 25°C. But due to environmental conditions, leakage measurements below this temperature are not representative of actual switch performance.

Typical Performance Curves (Continued)

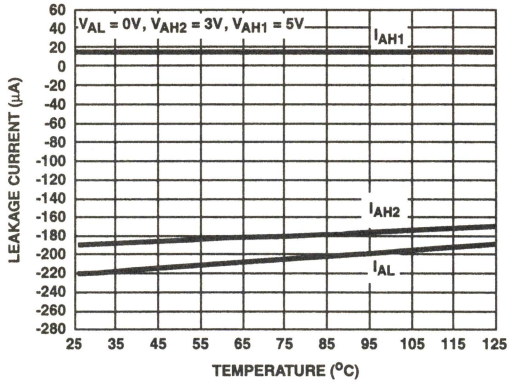


FIGURE 8. DIGITAL INPUT LEAKAGE CURRENT vs TEMPERATURE†

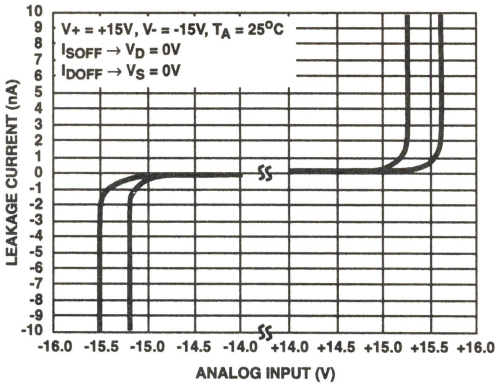


FIGURE 9. LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE

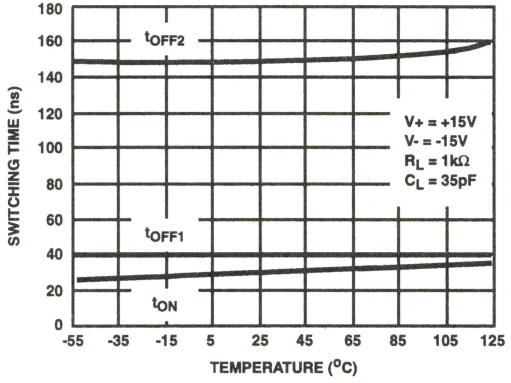


FIGURE 10. SWITCHING TIME vs TEMPERATURE

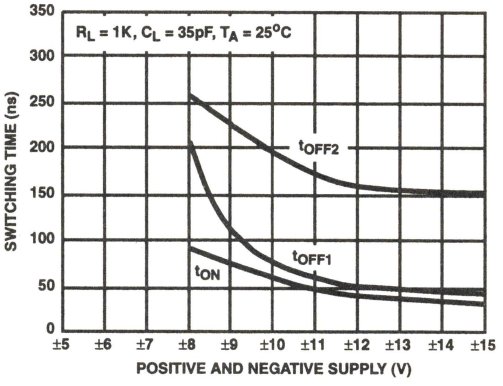


FIGURE 11. SWITCHING TIME vs POSITIVE AND NEGATIVE SUPPLY VOLTAGE

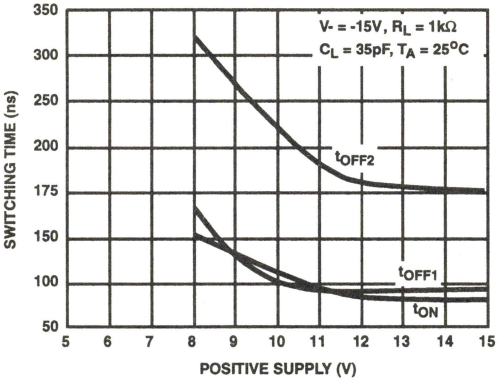


FIGURE 12. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE

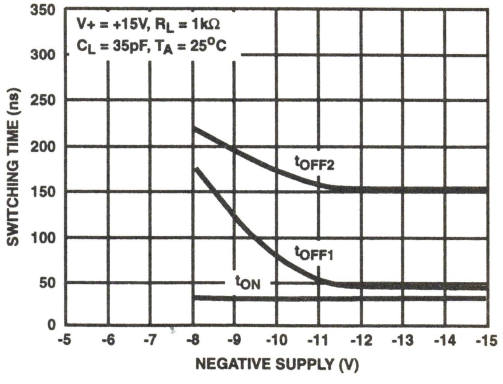


FIGURE 13. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

† Theoretically, leakage current will continue to decrease below 25°C. But due to environmental conditions, leakage measurements below this temperature are not representative of actual switch performance.

Typical Performance Curves (Continued)

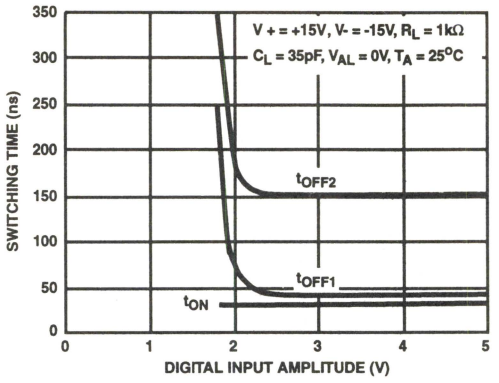


FIGURE 14. SWITCHING TIME vs INPUT LOGIC AMPLITUDE

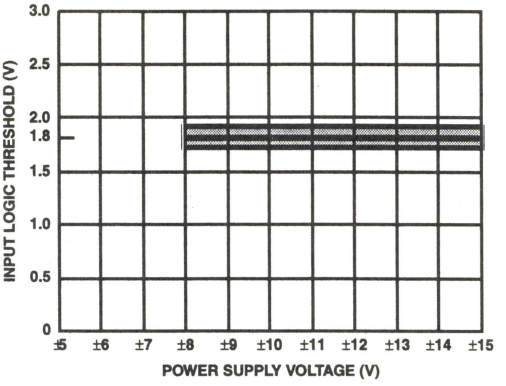


FIGURE 15. INPUT SWITCHING THRESHOLD vs POSITIVE AND NEGATIVE SUPPLY VOLTAGES

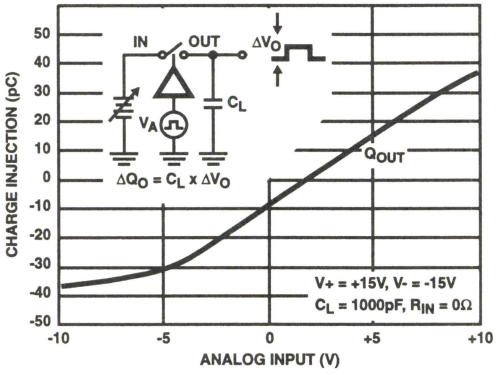


FIGURE 16. CHARGE INJECTION vs ANALOG INPUT

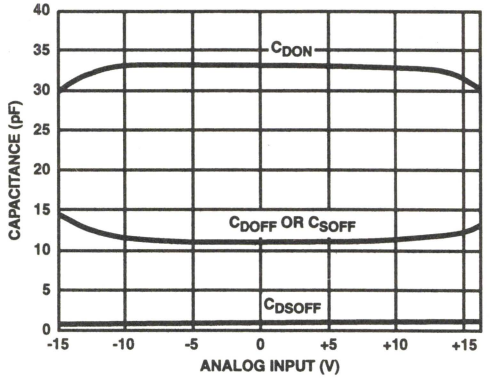


FIGURE 17. CAPACITANCE vs ANALOG INPUT

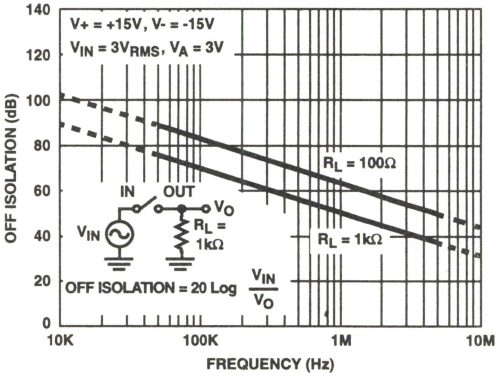


FIGURE 18. OFF ISOLATION vs FREQUENCY

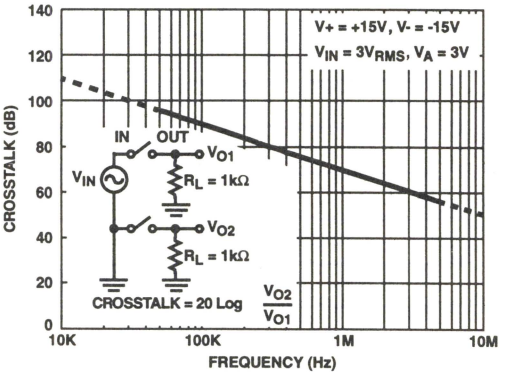


FIGURE 19. CROSSTALK vs FREQUENCY

Test Circuit

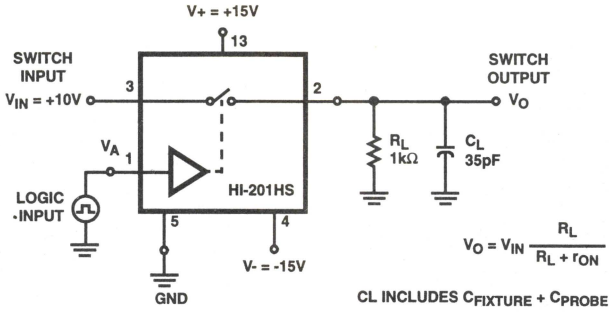


FIGURE 20. SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF1}, t_{OFF2})

Switching Characteristics

Typical delay, t_{ON}, t_{OFF}, settling time and switching transients in this circuit. If R_L or C_L is increased, there will be corresponding increases in rise and/or fall RC times.

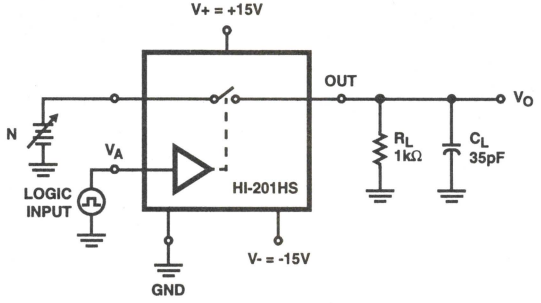


FIGURE 21A.

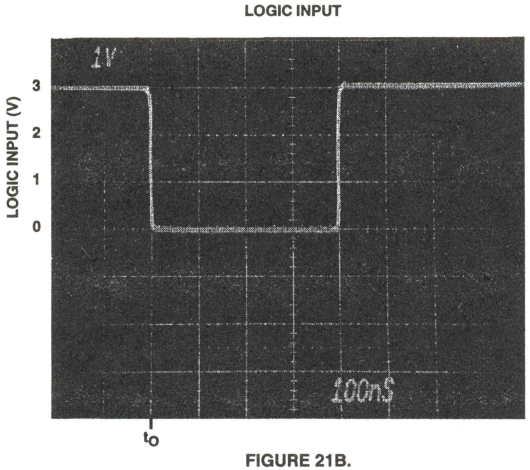


FIGURE 21B.

FIGURE 21. SWITCHING CHARACTERISTICS vs INPUT VOLTAGE

Switching Characteristics (Continued)

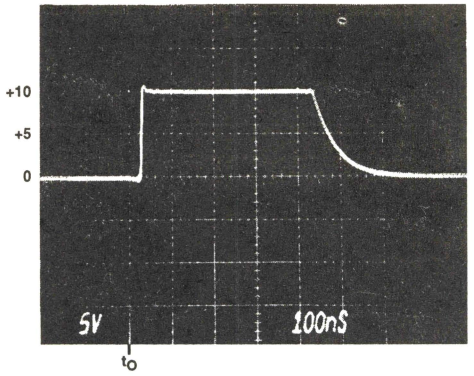


FIGURE 22A. V_{IN} = +10V

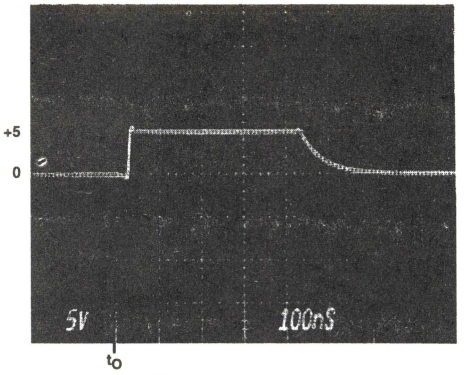


FIGURE 22B. V_{IN} = +5V

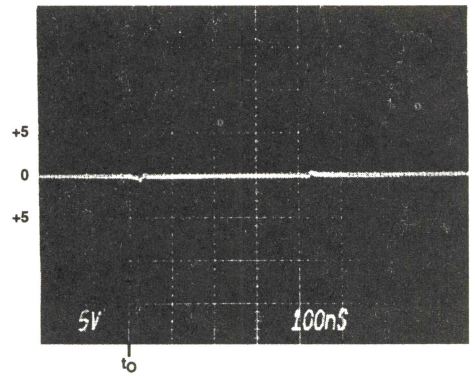


FIGURE 22C. V_{IN} = 0V

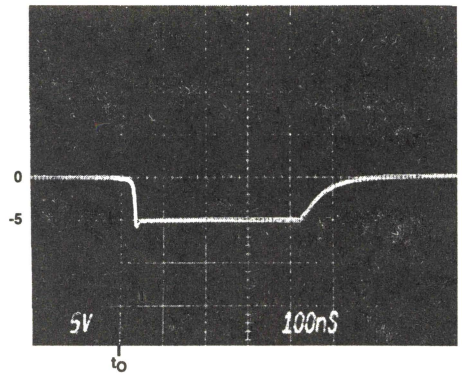


FIGURE 22D. V_{IN} = -5V

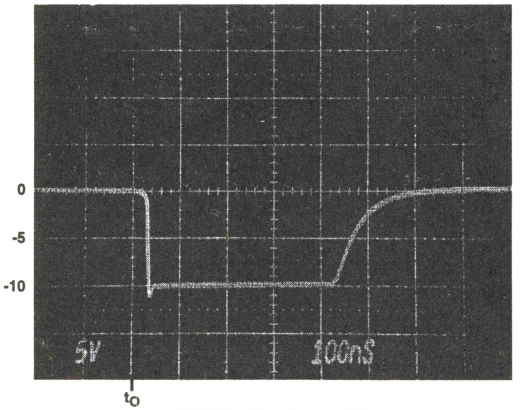


FIGURE 22E. V_{IN} = -10V

FIGURE 22. V_O - OUTPUT SWITCHING WAVEFORMS

Application Information

Logic Compatibility

The HI-201HS is TTL compatible. Its logic inputs (pins 1, 8, 9, and 16) are designed to react to digital inputs which exceed a fixed, internally generated TTL switching threshold. The HI-201HS can also be driven with CMOS logic (0V-15V), although the switch performance with CMOS logic will be inferior to that with TTL logic (0V-5V).

The logic input design of the HI-201HS is largely responsible for its fast switching speed. It is a design which features a unique input stage consisting of complementary vertical PNP and NPN bipolar transistors. This design differs from that of the standard HI-201 product where the logic inputs are MOS transistors.

Although the new logic design enhances the switching speed performance, it also increases the logic input leakage currents. Therefore, the HI-201HS will exhibit larger digital input leakage currents in comparison to the standard HI-201 product.

Charge Injection

Charge injection is the charge transferred, through the internal gate-to-channel capacitances, from the digital logic input to the analog output. To optimize charge injection performance for the HI-201HS, it is advisable to provide a TTL logic input with fast rise and fall times.

If the power supplies are reduced from ±15V, charge injection will become increasingly dependent upon the digital input frequency. Increased logic input frequency will result in larger output error due to charge injection.

Power Supply Considerations

The electrical characteristics specified in this data sheet are guaranteed for power supplies $\pm V_S = \pm 15V$. Power supply voltages less than ±15V will result in reduced switch performance. The following information is intended as a design aid only.

POWER SUPPLY VOLTAGES	SWITCH PERFORMANCE
$\pm 12 < \pm V_S \pm 15V$	Minimal Variation
$\pm V_S < \pm 12V$	Parametric variation becomes increasingly large (increased ON resistance, longer switching times).
$\pm V_S < \pm 10V$	Not Recommended.
$\pm V_S > \pm 16V$	Not Recommended.

Single Supply

The switch operation of the HI-201HS is dependent upon an internally generated switching threshold voltage optimized for ±15V power supplies. The HI-201HS does not provide the necessary internal switching threshold in a single supply system. Therefore, if single supply operation is required, the HI-300 series of switches is recommended. The HI-300 series will remain operational to a minimum +5V single supply.

Switch performance will degrade as power supply voltage is reduced from optimum levels (±15V). So it is recommended that a single supply design be thoroughly evaluated to ensure that the switch will meet the requirements of the application.

For Further Information See Application Notes AN520, AN521, AN531, AN532, AN543 and AN557.

Die Characteristics

DIE DIMENSIONS:

2440µm x 2860µm x 485µm ±25µm

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

PASSIVATION:

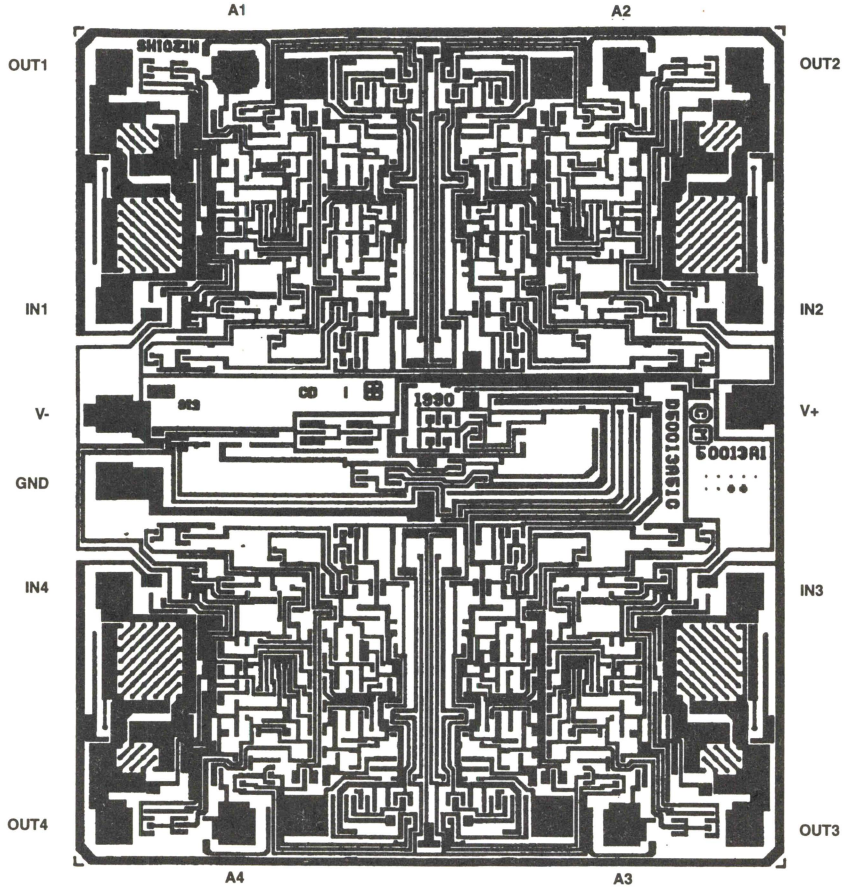
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

9.5×10^4 A/cm^2

Metallization Mask Layout

HI-201HS



HI-222

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

High Frequency/Video Switch

Features

- Wideband Operation 200MHz
- Differential Gain 0.03%
- Differential Phase . . . . . 0.003 Degrees
- Switching Speed 100ns
- r_{ON} 35Ω
- Off Isolation at 10MHz . . . . . -65dB
- Crosstalk at 10MHz . . . . . -80dB

Applications

- Routing Switchers
- Production Mixers
- High Definition TV
- Radar Signal Conditioning
- Medical Imaging
- Heads-Up Displays
- Simulators
- Sonar

Related Literature

- HI-222/883 Data Sheet in 1989 Military Analog Data Book

Description

The HI-222 is a high frequency analog switch that complements the Harris family of high speed op amps and buffers. Fabricated with our Dielectric Isolation process and using silicon gate technology, many key parameters have been enhanced.

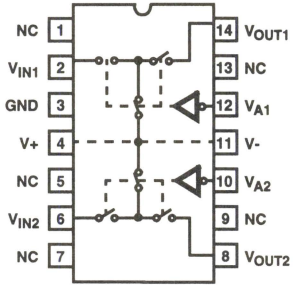
Crosstalk and off isolation are optimized with a T-switch configuration and the use of nonconnected pins for extended shielding. Other features of the HI-222 include wideband operation, low r_{ON}, fast switching speeds and low differential gain and phase. The characteristics of this TTL compatible device make it ideal for designs where improved switching performance is required.

The primary application of this dual SPST switch is the routing of high frequency signals in equipment ranging from video production mixers to military RF circuits.

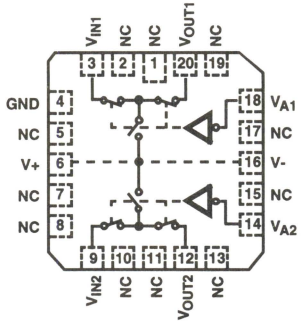
For specifications on HI-222/883, refer to Harris Military Analog Data book.

Pinouts

HI-222 (CERDIP, PDIP) (LOGIC "1" INPUT)
TOP VIEW



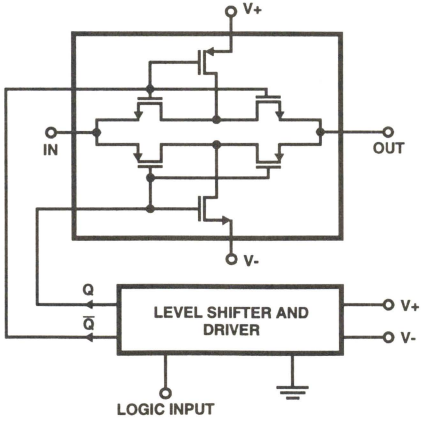
HI-222 (CLCC/PLCC) (LOGIC "0" INPUT)
TOP VIEW



Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI4P0222-5	0 to 75	20 Ld PLCC	N20.35
HI1-0222-5	0 to 75	14 Ld CERDIP	F14.3
HI3-0222-5	0 to 75	14 Ld PDIP	E14.3
HI1-0222/883	-55 to 125	14 Ld CERDIP	F14.3
HI4-0222/883	-55 to 125	20 Ld CLCC	J20.A

Functional Diagram



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output, respectively. They may be interchanged without affecting performance. All nonconnected pins should be tied to ground.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3124.1**

HARRIS SEMICONDUCTOR

HI-300 thru HI-307

August 1997

CMOS Analog Switches

Features

- Analog Signal Range (±15V Supplies) ..... ±15V
- Low Leakage at 25°C (Typ) 40pA
- Low Leakage at 125°C (Typ) 1nA
- Low On Resistance at 25°C (Typ) 35Ω
- Break-Before-Make Delay (Typ) 60ns
- Charge Injection 30pC
- TTL, CMOS Compatible
- Symmetrical Switch Elements
- Low Operating Power (Typ for HI-300 - 303) ... 1.0mW

Applications

- Sample and Hold (i.e., Low Leakage Switching)
- Op Amp Gain Switching (i.e., Low On Resistance)
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Description

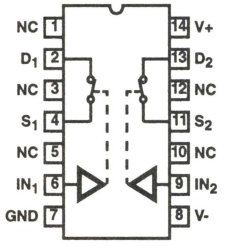
The HI-300 thru HI-307 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These switches feature break-before-make switching, (HI-301, HI-303, HI-305 and HI-307 only), low and nearly constant ON resistance over the full analog signal range, and low power dissipation, (a few mW for the HI-300 thru HI-303, a few hundred mW for the HI-304 thru HI-307).

The HI-300 thru HI-303 are TTL compatible and have a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4V. The HI-304 thru HI-307 switches are CMOS compatible and have a low state with an input less than 3.5V and a high state with an input greater than 11V. (See pinouts for switch conditions with a logic "1" input.)

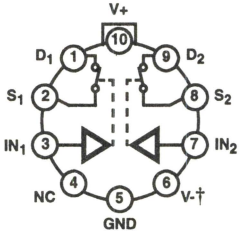
Pinouts (Switch States are for a Logic "1" Input)

DUAL SPST HI-300 AND HI-304
TOP VIEWS

(CERDIP, PDIP, SOIC)



(METAL CAN)

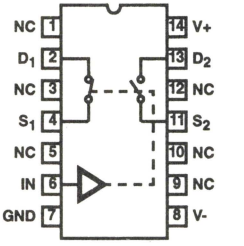


LOGIC	SWITCH
0	OFF
1	ON

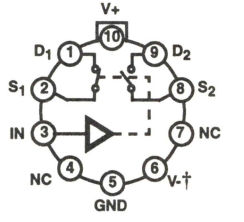
† The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

SPST HI-301 AND HI-305
TOP VIEWS

(CERDIP, PDIP, SOIC)



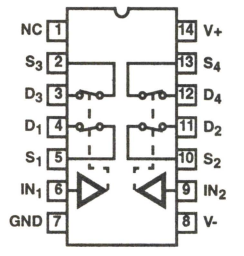
(METAL CAN)



LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

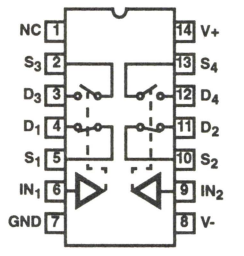
† The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-302 AND HI-306 (PDIP, CERDIP, SOIC)
TOP VIEW



LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT HI-303 AND HI-307 (PDIP, CERDIP, SOIC)
TOP VIEW



LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3125.1**

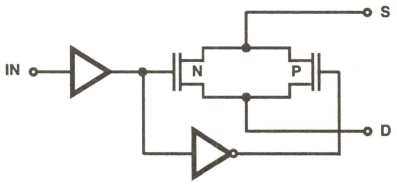
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0300-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0300-5	0 to 75	14 Ld CERDIP	F14.3
HI2-0300-2	-55 to 125	10 Pin Metal Can (TO-100)	T10.B
HI2-0300-5	0 to 75	10 Pin Metal Can (TO-100)	T10.B
HI3-0300-5	0 to 75	14 Ld PDIP	E14.3
HI1-0301-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0301-5	0 to 75	14 Ld CERDIP	F14.3
HI2-0301-2	-55 to 125	10 Pin Metal Can (TO-100)	T10.B
HI2-0301-5	0 to 75	10 Pin Metal Can (TO-100)	T10.B
HI3-0301-5	0 to 75	14 Ld PDIP	E14.3
HI9P0301-5	0 to 75	14 Ld SOIC	M14.15
HI1-0302-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0302-5	0 to 75	14 Ld CERDIP	F14.3
HI3-0302-5	0 to 75	14 Ld PDIP	E14.3
HI9P0302-5	0 to 75	14 Ld SOIC	M14.15
HI1-0303-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0303-5	0 to 75	14 Ld CERDIP	F14.3
HI3-0303-5	0 to 75	14 Ld PDIP	E14.3
HI9P0303-5	0 to 75	14 Ld SOIC	M14.15

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI9P0303-9	-40 to 85	14 Ld SOIC	M14.15
HI1-0304-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0304-5	0 to 75	14 Ld CERDIP	F14.3
HI2-0304-2	-55 to 125	10 Pin Metal Can (TO-100)	T10.B
HI2-0304-5	0 to 75	10 Pin Metal Can (TO-100)	T10.B
HI3-0304-5	0 to 75	14 Ld PDIP	E14.3
HI1-0305-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0305-5	0 to 75	14 Ld CERDIP	F14.3
HI2-0305-2	-55 to 125	10 Pin Metal Can (TO-100)	T10.B
HI2-0305-5	0 to 75	10 Pin Metal Can (TO-100)	T10.B
HI3-0305-5	0 to 75	14 Ld PDIP	E14.3
HI9P0305-5	0 to 75	14 Ld SOIC	M14.15
HI1-0306-5	0 to 75	14 Ld CERDIP	F14.3
HI3-0306-5	0 to 75	14 Ld PDIP	E14.3
HI1-0307-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0307-5	0 to 75	14 Ld CERDIP	F14.3
HI3-0307-5	0 to 75	14 Ld PDIP	E14.3
HI9P0307-5	0 to 75	14 Ld SOIC	M14.15

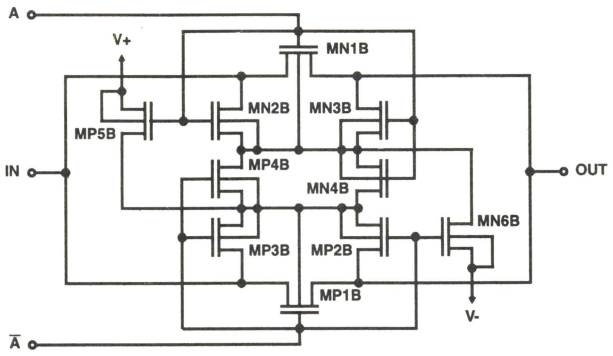
Functional Block Diagram

TYPICAL SWITCH HI-300 SERIES

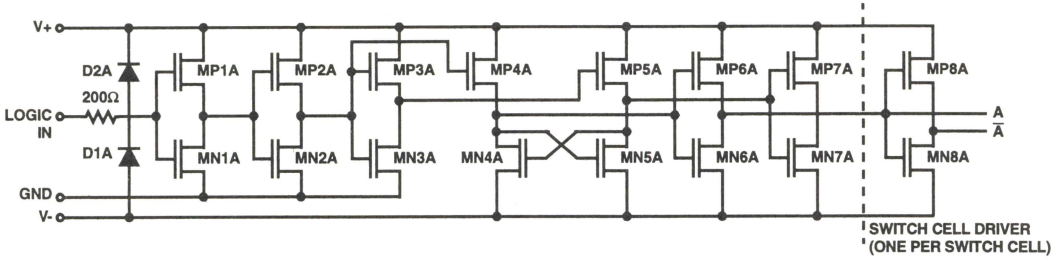


Schematic Diagrams

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

Voltage Between Supplies ..... 44V (±22V)
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage ..... $+V_{SUPPLY}$ +1.5V
$-V_{SUPPLY}$ -1.5V
Typical Derating Factor..... 1.5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Operating Conditions

Temperature Range
HI-3XX-2..... -55°C to 125°C
HI-3XX-5..... 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	95	40
PDIP Package	100	N/A
SOIC Package	120	N/A
10 Pin TO-100 Metal Can Package	160	75

Maximum Junction Temperature
CERDIP, TO-Can Packages ..... 175°C
PDIP, SOIC Packages ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s)..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{IN} = Logic Input. HI-300-303: V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V. HI-304-307: V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V, Unless Otherwise Specified

PARAMETER	TEMP (°C)	-55°C TO 125°C			0°C TO 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS								
Break-Before-Make Delay, t_{OPEN} (Note 15)	25	-	60	-	-	60	-	ns
Switch On Time, t_{ON} (Note 13)	25	-	210	300	-	210	300	ns
Switch Off Time, t_{OFF} (Note 13)	25	-	160	250	-	160	250	ns
Switch Off Time, t_{ON} (Note 14)	25	-	160	250	-	160	250	ns
Switch Off Time, t_{OFF} (Note 14)	25	-	100	150	-	100	150	ns
"Off Isolation" (Note 6)	25	-	60	-	-	60	-	dB
Charge Injection (Note 7)	25	-	3	-	-	3	-	mV
Input Switch Capacitance, $C_{S(OFF)}$	25	-	16	-	-	16	-	pF
Output Switch Capacitance, $C_{D(OFF)}$	25	-	14	-	-	14	-	pF
Output Switch Capacitance, $C_{D(ON)}$	25	-	35	-	-	35	-	pF
(High) Digital Input Capacitance, C_{IN}	25	-	5	-	-	5	-	pF
(Low) Digital Input Capacitance, C_{IN}	25	-	5	-	-	5	-	pF
DIGITAL INPUT CHARACTERISTICS								
Input Low Level, V_{INL} (Note 13)	Full	-	-	0.8	-	-	0.8	V
Input High Level, V_{INH} (Note 13)	Full	4	-	-	4	-	-	V
Input Low Level, V_{INL} (Note 14)	Full	-	-	3.5	-	-	3.5	V
Input High Level, V_{INH} (Note 14)	Full	11	-	-	11	-	-	V
Input Leakage Current (Low), I_{INL} (Note 5)	Full	-	-	1	-	-	1	µA
Input Leakage Current (High), I_{INH} (Note 5)	Full	-	-	1	-	-	1	µA
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON} (Note 2)	25	-	35	50	-	35	50	Ω
	Full	-	40	75	-	40	75	Ω
Off Input Leakage Current, $I_{S(OFF)}$ (Note 3)	25	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA

Electrical Specifications Supplies = +15V, -15V; V_{IN} = Logic Input. HI-300-303: V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V. HI-304-307: V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP (°C)	-55°C TO 125°C			0°C TO 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Off Output Leakage Current, $I_{D(OFF)}$ (Note 3)	25	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
On Leakage Current, $I_{D(ON)}$ (Note 4)	25	-	0.03	1	-	0.03	5	nA
	Full	-	0.5	100	-	0.2	100	nA
POWER SUPPLY CHARACTERISTICS								
Current, I+ (Notes 8, 13)	25	-	0.09	0.5	-	0.09	0.5	mA
	Full	-	-	1	-	-	1	mA
Current, I- (Notes 8, 13)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I+ (Notes 9, 13)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I- (Notes 9, 13)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I+ (Notes 10, 14)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I- (Notes 10, 14)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I+ (Notes 11, 14)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I- (Notes 11, 14)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA

NOTES:

1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.
2. $V_S = \pm 10V$, $I_{OUT} = \mp 10mA$. On resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V$, $V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1K.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. (HI-300 - 303) Switches are symmetrical; S and D may be interchanged. Logic Drive = 15V (HI-304 - 307).
8. V_{IN} = 4V (one input) (all other inputs = 0V).
9. V_{IN} = 0.8V (all inputs).
10. V_{IN} = 15V (all inputs).
11. V_{IN} = 0V (all inputs).
12. To drive from DTL/TTL circuits, pullup resistors to +5V supply are recommended.
13. HI-300 thru HI-303 only.
14. HI-304 thru HI-307 only.
15. HI-301, HI-303, HI-305, HI-307 only.

Typical Performance Curves

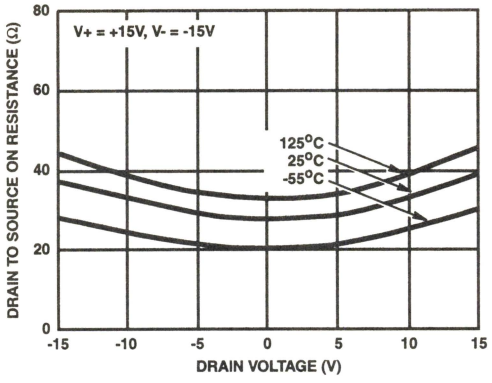


FIGURE 1. $R_{DS(ON)}$ vs V_D AND TEMPERATURE

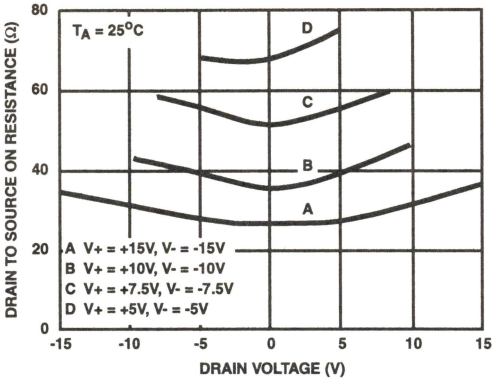


FIGURE 2. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

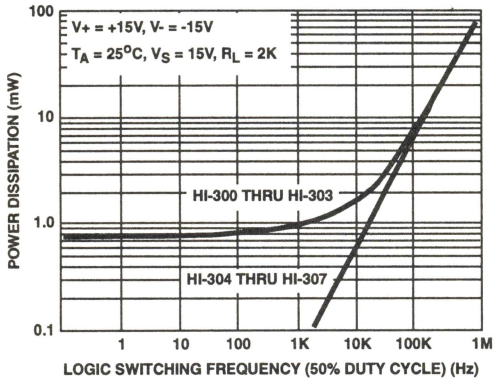


FIGURE 3. DEVICE POWER DISSIPATION vs SWITCHING FREQUENCY SINGLE LOGIC INPUT

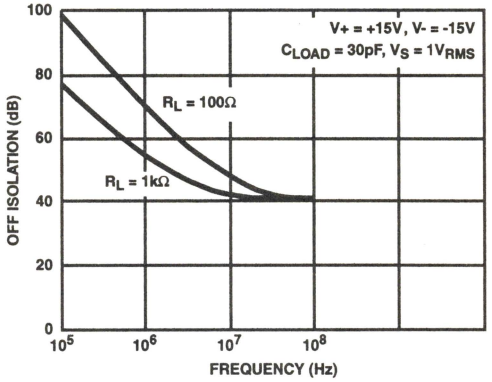


FIGURE 4. OFF ISOLATION vs FREQUENCY

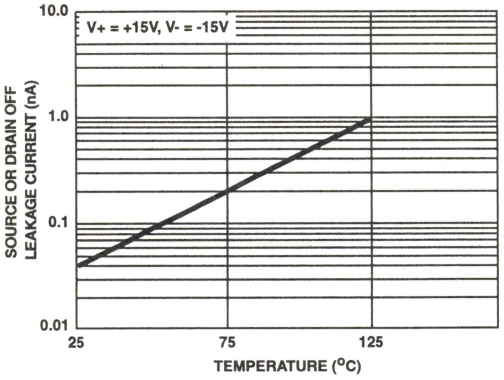


FIGURE 5. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE†

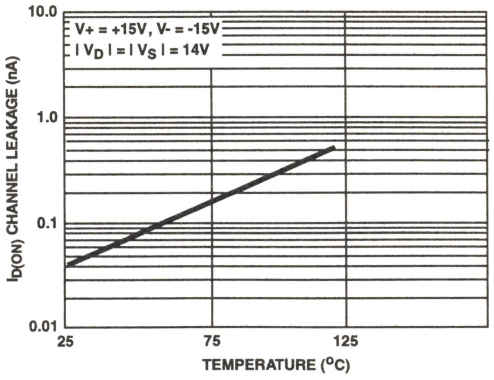


FIGURE 6. $I_{D(ON)}$ vs TEMPERATURE†

† The net leakage into the source or drain is the N-Channel leakage minus the P-Channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

Typical Performance Curves (Continued)

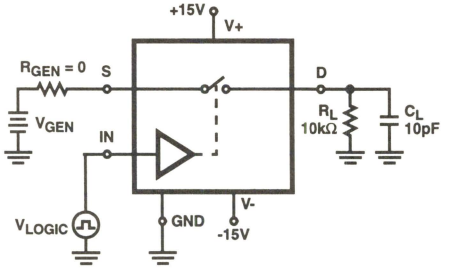


FIGURE 7A. TEST CIRCUIT

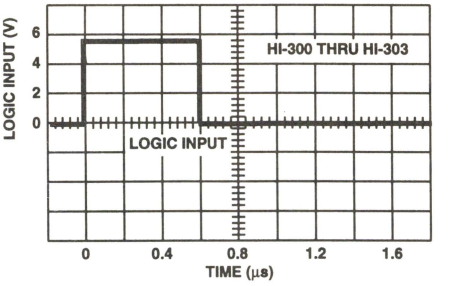


FIGURE 7B. $V_{IN(LOGIC)}$ vs TIME

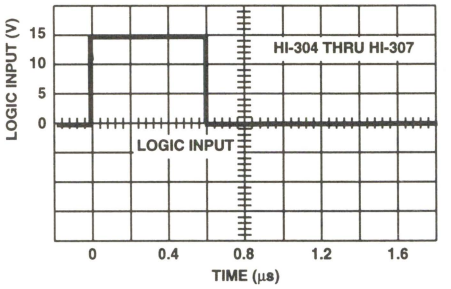


FIGURE 7C. $V_{IN(LOGIC)}$ vs TIME

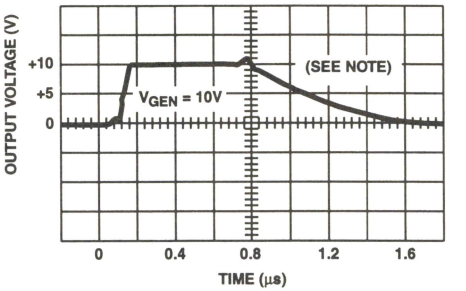


FIGURE 7D. V_{OUT} vs TIME

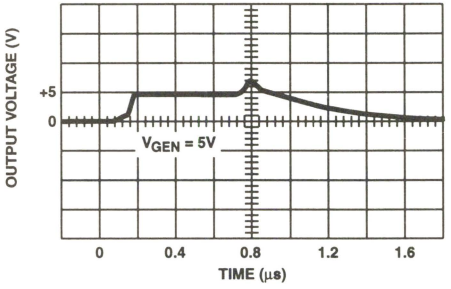


FIGURE 7E. V_{OUT} vs TIME

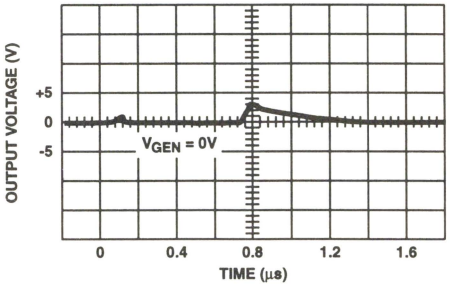


FIGURE 7F. V_{OUT} vs TIME

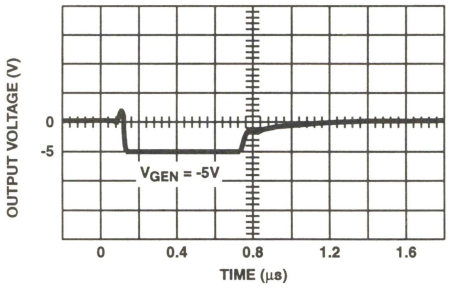


FIGURE 7G. V_{OUT} vs TIME

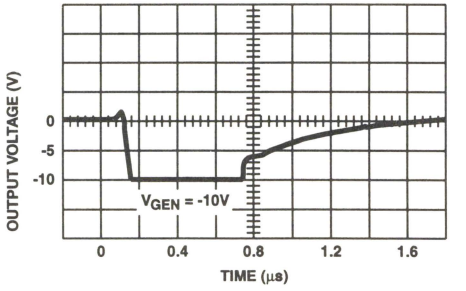


FIGURE 7H. V_{OUT} vs TIME

NOTE: If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

FIGURE 7. TYPICAL DELAY, RISE, FALL, SETTLING TIMES AND SWITCHING TRANSIENTS

Typical Performance Curves (Continued)

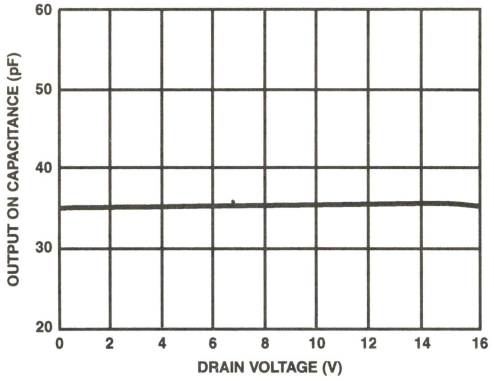


FIGURE 8. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE

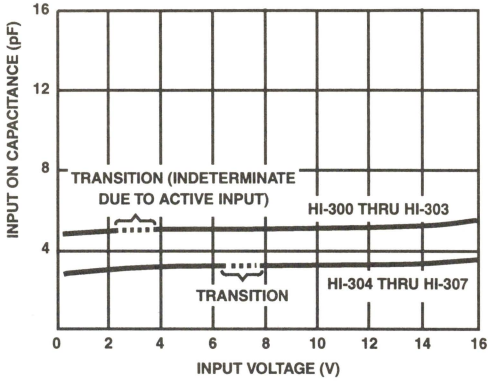


FIGURE 9. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE

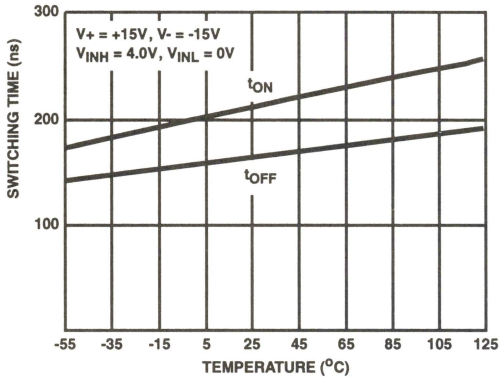


FIGURE 10. SWITCHING TIME vs TEMPERATURE, HI-300 THRU HI-303

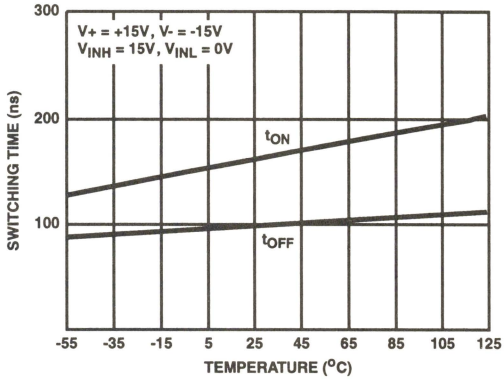


FIGURE 11. SWITCHING TIME vs TEMPERATURE, HI-304 THRU HI-307

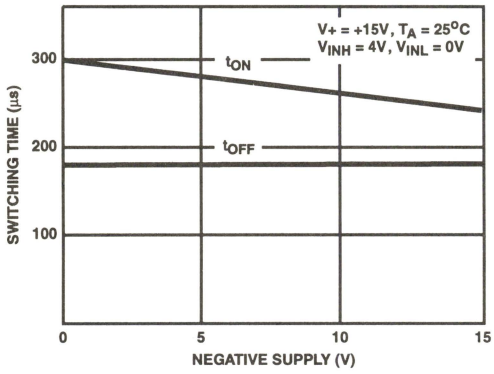


FIGURE 12. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE, HI-300 THRU HI-303

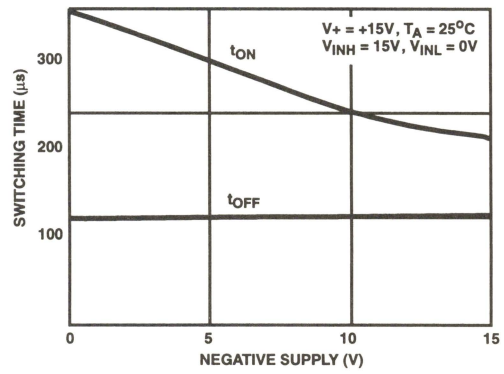


FIGURE 13. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE, HI-304 THRU HI-307

Typical Performance Curves (Continued)

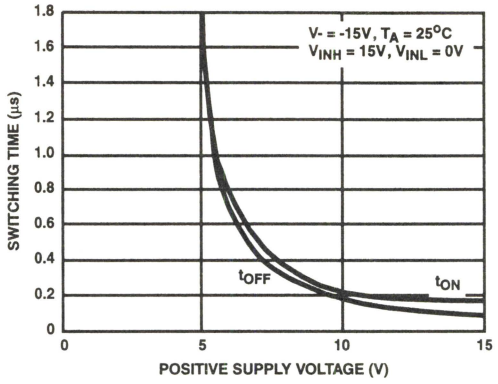


FIGURE 14. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE, HI-304 THRU HI-307

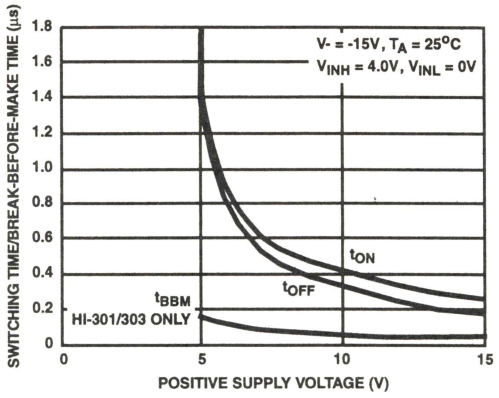


FIGURE 15. SWITCHING TIME AND BREAK-BEFORE-MAKE TIME vs POSITIVE SUPPLY VOLTAGE, HI-300 THRU HI-303

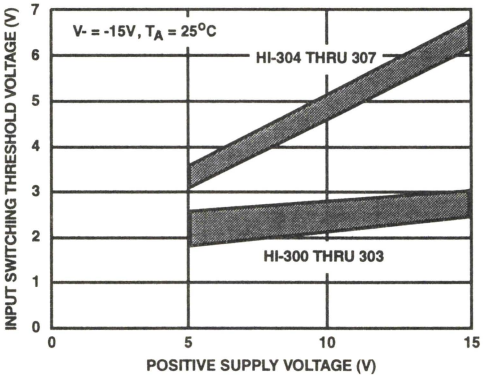
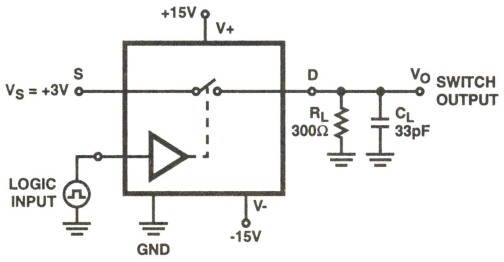


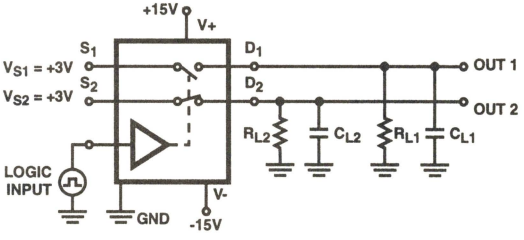
FIGURE 16. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE, HI-300 THRU HI-307

Test Circuits and Waveforms

SWITCH TYPE	V_{INH}
HI-300 thru HI-303	4V
HI-304 thru HI-307	15V

SWITCH TYPE	V_{INH}
HI-301, HI-303	5V
HI-305, HI-307	15V





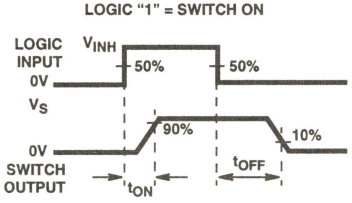


FIGURE 17. SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

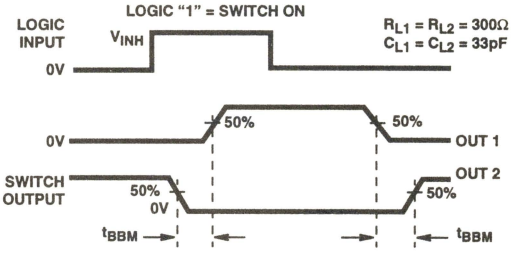


FIGURE 18. BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM}

HI-381 thru HI-390

August 1997

CMOS Analog Switches

Features

- Analog Signal Range (±15V Supplies) ..... ±15V
- Low Leakage 40pA
- Low On Resistance 35Ω
- Break-Before-Make Delay 60ns
- Charge Injection 30pC
- TTL Compatible
- Symmetrical Switch Elements
- Low Operating Power 1.0mW

Description

The HI-381 thru HI-390 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These devices are TTL compatible and are available in four switching configurations. (See device pinout for particular switching function with a logic "1" input.)

These switches feature low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

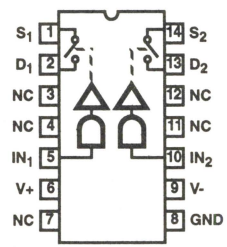
Applications

- Sample and Hold (i.e., Low Leakage Switching)
- Op Amp Gain Switching (i.e., Low On Resistance)
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

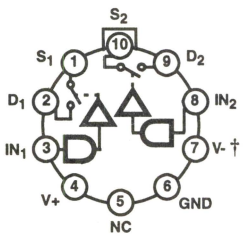
Pinouts (Switch States are for a Logic "1" Input)

DUAL SPST HI-300 AND HI-304
TOP VIEWS

(CERDIP, PDIP)



(METAL CAN)

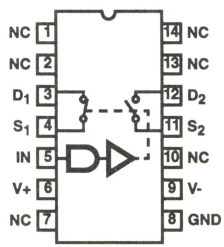


LOGIC	SWITCH
0	OFF
1	ON

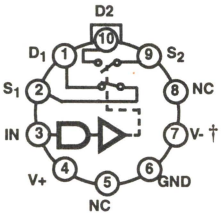
† The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

SPST HI-301 AND HI-305
TOP VIEWS

(CERDIP, PDIP)



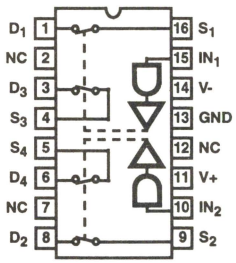
(METAL CAN)



LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

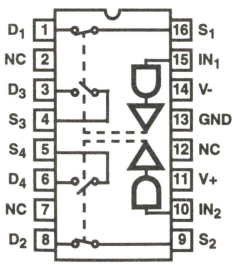
† The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-384 (CERDIP, PDIP)
TOP VIEW



LOGIC	SW 1 - 4
0	OFF
1	ON

DUAL SPDT HI-390 (CERDIP, PDIP, SOIC)
TOP VIEW



LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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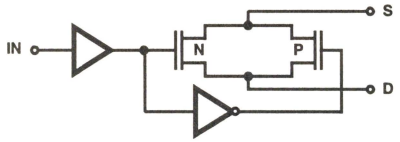
File Number **3126.1**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0381-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0381-5	0 to 75	14 Ld CERDIP	F14.3
HI1-0381/883	-55 to 125	14 Ld CERDIP	F14.3
HI2-0381-2	-55 to 125	10 Pin Metal Can	T10.B
HI2-0381-5	0 to 75	10 Pin Metal Can	T10.B
HI2-0381/883	-55 to 125	10 Pin Metal Can	T10.B
HI1-0384-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0384-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0384/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-0387-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0387-5	0 to 75	14 Ld CERDIP	F14.3
HI2-0387-2	-55 to 125	10 Pin Metal Can	T10.B
HI2-0387-5	0 to 75	10 Pin Metal Can	T10.B
HI1-0390-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0390-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0390/883	-55 to 125	16 Ld CERDIP	F16.3
HI9P0390-5	0 to 75	16 Ld SOIC	M16.3
HI3-0381-5	0 to 75	14 Ld PDIP	E14.3
HI1-0387/883	-55 to 125	14 Ld CERDIP	F14.3
HI2-0387/883	-55 to 125	10 Pin Metal Can	T10.B
HI3-0387-5	0 to 75	14 Ld PDIP	E14.3
HI3-0390-5	0 to 75	16 Ld PDIP	E16.3
HI3-0384-5	0 to 75	16 Ld PDIP	E16.3

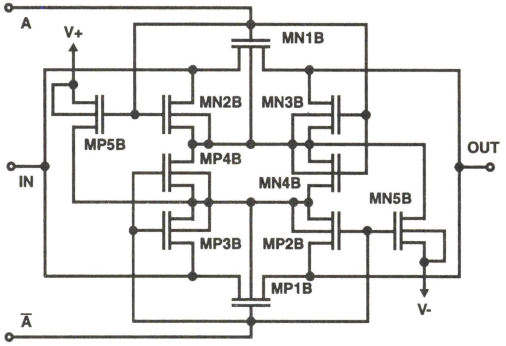
Functional Block Diagram

TYPICAL SWITCH 3XX SERIES

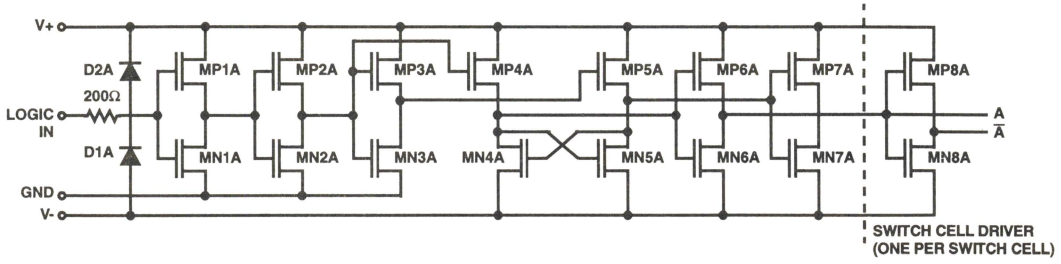


Schematic Diagrams

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

Voltage Between Supplies ..... 44V (±22V)
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage ..... $+V_{SUPPLY}$ +1.5V
$-V_{SUPPLY}$ -1.5V

Operating Conditions

Temperature Ranges
HI-3XX-2 ..... -55°C to 125°C
HI-3XX-5 ..... .0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld CERDIP Package	95	40
16 Ld CERDIP Package	90	36
PDIP Package	100	N/A
SOIC Package	100	N/A
Metal Can Package	160	75

Maximum Junction Temperature
Hermetic Package ..... 175°C
Plastic Package ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{IN} = Logic Input. V_{IN} for Logic "1" = 4V, for Logic "0" = 0.8V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-3XX-2			HI-3XX-5, 9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Break-Before-Make Delay, t_{OPEN} (HI-387/HI-390 Only)		25	-	60	-	-	60	-	ns
Switch On Time, t_{ON}		25	-	210	300	-	210	300	ns
Switch Off Time, t_{OFF}		25	-	160	250	-	160	250	ns
"Off Isolation"	(Note 5)	25	-	60	-	-	60	-	dB
Charge Injection	(Note 6)	25	-	3	-	-	3	-	mV
Input Switch Capacitance, $C_{S(OFF)}$		25	-	16	-	-	16	-	pF
Output Switch Capacitance, $C_{D(OFF)}$		25	-	14	-	-	14	-	pF
Output Switch Capacitance, $C_{D(ON)}$		25	-	35	-	-	35	-	pF
Digital Input Capacitance (High), C_{IN}		25	-	5	-	-	5	-	pF
Digital Input Capacitance (Low), C_{IN}		25	-	5	-	-	5	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Level, V_{INL}		Full	-	-	0.8	-	-	0.8	V
Input High Level, V_{INH}		Full	4	-	-	4	-	-	V
Input Leakage Current (Low), I_{INL}	(Note 4)	Full	-	-	1	-	-	1	µA
Input Leakage Current (High), I_{INH}	(Note 4)	Full	-	-	1	-	-	1	µA
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range		Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON}	(Note 1)	25	-	35	50	-	35	50	Ω
		Full	-	40	75	-	45	75	Ω
Off Input Leakage Current, $I_{S(OFF)}$	(Note 2)	25	-	0.04	1	-	0.04	5	nA
		Full	-	1	100	-	0.2	100	nA
Off Output Leakage Current, $I_{D(OFF)}$	(Note 2)	25	-	0.04	1	-	0.04	5	nA
		Full	-	1	100	-	0.2	100	nA
On Input Leakage Current, $I_{S(ON)}$	(Note 3)	25	-	0.03	1	-	0.03	5	nA
		Full	-	0.5	100	-	0.2	100	nA

Electrical Specifications Supplies = +15V, -15V; V_{IN} = Logic Input. V_{IN} for Logic "1" = 4V, for Logic "0" = 0.8V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-3XX-2			HI-3XX-5, 9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS									
Current, I+	(Note 7)	25	-	0.09	0.5	-	0.09	0.5	mA
		Full	-	-	1	-	-	1	mA
Current, I-	(Note 7)	25	-	0.01	10	-	0.01	100	µA
		Full	-	-	100	-	-	-	µA
Current, I+	(Note 8)	25	-	0.01	10	-	0.01	100	µA
		Full	-	-	100	-	-	-	µA
Current, I-	(Note 8)	25	-	0.01	10	-	0.01	100	µA
		Full	-	-	100	-	-	-	µA

NOTES:

2. $V_S = \pm 10V$, $I_{OUT} = \mp 10mA$. On resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V$, $V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1K, $C_L = C_{FIXTURE} + C_{PROBE}$ "off isolation" = 20 Log V_S/V_D.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged.
8. V_{IN} = 4V (one input) (all other inputs = 0V).
9. V_{IN} = 0.8V (all inputs).

Typical Performance Curves

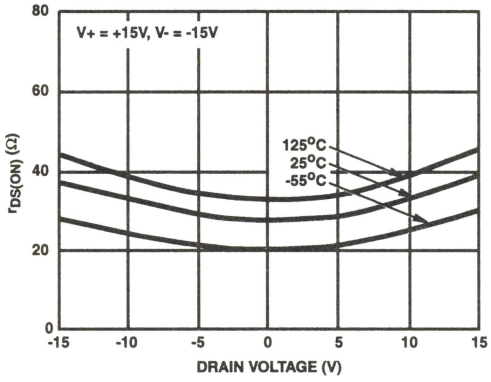


FIGURE 1. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

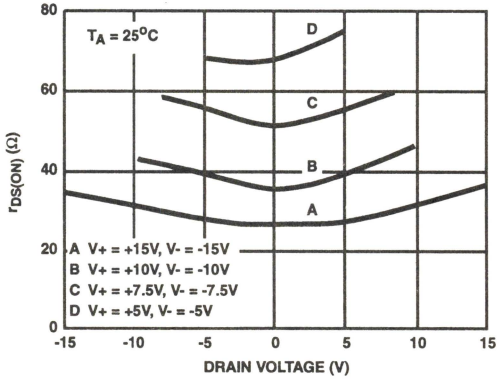


FIGURE 2. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

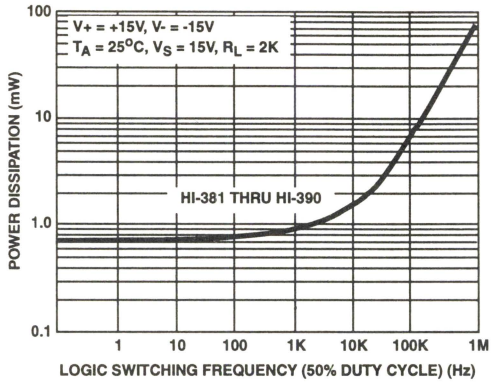


FIGURE 3. DEVICE POWER DISSIPATION vs SWITCHING FREQUENCY (SINGLE LOGIC INPUT)

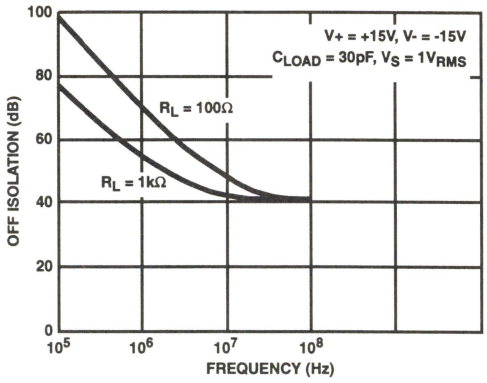


FIGURE 4. OFF ISOLATION vs FREQUENCY

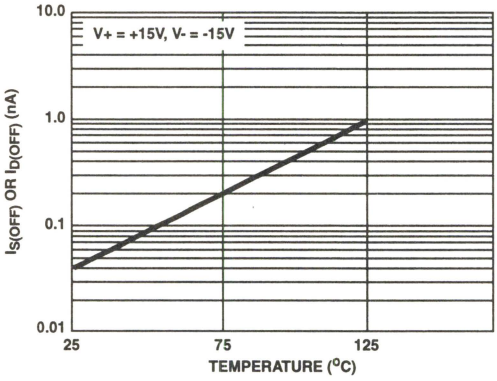


FIGURE 5. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE (NOTE)

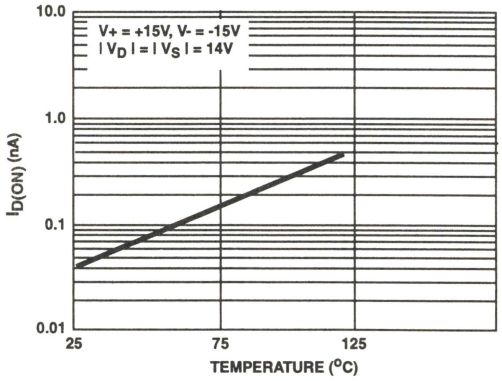


FIGURE 6. $I_{D(ON)}$ vs TEMPERATURE (NOTE)

NOTE: The net leakage into the source or drain is the N-Channel leakage minus the P-Channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

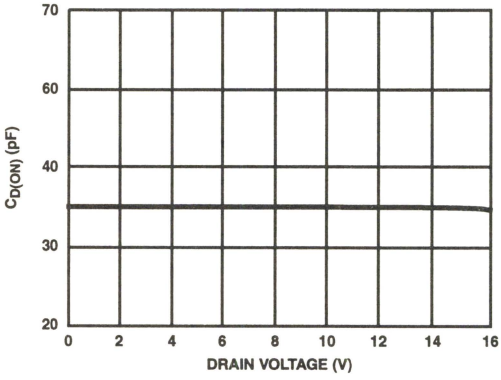


FIGURE 7. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE

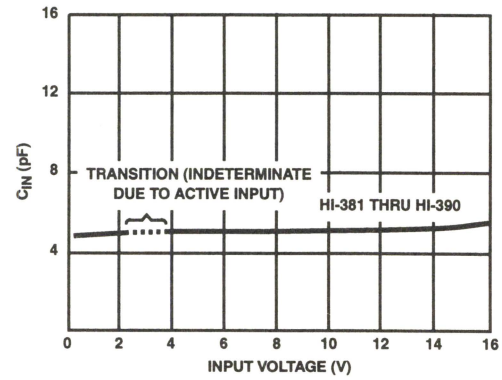


FIGURE 8. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE

Typical Performance Curves (Continued)

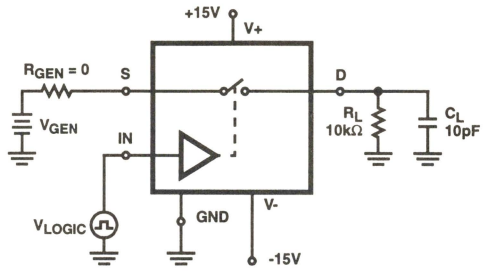


FIGURE 9A. TEST CIRCUIT

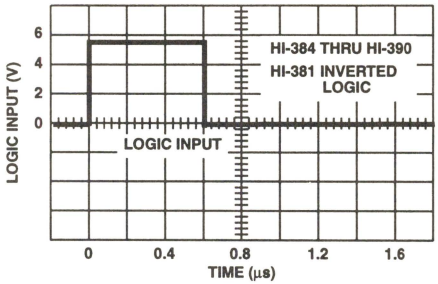


FIGURE 9B. V_{IN} LOGIC vs TIME

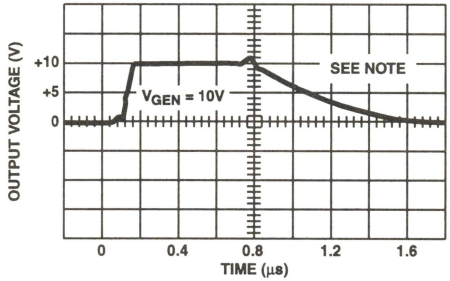


FIGURE 9C. V_{OUT} vs TIME

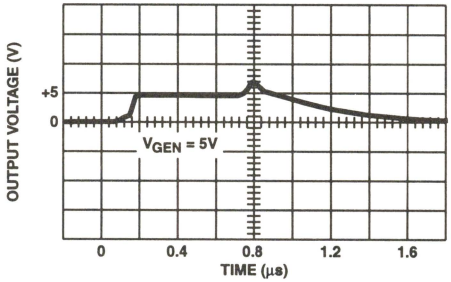


FIGURE 9D. V_{OUT} vs TIME

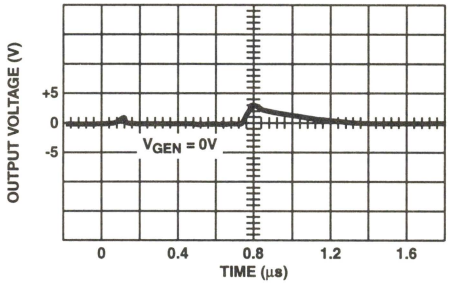


FIGURE 9E. V_{OUT} vs TIME

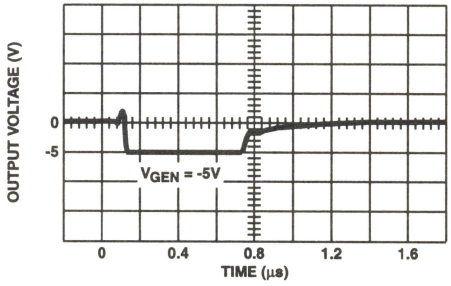


FIGURE 9F. V_{OUT} vs TIME

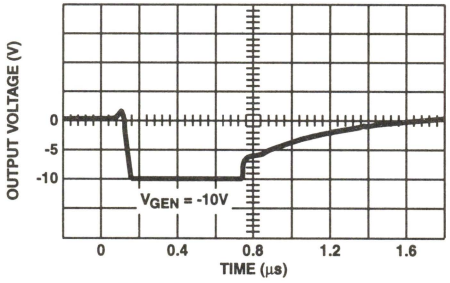


FIGURE 9G. V_{OUT} vs TIME

NOTE: If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

FIGURE 9. TYPICAL DELAY, RISE, FALL, SETTLING TIMES AND SWITCHING TRANSIENTS

Typical Performance Curves (Continued)

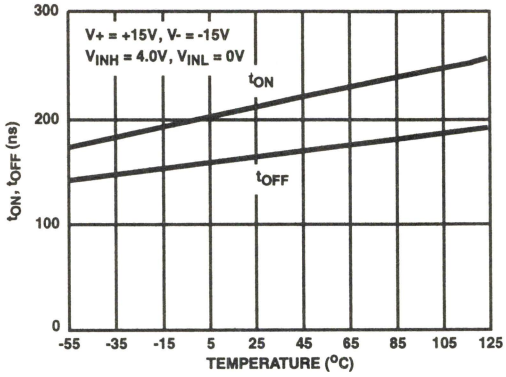


FIGURE 10. SWITCHING TIME vs TEMPERATURE, HI-381 THRU HI-390

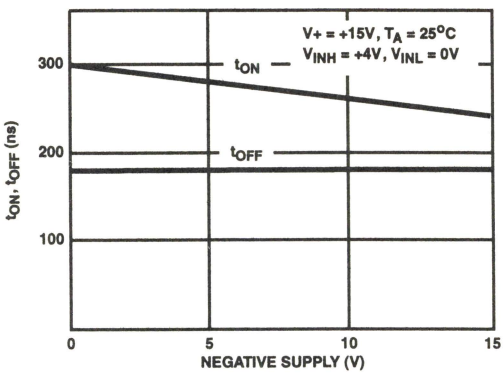


FIGURE 11. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE, HI-381 THRU HI-390

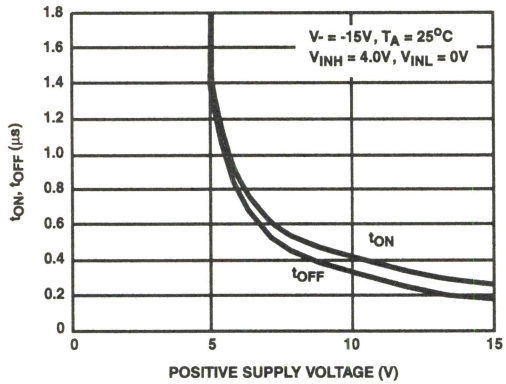


FIGURE 12. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE, HI-381 THRU HI-390

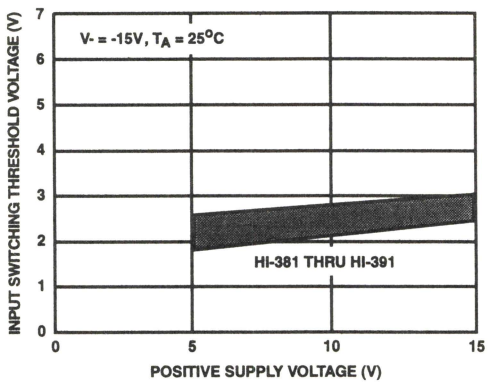


FIGURE 13. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE, HI-381 THRU HI-390

HI-5040 thru HI-5051, HI-5046A and HI-5047A

August 1997

CMOS Analog Switches

Features

- Wide Analog Signal Range ..... ±15V
- Low "ON" Resistance (Typ) 25Ω
- High Current Capability (Typ) 80mA
- Break-Before-Make Switching
  - Turn-On Time (Typ) 370ns
  - Turn-Off Time (Typ) 280ns
- No Latch-Up
- Input MOS Gates are Protected from Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

Description

This family of CMOS analog switches offers low resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. r_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and 75°C. r_{ON} is nominally 25Ω for HI-5048 through HI-5051 and HI-5046A and HI-5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at 25°C). This family of switches also features very low power operation (1.5mW at 25°C).

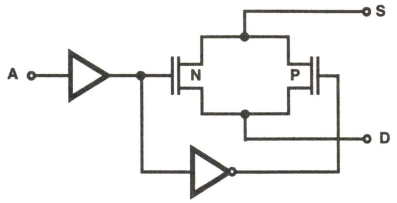
There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional Description). All devices are available in 16 lead DIP packages. The HI-5040 and HI-5050 switches can directly replace IH-5040 series devices except IH5048, and are functionally compatible with the DG180 and DG190 family. Each switch type is available in the -55°C to 125°C and 0°C to 75°C performance grades.

Functional Description

PART NUMBER	TYPE	r_{ON}
HI-5040	SPST	50Ω
HI-5041	Dual SPST	50Ω
HI-5042	SPDT	50Ω
HI-5043	Dual SPDT	50Ω
HI-5044	DPST	50Ω
HI-5045	Dual DPST	50Ω
HI-5046	DPDT	50Ω
HI-5046A	DPDT	25Ω
HI-5047	4PST	50Ω
HI-5047A	4PST	25Ω
HI-5048	Dual SPST	25Ω
HI-5049	Dual DPST	25Ω
HI-5050	SPDT	25Ω
HI-5051	Dual SPDT	25Ω

Functional Block Diagram

TYPICAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3127.1**

Ordering Information

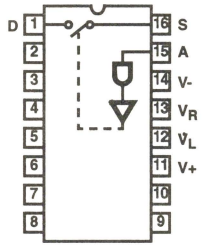
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3-5040-5	0 to 75	16 Ld PDIP	E16.3
HI1-5040-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5040-5	0 to 75	16 Ld CERDIP	F16.3
HI3-5041-5	0 to 75	16 Ld PDIP	E16.3
HI1-5041-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5041-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5042-5	0 to 75	16 Ld PDIP	E16.3
HI1-5042-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5042-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5043-7	0 to 75 + 96 Hr. Burn-In	16 Ld CERDIP	F16.3
HI1-5043-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5043-5	0 to 75	16 Ld PDIP	E16.3
HI1-5043-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5044-5	0 to 75	16 Ld CERDIP	F16.3
HI3-5044-5	0 to 75	16 Ld PDIP	E16.3
HI1-5045-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5045-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5045-5	0 to 75	16 Ld PDIP	E16.3
HI1-5046-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5046-5	0 to 75	16 Ld CERDIP	F16.3
HI3-5046-5	0 to 75	16 Ld PDIP	E16.3
HI3-5046A-5	0 to 75	16 Ld PDIP	E16.3
HI1-5046A-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5046A-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5047-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5047-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5047-5	0 to 75	16 Ld PDIP	E16.3
HI1-5047A-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5047A-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5047A-5	0 to 75	16 Ld PDIP	E16.3
HI1-5048-5	0 to 75	16 Ld CERDIP	F16.3
HI3-5048-5	0 to 75	16 Ld PDIP	E16.3
HI1-5048-2	-55 to 125	16 Ld CERDIP	F16.3

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-5049-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5049-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5049-5	0 to 75	16 Ld PDIP	E16.3
HI1-5050-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5050-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-5050-5	0 to 75	16 Ld PDIP	E16.3
HI1-5051-5	0 to 75	16 Ld CERDIP	F16.3
HI1-5051-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-5051-7	0 to 75 + 96 Hr. Burn-In	16 Ld CERDIP	F16.3
HI4P5051-5	0 to 75	20 Ld PLCC	N20.35
HI3-5051-5	0 to 75	16 Ld PDIP	E16.3
HI1-5040/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5041/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5042/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5043/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5044/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5045/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5046/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5046A/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5047/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5047A/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5048/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5049/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5050/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-5051/883	-55 to 125	16 Ld CERDIP	F16.3
HI4-5043/883	-55 to 125	20 Lead CLCC	J20.A
HI4-5045/883	-55 to 125	20 Lead CLCC	J20.A
HI4-5051/883	-55 to 125	20 Lead CLCC	J20.A
HI9P5043-5	0 to 75	16 Ld SOIC	M16.15
HI9P5045-5	0 to 75	16 Ld SOIC	M16.15
HI9P5051-5	0 to 75	16 Ld SOIC	M16.15
HI9P5043-9	-40 to 85	16 Ld SOIC	M16.15
HI9P5051-9	-40 to 85	16 Ld SOIC	M16.15

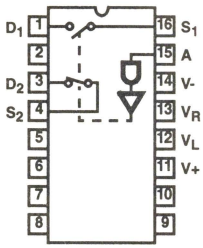
Pin Configurations Switch States are Logic "0" Input

SINGLE CONTROL

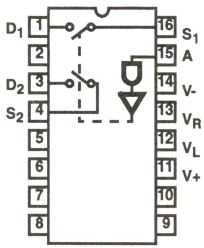
SPST
HI-5040 (50Ω)



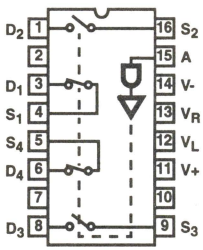
SPDT
HI-5042 (50Ω), HI-5050 (25Ω)



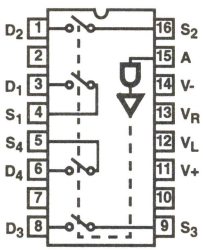
DPST
HI-5044 (50Ω)



DPDT
HI-5046 (50Ω), HI-5046A (25Ω)

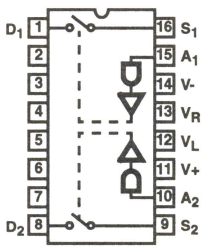


4PST
HI-5047 (50Ω), HI-5047A (25Ω)

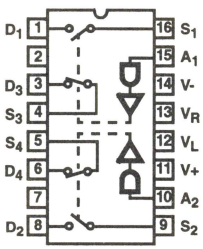


DUAL CONTROL

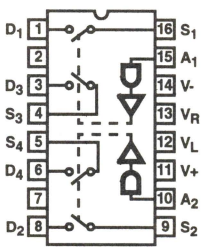
DUAL SPST
HI-5041 (50Ω)



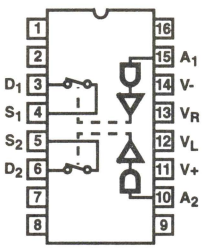
DUAL SPDT
HI-5043 (50Ω), HI-5051 (25Ω)



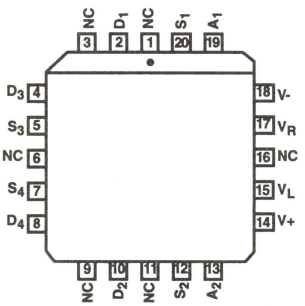
DUAL DPST
HI-5045 (50Ω), HI-5049 (25Ω)



DUAL SPST
HI-5048 (25Ω)



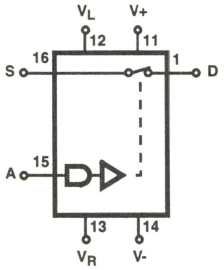
DUAL SPDT
HI-5043 (50Ω), HI-5051 (25Ω)



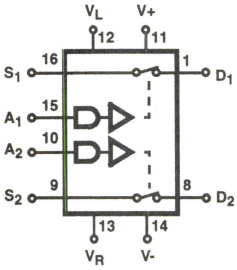
NOTE: Unused pins may be internally connected. Ground all unused pins.

Switch Functions Switch States are Logic "1" Input

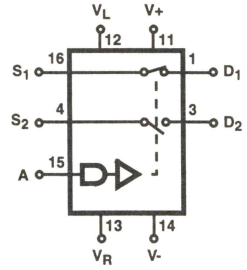
SPST
HI-5040 (50Ω)



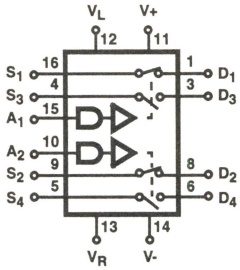
DUAL SPST
HI-5041 (50Ω)



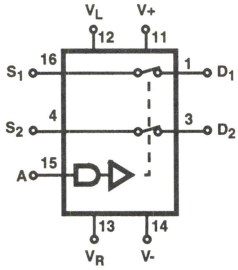
SPDT
HI-5042 (50Ω)



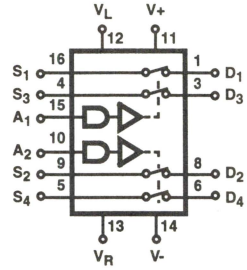
DUAL SPDT
HI-5043 (50Ω)



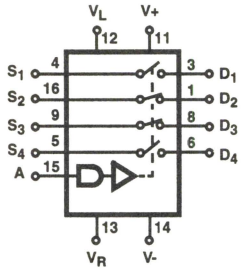
DPST
HI-5044 (50Ω)



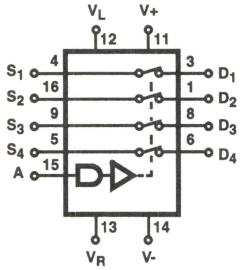
DUAL DPST
HI-5045 (50Ω)



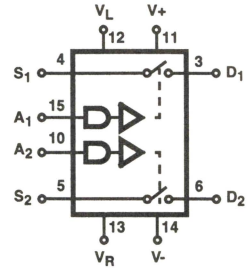
DPDT
HI-5046 (50Ω), HI-5046A (25Ω)



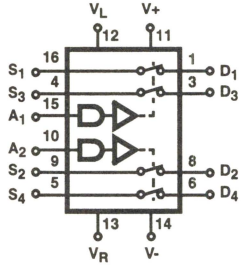
4PST
HI-5047 (50Ω), HI-5047A (25Ω)



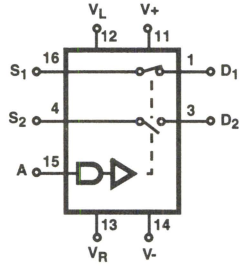
DUAL SPST
HI-5048 (25Ω)



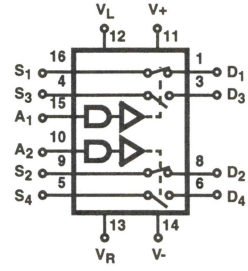
DUAL DPST
HI-5049 (25Ω)



SPDT
HI-5050 (25Ω)



DUAL SPDT
HI-5051 (25Ω)



Absolute Maximum Ratings

Supply Voltage (V+, V-) 36V
V_R to Ground . . . . . .V+, V-
Digital and Analog Input Voltage . . . $+V_{SUPPLY}$ +4V, $-V_{SUPPLY}$ -4V
Analog Current (S to D) Continuous. 30mA
Analog Current (S to D) Peak. 80mA

Operating Conditions

Temperature Range
HI-50XX-2. . . . . .-55°C to 125°C
HI-50XX-5, -7 . . . . . .0°C to 75°C
HI-50XX-9. . . . . .-40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	85	32
SOIC Package	120	N/A
PDIP Package	100	N/A
PLCC Package	80	N/A
CLCC Package	65	14

Maximum Junction Temperature
Plastic Packages . . . . . 150°C
Ceramic Packages. . . . . 175°C
Maximum Storage Temperature . . . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s). . . . . 300°C
(PLCC, SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, V_L = +5V, Unless Otherwise Specified. For Test Conditions, Consult Performance Characteristics, Unused Pins are Grounded

PARAMETER	TEST CONDITIONS	TEMP (°C)	-55°C TO 125°C			0°C TO 75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
t_{ON}, Switch On Time	(Note 5)	25	-	370	500	-	370	500	ns
t_{OFF}, Switch Off Time	(Note 5)	25	-	280	500	-	280	500	ns
Charge Injection	(Note 3)	25	-	5	20	-	5	-	mV
"Off Isolation"	(Note 4)	25	75	80	-	-	80	-	dB
"Crosstalk"	(Note 4)	25	80	88	-	-	88	-	dB
$C_{S(OFF)}$, Input Switch Capacitance		25	-	11	-	-	11	-	pF
$C_{D(OFF)}$, Output Switch Capacitance		25	-	11	-	-	11	-	pF
$C_{D(ON)}$, Output Switch Capacitance		25	-	22	-	-	22	-	pF
C_A, Digital Input Capacitance		25	-	5	-	-	5	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance		25	-	0.5	-	-	0.5	-	pF
DIGITAL INPUT CHARACTERISTICS									
V_{AL}, Input Low Threshold		Full	-	-	0.8	-	-	0.8	V
V_{AH}, Input High Threshold		Full	2.4	-	-	2.4	-	-	V
I_A, Input Leakage Current (High or Low)		Full	-	0.01	1.0	-	0.01	1.0	µA
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range		Full	-15	-	+15	-15	-	+15	V
r_{ON}, On Resistance	(Note 2A)	25	-	50	75	-	50	75	Ω
		Full	-	-	150	-	-	150	Ω
r_{ON}, On Resistance	(Note 2B)	25	-	25	45	-	25	45	Ω
		Full	-	-	50	-	-	50	Ω
r_{ON}, Channel-to-Channel Match	(Note 2A)	25	-	2	10	-	2	10	Ω
r_{ON}, Channel-to-Channel Match	(Note 2B)	25	-	1	5	-	1	5	Ω

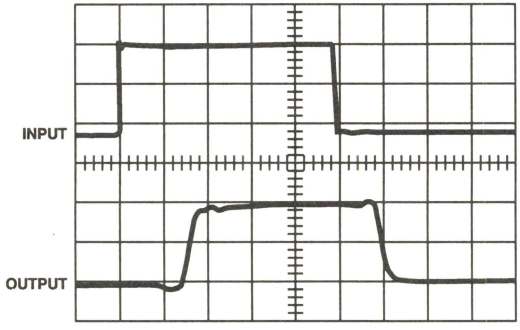
Electrical Specifications Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, V_L = +5V, Unless Otherwise Specified. For Test Conditions, Consult Performance Characteristics, Unused Pins are Grounded **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	-55°C TO 125°C			0°C TO 75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{S(OFF)} = I_{D(OFF)}$, Off Input or Output Leakage Current		25	-	0.8	2	-	0.8	2	nA
		Full	-	100	200	-	100	200	nA
$I_{D(ON)}$, On Leakage Current		25	-	0.01	2	-	0.01	2	nA
		Full	-	2	200	-	2	200	nA
POWER REQUIREMENTS									
P_D, Quiescent Power Dissipation		25	-	1.5	-	-	1.5	-	mW
I+, I-, I_L, I_R		25	-	-	0.2	-	-	0.3	mA
I+, +15V Quiescent Current	(Note 5)	Full	-	-	0.3	-	-	0.5	mA
I-, -15V Quiescent Current	(Note 5)	Full	-	-	0.3	-	-	0.5	mA
I_L, +5V Quiescent Current	(Note 5)	Full	-	-	0.3	-	-	0.5	mA
I_R, Ground Quiescent Current	(Note 5)	Full	-	-	0.3	-	-	0.5	mA

NOTES:

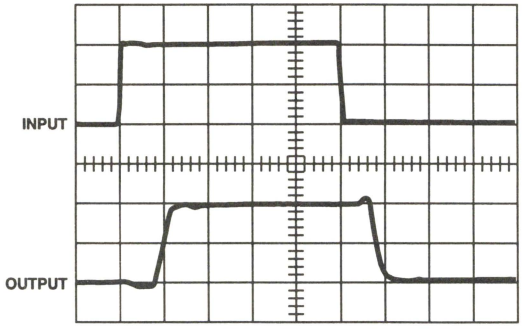
2. V_{OUT} = ±10V, I_{OUT} = ∓1mA
   A). For HI-5040 thru HI-5047
   B). For HI-5048 thru HI-5051, HI-5046A/5047A.
3. V_{IN} = 0V, C_L = 10,000pF.
4. R_L = 100Ω, f = 100kHz, V_{IN} = 2.0V_{P-P}, C_L = 5pF.
5. V_{AL} = 0V, V_{AH} = 5V.

Switching Waveforms



Top: TTL Input (1V/Div.)
V_{AH} = 5V, V_{AL} = 0V
Bottom: Output (2V/Div.)
Horizontal: 200ns/Div.

FIGURE 1.



Top: CMOS Input (5V/Div.)
V_{AH} = 10V, V_{AL} = 0V
Bottom: Output (5V/Div.)
Horizontal: 200ns/Div.

FIGURE 2.

Typical Performance Curves and Test Circuits

$T_A = 25^oC$, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3V and V_{AL} = 0.8V, Unless Otherwise Specified

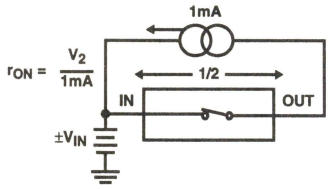


FIGURE 3. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE

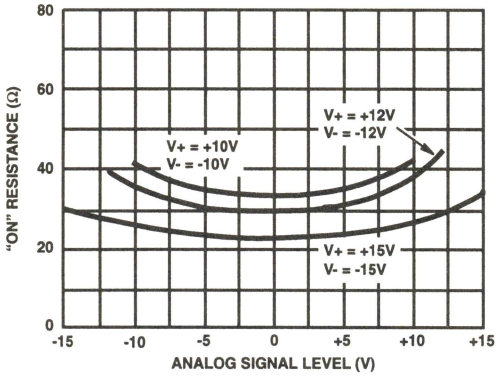


FIGURE 4. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

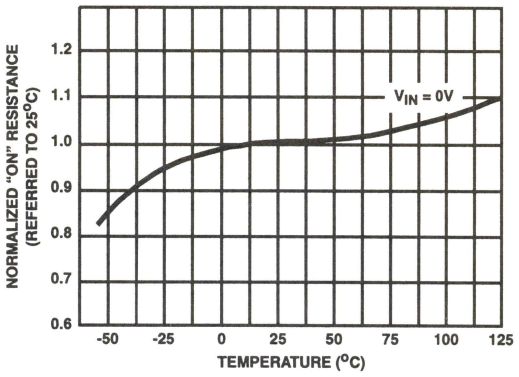
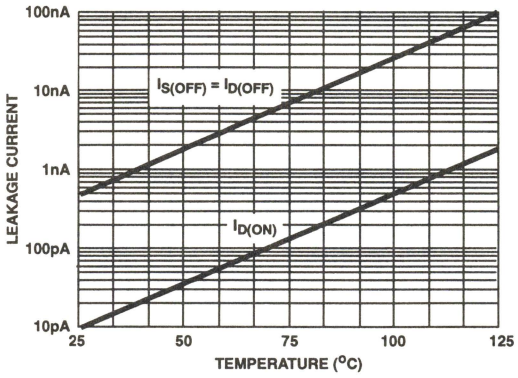
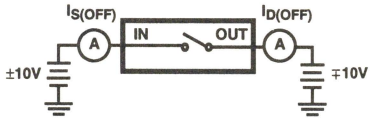


FIGURE 5. NORMALIZED "ON" RESISTANCE vs TEMPERATURE



OFF LEAKAGE CURRENT vs TEMPERATURE



ON LEAKAGE CURRENT vs TEMPERATURE

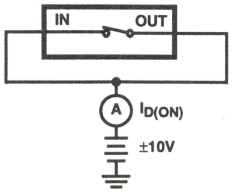
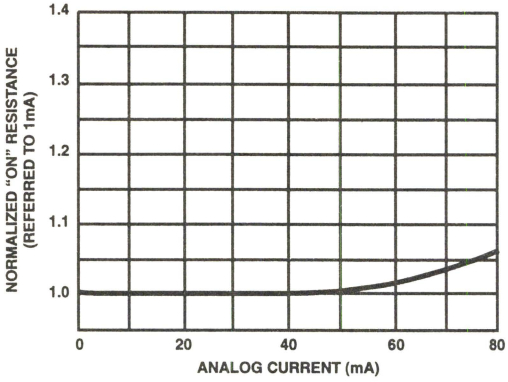


FIGURE 6. ON/OFF LEAKAGE CURRENT vs TEMPERATURE

Typical Performance Curves and Test Circuits

$T_A = 25^oC$, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3V and V_{AL} = 0.8V, Unless Otherwise Specified **(Continued)**



"ON" RESISTANCE vs ANALOG CURRENT

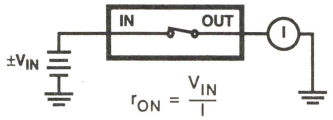
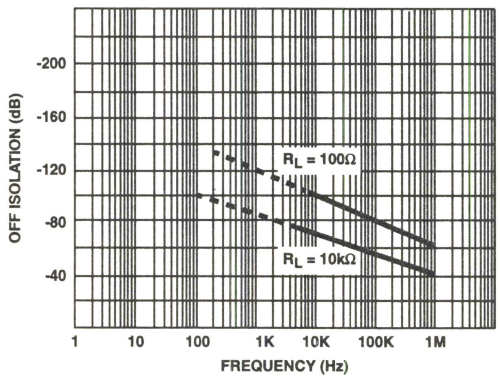
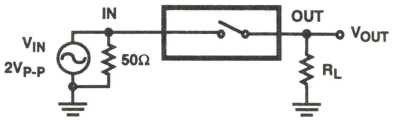


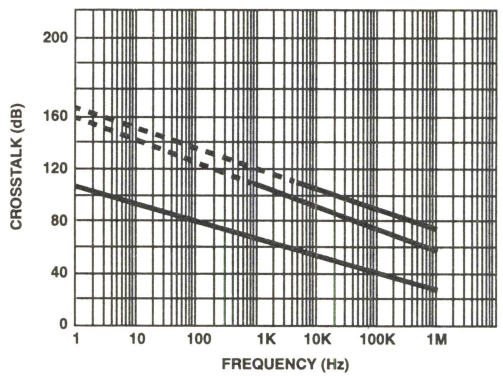
FIGURE 7. NORMALIZED "ON" RESISTANCE vs ANALOG CURRENT

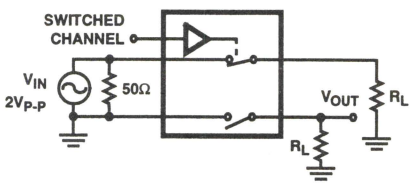




$$\text{OFF ISOLATION} = 20\ \text{Log}\left(\frac{V_{IN}}{V_{OUT}}\right)$$

FIGURE 8. "OFF" ISOLATION vs FREQUENCY



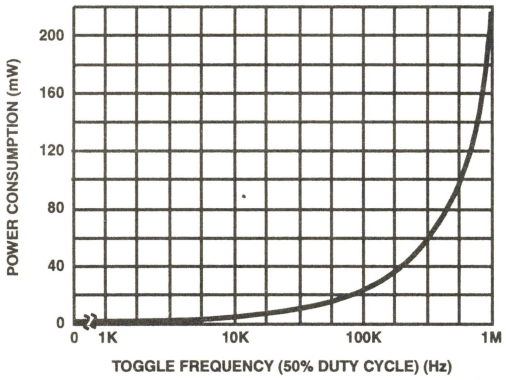


$$\text{CROSSTALK} = 20\ \text{Log}\left(\frac{V_{IN}}{V_{OUT}}\right)$$

FIGURE 9. CROSSTALK vs FREQUENCY

Typical Performance Curves and Test Circuits

$T_A = 25^oC$, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3V and V_{AL} = 0.8V, Unless Otherwise Specified **(Continued)**



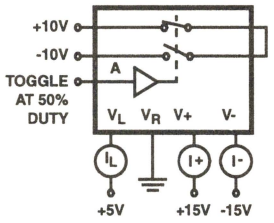


FIGURE 10. POWER CONSUMPTION vs FREQUENCY

Switching Characteristics

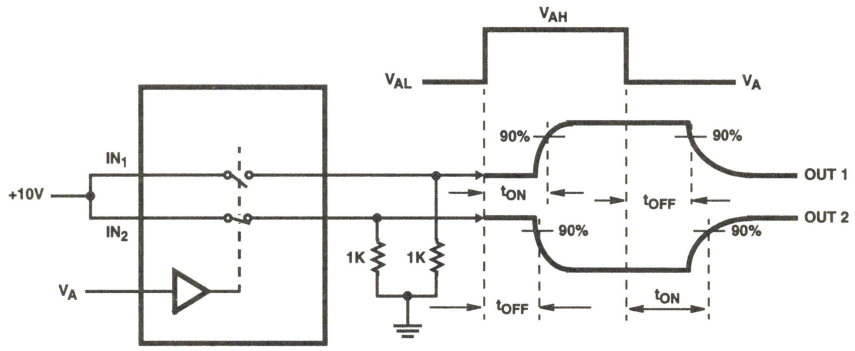


FIGURE 11. ON/OFF SWITCH TIME vs LOGIC LEVEL

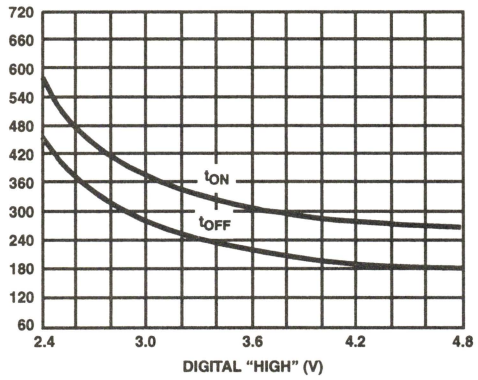


FIGURE 12. SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION

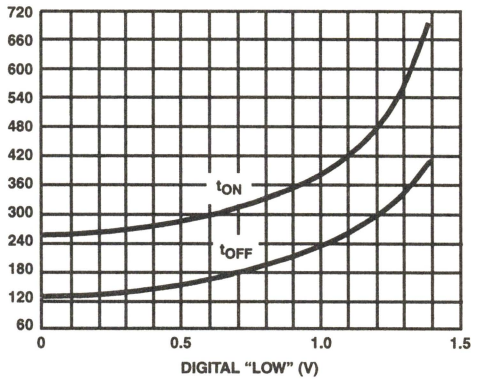
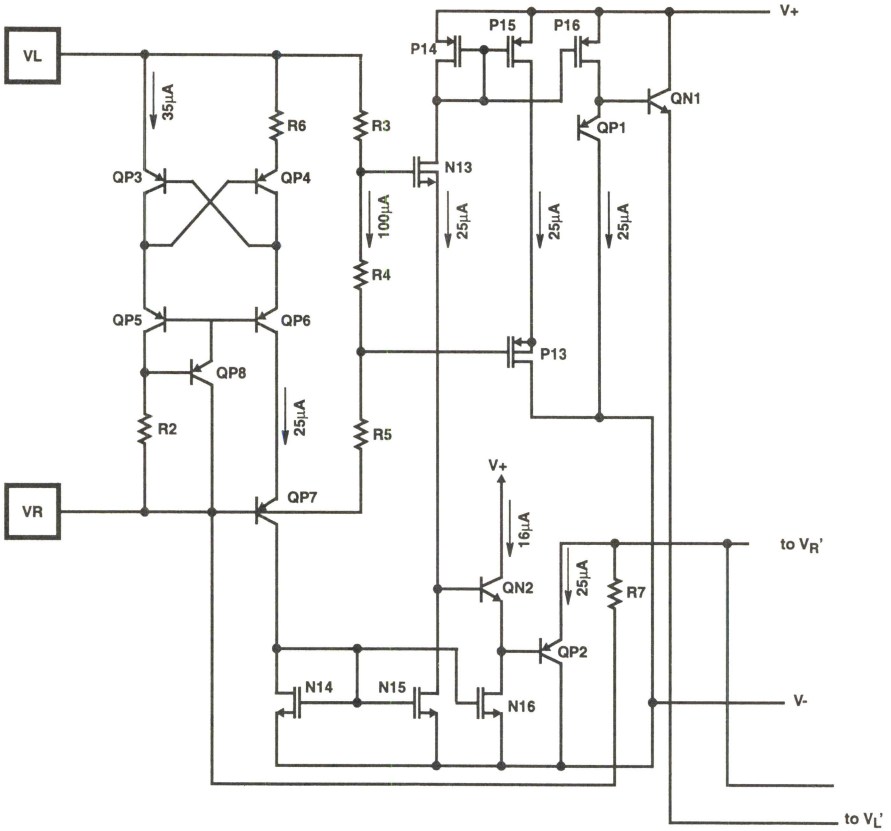


FIGURE 13. SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION

Switching Characteristics (Continued)



NOTE: Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

FIGURE 14. TTL/CMOS REFERENCE CIRCUIT (NOTE)

Switching Characteristics (Continued)

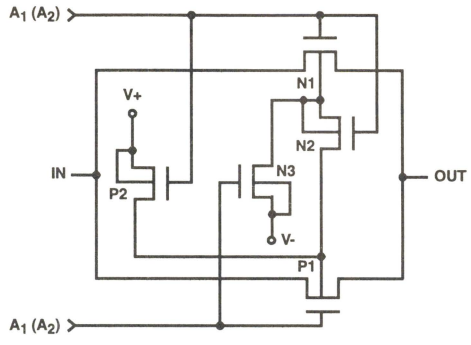
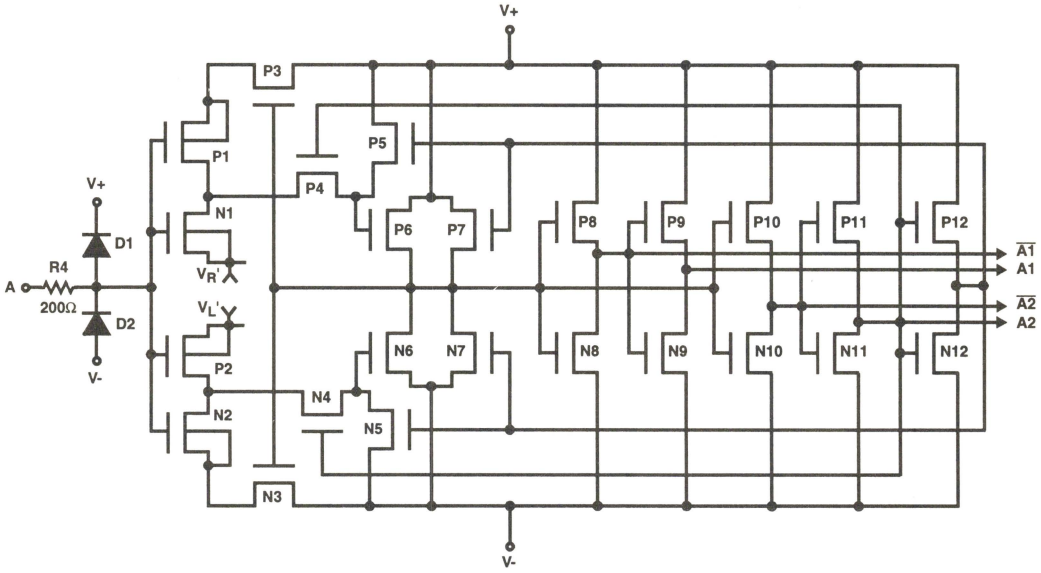


FIGURE 15. SWITCH CELL



NOTES:

1. All N-Channel bodies to V-, all P-Channel bodies to V+ except as shown.
2. For further information refer to Application Notes AN520, AN521, AN531, AN532 and AN557.

FIGURE 16. DIGITAL INPUT BUFFER AND LEVEL SHIFTER

HARRIS SEMICONDUCTOR

IH5043

August 1997

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

Dual SPDT CMOS Analog Switch

Features

- See HI504X and IH514X for Other Functions
- Dual SPDT
- Switches Greater than $20V_{P-P}$ Signals with ±15V Supplies
- Quiescent Current Less than 1mA
- Break-Before-Make Switching t_{OFF} 200ns, t_{ON} 300ns (Typ)
- TTL, DTL, CMOS, PMOS Compatible

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
IH5043MJE	-55 to 125	16 Ld CERDIP	F16.3
IH5043CJE	0 to 70	16 Ld CERDIP	F16.3
IH5043CPE	0 to 70	16 Ld PDIP	E16.3
IH5043CY	0 to 70	16 Ld SOIC	M16.15
IH5043MJE/883B	-55 to 125	16 Ld CERDIP	F16.3

Description

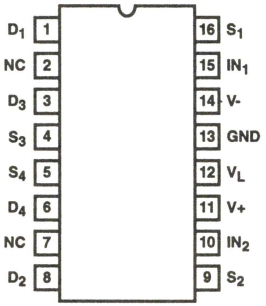
The IH5043 analog switch uses an improved, high voltage CMOS monolithic technology. These devices provide ease of use and performance advantages not previously available from solid state switches.

Key performance advantage is TTL compatibility and ultra low power operation. The quiescent current requirement is less than 1mA. Also, the IH5043 guarantees Break-Before-Make switching, accomplished by extending the t_{ON} time (300ns Typ), so that it exceeds t_{OFF} time (200ns Typ). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is eliminated.

The IH5043 is a pin-for-pin, improved performance replacement for other analog switches.

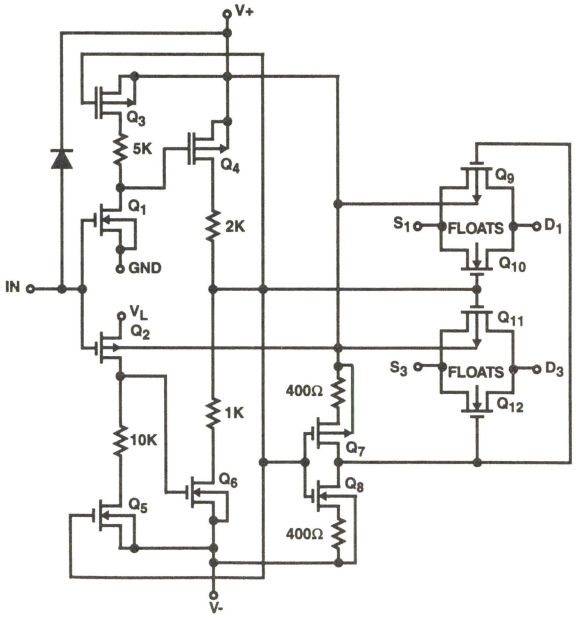
Pinout

IH5043
(CERDIP, PDIP, SOIC)
TOP VIEW



Functional Block Diagram

FUNCTIONAL DRIVER, TYPICAL DRIVER, GATE ($^1/_2$ AS SHOWN)



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **3130.1**

IH5052, IH5053

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

Quad CMOS Analog Switches

Features

- Switches Greater Than $20V_{P-P}$ Signals with ±15V Supplies
- Quiescent Current ..... <10µA
- Break-Before-Make Switching
  - t_{OFF} (Typ)..... 500ns
  - t_{ON} (Typ)..... 1000ns
- TTL, CMOS Compatible
- IH5052 4 Normally Closed Switches
- IH5053 4 Normally Open Switches
- Low $r_{DS(ON)}$ (Typ) 80Ω

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
IH5052CDE	-0 to 70	16 Ld SBDIP	D16.3
IH5052MDE	-55 to 125	16 Ld SBDIP	D16.3
IH5053CDE	-0 to 70	16 Ld SBDIP	D16.3
IH5053MDE	-55 to 125	16 Ld SBDIP	D16.3

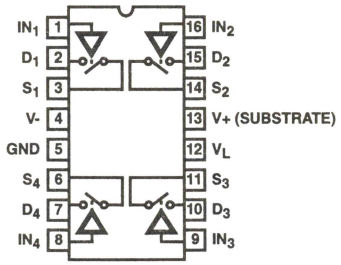
Description

The IH5052, IH5053 analog switches use an improved, high voltage CMOS technology, which provides performance advantages not previously available from solid state switches. Key performance advantages are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 10µA.

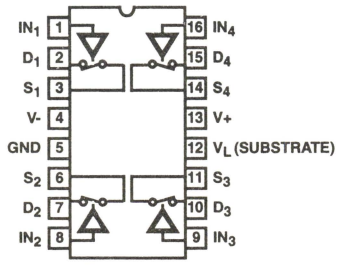
The IH5052, IH5053 also guarantees Break-Before-Make switching. This is accomplished by extending the t_{ON} time (1000ns) such that it exceeds t_{OFF} time (500ns). This insures that an ON channel will be turned OFF before an OFF channel can turn ON, and eliminates the need for external logic required to avoid channel to channel shorting during switching. With a logic "0" (0.8V or less) at its control inputs, the IH5052 switches are closed, while the IH5053 switches are closed with a logic "1" (2.4V or more) at its control inputs.

Pinouts

IH5052 (SBDIP)
TOP VIEW



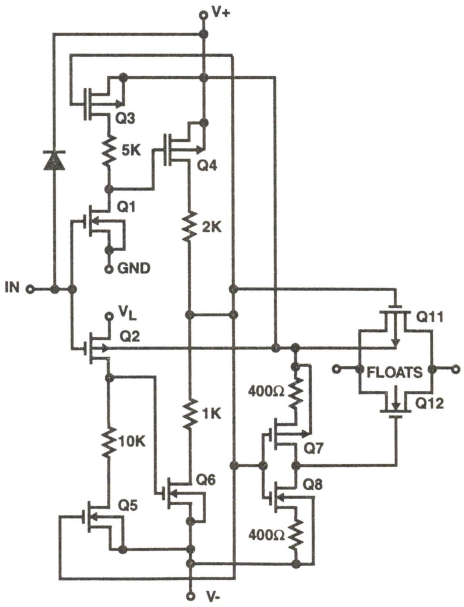
IH5053 (SBDIP)
TOP VIEW



Switch states shown for logic "1" input

Functional Diagram

($^1/_4$ AS SHOWN)



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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File Number 3131.1

HARRIS SEMICONDUCTOR

IH5151

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

August 1997

Dual SPDT, CMOS Analog Switch

Features

- Low $r_{DS(ON)}$ 25Ω
- Switches Greater than $20V_{P-P}$ Signals with ±15V Supplies
- Quiescent Current ..... <100μA
- Break-Before-Make Switching
  - t_{OFF} ..... 120ns (Typ)
  - t_{ON} ..... 200ns (Typ)
- TTL, CMOS Compatible
- Complete Monolithic Construction
- Supply Range ..... ±5V to ±15V

Description

The IH5151 solid state analog switch is designed using an improved, high voltage CMOS technology.

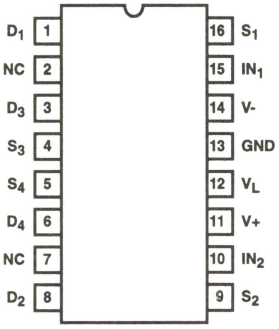
Key performance advantages in the IH5151 are TTL compatibility and ultra low power operation. $r_{DS(ON)}$ switch resistance is typically in the 14Ω to 18Ω area, for signals in the -10V to +10V range. Quiescent current is less than 10μA. The IH5151 also guarantees Break-Before-Make switching which is logically accomplished by extending the t_{ON} time (200ns typical) such that it exceeds t_{OFF} time (120ns typical). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is thus eliminated.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
IH5151CJE	0 to 70	16 Ld CERDIP	F16.3
IH5151MJE	-55 to 125	16 Ld CERDIP	F16.3
IH5151MJE/883B	-55 to 125	16 Ld CERDIP	F16.3

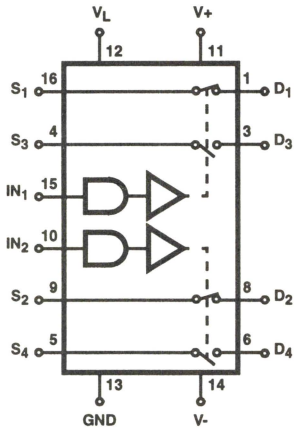
Pinout

IH5151
(CERDIP)
TOP VIEW



Switching State Diagram

SWITCH STATE SHOWN FOR LOGIC "I" INPUT



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 3133.1

HARRIS SEMICONDUCTOR

IH5341, IH5352

Dual SPST, Quad SPST, CMOS RF/Video Switches

August 1997

Features

- $r_{DS(ON)}$ . . . . . <75Ω
- Switch Attenuation Varies Less Than 3dB From DC to 100MHz
- "OFF" Isolation at 10MHz (Typ) . . . . . >70dB
- Cross Coupling Isolation at 10MHz . . . . . >60dB
- Compatible With TTL, CMOS Logic
- Wide Operating Power Supply Range
- Power Supply Current . . . . . <1μA
- "Break-Before-Make" Switching
- Fast Switching (Typ) 80ns/150ns

Applications

- Video Switch
- Communications Equipment
- Disk Drives
- Instrumentation
- CATV

Description

The IH5341 (IH5352) is a dual (quad) SPST, CMOS monolithic switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically t_{ON} = 150ns and t_{OFF} = 80ns. "Break-Before-Make" switching is guaranteed.

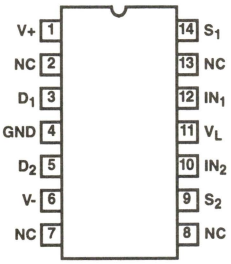
Switch "ON" resistance is typically 40Ω - 50Ω with ±15V power supplies, increasing to typically 175Ω for ±5V supplies.

Ordering Information

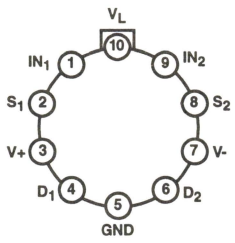
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
IH5341CPD	0 to 70	14 Ld PDIP	E14.3
IH5341ITW	-25 to 85	10 Pin Metal Can (TO-100)	T10.B
IH5341MTW	-55 to 125	10 Pin Metal Can (TO-100)	T10.B
IH5341MTW/883B	-55 to 125	10 Pin Metal Can (TO-100)	T10.B
IH5352CPE	0 to 70	16 Ld PDIP	E16.3
IH5352IJE	-25 to 85	16 Ld CERDIP	F16.3
IH5352MJE	-55 to 125	16 Ld CERDIP	F16.3
IH5352MJE/883B	-55 to 125	16 Ld CERDIP	F16.3
IH5352CBP	0 to 70	20 Ld SOIC	M20.3
IH5352IBP	-25 to 85	20 Ld SOIC	M20.3

Pinouts

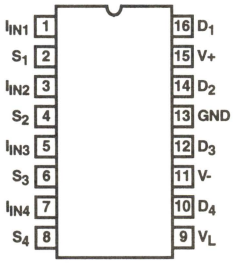
IH5341 (PDIP) TOP VIEW



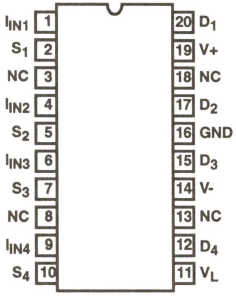
IH5341 (METAL CAN) TOP VIEW



IH5352 (CERDIP, PDIP) TOP VIEW



IH5352 (SOIC) TOP VIEW



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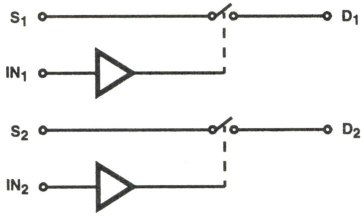
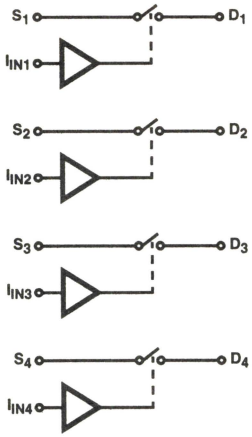
File Number **3134.1**

Functional Block Diagrams

IH5341

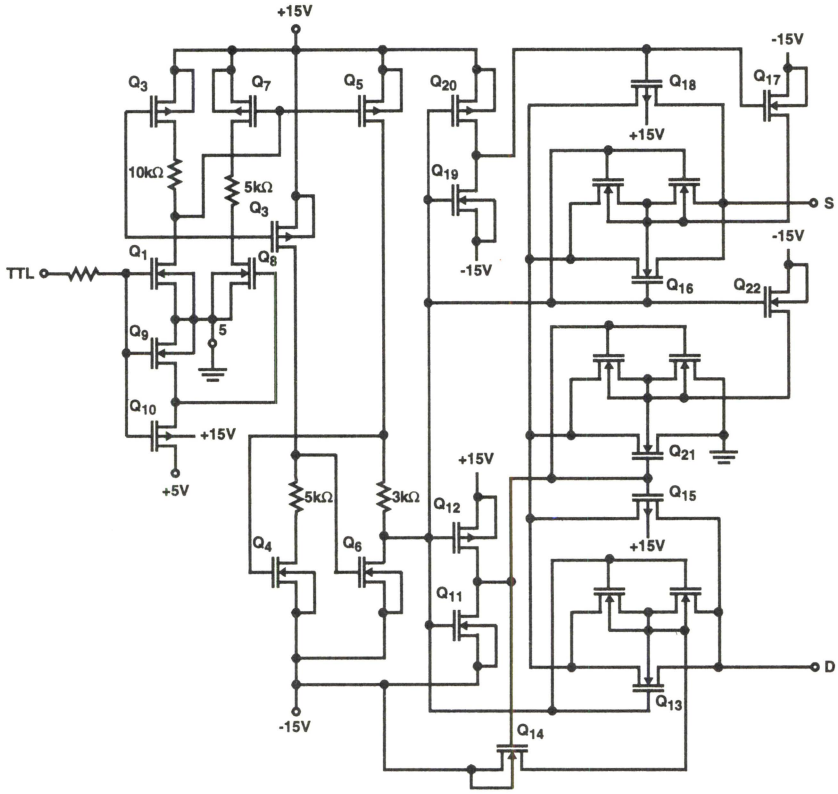


IH5352



Switches are open for a logic "0" control input, and closed for a logic "1" control input.

Schematic Diagram ($^1/_2$ IH5341, $^1/_4$ IH5352)



Absolute Maximum Ratings

V+ to Ground . . . . . +18V
V- to Ground . . . . . -18V
V_L to Ground . . . . . V+ to V-
Logic Control Voltage . . . . . V+ to V-
Analog Input Voltage . . . . . V+ to V-
Current (Any Terminal) 50mA

Operating Conditions

Temperature Ranges
(M Version) . . . . . -55^oC to 125^oC
(I Version) . . . . . -25^oC to 85^oC
(C Version) . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	75	18
Metal Can Package	160	75
SOIC Package	90	N/A
14 Ld PDIP Package	100	N/A
16 Ld PDIP Package	90	N/A

Maximum Junction Temperature (Ceramic Packages) . . . . . 175^oC
Maximum Junction Temperature (Plastic Packages) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V+ = +15V$, $V_L = +5V$, $V- = -15V$, $T_A = 25^oC$ Unless Otherwise Specified

PARAMETER	TEST CONDITIONS		(NOTE 2) TYP	M GRADE DEVICE			I/C GRADE DEVICE			UNITS
				-55^oC	25^oC	125^oC	-25^oC/ 0^oC	25^oC	85^oC/ 70^oC	
DC CHARACTERISTICS										
Supply Voltage Ranges	(Note 4)									
Positive Supply, V+			5 to 15	-	-	-	-	-	-	V
Logic Supply, V_L			5 to 15	-	-	-	-	-	-	V
Negative Supply, V-			-5 to -15	-	-	-	-	-	-	V
Switch "ON" Resistance, $r_{DS(ON)}$	$V_D = \pm5V$, $I_S = 10mA$, $V_{IN} \geq 2.4V$ (Note 5)		50	75	75	100	75	75	100	Ω
	$V_D = \pm10V$, $I_S = 10mA$, $V_{IN} \geq 2.4V$ (Note 5)		100	125	125	175	150	150	175	Ω
Switch "ON" Resistance, $r_{DS(ON)}$	$V+ = V_L = +5V$, $V_{IN} = 3V$, $V- = -5V$, $V_D = \pm3V$, $I_S = 10mA$		175	250	250	350	300	300	350	Ω
On Resistance Match Between Channels, $\Delta r_{DS(ON)}$	$I_S = 10mA$, $V_D = \pm5V$		5	-	-	-	-	-	-	Ω
Logic "I" Input Voltage, V_{IH}			>2.4	-	-	-	-	-	-	V
Logic "0" Input Voltage, V_{IL}			<0.8	-	-	-	-	-	-	V
Switch "OFF" Leakage, $I_{D(OFF)}$ or $I_{S(OFF)}$	$V_{S/D} = \pm5V$ or $\pm14V$, $V_{IN} \leq 0.8V$ (Notes 3 and 5)	IH5341	-	-	±0.5	50	-	±1	100	nA
		IH5352	-	-	±1	50	-	±2	100	nA
Switch "ON" Leakage, $I_{D(ON)} + I_{S(ON)}$	$V_{S/D} = \pm5V$, $V_{IN} \geq 2.4V$	IH5341	-	-	±1	50	-	±2	100	nA
	$V_{S/D} = \pm14V$, $V_{IN} \geq 2.4V$		-	-	±1	100	-	±2	100	nA
	$V_{S/D} = \pm5V$ or $\pm14V$, $V_{IN} \leq 0.8V$	IH5352	-	-	±1	100	-	±2	100	nA
Input Logic Current, I_{IN}	$V_{IN} > 2.4V$ or $< 0V$		0.1	±1	±1	10	±1	±1	10	mA
Positive Supply Quiescent Current, I+	$V_{IN} = 0V$ or $+5V$		0.1	1	1	10	1	1	10	mA
Negative Supply Quiescent Current, I-	$V_{IN} = 0V$ or $+5V$		0.1	1	1	10	1	1	10	µA
Logic Supply Quiescent Current, I_L	$V_{IN} = 0V$ or $+5V$		0.1	1	1	10	1	1	10	µA
AC CHARACTERISTICS										
Switch "ON" Time, t_{ON}			-	-	150	300	-	-	-	ns
Switch "OFF" Time, t_{OFF}			-	-	80	150	-	-	-	ns

Electrical Specifications $V+ = +15V$, $V_L = +5V$, $V- = -15V$, $T_A = 25^oC$ Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 2) TYP	M GRADE DEVICE			I/C GRADE DEVICE			UNITS
			-55°C	25°C	125°C	-25°C/ 0°C	25°C	85°C/ 70°C	
"OFF" Isolation Rejection Ratio, OIRR		-	-	70	-	-	-	-	dB
Cross Coupling Rejection Ratio, CCRR		-	-	60	-	-	-	-	dB
Switch Attenuation 3dB Frequency, f_{3dB}		-	-	100	-	-	-	-	MHz

NOTES:

2. Typical values are not tested in production. They are given as a design aid only.
3. Positive and negative voltages applied to opposite sides of switch, in both directions successively.
4. These are the operating voltages at which the other parameters are tested, and are not directly tested.
5. The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.

Typical Performance Curves

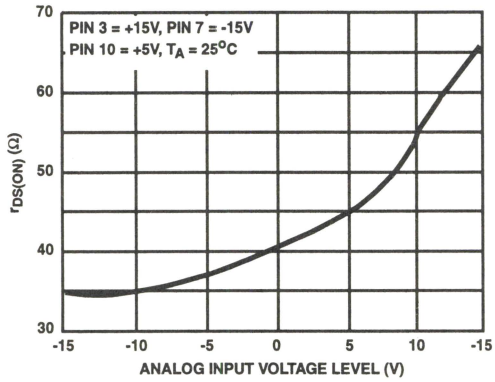


FIGURE 1. $r_{DS(ON)}$ vs ANALOG INPUT VOLTAGE WITH ±15V POWER SUPPLIES

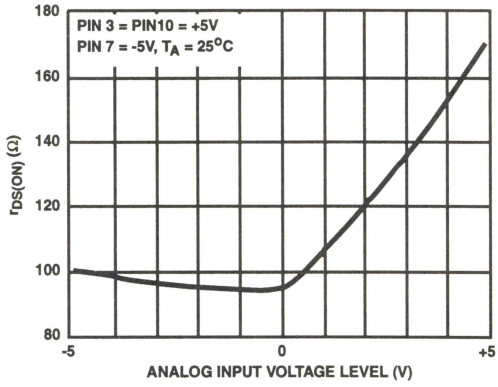


FIGURE 2. $r_{DS(ON)}$ vs ANALOG INPUT LEVEL WITH ±5V POWER SUPPLIES

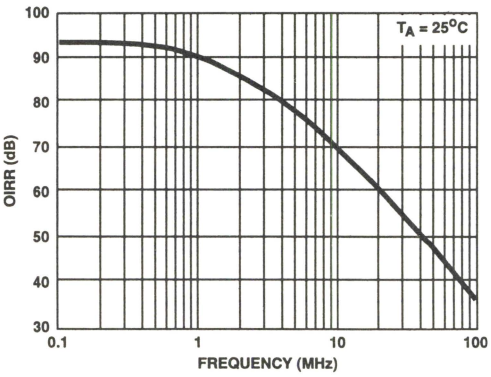


FIGURE 3. OFF ISOLATION REJECTION vs FREQUENCY (SEE FIGURE 8)

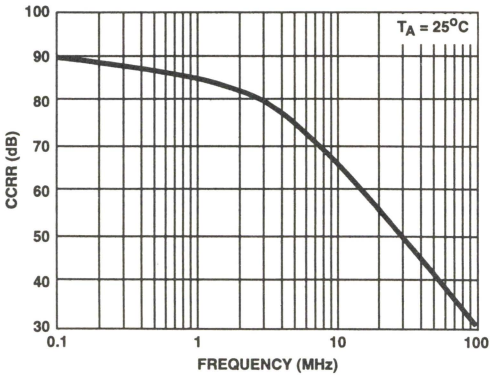


FIGURE 4. CROSS COUPLING REJECTION vs FREQUENCY (SEE FIGURE 9)

Typical Performance Curves (Continued)

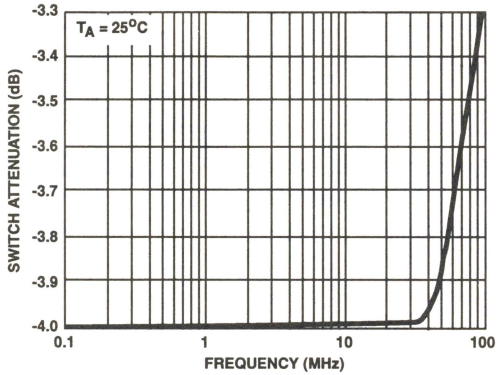
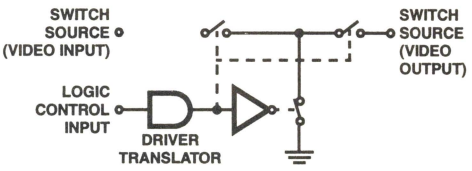


FIGURE 5. TYPICAL SWITCH ATTENUATION vs FREQUENCY (R_L = 75Ω, SEE FIGURE 10)

Detailed Description

Figure 6 shows the internal circuit of one channel of the IH5352. This is identical to the IH5341 "T-Switch" configuration. Here, a shunt switch is closed, and the two series switches are open when the video switch channel is open or off. This provides much better isolation between the input and output terminals than a simple series switch does, especially at high frequencies. The result is excellent off-isolation in the Video and RF frequency ranges when compared to conventional analog switches.

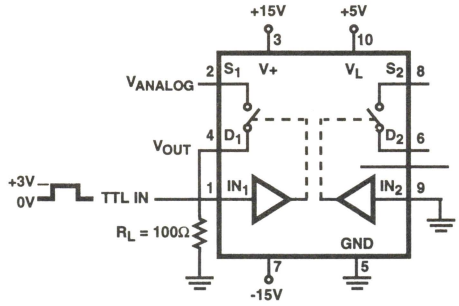
The control input level shifting circuitry is very similar to that of the IH5140 series of Analog Switches, and gives very high speed, guaranteed "Break-Before-Make" action, low static power consumption and TTL compatibility.



NOTE: 1 channel of 4 shown.

FIGURE 6. INTERNAL SWITCH CONFIGURATION

Test Circuits and Waveforms



NOTE: Only one channel shown. Other acts identically.

FIGURE 7A. SWITCHING TIME TEST CIRCUIT

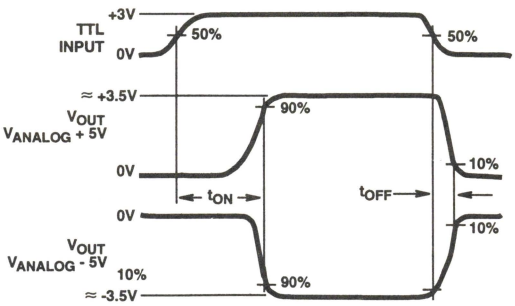
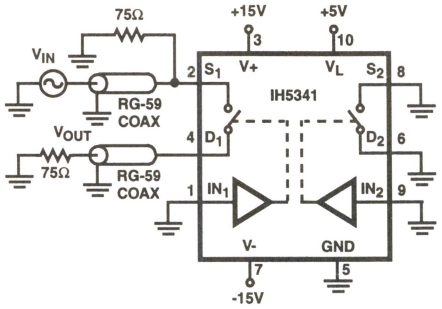


FIGURE 7B. SWITCHING TIME WAVEFORMS

Test Circuits and Waveforms (Continued)

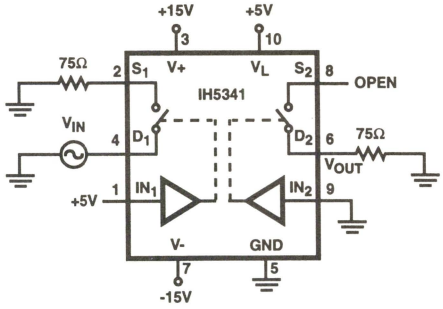


V_{IN} = ±5V(10V_{P-P}) at f = 10MHz

$$OIRR = 20Log \frac{V_{IN}}{V_{OUT}}$$

NOTE: Only one channel shown. Other acts identically.

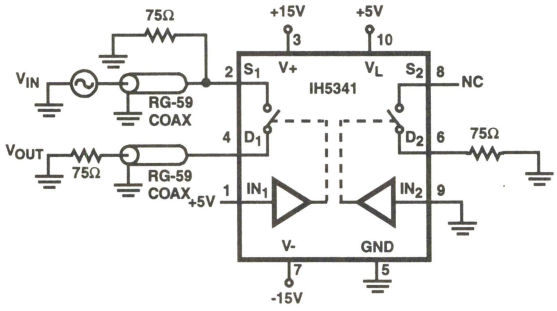
FIGURE 8. OFF ISOLATION TEST CIRCUIT



V_{IN} = 225mV_{RMS} at f = 10MHz

$$CCRR = 20Log \frac{V_{IN}}{V_{OUT}}$$

FIGURE 9. OFF ISOLATION TEST CIRCUIT



$$ATTN: = 20Log \frac{R_L}{r_{DS(ON)} + R_L}$$

Nominally, at DC, this ratio is equal to -4dB. When the attenuation reaches -1dB, the frequency at which this occurs is f_{3dB}.

NOTE: Only one channel shown. Other acts identically.

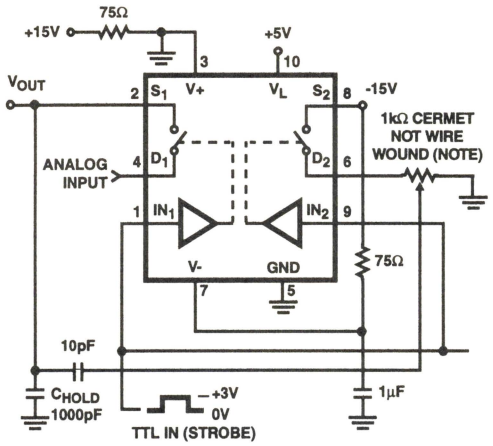
FIGURE 10. SWITCH ATTENUATION vs FREQUENCY

Typical Applications

Charge Compensation Techniques

Charge injection results from the signals out of the level translation circuit being coupled through the gate-channel and gate-source/drain capacitances to the switch inputs and outputs. This feedthrough is particularly troublesome in Sample-and-Hold or Track-and-Hold applications, as it causes a Sample (Track) to Hold offset. The IH5341 devices have a typical injected charge of 30pC-50pC (corresponding to 30mV-50mV in a 1000pF capacitor), at $V_{S/D}$ of about 0V.

This Sample (Track) to Hold offset can be compensated by bringing in a signal equal in magnitude but of the opposite polarity. The circuit of Figure 11 accomplishes this charge injection compensation by using one side of the device as a S & H (T & H) switch, and the other side as a generator of a compensating signal. The 1kΩ potentiometer allows the user to adjust the net injected charge to exactly zero for any analog voltage in the -5V to +5V range.



NOTE: Adjust pot for 0mV$_{P-P}$ step at V_{OUT} with no analog (AC) signal present.

FIGURE 11. CHARGE INJECTION COMPENSATION

Since individual parts are very consistent in their charge injection, it is possible to replace the potentiometer with a pair of fixed resistors, and achieve less than 5mV error for all devices without adjustment.

An alternative arrangement, using a standard TTL inverter to generate the required inversion, is shown in Figure 13. The capacitor needs to be increased, and becomes the only method of adjustment. A fixed value of 22pF is good for analog values referred to ground, while 35pF is optimum for AC coupled signals referred to -5V as shown in the figure. The choice of -5V is based on the virtual disappearance at this analog level of the transient component of switching charge injection. This combination will lead to a virtually "glitch-free" switch.

Overvoltage Protection

If sustained operation with no supplies but with analog signals applied is possible, it is recommended that diodes (such as 1N914) be inserted in series with the supply lines to the IH5341. Such conditions can occur if these signals come from a separate power supply or another location, for example. The diodes will be reverse biased under this type of operation, preventing heavy currents from flowing from the analog source through the IH5341.

The same method of protection will provide over ±25V overvoltage protection on the analog inputs when the supplies are present. The schematic for this connection is shown in Figure 12.

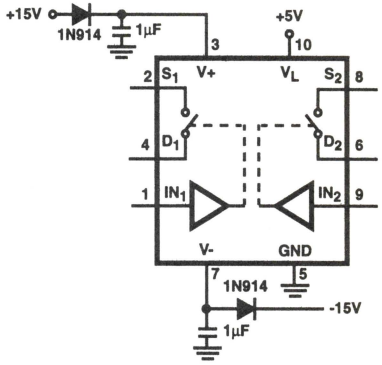


FIGURE 12. OVERVOLTAGE PROTECTION

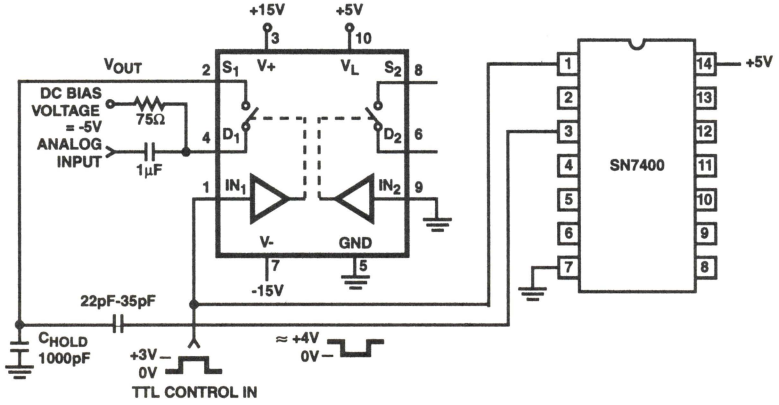


FIGURE 13. ALTERNATIVE COMPENSATION CIRCUIT

Die Characteristics

DIE DIMENSIONS:

2388µm x 2515µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

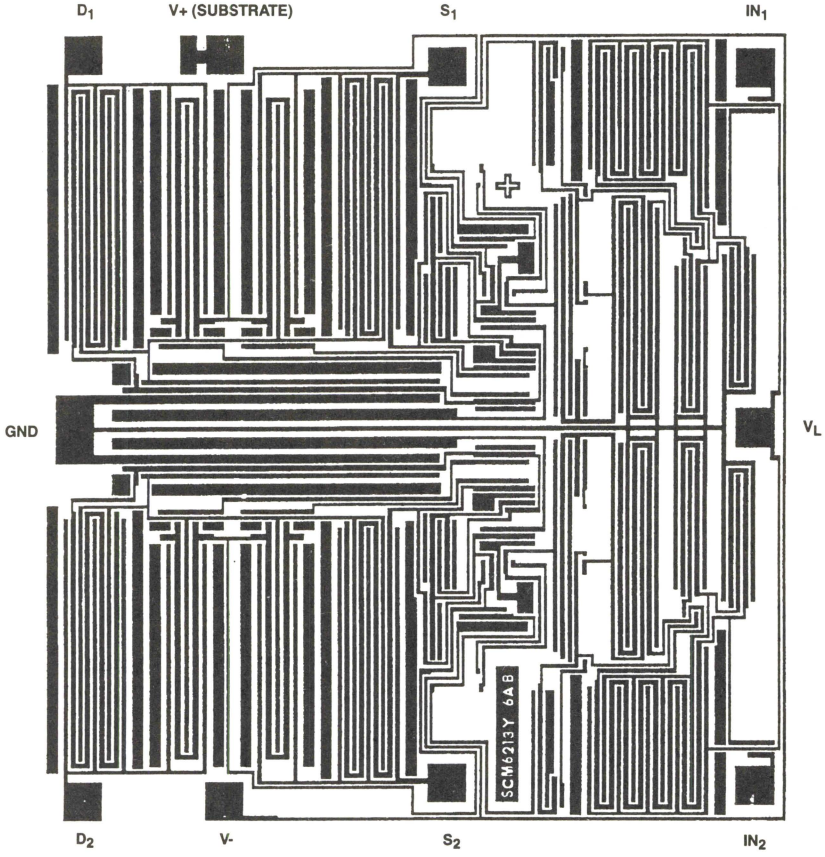
Type: PSG/Nitride
PSG Thickness: 7kÅ ±1.4kÅ
Nitride Thickness: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

IH5341



Die Characteristics

DIE DIMENSIONS:

2617µm x 5233µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

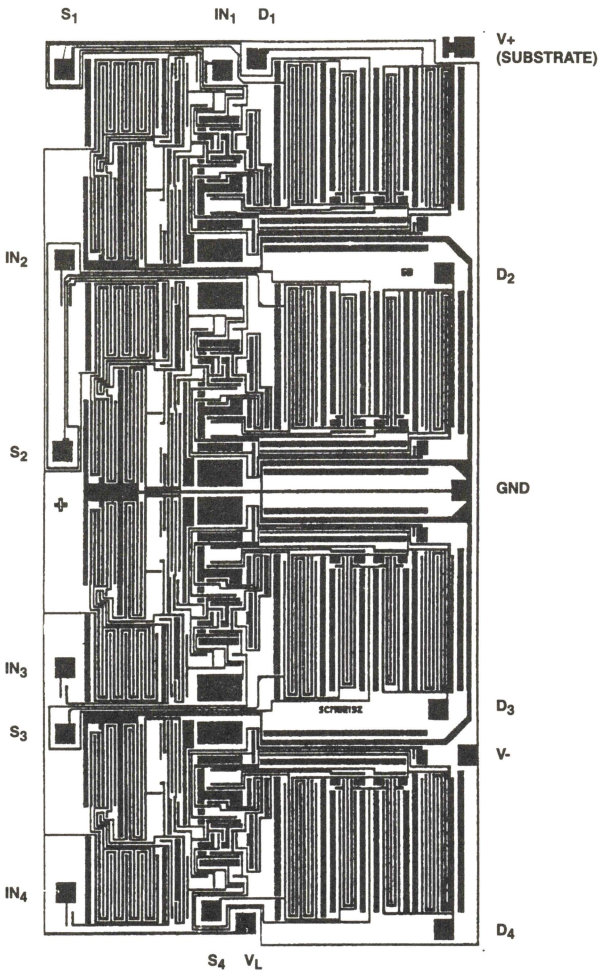
Type: PSG/Nitride
PSG Thickness: 7kÅ ±1.4kÅ
Nitride Thickness: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

IH5352



DATA ACQUISITION 14

HARRIS QUALITY AND RELIABILITY

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Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force – from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX, Quality professionals support other continuous improvement tools such as control charts, measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

True to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs – with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

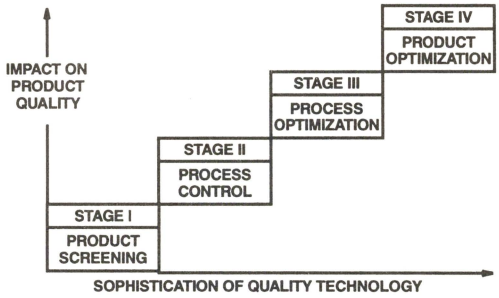


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage III to Stage IV, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

ISO 9000 Certification

The manufacturing operations of Harris Semiconductor have all received ISO certification. The ISO 9000 series of standards were very consistent with our goals to build an even stronger quality system foundation.

Qualified Manufacturing List (QML)

Harris Semiconductor has supplied military grade integrated circuits for over 20 years. The government's certifying body had audited and granted approval to ship JAN, 883 compliant, and Source Military Drawing parts used in ground and space applications. The discipline required to manufacture high reliability components has been beneficial to the commercial product lines. Harris has now taken the next evolutionary step by transitioning into QML as defined in MIL-PRF-38535. These guidelines incorporate the best commercial practices for semiconductor manufacturing.

Designing for Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	CONTROLS/MONITORS
Wafer Fab	• Internal Audits • Environmental - Room/Hood Particulates - Temperature/Humidity - Water Quality • Product - Junction Depth - Sheet Resistivities - Defect Density - Critical Dimensions - Visual Inspection - Lot Acceptance • Process - Film Thickness - Implant Dosages - Capacitance Voltage Changes - Conformance to Specification • Equipment - Repeatability - Profiles - Calibration - Preventive Maintenance
Assembly	• Internal Audits • Environmental - Room/Hood Particulates - Temperature/Humidity - Water Quality • Product - Documentation Check - Dice Inspection - Wire Bond Pull Strength/Controls - Ball Bond Shear/Controls - Die Shear Controls - Post-Bond/Pre-Seal Visual - Fine/Gross Leak - PIND Test - Lead Finish Visuals, Thickness - Solderability • Process - Operator Quality Performance - Saw Controls - Die Attach Temperatures - Seal Parameters - Seal Temperature Profile - Sta-Bake Profile - Temp Cycle Chamber Temperature - ESD Protection - Plating Bath Controls - Mold Parameters

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (Continued)

AREA	CONTROLS/MONITORS
Test	• Internal Audits • Temperature/Humidity • ESD Controls • Temperature Test Calibration • Test System Calibration/Control • Test Procedures • Control Unit Compliance • Lot Acceptance Conformance • Mechanical Outline Conformance
Probe	• Internal Audits • Wafer Repeat Correlation • Test System Calibration/Control • Visual Requirements • Temperature/Humidity • Documentation • Process Performance
Burn-In	• Internal Audits • ESD Controls • Functionality Board Check • Oven Temperature Controls • Oven Calibration • Procedural Conformance
Brand	• Internal Audits • ESD Controls • Brand Permanency • Temperature/Humidity • Procedural Conformance
QCI Inspection	• Internal Audits • ESD Controls • Group B Conformance • Group C and D Conformance

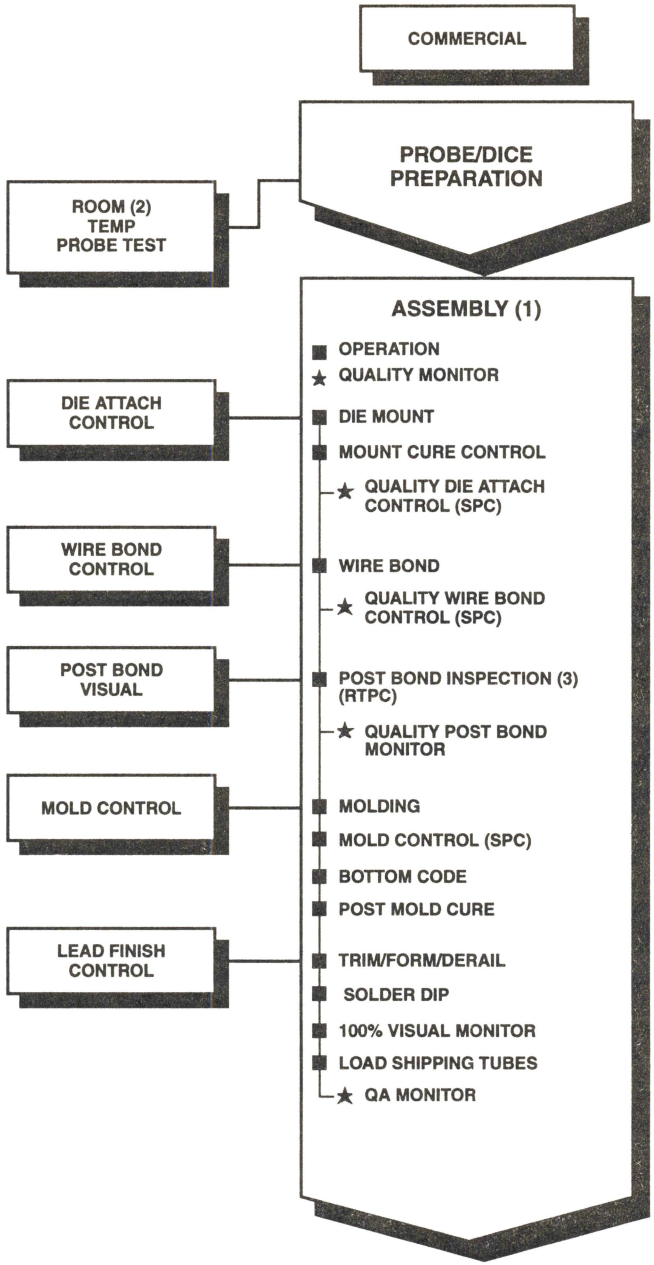
NOTE: QCI Inspection is applicable only to Hi-Rel products.

Commerical product is verified through Matrix Monitor program. Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 3).

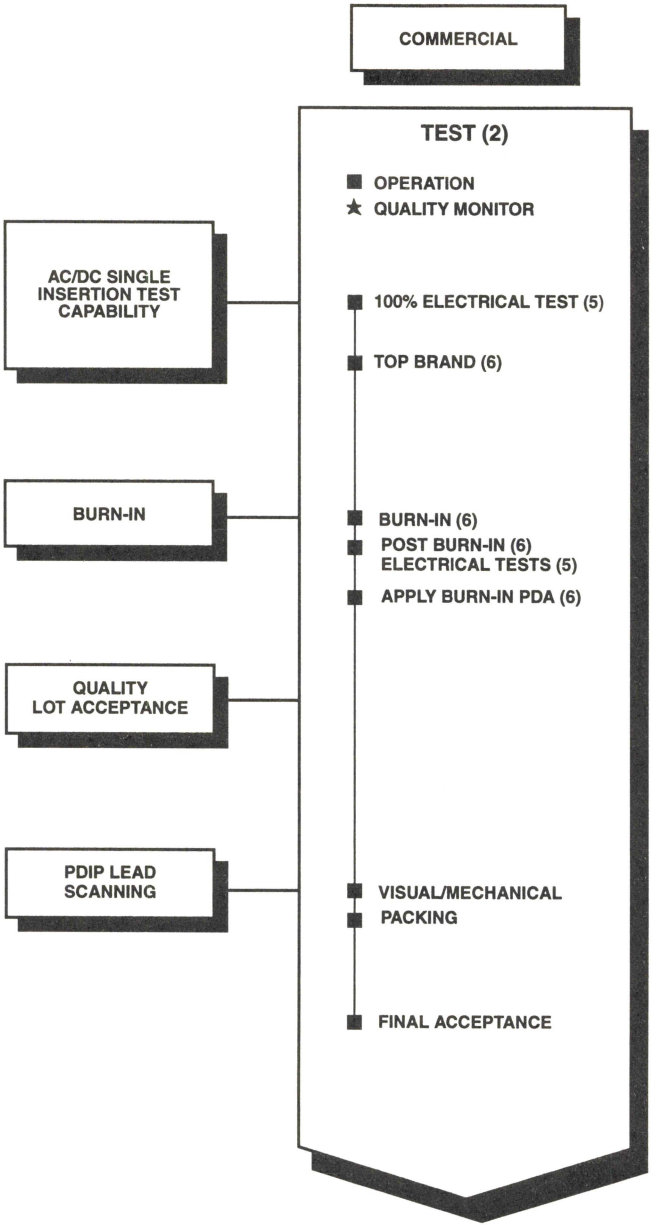


NOTES:

1. Example for a PDIP, Plastic Dual In-Line Package Part for commericial grade. Examples of military product flows access the Quality Management plan through the Harris internet web page http://www.semi.harris.com/quality/index.htm or through your local sales office.
2. High Temperature probe per specific product flow.
3. Visual inspection is modified Mil-STD-883 method 2010 condition B.

FIGURE 2.

Harris Semiconductor Standard Processing Flow



NOTES:

4. Example for a Linear Part in PDIP, Plastic Dual In-Lline Package Part.
5. 100% of the product will receive a minimum of one electrical test insertion per the applicable manufacturing flow.
6. If applicable.

FIGURE 3.

TABLE 2. SUMMARIZING CONTROL APPLICATIONS

FAB			
• Diffusion - Junction Depth - Sheet Resistivities - Oxide Thickness - Implant Dose Calibration - Uniformity	• Thin Film - Film Thickness - Uniformity - Refractive Index - Film Composition - Particles Added	• Photo Resist - Critical Dimension - Resist Thickness - Etch Rates - Energy Monitor (E_O)	• Measurement Equipment - Critical Dimension - Film Thickness - Resistivity
ASSEMBLY			
• Pre-Seal - Die Prep Visuals - Yields - Die Attach Heater Block - Die Shear - Wire Pull - Ball Bond Shear - Saw Blade Wear - Pre-Cap Visuals	• Post-Seal - Internal Package Moisture - Tin Plate Thickness - PIND Defect Rate - Solder Thickness - Leak Tests - Seal - Temperature Cycle	• Measurement - XRF - Radiation Counter - Thermocouples - GM-Force Measurement - Temperature - Humidity	
TEST			
	- Handlers/Test System - Defect Pareto Charts - Lot % Defective - ESD Failures per Month	- Monitor Failures - Lead Conformance - After Burn-In PDA - Temperature - Humidity	
OTHER			
• IQC - Vendor Performance - Material Criteria - Quality Levels	• Environment - Water Quality - Clean Room Control - Temperature - Humidity	• IQC Measurement/Analysis - XRF - ADE - 4 Point Probe - Chemical Analysis Equipment	

Special Testing

Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25°C. The flow shown in Figure 2 and Figure 3 indicates the Harris standard processing flow for a commercial linear part in a PDIP package. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for nonstandard environmental stress screening. Consult your field sales representative for details.

TABLE 3. HARRIS I.C. DESIGN TOOLS

DESIGN STEP	PRODUCTS	
	ANALOG	DIGITAL
Functional Simulation	Cds Spice	Cds Spice Verilog
Parametric Simulation	Cds Spice Monte Carlo	Cds Spice
Schematic Capture	Cadence	Cadence
Functional Checking	Cadence	Cadence
Rules Checking	Cadence	Cadence
Parasitic Extraction	Cadence	Cadence

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use control charts to determine the normal variabilities in processes, materials, and products. Critical process variables and performance characteristics are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a nonrandom pattern inside the limits. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 2 lists some typical manufacturing applications of control charts at Harris Semiconductor.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost (see Table 4).

TABLE 4. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at upgrading process performance by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in ANSI/ASQC Z1.4, MIL-STD-883 and MIL-PRF-38535 are used as a reference.

The focus on this quality parameter has resulted in a continuous improvement to less than 25 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of Harris statisticians, private consultants, and internally developed programs, training of engineers, facilitators, and operators/technicians has been an ongoing activity in Harris Semiconductor.

Over the past years, Harris has also deployed a comprehensive training program for hourly operators and facilitators in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of silicon, chemicals, gases and other materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

SPC seminars, development of open working relationships, understanding of Harris's manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials. Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	TOPICS COVERED
SPC, Basic	Manufacturing Operators, Non-Manufacturing Personnel	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts
SPC, Intermediate	Manufacturing Supervisors, Technicians	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Introduction to Capability
SPC, Advanced	Manufacturing Engineers, Manufacturing Managers	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Advanced Control Charts, Variance Component Analysis, Capability Analysis
Design of Experiments (DOX)	Engineers, Managers	Factorial and Fractional Designs, Blocking Designs, Nested Models, Analysis of Variance, Normal Probability Plots, Statistical Intervals, Variance Component Analysis, Multiple Comparison Procedures, Hypothesis Testing, Model Assumptions/Diagnostics
Regression	Engineers, Managers	Simple Linear Regression, Multiple Regression, Coefficient Interval Estimation, Diagnostic Tools, Variable Selection Techniques
Response Surface Methods (RSM)	Engineers, Managers	Steepest Ascent Methods, Second Order Models, Central Composite Designs, Contour Plots, Box-Behnken Designs
Capability Studies	Techs, Facilitators, Engineers	Capability Indices (C_P and C_{PK}), Variance Components, Nested Models, Fixed and Random Effects

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Warp • Thickness • Total Thickness Variation • Backside Criteria • Oxygen	• Equipment Capability Control Charts - Oxygen - Resistivity - Total Thickness Variation - Total Indicated Reading • Control Charts from On-Line Processing • Certificate of Conformance
Chemicals/Photoresists/ Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids	• Certificate of Analysis on all Critical Parameters • Certificate of Conformance • Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbency - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters • Certificate of Conformance
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Bondability • Intermetallic Layer Adhesion • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Certificate of Conformance • Process Control Charts on In-Line Process Controls

Calibration Laboratory

Another important resource in the product assurance system is a calibration lab in each Harris Semiconductor operation site. These labs are responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both production and engineering areas. The accuracy of instruments used at Harris is traceable to a national standards. Each lab maintains a system which conforms to the current revision of ANSI/NCSL Z540-1.

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Manufacturing Science - CAM, JIT, TPM

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened - in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

The major focus of JIT is cycle time reduction and linear production. Significant improvements in these areas result in large benefits to the customer. JIT is a part of the Total Quality Management philosophy at Harris and includes Employee Involvement, Total Quality Control, and the total elimination of waste.

Some key JIT methods used for improvement are sequence of events analysis for the elimination of non-value added activities, demand/pull to improve production flow, TQC check points and Employee Involvement Teams using root cause analysis for problem solving.

JIT implementations at Harris Semiconductor have resulted in significant improvements in cycle time and linearity. The benefits from these improvements are better on time delivery, improved yield, and a more cost effective operation.

JIT, SPC, and TPM are complementary methodologies and used in conjunction with each other create a very powerful force for manufacturing improvement.

Total Productive Maintenance (TPM)

TPM or Total Productive Maintenance is a specific methodology which utilizes a definite set of principles and tools focusing on the improvement of equipment utilization. It focuses on the total elimination of the six major losses which are equipment failures, setup and adjustment, idling and minor stoppages, reduced speed, process defects, and reduced yield. A key measure of progress within TPM is the overall equipment effectiveness which indicates what percentage of the time is a particular equipment producing good parts. The basic TPM principles focus on maximum equipment utilization, autonomous maintenance, cross functional team involvement, and zero defects. There are some key tools within the TPM technical set which have proven to be very powerful to solve long standing problems. They are initial clean, P-M analysis, condition based maintenance, and quality maintenance.

Utilization of TPM has shown significant increases in utilization on many tools across the Sector and is rapidly becoming widespread and recognized as a very valuable tool to improve manufacturing competitiveness.

The major benefits of TPM are capital avoidance, reduced costs, increased capability, and increased quality. It is also very compatible with SPC techniques since SPC is a good stepping stone to TPM implementation and it is in turn a good stepping stone to JIT because a high overall equipment effectiveness guarantees the equipment to be available and operational at the right time as demanded by JIT.

Harris Reliability

Introduction

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing processes. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life.

Reliability Engineering

The Reliability Engineering department is responsible for all aspects of reliability assurance at Harris Semiconductor:

- Charter
  - To ensure that Harris is recognized by our customers and competitors as a company that consistently delivers products with high reliability.

- Mission
  - To develop systems for assessing, enhancing, and assuring that quality and reliability are integrated into all aspects of our business.

- Vision
  - To establish excellence and integrity through all design and manufacturing processes as it relates to quality and reliability.

Values

- To be considered responsive and service oriented by our customers.
- To be acknowledged by Harris as a highly qualified resource for reliability assurance, product analysis, and electronic materials characterization.
- To successfully utilize the organization's talents through trained, empowered employees/employee team participation.
- To maintain an attitude of integrity, dignity and respect for all.

Strategy

- To provide quantitative assessments of product reliability focusing on the identification and timely elimination of design and processing deficiencies that degrade product performance and operating life expectancy.
- To provide systems for continuous improvement of reliability and quality through the assessment of existing processes, products, and packages.
- To perform product analysis as a means of problem solving and feedback to our customers, both internal and external.
- To exercise full authority over the internal qualifications of new products, processes, and packages.

The reliability organization is comprised of a team that possesses a broad cross section of expertise in these areas:

- Custom Military (Radiation Hardened)
- Automotive ASICs
- Harsh Environment Plastic Packaging
- Advanced Methods for Design for Reliability (DFR)
- Strength in Power Semiconductor
- Chemical/Surface Analysis Capabilities
- Failure Analysis Capabilities

The reliability focus is customer satisfaction (external and internal) and is accomplished through the development of standards, performance metrics, and service systems. These major systems are summarized below:

- A process and product development system known as ACT PTM (Applying Concurrent Teams to Product-To-Market) has been established. The ACT PTM philosophy is one of new product development through a team that pursues customer involvement. The team has the authority, responsibility, and training necessary to successfully bring the product to market. This not only includes product definition and design, but also all manufacturing capabilities as well.
- Standard test vehicles (over 100) have been developed for process characterization of wear-out failure mechanisms. These vehicles are used for conventional stresses (for modeling failure rates) and for wafer level reliability characterization during development.
- Common qualification standards have been established for all sites.
- A reliability monitoring system (known as the Matrix Monitoring System) is utilized for products in production to ensure ongoing reliability and drive continuous improvement.
- The field return system is designed to handle a variety of customer issues in a timely manner. Product issues are often handled by routing the product into the PFAST (Product Failure Analysis Solution Team) system. Return authorizations (RAs) are issued when an entire lot of product needs to be returned to Harris. The Customer Return Services (CRS) group is responsible for the administration of this system (see Customer Return Services.)
- The PFAST system has been established to expedite failure analysis, root cause determination, and corrective actions for field returns. PFAST is a team effort involving many functional areas at all Harris sites. The purpose of this system is to enable Harris' Field Sales and Quality operations to properly route, track, and respond to our customer's needs as they relate to product analysis.

Design for Reliability (Wear-Out Characterization)

The concept of "Design for Reliability" focuses on moving reliability assessment away from tests on sample product to a point much earlier in the design cycle. Effort is directed at building in and verifying the reliability of a new process well before manufacture of the first shippable product that uses that technology. This gives these first new products a higher probability of success and achieves reduced product-to-market cycle times.

In practice, a set of standardized test vehicles containing special test structures are transferred to the new process using the layout ground rules specified for that process. Each test structure is designed for a specific wear-out failure mechanism. Highly accelerated stress tests are performed on these structures and the results can be extrapolated to customer use conditions. Generally, log-normal statistics are used to define wear-out distributions for the life prediction models. The results are used to establish reliability design ground rules and critical node lists for each process. These ground rules and critical nodes ensure that wear-out failures do not occur during the customer's projected use of the product.

Process/Product/Package Qualifications

Once the new process has successfully completed wear-out characterization, the final qualification consists of more conventional testing (e.g. biased life, storage life, temp cycle etc.). These tests are performed on the first new product designs (sampled across multiple wafer production lots). Successful completion of the final qualification tests concurrently qualifies the new process and the new products that were used in the qualification. Subsequent products designed within the now-established ground rules are qualified individually prior to introduction. New package configurations are also qualified individually prior to being available for use with new products.

Harris's qualification procedures are specified via controlled documentation and the same standard is used at Harris's sites worldwide. Figure 4 gives more information on the new process/product development and life cycle.

Product/Package Reliability Monitors

Many of the accelerated stress-tests used during initial reliability qualification are also employed during the routine monitoring of standard product. Harris's continuing reliability monitoring program consists of three groups of stress tests, labeled Matrix I, II and III. Table 7 outlines the Matrix tests used to monitor plastic packaged ICs in Harris's off-shore assembly plants, where each wafer fab technology is sampled. Matrix I consists of highly accelerated, short duration (typically 48 hours) tests, sampled biweekly, which provide real-time feedback on product reliability. Matrix II consists of the more conventional, longer term stress-tests, sampled monthly, which are similar to those used for product qualification. Finally, Matrix III, performed monthly on each package style, monitors the mechanical reliability aspects of the package. Any failures occurring on the Matrix monitors are fully analyzed and the failure mechanisms identified, with containment and corrective actions obtained from Manufacturing and Engineering. This information along with all of the test results are routinely transmitted to a central data base in Reliability Engineering, where failure rate trends are analyzed and tracked on an ongoing basis. These data are used to drive product improvements, to ensure that failure rates are continuously being reduced over time.

Reliability data, including the Matrix Monitor results, can be obtained by contacting your local Harris sales office, or on the worldwide web at URL:http://rel.semi.harris.com.

TABLE 7. PLASTIC PACKAGED IC MONITORING TESTS

MATRIX I

TEST	CONDITIONS	DURATION	SAMPLE-ACCEPT NUM.
Autoclave	+121°C, 100%RH, 15PSIG	96 Hours	45/0
Biased Life	+175°C	48 Hours	45/0
Biased Life	+125°C	48 Hours	45/0
HAST	+135°C, 85% RH	48 Hours	45/0
Thermal Shock	-65°C to +150°C	200 Cycles	45/0

MATRIX II

TEST	CONDITIONS	DURATION	SAMPLE-ACCEPT NUM.
Autoclave	+121°C, 100%RH, 15PSIG	192 Hours	45/0
Biased Humidity	+85°C, 85% RH	1000 Hours	45/0
Biased Life	+125°C	1000 Hours	45/0
Dynamic Life	+125°C	1000 Hours	45/0
Storage Life	+150°C	1000 Hours	45/0
Temp. Cycle	-65°C to +150°C	1000 Cycles	45/0

MATRIX III

TEST	CONDITIONS	SAMPLE-ACCEPT NUM.
Brand Adhesion	MIL-STD-883/2015	15/0
Flammability	(UL-94 Vertical Burn)	11/0
Lead Fatigue	MIL-STD-883/2004	15/0
Physical Dimensions	MIL-STD-883/2016	11/0
Solderability	MIL-STD-883/2003	45/0
Acoustic Microscopy	JEDEC 22/A112/A113	11/0
Terminal Strength	MIL-STD-883/2004	15/0

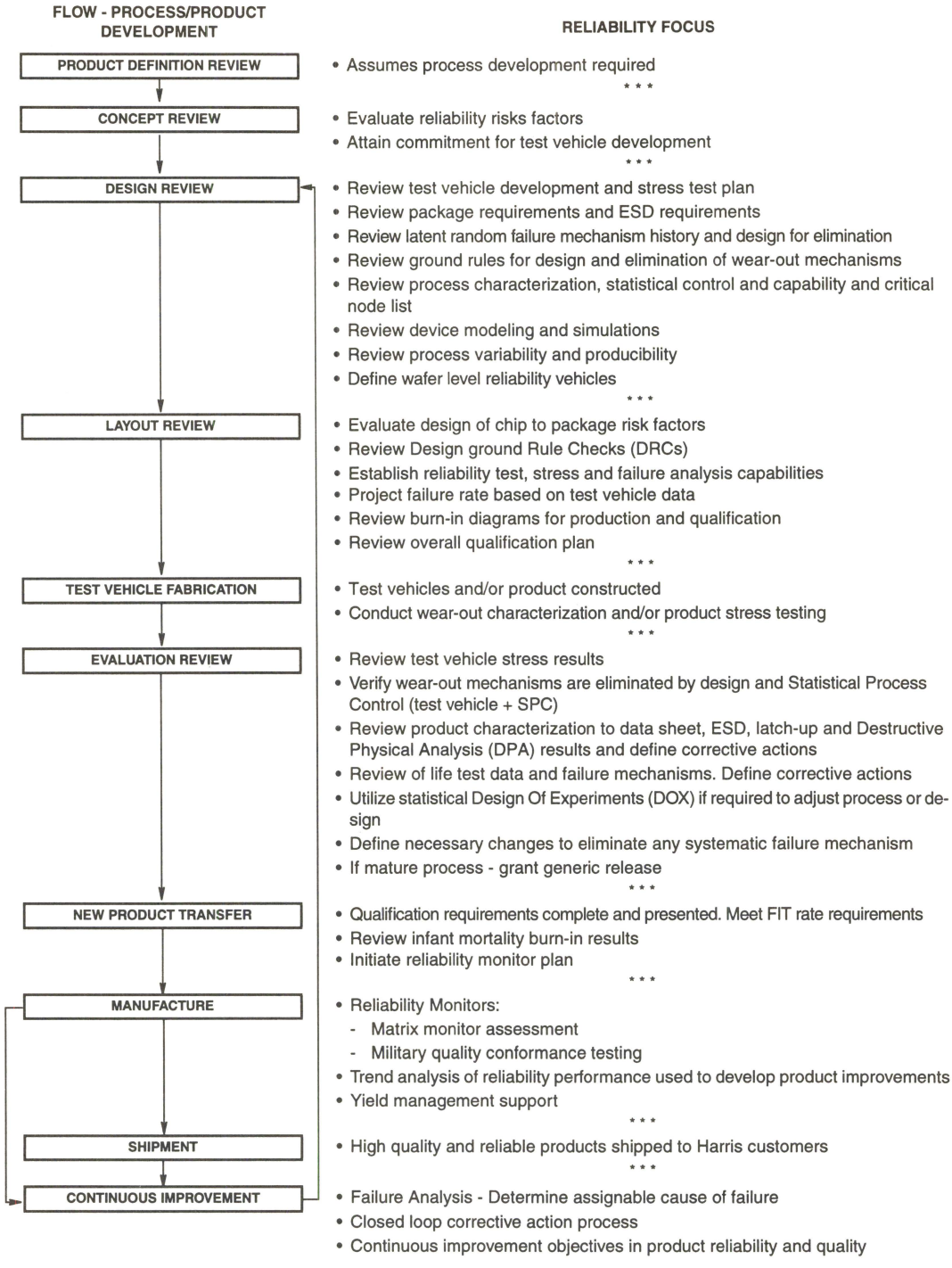


FIGURE 4. NEW PROCESS/PRODUCT DEVELOPMENT AND LIFE CYCLE

Customer Return Services

Harris places a high priority on resolving customer return issues. The Customer Return Services (CRS) department is responsible for determining the best manner to handle a return issue as illustrated in Figure 5.

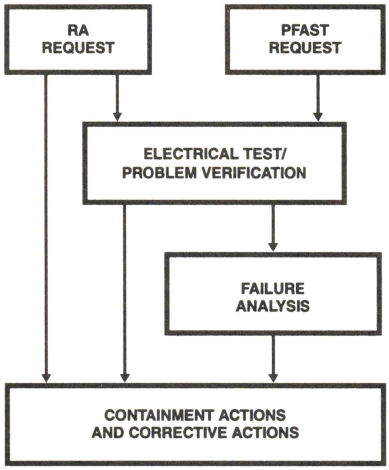


FIGURE 5. GENERAL RETURN FLOW

The diversity of return reasons requires that many different organizations be involved to test, analyze, and correct field return issues. The CRS group coordinates the responses from the supporting organizations to drive closure of issues within the customer response time requirements, see Figure 6. The results from the work performed on customer returns are used to initiate corrective actions and continuous improvements within the factories.

The two methods used to return devices are by a RA (Return Authorization) request or by a PFAST (Product Failure Analysis Solution Team) request. The main difference between RA and PFAST is that the PFAST requests often require extensive analysis and a more formal response to the customer. All returns follow the same general procedure from the customer's perspective as seen in steps one to four of the customer return procedure.

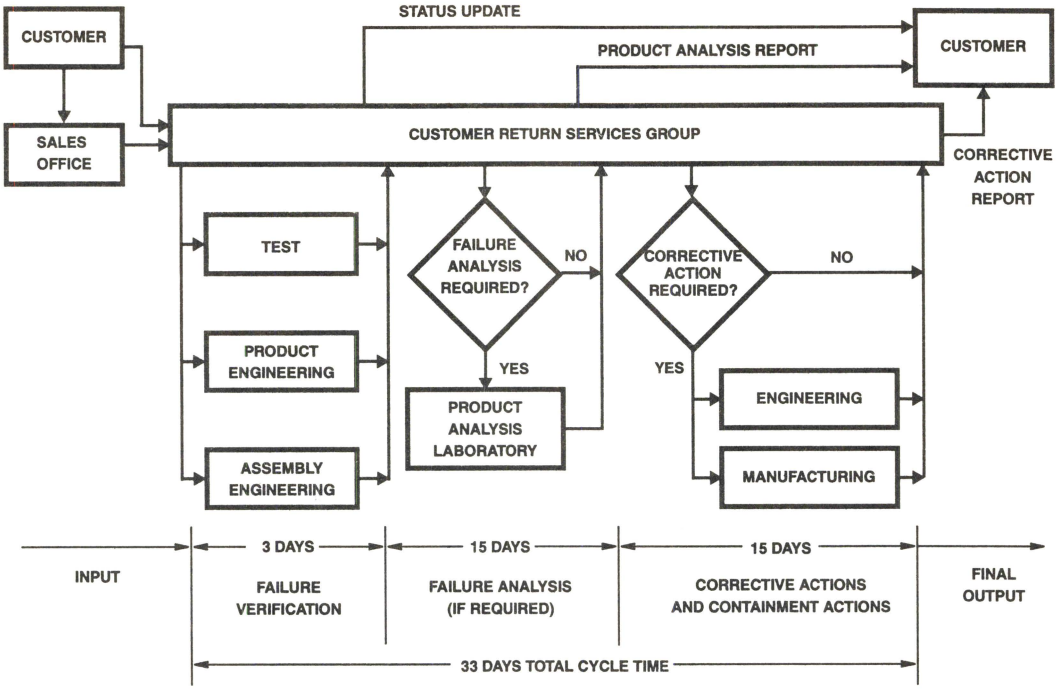
- **Step 1** - Customer or Sales office contacts the Customer Return Services department. If a return is to be routed into the PFAST system, then a PFAST Action Request (see the PFAST form in this section) needs to be completed to understand the customer's issue and direct the analysis efforts.
  - **Phone Number: (407)-724-7400**
  - **FAX Number: (407)-724-7658**
  - **Internet: creturn@harris.com**
  - **PROFS: CRETURN**
- **Step 2** - The Customer Return Services department notifies all affected sales, factory, and engineering organizations of the issue.
- **Step 3** - When product is received, the issue is verified and any required analysis is performed. Where applicable, a preliminary analysis report is sent to the customer.
- **Step 4** - A determination of the root cause of failure initiates the corrective actions to address the source of the problem. A final corrective action report is sent to the customer if requested.

The RA request is used to return and replace an entire lot of product. The lot is returned to Harris for replacement or credit. Once the product is received various tests and evaluations will be performed to determine the appropriate actions that should be taken to resolve any problems or issues.

A PFAST request is used to return a small sample for analysis of a problem. The ultimate outcome of both types of requests is to determine corrective actions that would preclude the same problem occurring in the future. Where appropriate, a containment plan is also implemented to prevent a re-occurrence of the problem in the field. The customer return flow diagram (Figure 6) provides the typical activities and cycle times for processing a PFAST request. See Figure 7 for the PFAST request form which contains data supplied by the customer that is essential to timely and accurate failure analysis.

CUSTOMER RETURN SERVICES

CHARTER	MISSION	RESPONSIBILITIES
To resolve product quality issues while providing feedback to both external and internal customers to facilitate corrective actions and continuous improvement of the product.	To provide a single point interface between the customer and the factory for resolving technical problems, issues, and field returns.	1. Maintain customer return history. 2. Track returns through the factory. 3. Establish a history library of problems and corrective actions. 4. Ensure closure with customers.



NOTE: The days indicated are the typical number of 'working days' not calendar days. Analysis difficulty and the nature of the corrective actions may either improve or degrade the total cycle time.

FIGURE 6. CUSTOMER RETURN FLOW DIAGRAM

Product Analysis Lab

The Product Analysis Laboratory capabilities and charter encompass the isolation and identification of failure modes and mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. The primary activities of the Product Analysis Lab are electrical verification/characterization of the failure, package inspection/analysis, die inspection/analysis, and circuit isolation/probing. A variety of tools and techniques have been developed to ensure the accuracy and integrity of the product analysis. This section lists some of the tools and techniques that are employed during a typical analysis.

The electrical verification/characterization of devices failing electrical parameters is essential prior to performing an analysis. The information obtained from the electrical verification provides a direction for the analysis efforts. The following electrical verification/characterization equipment may be used to obtain electrical data on a device:

- HP82000M Mixed Signal Tester
- LV500 ASIC verification system
- LTS2020 Analog tester
- Curve Tracer
- Parametric Analyzer

Prior to die level analysis, package inspection and analysis are performed. These steps are performed routinely since valuable data may not be obtainable once the package is opened. The package inspection and analysis may require the use of some of the following lab equipment:

- X-Ray
- C-Mode Scanning Acoustic Microscope (C-SAM)
- Optical inspection microscopes
- Package opening tools and techniques

HARRIS SEMICONDUCTOR

(PFAST) ACTION REQUEST

Product Failure Analysis Solution Team

PFAST#_____ Date_____

Customer Ref#(SCAR) _____

Customer:_____	**Sales:**_____	**Distributor:**_____
Address:_____	**Address:**_____	**Address:**_____
City/State/Zip:_____	**City/State/Zip:**_____	**City/State/Zip:**_____
Phone#:_____	**Phone#:**_____	**Phone#:**_____
Fax#:_____	**Fax#:**_____	**Fax#:**_____
E-Mail:_____	**E-Mail:**_____	**E-Mail:**_____
Contact Name:_____	**Contact Name:**_____	**Contact Name:**_____

Product Information: *Please supply a copy of the shipper if available.

Harris Part#_____ Customer Part#:_____

Qty Purchased:_____ PO#:_____

Qty Failed:_____ SO#:_____

Sample Qty Returned:_____ Lot#:_____

Date Code/Bottom Code(s):_____ Package/Lead Count:_____

Check All Boxes That Are Required:

Test Verification: _____

Failure Analysis: _____

Corrective Action: _____

Product Return Pending:y/n _____ (Qty):_____

Apps. Engineer contacted?:_____

Please place an "X" next to the appropriate failure category and give specific details about the failure in the Problem Description area.

Administrative Problem:

Ship Quantity: ____ Mixed Product: ____ Other: ____

Packaging: ____ Wrong Product: ____ Labeling:____

Insufficient Test: ____ Shipping Damage: ____

Brand Error(Incorrect/Typo)_____**Include all information about brand under the problem description.

Visual/Mechanical Failure:

Where was failure detected: Incoming__ Board__ or Field__

Package Dimensions: ____ Hermeticity: ____

Internal Die/Assembly Visual: ____ PIND: ____

External Package Visual: ____ Bent Leads: ____

Solderability/Lead Finish: ____ Other: ____

Brand(Adherence): ____

Tape & Reel (Loose tape, peel strength, orientation): ____***

***Include tape sealing information off the reel: _____

Electrical Failure: **Please remove conformal coating**

	Qty Tested	Qty Failed	Not Performed
Incoming	___	___	___
Board	___	___	___
System	___	___	___
Field	___	___	___

Tester Mfg_____

Test Temp_____°C

Failure Mode: AC___ DC___ Non-Functional_____

Hours of operation before failure_____. Estimated failure rate_____%

Do other date codes work? yes___ no___. If yes, list D/C's:_____

Describe failure with reference to supply voltages. Attach an additional sheet or schematics if necessary: _____

PROM: Please supply master unit or disk (Data I/O format) with pattern.

Problem Description: Please describe the failure in detail and list all processing that occurred prior to the failure (attach additional paper as needed):

Technical Contact:_____ Phone Number:_____

Harris Internal Use:

Mask_____	Pkg_____	PE_____	D/C_____	B/S_____	D/C_____	B/S_____	D/C_____	B/S_____
Fab_____	Assy_____	Test_____	D/C_____	B/S_____	D/C_____	B/S_____	D/C_____	B/S_____
T&R Seal Date_____		Probe_____	D/C_____	B/S_____	D/C_____	B/S_____	D/C_____	B/S_____

***If you need assistance completing this form please call 407/724-7400 or e-mail creturn@harris.com or fax 407/724-7658 Rev#: 2

Once the device has been opened, die inspection and analysis can be performed. Depending on the type of failure, several tools and techniques may be used to identify the failure mechanism. Usually the faster and easier to use operations are performed first in an attempt to expedite the analysis. The list of equipment and techniques for performing die inspection and analysis is as follows:

- Optical microscopes
- Liquid crystal
- Emission microscope
- Scanning electron microscopes - SEM

The final step of circuit isolation is ready to be performed when an area of the circuit has been identified as the source of the problem through one of the previous analysis efforts. Circuit analysis is performed using the following probing and isolation tools:

- Mechanical probing
- Laser cutter and isolation
- E-Beam probing
- Cross sectioning and chemical deprocessing

A typical analysis flow is shown in the Figure 8 below. The exact analysis steps and sequence are determined as the situation dictates. For the analysis to be conclusive, it is essential that the failure mechanism correlates to the initial product failure conditions. Some failure mechanisms require elemental and chemical analysis to identify the root cause within the manufacturing process. Elemental and chemical analysis tasks are sent to the Analytical Services Lab for further evaluation.

The results of each analysis are entered into a computer data base. This data base is used to search for specific types of problems, to identify trends, and to verify that the corrective actions were effective.

Analytical Services Laboratory

Chemical and physical analysis of materials and processes is an integral part of Harris' Total Quality/Continuous Improvement efforts to build reliability into processes and products. Manufacturing operations are supported with real-time analyses to help maintain robust processes. Analyses are run in cooperation with raw material suppliers to help them provide controlled materials in dock-to-stock procurement programs.

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies.

The department also maintains ongoing working arrangements with commercial laboratories, universities, and equipment manufacturers to obtain any materials analysis in cases where instrumental capabilities are not available in our own facility. Figure 9 and Figure 10 show the capabilities of each area.

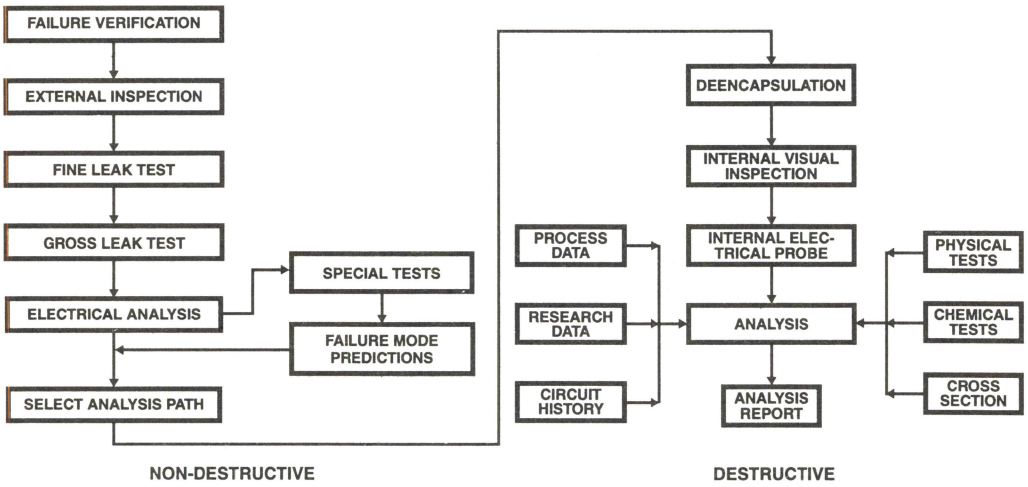


FIGURE 7. ANALYSIS SEQUENCE

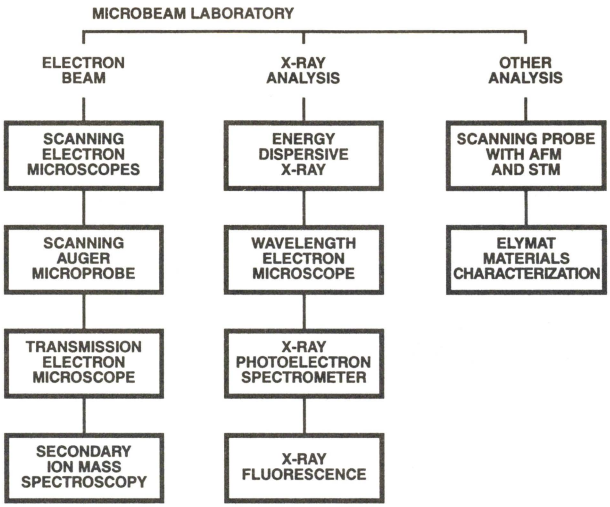


FIGURE 8. MICROBEAM LABORATORY

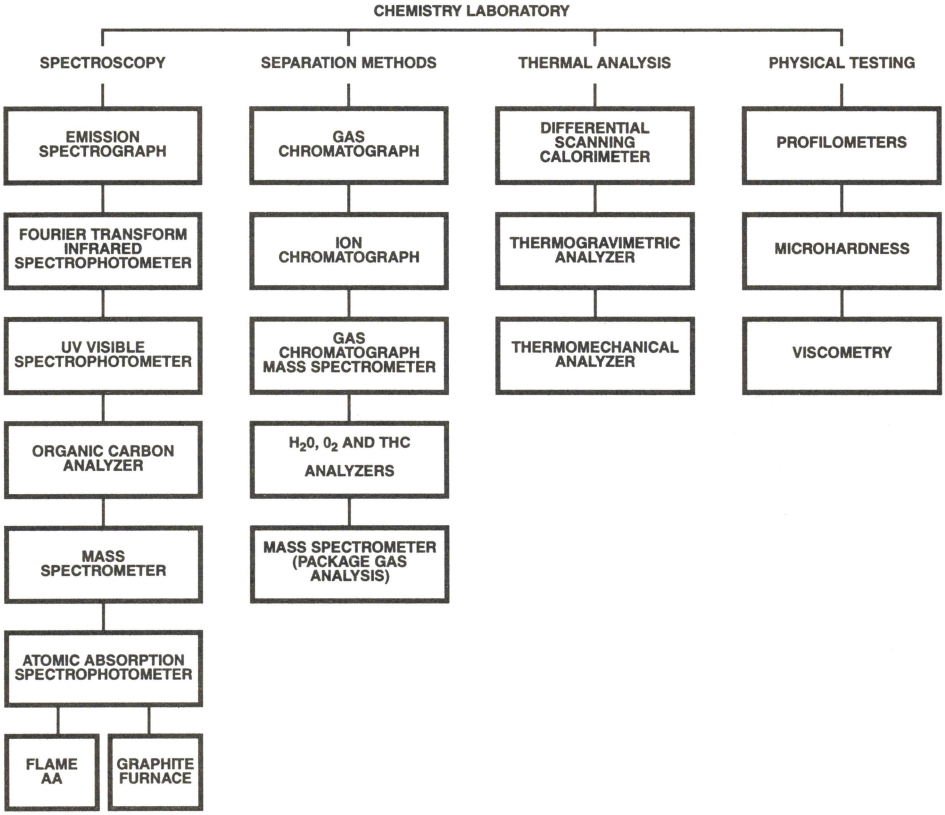


FIGURE 9. CHEMISTRY LABORATORY

Reliability Fundamentals and Calculation of Failure Rate

Table 9 defines some of the more important terminology used in describing the lifetime of integrated circuits. Of prime importance is the concept of "failure rate" and its calculation.

Failure Rate Calculations

Since reliability data can be accumulated from a number of different life tests with several different failure mechanisms, a comprehensive failure rate is desired. The failure rate calculation can be complicated if there are more than one failure mechanism in a life test, since the failure mechanisms are thermally activated at different rates The equation below accounts for these considerations along with a statistical factor to obtain the upper confidence level (UCL) for the resulting failure rate.

$$\lambda = \left[\sum_{i=1}^{\beta} \frac{x_i}{\sum_{j=1}^{k} TDH_j \, AF_{ij}} \right] \times \frac{M \times 10^9}{\sum_{i=1}^{\beta} x_i}$$

where,

λ = failure rate in FITs (Number fails in 10^9 device hours)

β = number of distinct possible failure mechanisms

k = number of life tests being combined

x_i = number of failures for a given failure mechanism $i = 1, 2, \ldots \beta$

TDH_j = Total device hours of test time (unaccelerated) for Life Test $j, j = 1, 2, 3, \ldots k$

AF_{ij} = Acceleration factor for appropriate failure mechanism $i = 1, 2, \ldots k$

$M = X^2_{(\alpha, 2r+2)}/2$
where,
X^2 = chi square factor for $2r + 2$ degrees of freedom
r = total number of failures (Σx_i)
α = risk associated with UCL;
i.e. α = (100-UCL(%))/100

In the failure rate calculation, Acceleration Factors (AF_{ij}) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. Although no standard exists, a temperature of +55°C has been popular. Harris Semiconductor Reliability Reports will derate to +55°C and will express failure rates at 60% UCL. Other derating temperatures and UCLs are available upon request.

TABLE 8. FAILURE RATE PRIMER

TERMS	DEFINITIONS/DESCRIPTION
Failure Rate λ	Measure of failure per unit of time. The early life failure rate is typically higher, decreases slightly, and then becomes relatively constant over time. The onset of wear-out will show an increasing failure rate, which should occur well beyond useful life. The useful life failure rate is based on the exponential life distribution.
FIT (Failure In Time)	Measure of failure rate in 10^9 device hours; e.g., 1 FIT = 1 failure in 10^9 device hours, 100 FITS = 100 failure in 10^9 device hours, etc.
Device Hours	The summation of the number of units in operation multiplied by the time of operation.
MTTF (Mean Time To Failure)	Mean of the life distribution for the population of devices under operation or expected lifetime of an individual, MTTF = $1/\lambda$, which is the time where 63.2% of the population has failed. Example: For λ = 10 FITS (or 10 E-9/Hr.), MTTF = $1/\lambda$ = 100 million hours.
Confidence Level (or Limit)	Probability level at which population failure rate estimates are derived from sample life test: 10 FITs at 95% UCL means that the population failure rate is estimated to be no more that 10 FITs with 95% certainty. The upper limit of the confidence interval is used.
Acceleration Factor (AF)	A constant derived from experimental data which relates the times to failure at two different stresses. The AF allows extrapolation of failure rates from accelerated test conditions to use conditions.

Acceleration Factors

Acceleration factor is determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and has been found to be an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP\left[\frac{E_a}{k}\left(\frac{1}{T_{USE}} - \frac{1}{T_{STRESS}}\right)\right]$$

where,

AF = Acceleration Factor

E_a = Thermal Activation Energy (See Table 10)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature.

Activation Energy

The Activation Energy (E_a) of a failure mechanism is determined by performing at least two tests at different levels of stress (temperature and/or voltage). The stresses will provide the time to failure (t_f) for the two (or more) populations thus allowing the simultaneous solution for the activation energy as follows:

$$\ln(t_{f1}) = C + \frac{E_a}{kT_1} \qquad \ln(t_{f2}) = C + \frac{E_a}{kT_2}$$

By subtracting the two equations and solving for the activation energy, the following equation is obtained:

$$E_a = \frac{k[\ln(t_{f1}) - \ln(t_{f2})]}{(1/T1 - 1/T2)}$$

where,

E_a = Thermal Activation Energy (See Table 10)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

T_1, T_2 = Life test temperatures in degrees Kelvin

TABLE 9. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3eV - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3eV - 0.5eV	HTOL and voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress testing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5eV - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes, proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation.
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles, Statistical Process Control of photoresist/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test and HTOL.	Statistical Process Control of C-V data, oxide/ interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL and oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

DATA ACQUISITION 15

APPLICATION NOTE AND TECHNICAL BRIEF ABSTRACTS

PART NUMBER/ DOCUMENT NUMBER	TITLE	ABSTRACT
	APPLICATION NOTES	
(General DAQ) AN001	Glossary of Data Conversion Terms (6 pages)	Specification definitions and most-often-used terms used in the field of data acquisition.
(General DAQ) AN002	Principles of Data Acquisition and Conversion (20 pages)	Basic Data Acquisition system design, quantizing theory, sampling theory, data coding, amplifiers and filters, settling time, DAC types, ADC types, reference circuits, analog multiplexers, sample and holds, specifications, and selection criteria.
(General DAQ) AN009	Pick Sample-Holds by Accuracy and Speed and Keep Hold Capacitors in Mind (7 pages)	Monolithic considerations, error analysis, droop discussion, capacitor characteristics, deglitching sample and holds, and cascaded sample and hold designs.
(General DAQ) AN012	Switching Signals with Semiconductors (4 pages)	Analog switches are fast, low cost, and work well with the high impedance of most signal circuits. Often they can replace reed relays.
(General DAQ) AN016	Selecting A/D Converters (7 pages)	Important selection parameters, the integrating converter, the SAR type converter, multiplexed data systems, and a definition of terms.
(General DAQ) AN018	Do's and Don'ts of Applying A/D Converters (4 pages)	System power routing errors, PCB layout rules, component selection, thermal effects, and maximizing the FSR range of the converter.
(General DAQ) AN020	A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing (23 pages)	High speed system block diagram, layout considerations, multiplexer considerations differential amplifiers, sample and hold amplifier, SAR type ADCs, DAC design, and microprocessor interfacing.
(General DAQ) AN043	Video Analog-to-Digital Conversion (6 pages)	Comparator based flash converters, quantization noise, the decoder, a two-stage flash converter, and hybrid considerations.
(General DAQ) AN047	Games People Play with A/D Converters (27 pages)	Various real world applications for A/D converters, LCD annunciator drivers, decimal point drivers, a low battery detect application, blanking the display on low battery detect, controlling LED brightness, instant continuity detector, high voltage display driver, a gas discharge plasma display, DVM circuit, a tachometer design, measuring the gain of a transistor, running off a 1.5V supply, a simple capacitor meter, and a weighing system.
(General DAQ) AN048	Know Your Converter Codes (5 pages)	Analyzing digital codes, ADC and DAC operating basics, Bipolar coding techniques, and coding limitations.
(General DAQ) AN520	CMOS Analog Multiplexers and Switches; Application Considerations (9 pages)	Switch selection criteria, data sheet definitions, care and feeding of multiplexers and switches, digital interface, practical multiplexer applications alternative to CMOS switches and multiplexers.
(General DAQ) AN521	Getting the Most Out of CMOS Devices for Analog Switching Jobs (7 pages)	CMOS vs bipolar device performances, overvoltage and channel interaction conditions, JI technology and latch-up, floating body JI technology, fool-proof CMOS analog multiplexer, other DI benefits.

Technical Literature Abstracts (Continued)

PART NUMBER/ DOCUMENT NUMBER	TITLE	ABSTRACT
(General DAQ) AN522	Digital-to-Analog Converter Terminology (3 pages)	Explains DAC terminology, Resolution Gain Error, Offset Error, Linearity Error, Differential Linearity Error, Drift, Settling Time, etc.
(General DAQ) AN524	Digital-to-Analog Converter High Speed ADC Applications (3 pages)	Use of High Speed DACs in tracking, servo, and successive approximation Analog-to-Digital Converters. Design ideas for Data Acquisition Systems.
(General DAQ) AN531	Analog Switch Applications in A/D Data Conversion Systems (4 pages)	System configurations, analog switch types, CMOS switch selection guidelines, alternative uses of CMOS switches.
(General DAQ) AN532	Common Questions Concerning CMOS Analog Switches (4 pages)	Power supply considerations, input overvoltage protection, single supply operation, various questions about Harris DI switches.
(General DAQ) AN535	Design Considerations for Data Acquisition Systems (DAS) (7 pages)	A collection of guidelines for the design of a Data Acquisition System. Includes signal conditioning, transducers, single-ended vs differential signal paths, low level signals, filters, Programmable Gain Amplifiers, sampling rate, and computer interfacing.
(General DAQ) AN557	Recommended Test Procedures for Analog Switches (6 pages)	Description of analog switch test methods employed at Harris Semiconductor.
(General DAQ) AN9337	Reduce CMOS-Multiplexer Troubles Through Proper Device Selection (6 pages)	How to deal with output leakage, Overvoltage fault protection techniques, and new architectural designs to provide better fault protection.
(General DAQ) AN9419	Using the DAC Reconstruct Board (8 pages)	The DAC reconstruct board is designed to provide an analog reconstruction of the digital data from an A/D converter. It can be used along with most Harris A/D converters to perform linearity, bandwidth or video testing.
(General DAQ) TB330	Higher Speed Clock Rates Help Ease Filtering Requirements in Communication D/As (2 pages)	A complete discussion on increasing the Digital-to-Analog clock frequency to ease the burden of filtering. This helps to simplify any filtering choce by moving harmonics and clock aliases away from the frequency band of interest.
(General DAQ) TB334	Guidelines for Soldering Surface Mount Components to PC Boards (2 pages) TB334	The most commonly used techniques for soldering surface mounted devices (SMDs) to PC boards are Infrared (IR) and Vapor Phase (VP). This article details both methods.
(General DAQ), HI5721 TB325	Understanding Glitch In A High Speed D/A Converter (2 pages)	A complete discussion of glitch area and its effect on high speed Digital-to-Analog systems.
(General DAQ), HI5721 TB326	Measuring Spurious Free Dynamic Range in a D/A Converter (2 pages)	As high-speed DACs migrate into digital receivers and transmitters, spectral specifications become more important to the system designer. This paper covers Signal to Noise Ration (SNR), Total Harmonic Distortion (TDH) and Spurious Free Dynamic Rang (SFDR).
(General DAQ), HI5721 TB328	Setup and Hold Considerations When Using the HI5721 (2 pages)	High-speed D/A converters put great demands on the system designer when integrating them into the system. Logic timing must be carefully examined to ensure setup and hold times are satisfied.
(General DAQ, HI5800) TB324	Clamping the Analog Input of the HI5800 (1 page)	There are various reasons for clamping the input to the HI5800. This article details possible applications.

Technical Literature Abstracts (Continued)

PART NUMBER/ DOCUMENT NUMBER	TITLE	ABSTRACT
(General A/D Converters) AN9675	A Tutorial in Coherent and Windowed Sampling with A/D Converters (8 pages) AN9675	A complete discussion of Coherent and Windowed Sampling with A/D Converters.
CA3304, CA3306, CA3318, HI-5700, HI5701, HI5800, HI1166, HI1175, HI1176, HI1276, HI1386, HI1396 AN9214	Using Harris' High-Speed A/D Converters (10 pages) AN9214.2	PCB layout, grounding and power considerations for high speed converter board design, suggested voltage reference circuits, analog input buffers, bandwidth considerations, accuracy adjustments, logic family compatibility and interface examples, anti-aliasing filter theory, multiplexed inputs and input clamping for video signals.
CDP68HC05C4 AN8759	Low Cost Data Acquisition System Features SPI A/D Converter (9 pages)	Discussions of a typical serial interface system, detailed description of the 68HC68 architecture, multiple zone heating system design, digital storage scope design, and microcode for a low cost DAS.
HA-2420, HA-2425, HA-5330 AN517	Applications of Monolithic Sample and Hold Amplifier (5 pages)	General Sample and Hold information and fourteen specific applications, including filtered Sample and Hold DAC de-glitcher Integrate-Hold-Reset, gated op amp, etc.
HA-2546, HA-5020, HA-5033, HA-5177, HI-5700 AN9313	Circuit Considerations in Imaging Applications (8 pages)	Discussions of Video formats such as RS170, circuit design considerations, system design, test results and time division multiplexed systems.
HA-5320 AN538	Monolithic Sample/Hold Combines Speed and Precision (6 pages)	Description and electrical specifications for the HA-5320 Sample/Hold Amplifiers, explanation of error sources, and HA-5320 applications.
HI-0201 AN9402	Keeping the HI-0201 Switch Closed when Removing the V+ Supply (1 page)	In certain applications it is desirable to keep the switch in a certain state when one or both supplies are removed. This application note describes keeping the switch closed when the positive supply is removed.
HI-201HS AN543	New High Speed Switch Offers Sub-50ns Switching Times (7 pages)	Application enhancement using the HI-201HS, high speed multiplexers, high speed sample and hold, analog switch and op amp circuitry, integrator with start/reset, low pass filter with select break frequency, amplifier with programmable gain, future applications.
HI-222 AN559	HI-222 Video/HF Switch Optimizes Key Parameters (7 pages)	Description of the key specifications of the HI-222 such as power supply range vs r_{ON}, t_{ON}, differential gain and phase errors, switching transients and charge injection, continuous and peak current capability, off isolation, crosstalk and PC board layout.
HI-222 AN9316	Power Supply Considerations for the HI-222 High Frequency Video Switch (2 pages)	A guide to proper power supply sequencing for the HI-222 Video Switch.
HI-300 AN534	Additional Information on the HI-300 Series Switch (5 pages)	"ON" resistance, leakage currents, switching speeds, power supply requirements, internal switch operation and schematics, single supply operation, charge injection, power supplies, conditions and protective circuitry.
HI1166 AN9328	Using the HI1166 Evaluation Board (9 pages)	A description of how to use the HI1166, 250MHz, 8-bit A/D evaluation board.
HI1171 AN9411	Using the HI1171 Evaluation Kit (6 pages)	A description of how to use the HI1171 evaluation board.

Technical Literature Abstracts (Continued)

PART NUMBER/ DOCUMENT NUMBER	TITLE	ABSTRACT
HI1171, HI1176 AN9329	Using the HI1176/HI1171 Evaluation Board (5 pages)	A description of how to use the HI1176/1171 Video A/D and D/A evaluation board.
HI1175 AN9331	Using the HI1175 Evaluation Board (10 pages)	A description of how to use the HI1175 Video A/D evaluation board.
HI1176, HI1179 AN9407	Using the HI1176/HI1179 Evaluation Board (13 pages)	A description of how to use the HI1176 / HI1179 evaluation board.
HI1176 AN9533	Design Considerations When Using the HI1176 Input Clamp Circuit (4 pages) AN9533	A discussion on the use of the built-in clamp circuit of the HI1176 device.
HI1386 AN9333	Using the HI1386 Adapter Board (2 pages)	A description of how to use the HI1386, 75MHz, 8-bit A/D adaptor board. To be used with HI1396 evaluation board.
HI1396 AN9330	Using the HI1396 Evaluation Board (9 pages)	A description of how to use the HI1396, 125MHz, 8-bit A/D evaluation board.
HI20201, HI20203 AN9406	Using the HI20201/03 Evaluation Kit (11 pages)	A description of how to use the HI20201 / HI20203 evaluation board.
(General DAQ) HI-5700, HI-5701 AN9213	Advantages and Application of Display Integrating A/D Converters (6 pages)	Theory of operation of a dual slope integrating type A/D converter used for bridge measurement, low-level sensors and several application circuits including a capacitance meter and digital thermometer.
HI-5701 AN9216	Using the HI-5701 Evaluation Board (8 pages)	Theory of operations discussion for the HI5701, a description and use of the evaluation board, typical performance curve data on the HI5701, board layout and schematics.
HI-5701 TB323	Replacing an MP7682 with an HI5701 (1 pages)	A detailed discussion on upgrading from the Micro Power MP7682 to the Harris HI5701.
HI5702 AN9413	Driving the Analog Input of the HI5702 (3 pages)	The analog input can be configured in various ways depending on the signal source and the required level of performance. This paper details the theory and operation of this device.
HI5702, HI5703, HSP43220, HSP45116 AN9509	Digital IF Sub Sampling Using the HI5702, HSP45116 and HSP43220 (5 pages) AN99509.1	This note is about the conversion of previously analog receiver designs into a digital form. It includes a technique for IF sub sampling that can simplify the digital circuits. An example of a digital receiver design, based on standard Harris components, is included.
HI5703 AN9534	Using the HI5703 Evaluation Board (13 pages) AN9534.1	A description of how to use the HI5703 evaluation board.
HI5710 AN9511	Using the HI5710 Evaluation Board (13 pages) AN9511	A description of how to use the HI5710 evaluation board.
HI5714 AN9517	Using the HI5714 Evaluation Board (11 pages) AN9517	A description of how to use the HI5714 evaluation board.
HI5721 AN9410	Using The HI5721 Evaluation Module (11 pages) AN9410.1	A description of how to use the HI5721 evaluation board.
HI5721 AN9501	Understanding the HI5721 D/A Converter Spectral Specifications (3 pages) AN9501.1	Discussion of the HI5721 D/A Converter Spectral Specifications including SFDR, FFT and ENOB.
HI5731 AN9602	Using The HI5731 Evaluation Module (11 pages) AN9602	A description of how to use the HI5731 evaluation board.

Technical Literature Abstracts (Continued)

PART NUMBER/ DOCUMENT NUMBER	TITLE	ABSTRACT
HI5741 AN9619	Optimizing Setup Conditions for High Accuracy Measurements of the HI5741 (4 pages) AN9619	Details the optimized design techniques required to realize the full SFDR and low glitch capability of this 14-bit, 100MHz DAC.
HI5741 AN9626	Using The HI5741 Evaluation Module (12 pages) AN9626	A description of how to use the HI5741 evaluation board.
HI5741 AN9629	Multi-Tone Performance of the HI5741 (3 pages) AN9629	Provides a complete discussion of Multi-tone measurement.
HI5746, HI5703 AN9631	Performance Evaluation of the HI5746 Using the HI5703 Evaluation Board (7 pages) AN9631	A guide for using the robust HI5703 evaluation board to measure the performance of the new HI5746 device.
HI5780 AN9530	Using The HI5780 Evaluation Module (9 pages) AN9530	A description of how to use the HI5780 evaluation board.
HI5800 AN9203	Using the HI5800 Evaluation Board (13 pages)	A description of how to use the HI5800 evaluation board.
HI5804EVAL AN9647	Using the HI5804 Evaluation Board (14 pages) AN9647	A description of how to use the HI5804 evaluation board.
HI5805EVAL1 AN9707	Using the HI5805EVAL1 Evaluation Board (15 pages) AN9707	A description of how to use the HI5805 evaluation board.
HI5810, HI5812, HI5813, HI5816 TB335	Driving the Analog Input of the HI581X Family of 12-Bit Analog-to-Digital Converters (2 pages) TB335	Driving the Analog Input of the HI581X Family of 12-Bit Analog-to-Digital Converters.
HI5812, HI5813 AN9326	A Complete Analog-to-Digital Converter Operating from a Single 3.3V Power Supply (4 pages)	A discussion of the Harris HI5812, 12-bit, Analog-to-Digital Converter Operating from a Single 3.3V Power Supply
HI7188 AN9518	Using The HI7188 Evaluation Kit (22 pages) AN9518.1	A description of how to use the HI7188 evaluation kit. Included in the evaluation kit is the evaluation board, software (DOS and LabWindows), sample and literature. The literature includes the datasheet, application notes and technical briefs pertaining to this device.
HI7188 AN9538	Using The HI7188 Serial Interface (5 pages) AN9538	Describes the communication with the device via the serial interface. Includes a discussion of the communication cycles and examples of single byte or multi-byte transfers.
HI7188 AN9610	Interfacing the HI7188 to a Microcontroller (7 pages) AN9610	This application note discusses the HI7188 serial port and details two application circuits and pseudo code useful in demonstrating how to interface the HI7188 to a microcontroller.
HI7188 AN9620	Using the HI7188 with a Single Supply (3 pages) AN9620	Informs the system designer how to use the HI7188 with a single positive supply if a negative supply is not available. One approach is to offset the positive supply and the other is to use the ICL7660S to derive a negative supply.
HI7188 AN9634	Using the HI7188 to Create a 64 Channel Multiplexed System (5 pages) AN9634	The purpose of this application note is to demonstrate the power and flexibility of the HI7188 to create a differential 64-channel A/D system.

Technical Literature Abstracts (Continued)

PART NUMBER/ DOCUMENT NUMBER	TITLE	ABSTRACT
HI7188 AN9669	HI7188 LabWindows Evaluation Board Program (6 pages) AN9669	Provides information about the LabWindows software written to support the HI7188 evaluation board. This program is windows-based and makes it very easy to program the HI7188 device.
HI7188 TB345	Amended Information to Using the HI7188 Clock Input (1 page) TB345	An update on a temporary change to the clock requirements for the HI7188.
HI7188, HI7190, HI7191 TB329	Harris Sigma-Delta Calibration Technique (3 pages) TB329	Describes the calibration procedure and theory for the HI7188, HI7190 and HI7191 A/D converters.
HI7190 TB331	Using the HI7190 Serial Interface (3 pages) TB331	Describes the communication with the device via the serial interface. Includes a discussion of the communication cycles and examples of single byte or multi-byte transfers.
HI7190 AN9504	A Brief Introduction to Sigma Delta Conversion (7 pages) AN9504	A complete discussion of the sigma-delta modulator theory.
HI7190, ICL7660S AN9601	Using the HI7190 with Single +5V Supply (2 pages) AN9601	Informs the system designer how to use the HI7190 with a single positive supply if a negative supply is not available. This is accomplished by using the ICL7660S to derive a negative supply.
HI7190 AN9505	Using the HI7190 Evaluation Kit (11 pages)	A description of how to use the HI7190/1 evaluation board.
HI7190 AN9527	Interfacing the HI7190 to a Microcontroller (5 pages) AN9527	This application note discusses the HI7190 serial port and details two application circuits and pseudo code useful in demonstrating how to interface the HI7190 to a microcontroller.
HI7190 AN9532	Using the HI7190 in a Multiplexed System (3 pages) AN9532	The purpose of this application note is to demonstrate the power and flexibility of the HI7188 to create a differential 64-channel A/D system.
ICL7103A, ICL8052 AN028	Build an Auto-Ranging DMM with the ICL7103A/8052A A/D Converter Pair (6 pages)	Basic circuit configuration and operation, decimal point drive, interface to parallel data systems, auto-ranging designs, issues and solutions for proper operation.
ICL7104 AN030	ICL7104: A Binary Output A/D Converter for Microprocessors (16 pages)	Interfacing to a digital system in non-handshaking mode, a handshaking mode interface to various processors, performance enhancement techniques, and an auto-zero loop discussion.
ICL7106 AN023	Low Cost Digital Panel Meter Designs (5 pages)	Cost advantages of display converters, Evaluation kit usage, display types, capacitors recommended, and proper power supply range.
ICL7106 AN046	Building a Battery Operated Auto Ranging DVM with the ICL7106 (5 pages)	Auto-ranging circuitry design, the input range/resistor divider, an auto-range clock circuit design, power supply requirements, measuring resistance and transconductance, and using the ICL7126 and ICL7107.
ICL7106 AN059	Digital Panel Meter Experiments for the Hobbyist (7 pages)	Discusses the fundamentals of designing a panel meter for measuring, DC Voltages, AC Voltages, resistance measurements, current measurements, temperature measurement, and designing multi-range DVMs.

Technical Literature Abstracts (Continued)

PART NUMBER/ DOCUMENT NUMBER	TITLE	ABSTRACT
ICL7106, ICL7107, ICL7109 AN032	Understanding the Auto-Zero and Common Mode Performance of the ICL7106/ 7107/7109 Family (8 pages)	Theory of operation for the four integration phases, CMRR and the common mode voltage effects, the auto-zero loop residual, and in-depth error analysis.
ICL7106, ICL7117, ICL7126, ICL7107, ICL7116 AN052	Tips for Using Single Chip 3.5 Digit A/D Converters (9 pages)	Some of the more commonly asked questions concerning the $3^1/_2$ digital display converters ranging from power supply inputs, display types and drive, to timing, ratiometric operation, and component selection. A troubleshooting guide is provided.
ICL7106, ICL7107, ICL7116, ICL7117, ICL7129, ICL7131, ICL7133, ICL7136, ICL713 AN9609	Overcoming Common-Mode Range Issues When Using Harris Integrating Converters (3 pages) AN9609.1	A design technique to resolve excessive common-mode range when using Harris Integrating A/D Converters.
ICL7109 AN049	Applying the 7109 A/D Converter (5 pages)	A description of the ICL7109s, differential input section, differential reference, digital section and how to measure bridges, and offsets. Interface examples to parallel processors, serial interfaces and how to replace Voltage-to-frequency converters.
ICL7135 AN054	Display Driver Family Combines Convenience of Use with Microprocessor Interfaceability (18 pages)	Advantages of IC display drivers, non-multiplexed display operation, functional block diagrams, multiplexed display operation, and binary to bar graph display applications circuits.
ICL7135 AN017	The Integrating A/D Converter (5 pages)	The dual slope conversion technique, analyzing errors, capacitor induced errors and a noise discussion.
ICL7139 AN9336	Multi-Meter Display Converter Eases DMM Design (6 pages)	A detailed discussion of the Harris dual-slope A/D converter which can easily be used to create a cost-effective digital multi-meter(DMM).
ICL8052 AN042	Interpretation of Data Converter Accuracy Specifications (11 pages)	A Discussion of data converter transfer functions, quantization noise and dynamic range, non-ideal data converter operation, nonlinearity, temperature induced errors, error budgets, layout and grounding rules.
IH5009 AN004	The IH5009 Analog Switch Series (9 pages)	Circuit operation, logic compatibility, switching speed and crosstalk, and application circuits.

DATA ACQUISITION 16

PACKAGING INFORMATION

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Data Acquisition Package Selection Guide

Using the Selection Guide:

The first character of each entry indicates the package type, while the number preceding the decimal point details the package lead count. Except for MQFP, LCC, SIP, and Can packages, the decimal point and succeeding numbers specify the reference package width in inches (e.g. __.150 = 150 mil width).

PART NUMBER	PDIP	SOIC/ SSOP	PLCC	MQFP	CERDIP	SIDE-BRAZE	LCC	SIP	CAN
AD590									T3.A
AD7520	E16.3				F16.3				
AD7521	E18.3								
AD7523	E16.3								
AD7530	E16.3								
AD7531	E18.3								
AD7533	E16.3								
AD7541	E18.3								
AD7545	E20.3								
ADC0802	E20.3				F20.3				
ADC0803	E20.3	M20.3			F20.3				
ADC0804	E20.3				F20.3				
CA3161	E16.3								
CA3162	E16.3								
CA3162A	E16.3								
CA3304	E16.3	M16.3			F16.3				
CA3306	E18.3	M20.3			F18.3		J20.B		
CA3310	E24.3	M24.3			F24.3				
CA3318	E24.6	M24.3			F24.6				
CA3338	E16.3	M16.3			F16.3				
CA555	E8.3	M8.15							T8.C
DG200	E14.3				F14.3				T10.B
DG201	E16.3				F16.3				
DG201A	E16.3	M16.3			F16.3				
DG202	E16.3				F16.3				
DG211	E16.3	M16.15							
DG212	E16.3	M16.15							
DG300A	E14.3				F14.3				T10.B
DG301A	E14.3				F14.3				T10.B
DG302A	E14.3				F14.3				
DG303A	E14.3	M16.3			F14.3				
DG308A	E16.3	M16.15			F16.3				
DG309	E16.3	M16.15			F16.3				
DG401	E16.3	M16.15			F16.3				
DG403	E16.3	M16.15			F16.3				
DG405	E16.3	M16.15			F16.3				
DG406	E16.3	M16.15							

EXAMPLE: **M 16 .15**

PACKAGE TYPE — LEAD COUNT — BODY WIDTH

Data Acquisition Package Selection Guide

PART NUMBER	PDIP	SOIC/ SSOP	PLCC	MQFP	CERDIP	SIDE-BRAZE	LCC	SIP	CAN
DG407	E28.6	M16.15							
DG408	E16.3	M16.15			F16.3				
DG409	E16.3	M16.15			F16.3				
DG411	E16.3	M16.15			F16.3				
DG412	E16.3	M16.15			F16.3				
DG413	E16.3	M16.15			F16.3				
DG441	E16.3	M16.15			F16.3				
DG442	E16.3	M16.15			F16.3				
DG444	E16.3	M16.15							
DG445	E16.3	M16.15							
DG506A	E28.6	M28.3			F28.6				
DG507A	E28.6	M28.3			F28.6				
DG508A	E16.3	M16.3			F16.3				
DG509A	E16.3	M16.3			F16.3				
HA7210	E8.3	M8.15							
HA7211		M8.15							
HI-0200	E14.3				F14.3				T10.B
HI-0201	E16.3	M16.15	N20.35		F16.3				
HI-0201-HS	E16.3	M16.3	N20.35		F16.3		J20.A		
HI-0300	E14.3	M14.15			F14.3				T10.B
HI-0301	E14.3	M14.15			F14.3				T10.B
HI-0302	E14.3	M14.15			F14.3				
HI-0303	E14.3	M14.15			F14.3				
HI-0304	E14.3	M14.15			F14.3				T10.B
HI-0305	E14.3	M14.15			F14.3				T10.B
HI-0306	E14.3	M14.15			F14.3				
HI-0307	E14.3	M14.15			F14.3				
HI-0381	E14.3	M14.15			F14.3				T10.B
HI-0384	E16.3	M16.3			F16.3				
HI-0387	E14.3	M14.15			F14.3				T10.B
HI-0390	E16.3	M16.3			F16.3				
HI-0506	E28.6	M28.3	N28.45		F28.6		J28.A		
HI-0506A	E28.6				F28.6				
HI-0507	E28.6	M28.3	N28.45		F28.6		J28.A		
HI-0507A	E28.6				F28.6				
HI-0508	E16.3	M16.15	N20.35		F16.3		J20.A		
HI-0508A	E16.3				F16.3				
HI-0509	E16.3	M16.15	N20.35		F16.3		J20.A		
HI-0509A	E16.3				F16.3				
HI-0516	E28.6	M28.3	N28.45		F28.6		J28.A		
HI-0518	E18.3	M18.3	N20.35		F18.3		J20.A		

EXAMPLE: M 16 .15

PACKAGE TYPE — LEAD COUNT — BODY WIDTH

Data Acquisition Package Selection Guide

PART NUMBER	PDIP	SOIC/ SSOP	PLCC	MQFP	CERDIP	SIDE-BRAZE	LCC	SIP	CAN
HI-0524	E18.3		N20.35		F18.3		J20.A		
HI-0539	E16.3		N20.35		F16.3				
HI-0546	E28.6	M28.3	N28.45		F28.6		J28.A		
HI-0547	E28.6	M28.3	N28.45		F28.6		J28.A		
HI-0548	E16.3	M16.15	N20.35		F16.3		J20.A		
HI-0549	E16.3	M16.15	N20.35		F16.3		J20.A		
HI-0565A						D24.6			
HI-0574A	E28.6					D28.6	J44.A		
HI-0674A	E28.6					D28.6	J44.A		
HI-0774	E28.6					D28.6	J44.A		
HI1106	E24.4-S	M24.2-S							
HI1166							J68.A		
HI1171		M24.2-S							
HI1172	E16.3A-S	M16.2-S							
HI1175	E24.4-S	M24.2-S							
HI1176				Q32.7x7-S					
HI1177				Q32.7x7-S					
HI1178				Q48.12x12-S					
HI1179				Q32.7x7-S					
HI1260				Q48.12 x 12-S					
HI1276							J68.B		
HI1386	E28.6A-S						J44.B		
HI1396						D42.6	J68.A		
HI1826				Q32.7x7-S					
HI1866				Q48.12x12-S					
HI2300				Q32.7x7-S					
HI2301				Q32.7x7-S					
HI2302				Q32.7x7-S					
HI2303				Q80.14x20-S					
HI2304				Q48.7x7-S					
HI2307				Q64.10x10-S					
HI2309				Q48.12x12-S					
HI2315				Q32.7x7-S					
HI3026				Q48.12x12-S					
HI3026A				Q48.12x12-S					
HI3086				Q48.12x12-S					
HI3197				TBD					
HI3050				Q64.14x20-S					
HI-1818A	E16.3		N20.35		F16.3				
HI-1828A	E16.3		N20.35		F16.3		J20.A		
HI-5040	E16.3				F16.3				
HI-5041	E16.3				F16.3				

EXAMPLE: **M 16 .15**

PACKAGE TYPE — LEAD COUNT — BODY WIDTH

Data Acquisition Package Selection Guide

PART NUMBER	PDIP	SOIC/ SSOP	PLCC	MQFP	CERDIP	SIDE-BRAZE	LCC	SIP	CAN
HI-5042	E16.3				F16.3				
HI-5043	E16.3	M16.15			F16.3		J20.A		
HI-5044	E16.3				F16.3				
HI-5045	E16.3	M16.15			F16.3				
HI-5046	E16.3				F16.3				
HI-5046A	E16.3				F16.3				
HI-5047	E16.3				F16.3				
HI-5047A	E16.3				F16.3				
HI-5048	E16.3				F16.3				
HI-5049	E16.3	M16.15			F16.3				
HI-5050	E16.3				F16.3				
HI-5051	E16.3	M16.15	N20.35		F16.3		J20.A		
HI5662				Q44.10x10					
HI-5701	E18.3	M18.3							
HI5702		M28.3							
HI5703		M28.3							
HI5710				Q48.7x7-S					
HI5714		M24.3							
HI5721	E28.6	M28.3							
HI5728				Q44.10x10					
HI5731	E28.6	M28.3							
HI5735	E28.6	M28.3							
HI5741	E28.6	M28.3							
HI5746		M28.3							
HI5760		M28.3							
HI5762				Q44.10x10					
HI5766		M28.3							
HI5767		M28.3							
HI5780				Q32.7x7-S					
HI5800						D40.6			
HI5804		M28.3							
HI5805		M28.3							
HI5808		M28.3							
HI5810	E24.3	M24.3			F24.3				
HI5812	E24.3	M24.3			F24.3				
HI5813	E24.3	M24.3			F24.3				
HI5905				Q44.10x10					
HI7131	E40.6			Q44.10x10					
HI7133	E40.6			Q44.10x10					
HI7159A	E28.6								
HI7188	E40.6			Q44.10x10					

EXAMPLE: M 16 .15

PACKAGE TYPE — LEAD COUNT — BODY WIDTH

Data Acquisition Package Selection Guide

PART NUMBER	PDIP	SOIC/ SSOP	PLCC	MQFP	CERDIP	SIDE-BRAZE	LCC	SIP	CAN
HI7190	E20.3	M20.3							
HI7191	E20.3	M20.3							
HI20201	E28.6A-S	M28.3A-S							
HI20203	E28.6A-S	M28.3A-S							
HI-DAC80V	E24.6								
HI-DAC85V	E24.6								
HIN200		M20.3							
HIN201		M16.3							
HIN202	E16.3	M16.3/ M16.209							
HIN203	E20.3	M20.3							
HIN204		M16.3							
HIN205	E24.3								
HIN206	E24.3	M24.3/ M24.209							
HIN207	E24.3	M24.3/ M24.209							
HIN208	E24.3	M24.3/ M24.209							
HIN209	E24.3	M24.3							
HIN211		M28.3/ M28.209							
HIN213		M28.3/ M28.209							
HIN230		M20.3							
HIN231		M16.3							
HIN232	E16.3	M16.3			F16.3				
HIN233	E20.3								
HIN234		M16.3							
HIN235	E24.3								
HIN236	E24.3	M24.3							
HIN237	E24.3	M24.3							
HIN238	E24.3	M24.3							
HIN239		M24.3							
HIN240				Q44.10x10					
HIN241		M28.3/ M28.209							
ICL232	E16.3	M16.3			F16.3				
ICL7106	E40.6			Q44.10x10					
ICL7107	E40.6			Q44.10x10					
ICL7109	E40.6				F40.6	D40.6			
ICL7116	E40.6			Q44.10x10					
ICL7117	E40.6								

EXAMPLE: **M 16 .15**

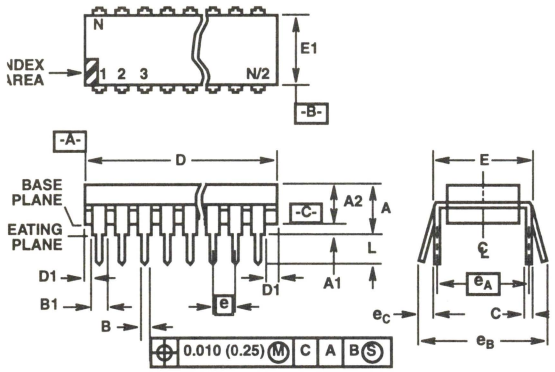
PACKAGE TYPE — LEAD COUNT — BODY WIDTH

Data Acquisition Package Selection Guide

PART NUMBER	PDIP	SOIC/ SSOP	PLCC	MQFP	CERDIP	SIDE-BRAZE	LCC	SIP	CAN
ICL7126	E40.6								
ICL71C03	E28.6								
ICL7129	E40.6			Q44.10x10					
ICL7135	E28.6								
ICL7136	E40.6			Q44.10x10					
ICL7137	E40.6			Q44.10x10					
ICL7139	E40.6								
ICL7149	E40.6			Q44.10x10					
ICL8052	E14.3				F14.3	D14.3			
ICL8068					F14.3	D14.3			
ICL8069		M8.15						Z3.05	T2.A
ICM7170	E24.6	M24.3			F24.6	D24.6			
ICM7211	E40.6			Q44.10x10					
ICM7212	E40.6								
ICM7213	E14.3								
ICM7216A	E28.6				F28.6				
ICM7216B	E28.6				F28.6				
ICM7216D	E28.6				F28.6				
ICM7217	E28.6				F28.6				
ICM7224	E40.6								
ICM7226A	E40.6								
ICM7226B					F40.6				
ICM7228	E28.6	M28.3			F28.6				
ICM7231	E40.6				F40.6				
ICM7232	E40.6				F40.6				
ICM7242	E8.3	M8.15							
ICM7243	E40.6				F40.6				
ICM7249	E48.6								
ICM7555	E8.3	M8.15							T8.C
ICM7556	E14.3				F14.3				
IH5043	E16.3	M16.15			F16.3				
IH5052					F16.3				
IH5053					F16.3				
IH5151	E16.3				F16.3				
IH5341	E14.3								T10.B
IH5352	E16.3	M20.3			F16.3				T10.B

EXAMPLE: **M 16 .15**

Dual-In-Line Plastic Packages (PDIP)



E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

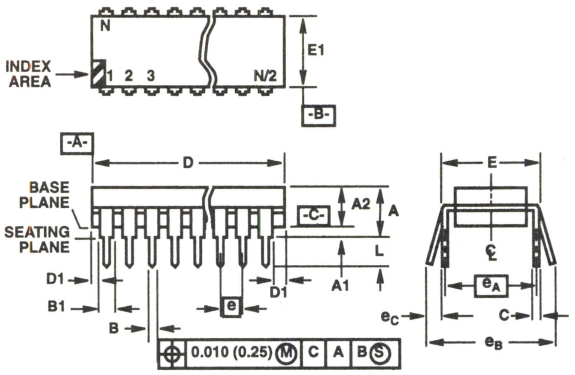
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



NOTES:

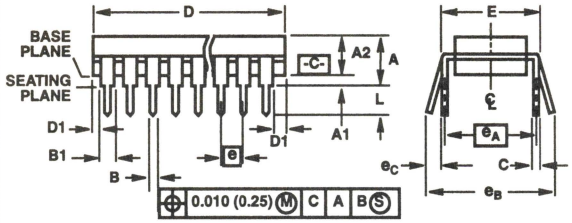
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (PDIP)



E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

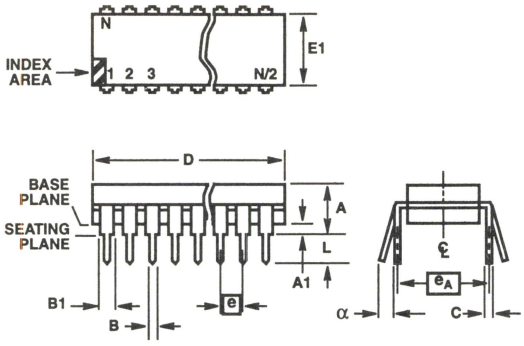
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E16.3A-S

16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.142	0.161	3.60	4.10	2
A1	0.020	-	0.50	-	2
B	0.016	0.023	0.40	0.60	-
B1	0.042	0.053	1.05	1.35	-
C	0.008	0.013	0.20	0.35	-
D	0.752	0.771	19.10	19.60	3
E1	0.244	0.263	6.30	6.70	3
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		4
L	0.119	-	3.00	-	2
N	16		16		5
α	0^o	15^o	0^o	15^o	-

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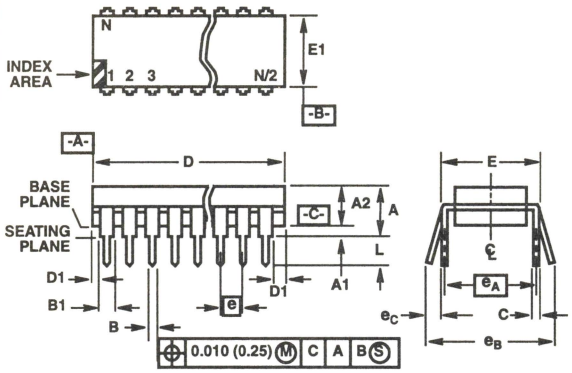
NOTES:

1. Controlling Dimensions: MILLIMETER. In case of conflict between English and Metric dimensions, the metric dimensions control.
2. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
3. D and E1 dimensions do not include mold flash or protrusions.
4. $\boxed{e_A}$ is measured with the leads constrained to be perpendicular to base plane.
5. N is the maximum number of terminal positions.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

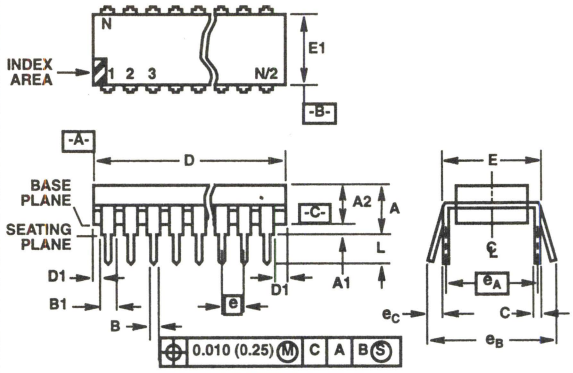
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E18.3 (JEDEC MS-001-BC ISSUE D)
18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.845	0.880	21.47	22.35	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	18		18		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (PDIP)



E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

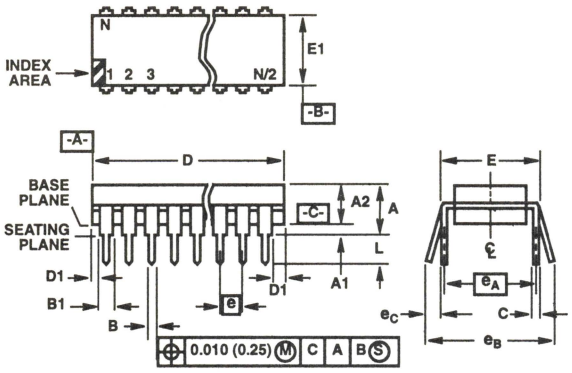
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E24.3 (JEDEC MS-001-AF ISSUE D)
24 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

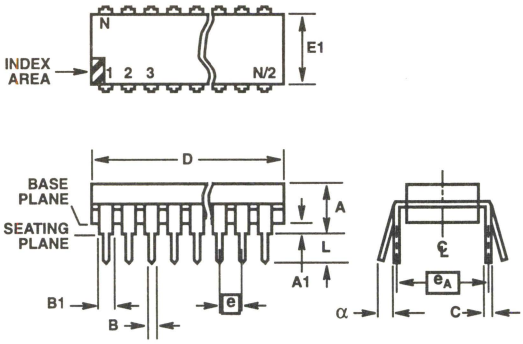
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	1.230	1.280	31.24	32.51	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	24		24		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E24.4-S

24 LEAD DUAL-IN-LINE PLASTIC PACKAGE (400 MIL)

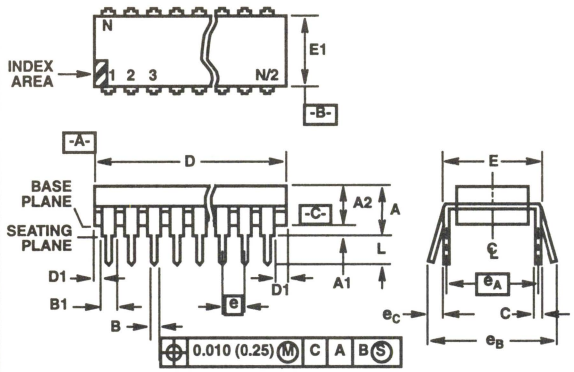
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.142	0.161	3.60	4.10	2
A1	0.020	-	0.50	-	2
B	0.016	0.023	0.40	0.60	-
B1	0.042	0.053	1.05	1.35	-
C	0.008	0.013	0.20	0.35	-
D	1.185	1.204	30.10	30.60	3
E1	0.331	0.346	8.40	8.80	3
e	0.100 BSC		2.54 BSC		-
e_A	0.400 BSC		10.16 BSC		4
L	0.119	-	3.0	-	2
N	24		24		5
α	0^o	15^o	0^o	15^o	-

Rev. 1 4/95

NOTES:

1. Controlling Dimensions: MILLIMETER. In case of conflict between English and Metric dimensions, the metric dimensions control.
2. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
3. D and E1 dimensions do not include mold flash or protrusions.
4. e_A is measured with the leads constrained to be perpendicular to base plane.
5. N is the maximum number of terminal positions.

Dual-In-Line Plastic Packages (PDIP)



E24.6 (JEDEC MS-011-AA ISSUE B)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

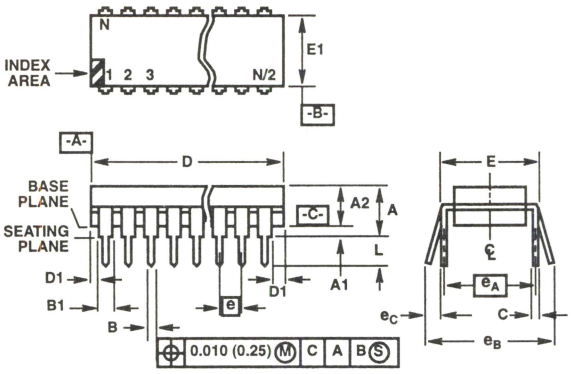
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	24		24		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

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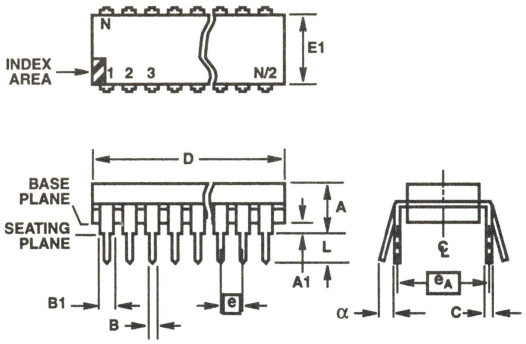
Dual-In-Line Plastic Packages (PDIP)



E28.6A-S

28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

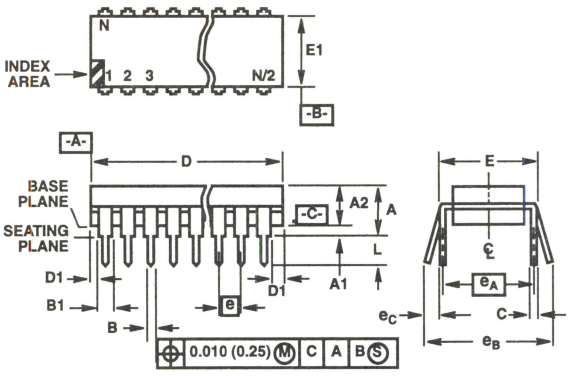
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.178	0.196	4.5	5.0	2
A1	0.020	-	0.50	-	2
B	0.016	0.023	0.40	0.60	-
B1	0.042	0.053	1.05	1.35	-
C	0.008	0.13	0.20	0.35	-
D	1.485	1.503	37.7	38.2	3
E1	0.508	0.523	12.9	13.3	3
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		4
L	0.119	-	3.0	-	2
N	28		28		5
α	0°	15°	0°	15°	-

Rev. 1 4/95

NOTES:

1. Controlling Dimensions: MILLIMETER. In case of conflict between English and Metric dimensions, the metric dimensions control.
2. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
3. D and E1 dimensions do not include mold flash or protrusions.
4. e_A is measured with the leads constrained to be perpendicular to base plane.
5. N is the maximum number of terminal positions.

Dual-In-Line Plastic Packages (PDIP)



E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

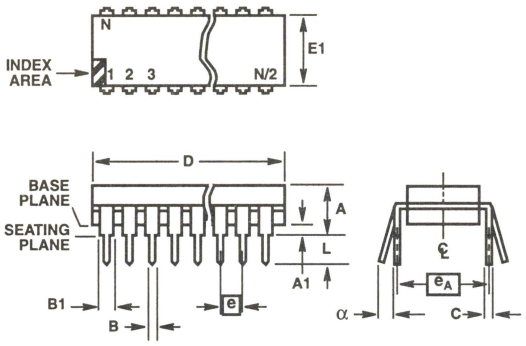
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Shrink Dual-In-Line Plastic Packages (SPDIP)



E42.6B-S

42 LEAD SHRINK DUAL-IN-LINE PLASTIC PACKAGE

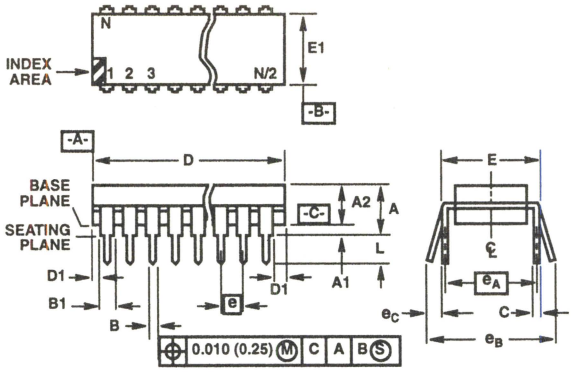
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.178	0.190	4.50	5.00	2
A1	0.020	-	0.50	-	2
B	0.016	0.023	0.40	0.60	-
B1	0.030	0.041	0.75	1.405	-
C	0.008	0.013	0.20	0.35	-
D	1.485	1.503	37.70	38.20	3
E1	0.508	0.523	12.90	13.30	3
e	0.070 BSC		1.778 BSC		-
e_A	0.600 BSC		15.24 BSC		4
L	0.119	-	3.00	-	2
N	42		42		5
α	0^o	15^o	0^o	15^o	-

Rev. 0 2/96

NOTES:

1. Controlling Dimensions: MILLIMETER. In case of conflict between English and Metric dimensions, the metric dimensions control.
2. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
3. D and E1 dimensions do not include mold flash or protrusions.
4. e_A is measured with the leads constrained to be perpendicular to base plane.
5. N is the maximum number of terminal positions.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

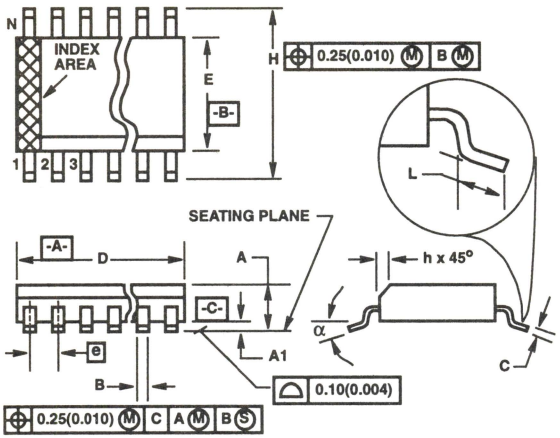
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E48.6 (JEDEC MS-011-AD ISSUE B)
48 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	2.385	2.480	60.70	63.1	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	48		48		9

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



NOTES:

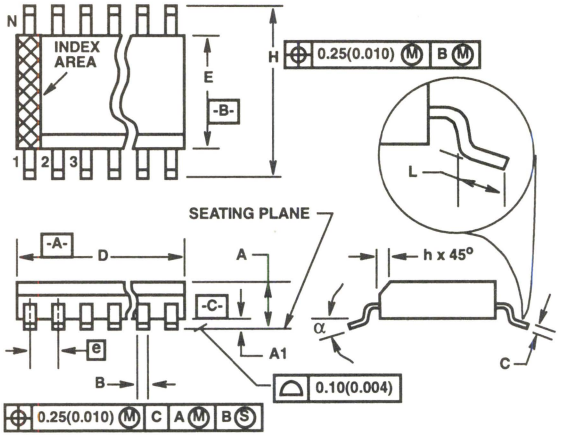
1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

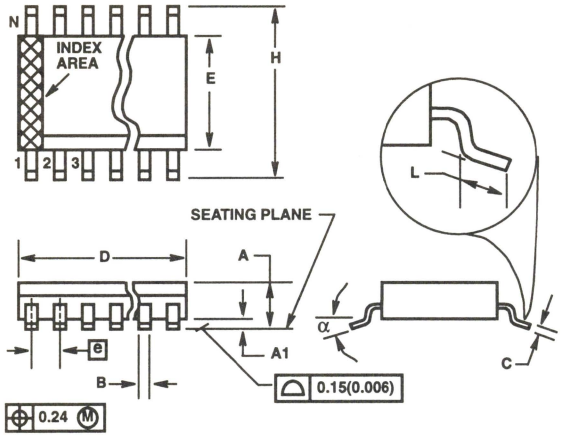
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M16.2-S

16 LEAD SMALL OUTLINE PLASTIC PACKAGE (200 MIL)

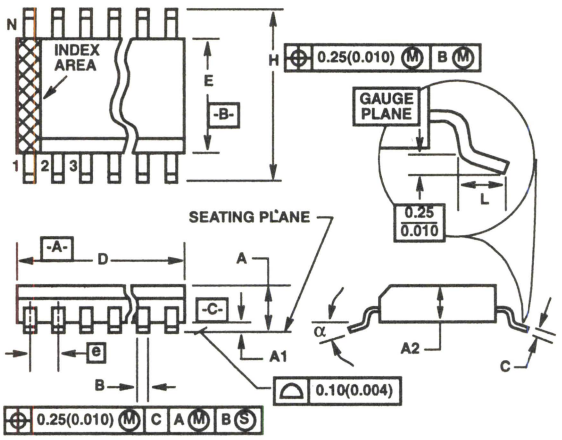
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.067	0.078	1.70	2.00	-
A1	0.002	0.011	0.05	0.30	-
B	0.014	0.021	0.35	0.55	-
C	0.006	0.011	0.15	0.30	-
D	0.386	0.405	9.80	10.30	1
E	0.205	0.220	5.20	5.60	2
e	0.050 BSC		1.27 BSC		-
H	0.296	0.326	7.50	8.3	-
L	0.012	0.027	0.30	0.70	3
N	16		16		4
α	0^o	10^o	0^o	10^o	-

Rev. 0 2/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SSOP)



M16.209 (JEDEC MO-150-AC ISSUE B)
16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

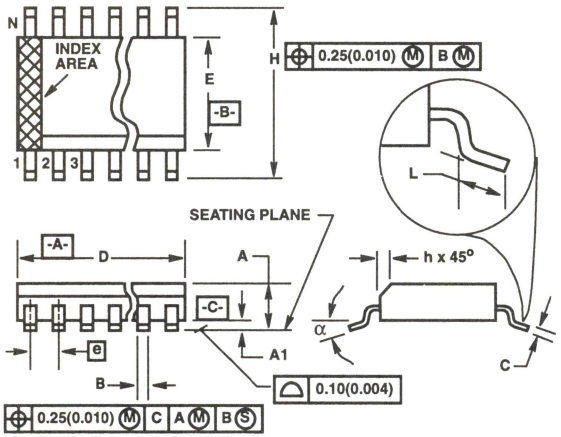
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.233	0.255	5.90	6.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

Rev. 2 3/95

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

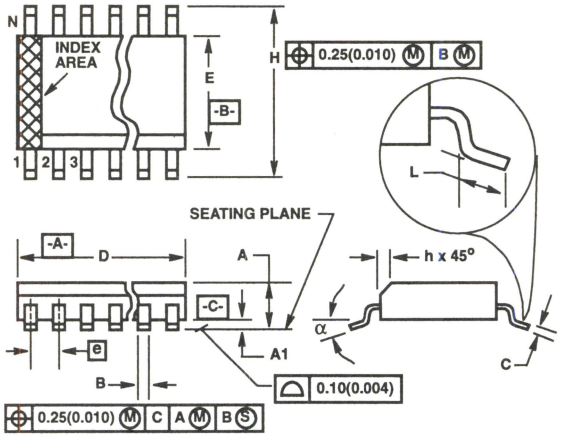
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M18.3 (JEDEC MS-013-AB ISSUE C)
18 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

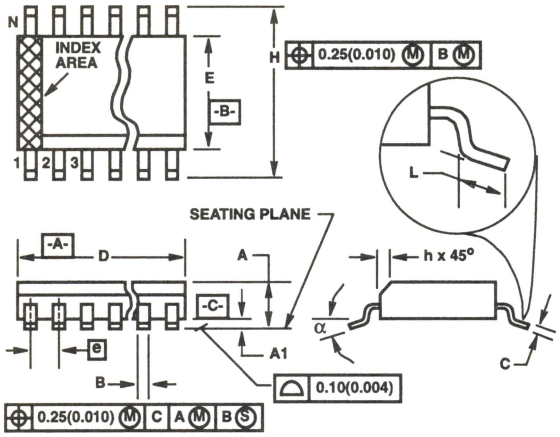
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4469	0.4625	11.35	11.75	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	18		18		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

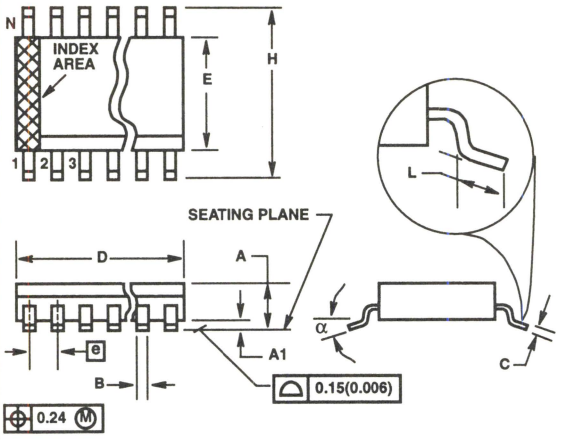
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M24.2-S

24 LEAD SMALL OUTLINE PLASTIC PACKAGE (200 MIL)

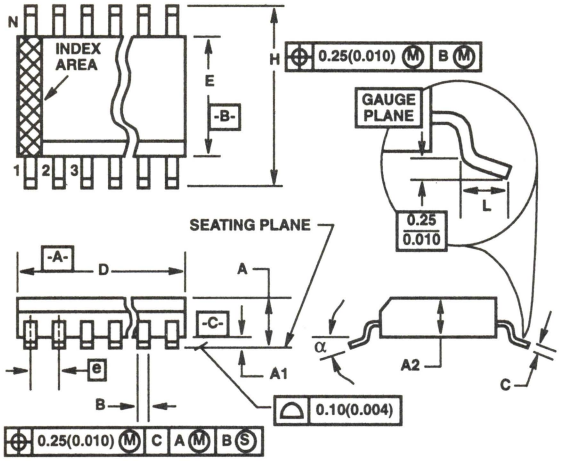
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.067	0.088	1.70	2.25	-
A1	0.002	0.011	0.05	0.30	-
B	0.014	0.021	0.35	0.55	-
C	0.006	0.011	0.15	0.30	-
D	0.587	0.606	14.9	15.4	1
E	0.205	0.220	5.2	5.6	2
e	0.050 BSC		1.27 BSC		-
H	0.296	0.326	7.5	8.3	-
L	0.012	0.027	0.30	0.70	3
N	24		24		4
α	0°	10°	0°	10°	-

Rev. 1 4/95

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)



M24.209 (JEDEC MO-150-AG ISSUE B)
24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

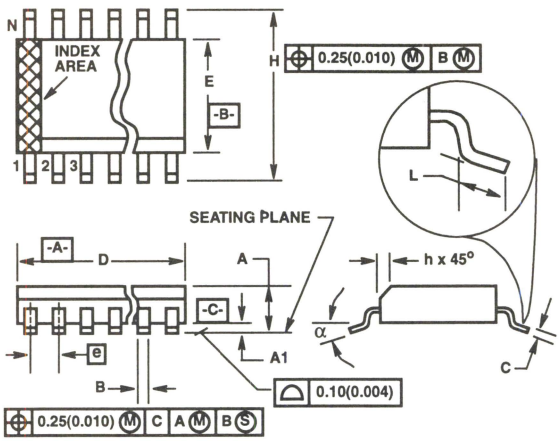
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.312	0.334	7.90	8.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 1 3/95

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

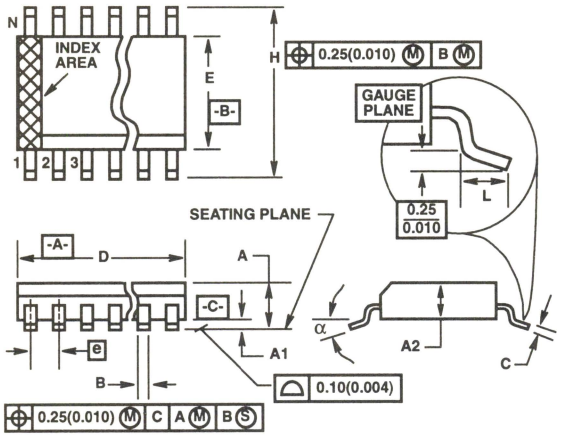
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact

Shrink Small Outline Plastic Packages (SSOP)



M28.209 (JEDEC MO-150-AH ISSUE B)
28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

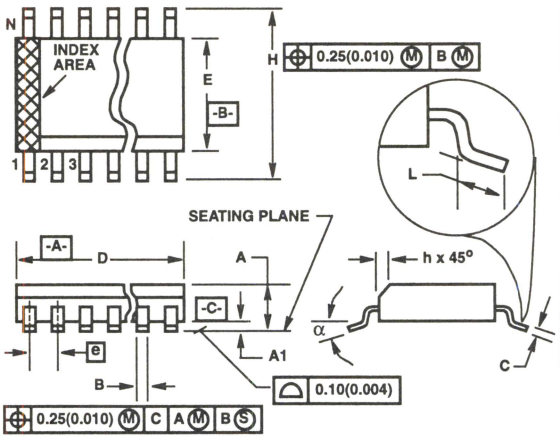
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.390	0.413	9.90	10.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

Rev. 1 3/95

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

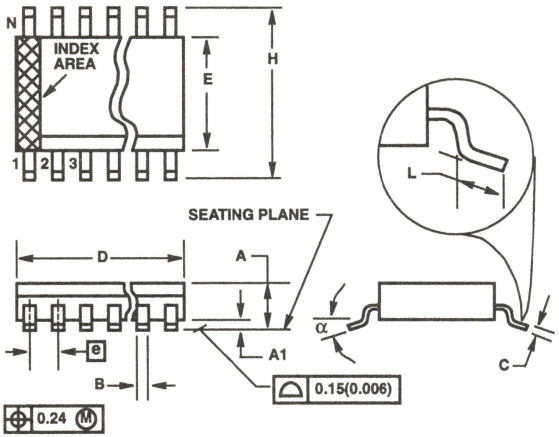
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M28.3A-S

28 LEAD SMALL OUTLINE PLASTIC PACKAGE (300 MIL)

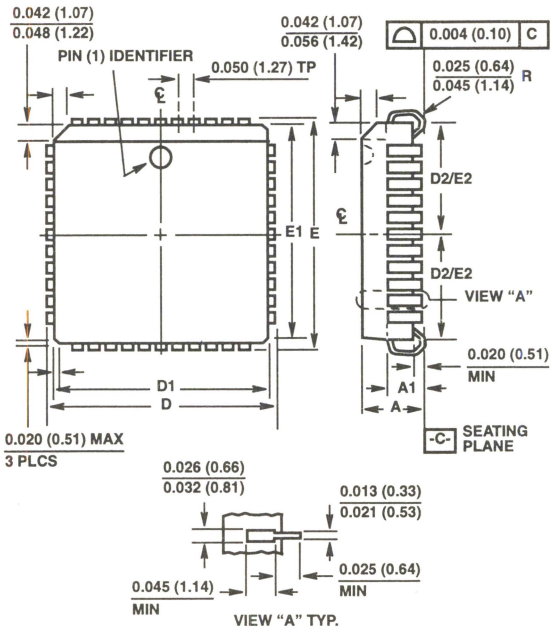
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.085	0.106	2.15	2.7	-
A1	0.002	0.011	0.05	0.30	-
B	0.014	0.021	0.35	0.55	-
C	0.004	0.009	0.10	0.25	-
D	0.737	0.755	18.7	19.2	1
E	0.296	0.311	7.50	7.90	2
e	0.05 BSC		1.27 BSC		-
H	0.390	0.421	9.90	10.70	-
L	0.012	0.027	0.30	0.70	3
N	28		28		4
α	0°	10°	0°	10°	-

Rev. 1 4/95

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Plastic Leaded Chip Carrier Packages (PLCC)



N20.35 (JEDEC MS-018AA ISSUE A)
20 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

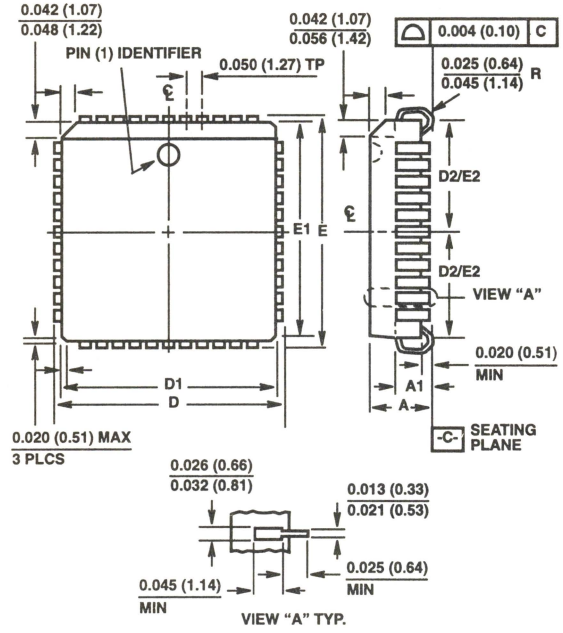
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.385	0.395	9.78	10.03	-
D1	0.350	0.356	8.89	9.04	3
D2	0.141	0.169	3.59	4.29	4, 5
E	0.385	0.395	9.78	10.03	-
E1	0.350	0.356	8.89	9.04	3
E2	0.141	0.169	3.59	4.29	4, 5
N	20		20		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

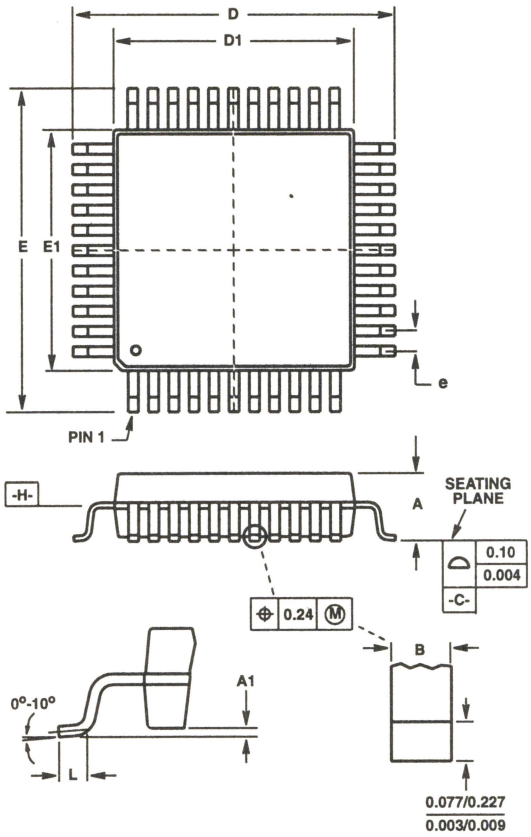
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q32.7x7-S

32 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

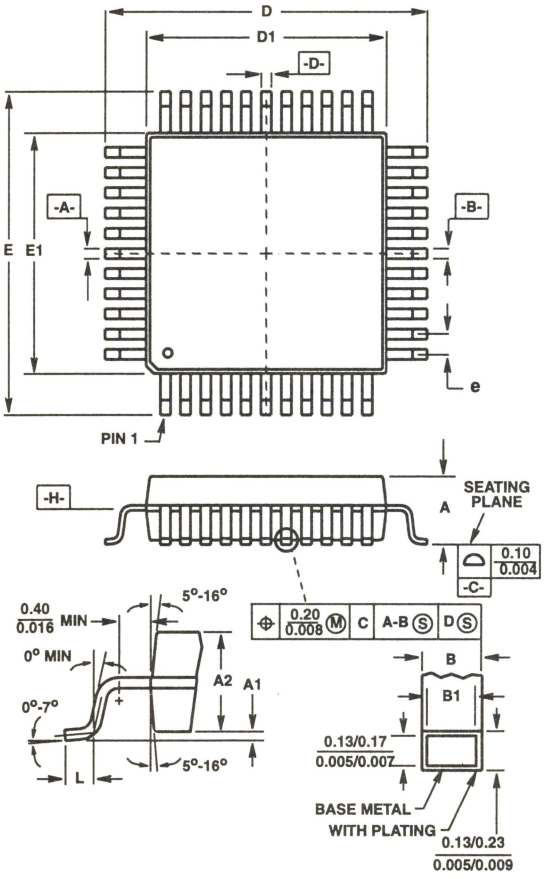
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.054	0.072	1.35	1.85	-
A1	0.000	0.011	0.00	0.30	-
B	0.008	0.017	0.20	0.45	5
D	0.347	0.362	8.80	9.20	2
D1	0.272	0.287	6.90	7.30	3, 4
E	0.347	0.362	8.80	9.20	2
E1	0.272	0.287	6.90	7.30	3, 4
L	0.012	0.027	0.30	0.70	-
N	32		32		6
e	0.032 BSC		0.80 BSC		-

Rev. 2 4/95

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q44.10x10 (JEDEC MO-108AA-2 ISSUE A)
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

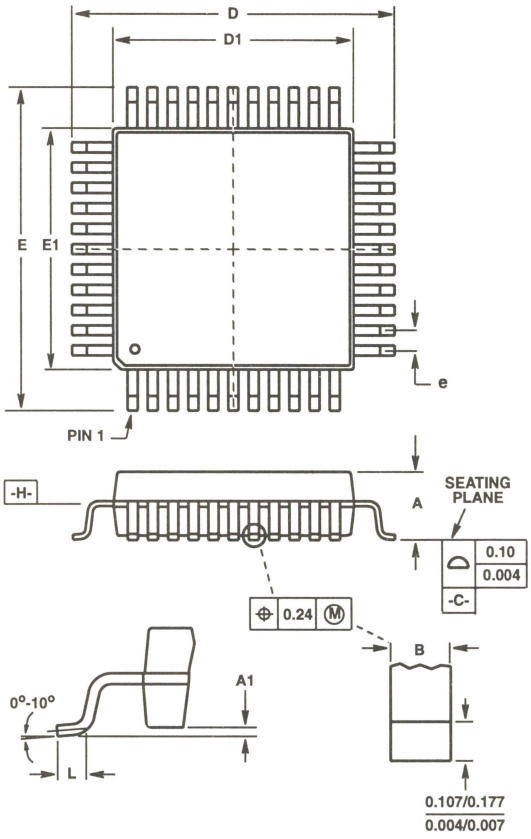
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.093	-	2.35	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.510	0.530	12.95	13.45	3
D1	0.390	0.398	9.90	10.10	4, 5
E	0.510	0.530	12.95	13.45	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 1 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q48.7x7-S

48 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

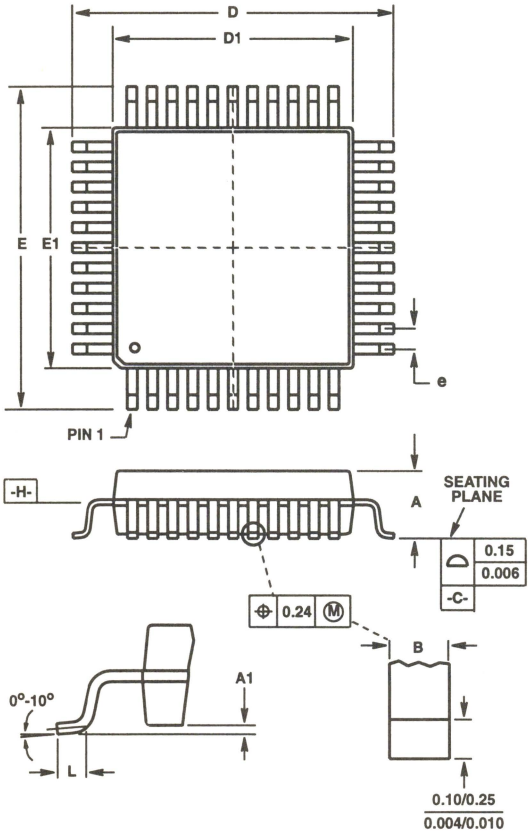
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.056	0.066	1.40	1.70	-
A1	0.000	0.007	0.00	0.20	-
B	0.006	0.010	0.15	0.26	5
D	0.347	0.362	8.80	9.20	2
D1	0.272	0.279	6.90	7.10	3, 4
E	0.347	0.362	8.80	9.20	2
E1	0.272	0.279	6.90	7.10	3, 4
L	0.012	0.027	0.30	0.70	-
N	48		48		6
e	0.020 BSC		0.500 BSC		-

Rev. 1 4/95

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q48.12x12-S

48 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

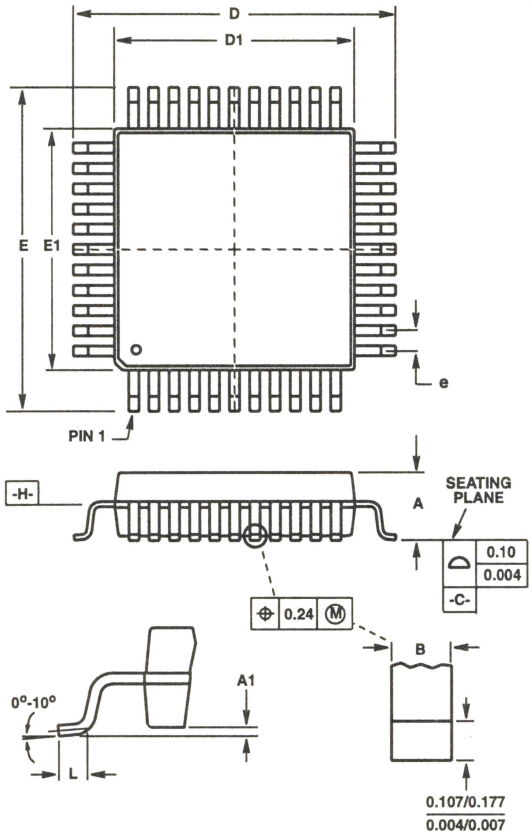
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.081	0.100	2.05	2.55	-
A1	0.000	0.011	0.00	0.30	-
B	0.008	0.017	0.20	0.45	5
D	0.587	0.618	14.90	15.70	2
D1	0.469	0.488	11.90	12.40	3, 4
E	0.587	0.618	14.90	15.70	2
E1	0.469	0.488	11.90	12.40	3, 4
L	0.028	0.043	0.70	1.10	-
N	48		48		6
e	0.032 BSC		0.80 BSC		-

Rev. 0 2/96

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q64.10x10-S

64 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

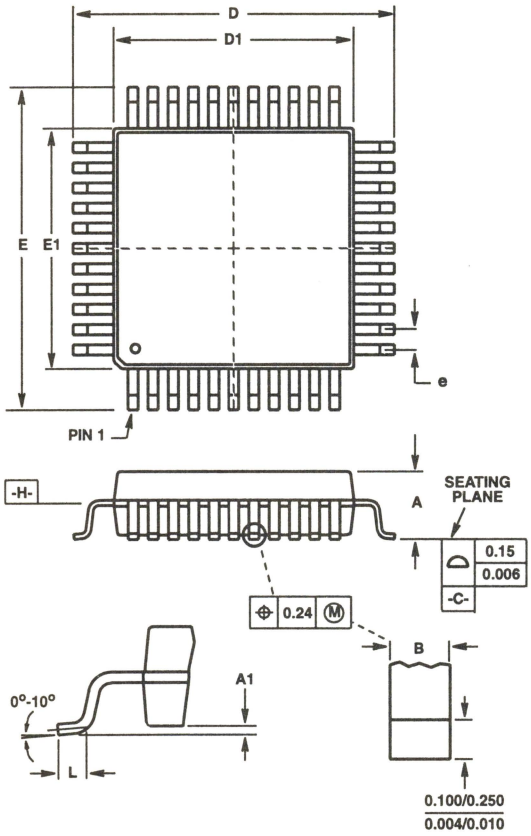
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.056	0.066	1.40	1.70	-
A1	0.000	0.007	0.00	0.20	-
B	0.006	0.010	0.15	0.26	5
D	0.465	0.480	11.80	12.20	2
D1	0.390	0.397	9.90	10.10	3, 4
E	0.465	0.480	11.80	12.20	2
E1	0.390	0.397	9.90	10.10	3, 4
L	0.012	0.027	0.30	0.70	-
N	64		64		6
e	0.020 BSC		0.50 BSC		-

Rev. 0 2/96

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q64.14x20-S

64 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

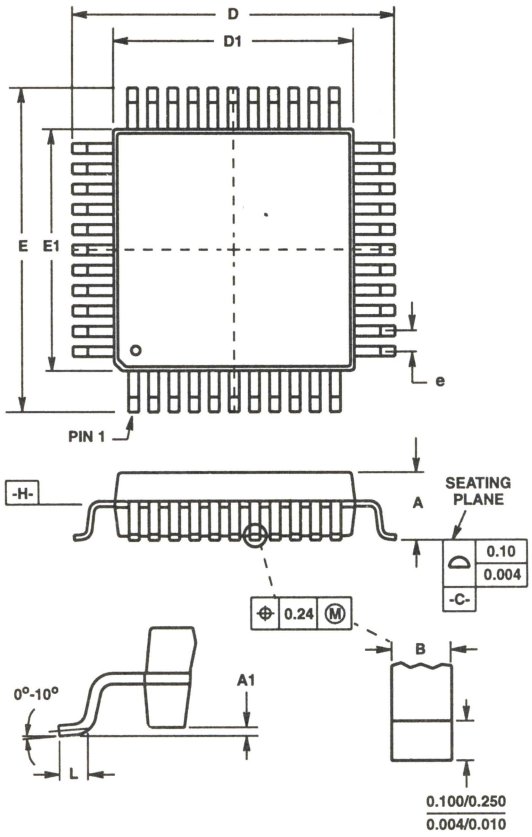
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.103	0.122	2.60	3.10	-
A1	0.002	0.011	0.05	0.30	-
B	0.012	0.021	0.30	0.55	5
D	0.926	0.956	23.50	24.30	2
D1	0.784	0.803	19.90	20.40	3, 4
E	0.689	0.720	17.50	18.30	2
E1	0.548	0.566	13.90	14.40	3, 4
L	0.024	0.039	0.60	1.00	-
N	64		64		6
e	0.039 BSC		1.00 BSC		-
ND	19		19		-
NE	13		13		-

Rev. 1 4/95

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q80.14x20-S

80 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

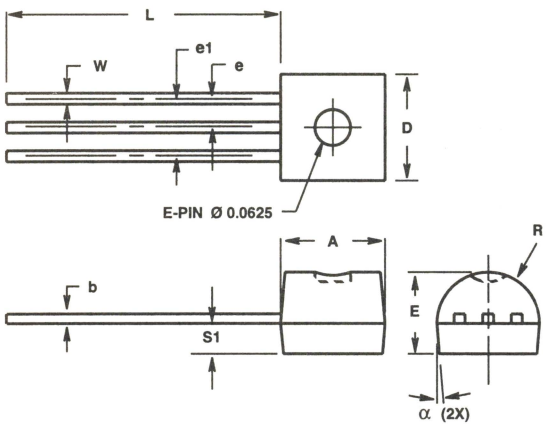
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.103	0.122	2.60	3.10	-
A1	0.002	0.011	0.05	0.30	-
B	0.010	0.019	0.25	0.50	5
D	0.926	0.956	23.50	24.30	2
D1	0.784	0.803	19.90	20.40	3, 4
E	0.689	0.720	17.50	18.30	2
E1	0.548	0.566	13.90	14.40	3, 4
L	0.024	0.039	0.60	1.00	-
N	80		80		6
e	0.032 BSC		0.80 BSC		-
ND	24		24		-
NE	16		16		-

Rev. 0 5/97

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

Single-In-Line Plastic Packages (SIP)



Z3.05 (JEDEC STYLE TO-92 MODIFIED)
3 LEAD PLASTIC SINGLE-IN-LINE PACKAGE

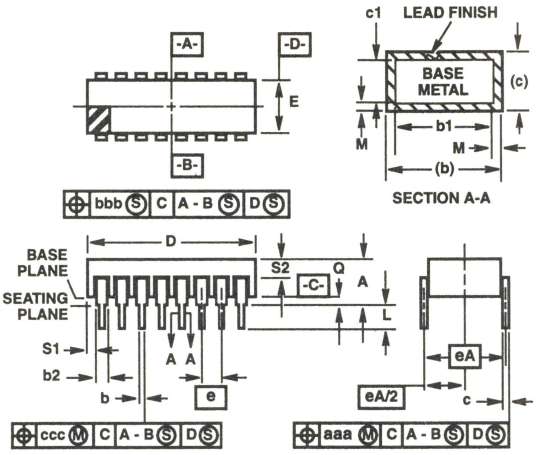
SYM-BOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.195	4.32	4.95	1
b	0.014	0.020	0.36	0.51	2
E	0.130	0.155	3.30	3.94	1
e	0.045	0.055	1.14	1.40	-
e1	0.095	0.105	2.41	2.67	-
L	0.500	0.610	12.70	15.49	-
R	0.085	0.095	2.16	2.41	-
S1	0.045	0.060	1.14	1.52	-
W	0.016	0.022	0.41	0.56	2
D	0.175	0.195	4.45	4.95	1
α	4°	6°	4°	6°	-

Rev. 0 2/94

NOTES:

1. Package body dimensions do not include any mold flash or protrusions.
2. Package outline dimensions do not include burrs.
3. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C)
14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

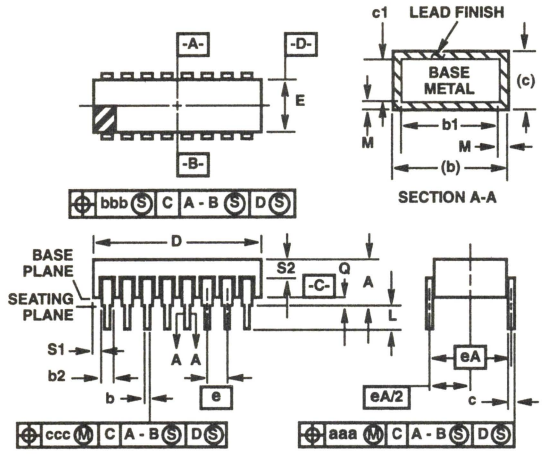
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D24.6 MIL-STD-1835 CDIP2-T24 (D-3, CONFIGURATION C)
24 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

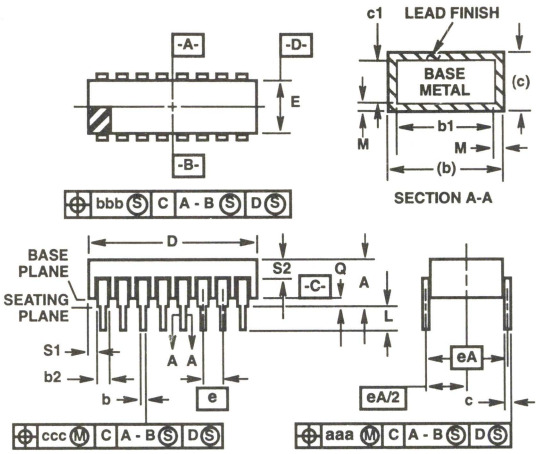
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	-
E	0.500	0.610	12.70	15.49	-
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	24		24		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D28.6 MIL-STD-1835 CDIP2-T28 (D-10, CONFIGURATION C)
28 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

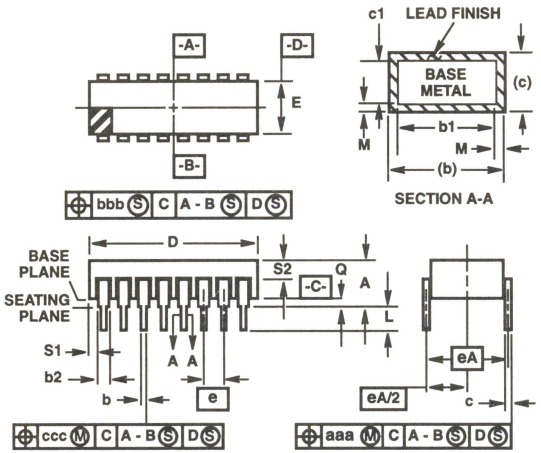
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	-
E	0.500	0.610	12.70	15.49	-
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	28		28		8

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D40.6 MIL-STD-1835 CDIP2-T40 (D-5, CONFIGURATION C)
40 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

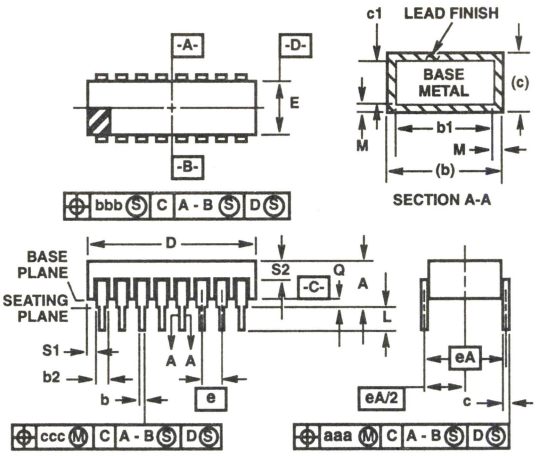
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	4
E	0.510	0.620	12.95	15.75	4
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	40		40		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D42.6

42 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

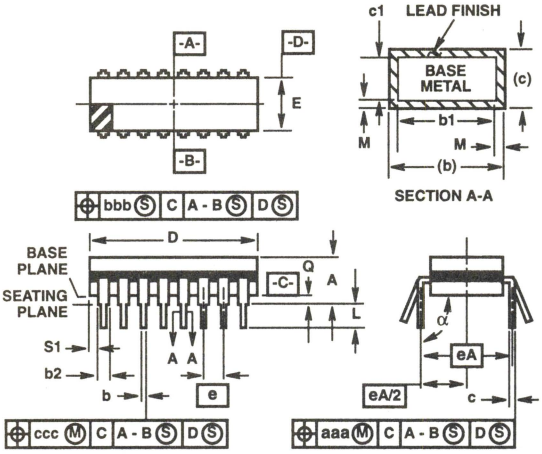
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.142	0.225	3.60	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.022	0.36	0.56	3
b2	0.035	0.043	1.90	1.10	-
b3	-	-	-	-	4
c	0.009	0.015	0.23	0.38	2
c1	0.009	0.012	0.23	0.30	3
D	2.083	2.122	52.9	53.9	-
E	0.510	0.620	12.95	15.75	-
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.130	-	3.30	-	-
Q	0.039	-	1.00	-	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^{o}	105^{o}	90^{o}	105^{o}	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	42		42		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

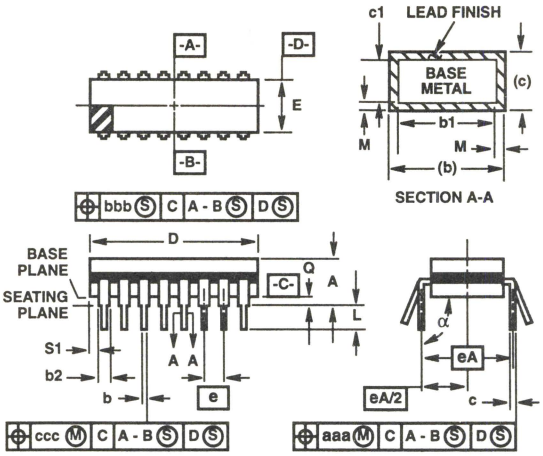
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

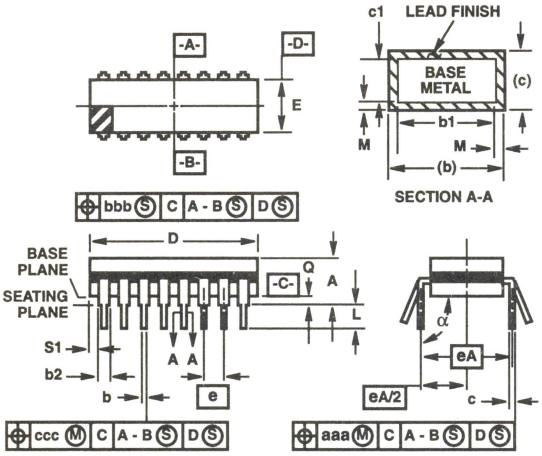
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F18.3 MIL-STD-1835 GDIP1-T18 (D-6, CONFIGURATION A)
18 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

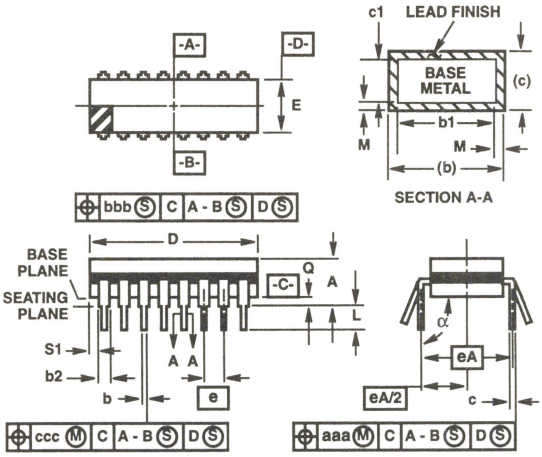
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.960	-	24.38	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	18		18		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F20.3 MIL-STD-1835 GDIP1-T20 (D-8, CONFIGURATION A)
20 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

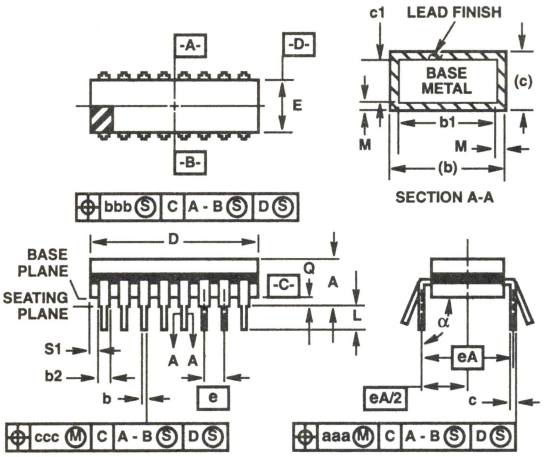
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.060	-	26.92	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	20		20		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F24.3 MIL-STD-1835 GDIP3-T24 (D-9, CONFIGURATION A)
24 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

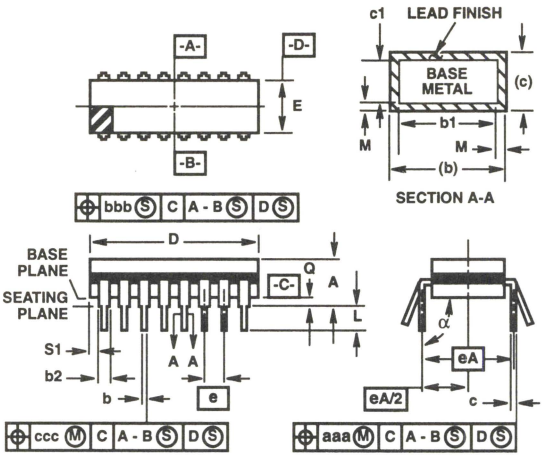
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.220	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.280	-	32.51	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	24		24		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

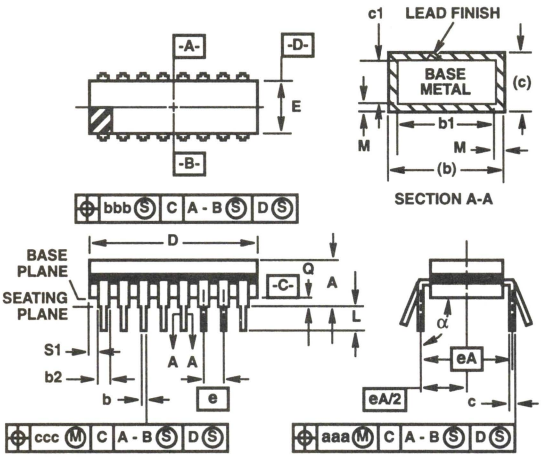
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F24.6 MIL-STD-1835 GDIP1-T24 (D-3, CONFIGURATION A)
24 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	24		24		8

Rev. 0 4/94

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

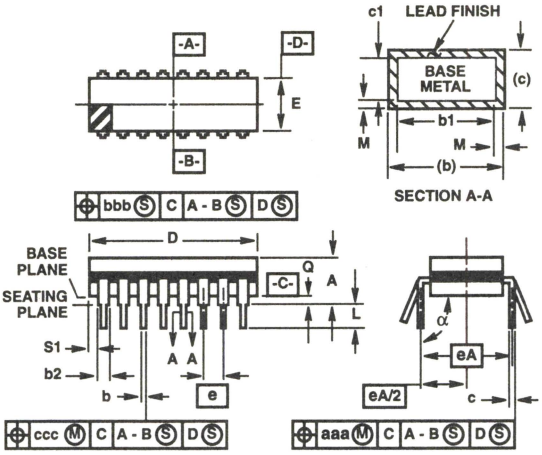
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	28		28		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F40.6 MIL-STD-1835 GDIP1-T40 (D-5, CONFIGURATION A)
40 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

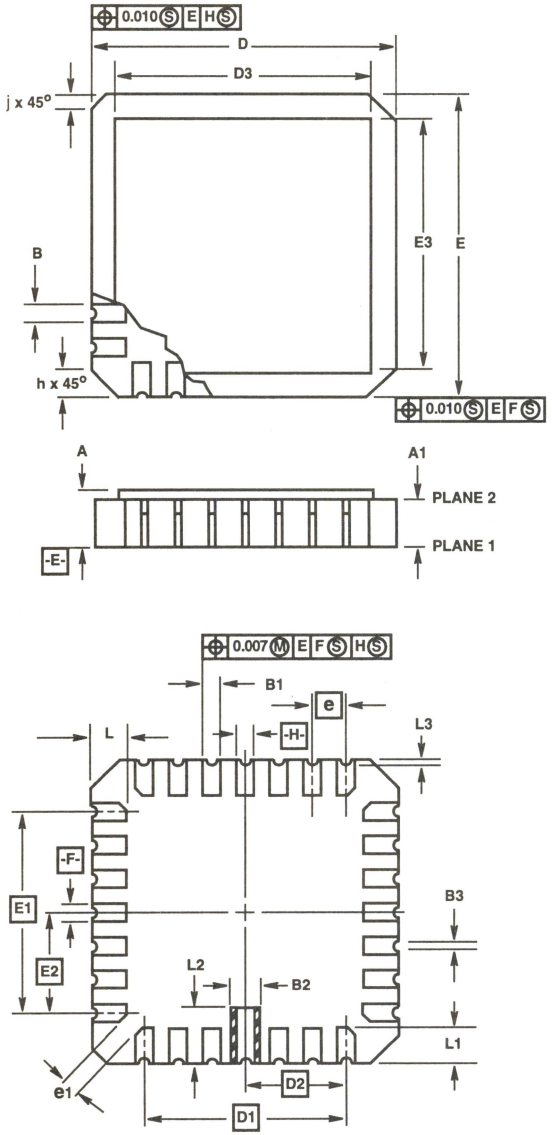
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	5
E	0.510	0.620	12.95	15.75	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	40		40		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)



J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

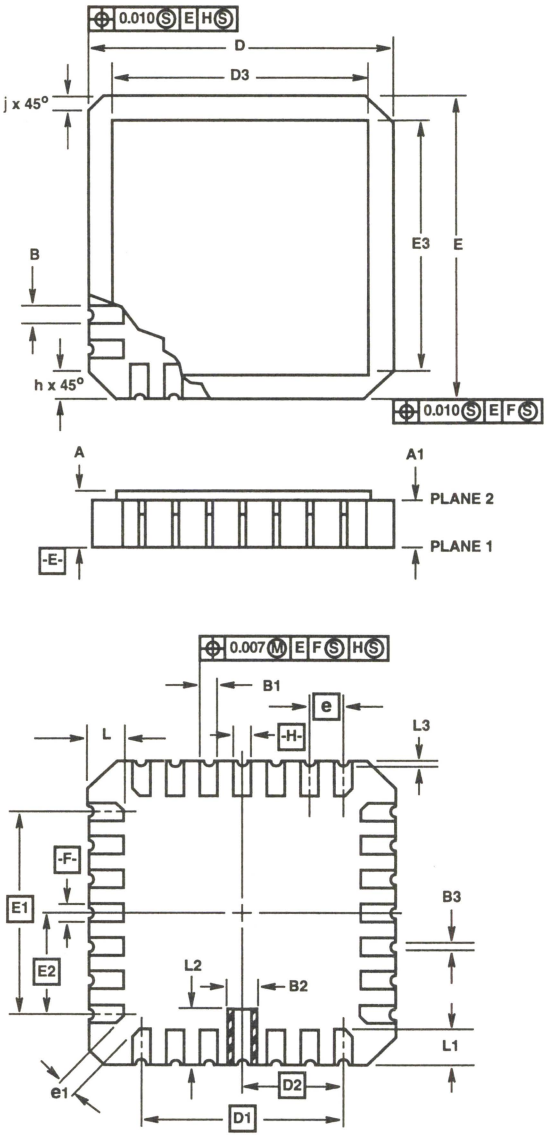
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)



J20.B

20 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

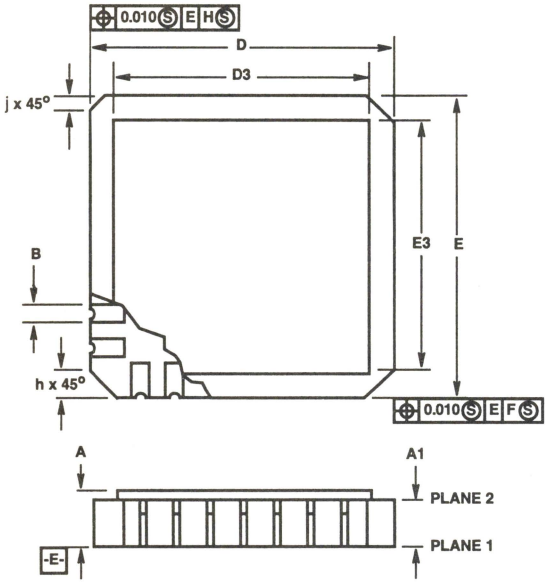
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.070	0.097	1.78	2.46	6, 7
A1	0.054	0.077	1.37	1.96	-
B	-	-	-	-	-
B1	0.020	0.030	0.51	0.76	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	0.325	0.335	8.26	8.51	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	0.325	0.335	8.26	8.51	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.042	0.058	1.07	1.47	-
L1	0.042	0.058	1.07	1.47	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

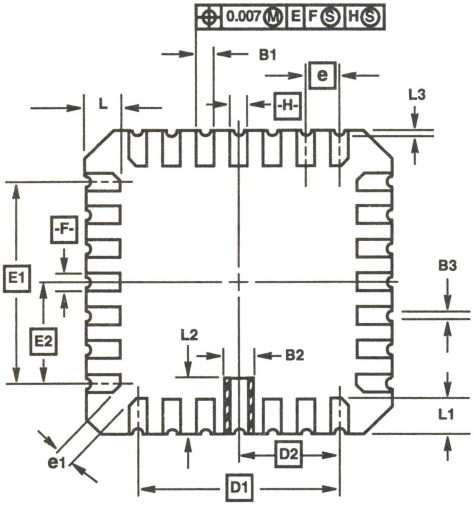
Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)





J28.A MIL-STD-1835 CQCC1-N28 (C-4)
28 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

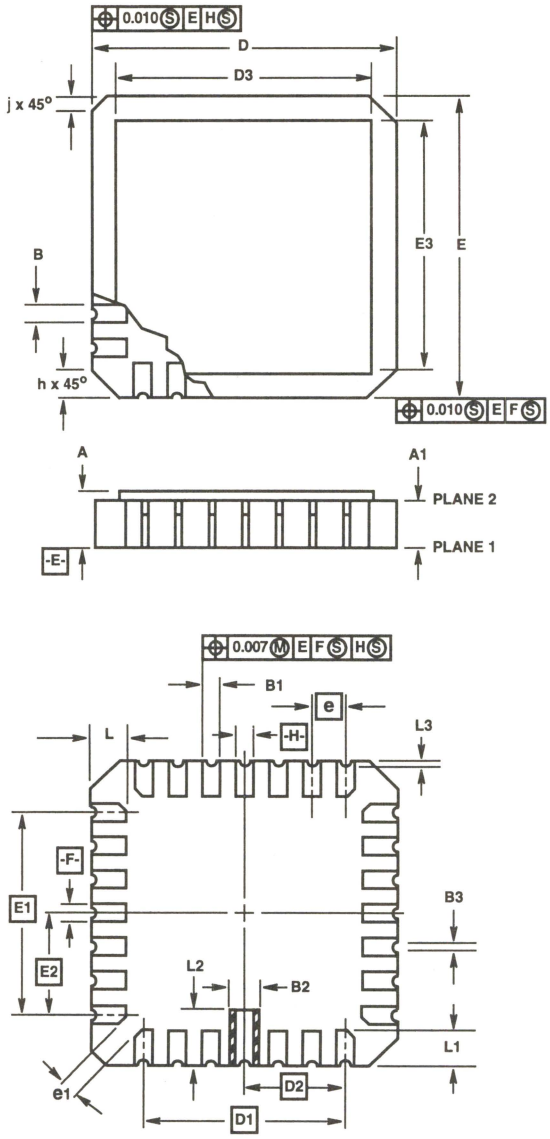
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.442	0.460	11.23	11.68	-
D1	0.300 BSC		7.62 BSC		-
D2	0.150 BSC		3.81 BSC		-
D3	-	0.460	-	11.68	2
E	0.442	0.460	11.23	11.68	-
E1	0.300 BSC		7.62 BSC		-
E2	0.150 BSC		3.81 BSC		-
E3	-	0.460	-	11.68	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.90	2.41	-
L3	0.003	0.015	0.08	0.038	-
ND	7		7		3
NE	7		7		3
N	28		28		3

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)



J44.A MIL-STD-1835 CQCC1-N44 (C-5)
44 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

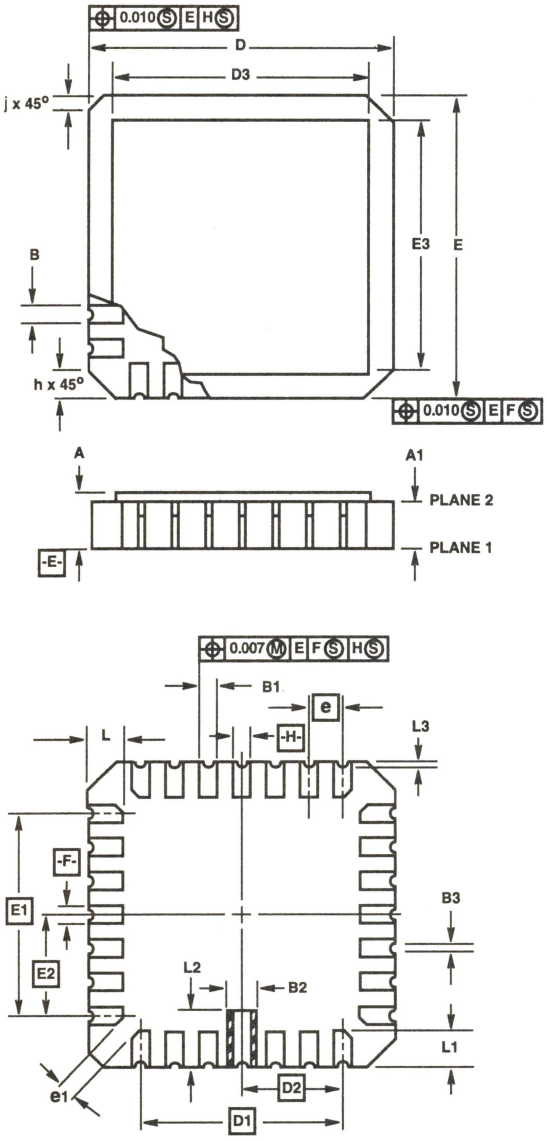
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.120	1.63	3.05	6, 7
A1	0.054	0.088	1.37	2.24	-
B	0.033	0.039	0.84	0.99	4
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.640	0.662	16.26	16.81	-
D1	0.500 BSC		12.70 BSC		-
D2	0.250 BSC		6.35 BSC		-
D3	-	0.662	-	16.81	2
E	0.640	0.662	16.26	16.81	-
E1	0.500 BSC		12.70 BSC		-
E2	0.250 BSC		6.35 BSC		-
E3	-	0.662	-	16.81	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.90	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	11		11		3
NE	11		11		3
N	44		44		3

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)



J68.A

68 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

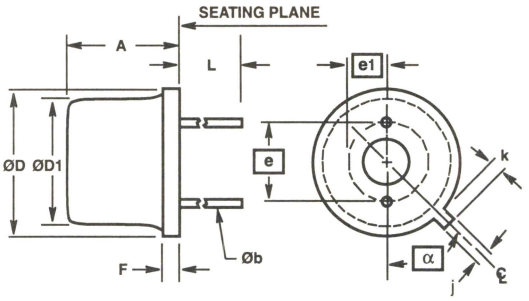
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.067	0.087	1.70	2.20	6, 7
A1	0.058	0.072	1.47	1.83	-
B	-	-	-	-	-
B1	0.033	0.039	0.85	0.99	2, 4
B3	0.006	0.022	0.15	0.56	-
D	0.940	0.965	23.88	24.51	-
D1	0.800 BSC		20.32 BSC		-
D2	0.400 BSC		10.16 BSC		-
D3	0.616	0.632	15.65	16.05	2
E	0.940	0.965	23.88	24.51	-
E1	0.800 BSC		20.32 BSC		-
E2	0.400 BSC		10.16 BSC		-
E3	0.616	0.632	15.65	16.05	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
j	0.040 Ref		1.00 Ref		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	17		17		3
NE	17		17		3
N	68		68		3

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Metal Can Packages (Can)



NOTES:

1. Measured from maximum diameter of the actual device.
2. Measured from tab centerline.
3. N is number of leads.
4. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
5. Controlling dimension: INCH.

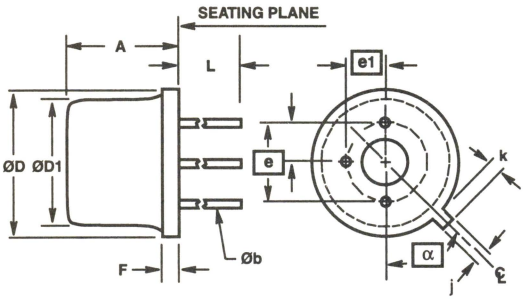
T2.A

2 LEAD METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.130	0.150	3.30	3.81	-
b	0.016	0.019	0.41	0.48	-
D	0.205	0.22	5.21	5.59	-
D1	0.180	0.190	4.57	4.83	-
F	0.010	0.025	0.25	0.64	-
k	0.033	0.046	0.84	1.17	1
j	0.033	0.045	0.84	1.14	-
L	0.500	0.560	12.70	14.22	-
e	0.100 BSC		2.54 BSC		-
e1	-		-		-
α	45		45		2
N	2		2		3

Rev. 0 4/94

Metal Can Packages (Can)



T3.A
3 LEAD METAL CAN PACKAGE

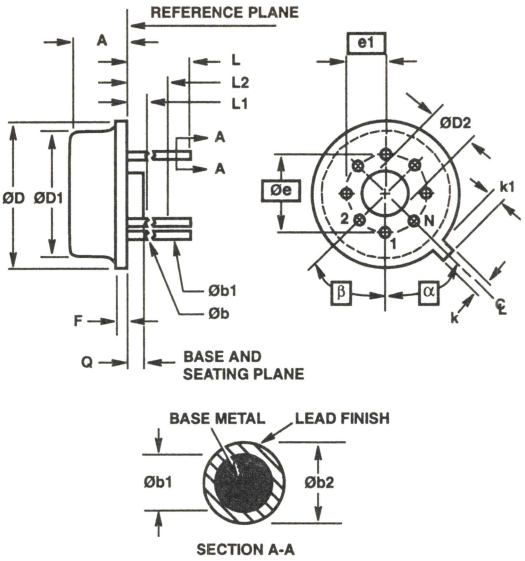
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.130	0.150	3.30	3.81	-
b	0.016	0.019	0.41	0.48	-
D	0.205	0.220	5.21	5.59	-
D1	0.180	0.190	4.57	4.83	-
F	0.010	0.025	0.25	0.64	-
k	0.033	0.048	0.84	1.22	1
j	0.036	0.046	0.91	1.17	-
L	0.500	0.560	12.70	14.22	-
e	0.100 BSC		2.54 BSC		-
e1	0.050 BSC		1.27 BSC		-
α	45		45		2
N	3		3		3

Rev. 0 4/94

NOTES:

1. Measured from maximum diameter of the actual device.
2. Measured from tab centerline.
3. N is number of leads
4. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
5. Controlling dimension: INCH.

Metal Can Packages (Can)



T8.C MIL-STD-1835 MACY1-X8 (A1)
8 LEAD METAL CAN PACKAGE

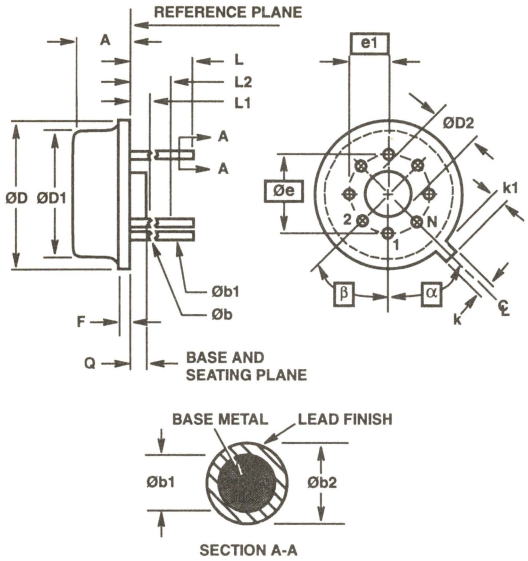
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45° BSC		45° BSC		3
β	45° BSC		45° BSC		3
N	8		8		4

Rev. 0 5/18/94

NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

Metal Can Packages (Can)



T10.B MIL-STD-1835 MACY1-X10 (A2)
10 LEAD METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.52	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.230 BSC		5.84 BSC		-
e1	0.115 BSC		2.92 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	36° BSC		36° BSC		3
β	36° BSC		36° BSC		3
N	10		10		4

Rev. 0 5/18/94

NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

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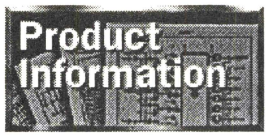

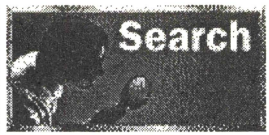

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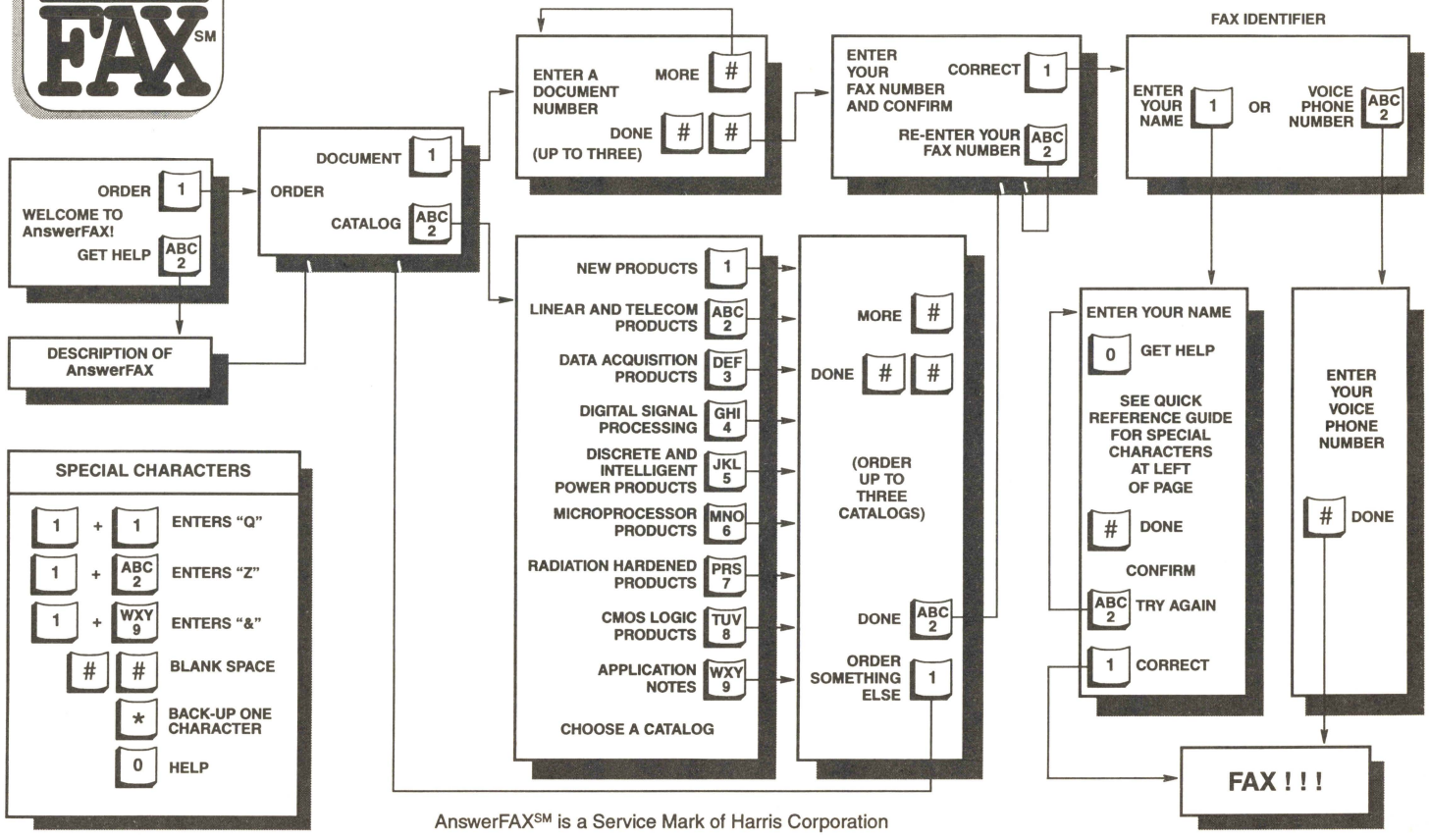

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FAI - Future Active Industrial
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